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CY8C20111/CY8C20121

CapSense® Express™ – One Button and Two Button Capacitive Controllers

Features

- Capacitive button input tied to a configurable output
  - Robust sensing algorithm
  - High sensitivity, low noise
  - Immunity to RF and AC noise
  - Low radiated EMC noise
  - Supports wide range of input capacitance, sensor shapes, and sizes
- Target Applications
  - Printers
  - Cellular handsets
  - LCD monitors
  - Portable DVD players
- Industry's best configurability
  - Custom sensor tuning
  - Output supports strong 20 mA sink current
  - Output state can be controlled through I^2C or directly from CapSense input state
  - Run time reconfigurable over I^2C
- Advanced features
  - Plug-and-play with factory defaults – tuned to support up to 1 mm overlay
  - Nonvolatile storage of custom settings
  - Easy integration into existing products – configure output to match system
  - No external components required
  - World class free configuration tool
- Wide range of operating voltages
  - 2.45 V to 2.9 V
  - 3.10 V to 3.6 V
  - 4.75 V to 5.25 V
- I^2C communication
  - Supported from 1.8 V
  - Internal pull-up resistor support option
  - Data rate up to 400 kbps.
  - Configurable I^2C addressing
- Industrial temperature range: –40 °C to +85 °C
- Available in 8-pin SOIC package

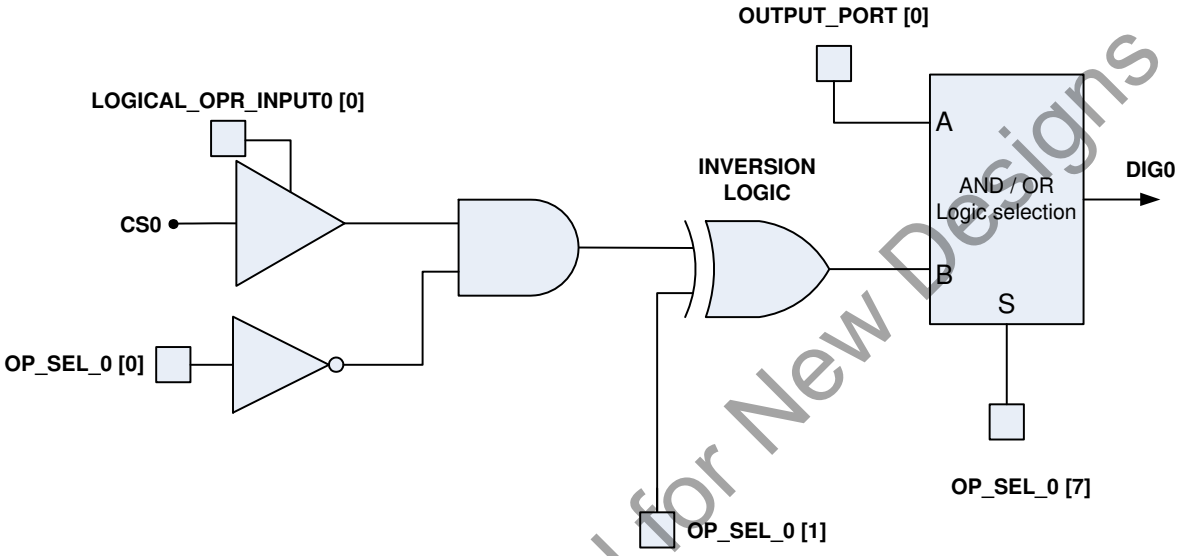
Overview

The CapSense® Express™ controllers support two capacitive sensing (CapSense) buttons and two general purpose outputs in CY8C20121 and one CapSense button and one general purpose output in CY8C20111. The device functionality is configured through the I^2C port and can be stored in on-board nonvolatile memory for automatic loading at power on. The digital outputs are controlled from CapSense inputs in factory default settings, but are user configurable for direct control through I^2C.

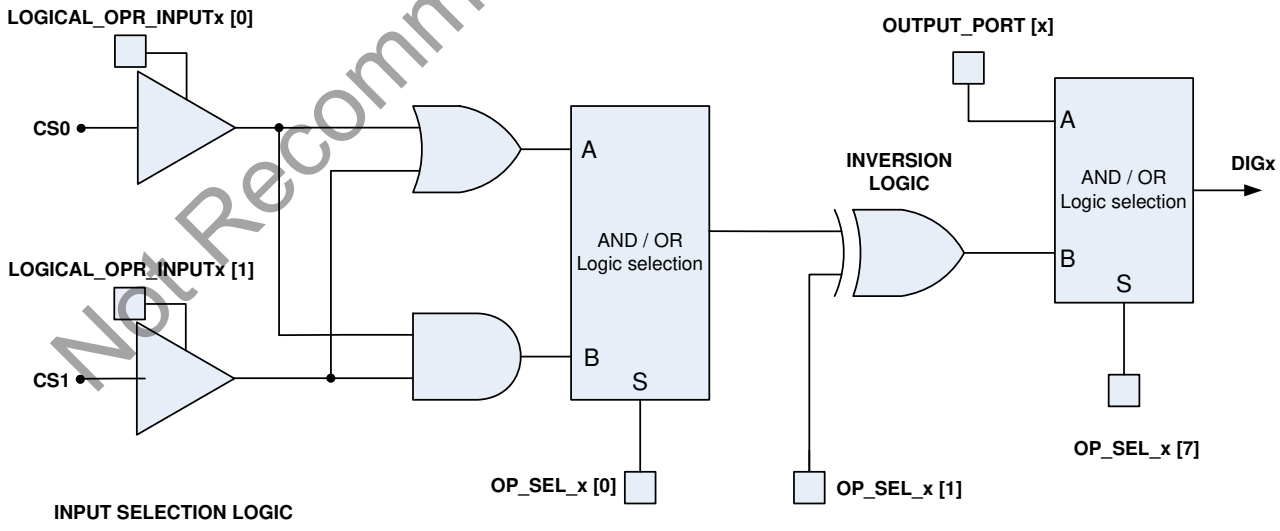
The four key blocks that make up the CY8C20111 and CY8C20121 controllers are: a robust capacitive sensing core with high immunity against radiated and conductive noise, control registers with nonvolatile storage, configurable outputs, and I^2C communications. The user can configure registers with parameters needed to adjust the operation and sensitivity of the CapSense buttons and outputs and permanently store the settings. The standard I^2C serial communication interface allows the host to configure the device and read sensor information in real time. I^2C address is fully configurable without any external hardware strapping.

Errata: For information on silicon errata, see "Errata" on page 41. Details include trigger conditions, devices affected, and proposed workaround.

CY8C20111 Digital Logic Diagram



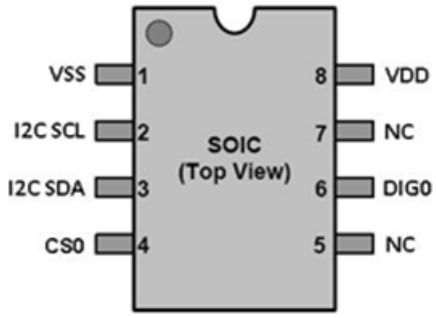
CY8C20121 Digital Logic Diagram



Contents

Pinouts

Figure 1. 8-pin SOIC (150 Mils) pinout
CY8C20111 (1 Button)



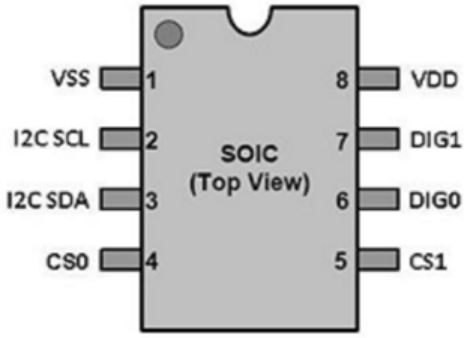
Pin Definitions

8-pin SOIC
CY8C20111 (1 Button)

Pin No	Name	Description
1	V_{SS}	Ground
2	I2C SCL	I^2C Clock
3	I2C SDA	I^2C Data
4	CS0	CapSense Input
5	NC	No Connect
6	DIG0	Digital Output
7	NC	No Connect
8	V_{DD}	Supply Voltage

Pinouts

Figure 2. 8-pin SOIC (150 Mils) pinout
CY8C20121 (2 Button)



Pin Definitions

8-pin SOIC
CY8C20121 (2 Button)

Pin No	Name	Description
1	V_{SS}	Ground
2	I2C SCL	I^2C Clock
3	I2C SDA	I^2C Data
4	CS0	CapSense Input
5	CS1	CapSense Input
6	DIG0	Digital Output
7	DIG1	Digital Output
8	V_{DD}	Supply Voltage

Typical Circuits

Figure 3. Circuit-1: One Button and One LED[1]

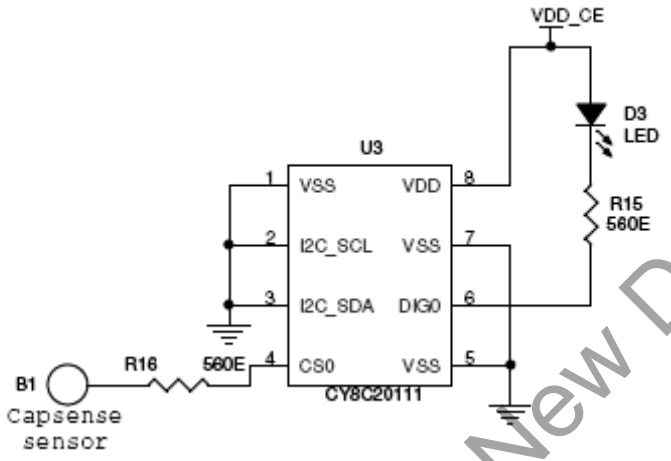
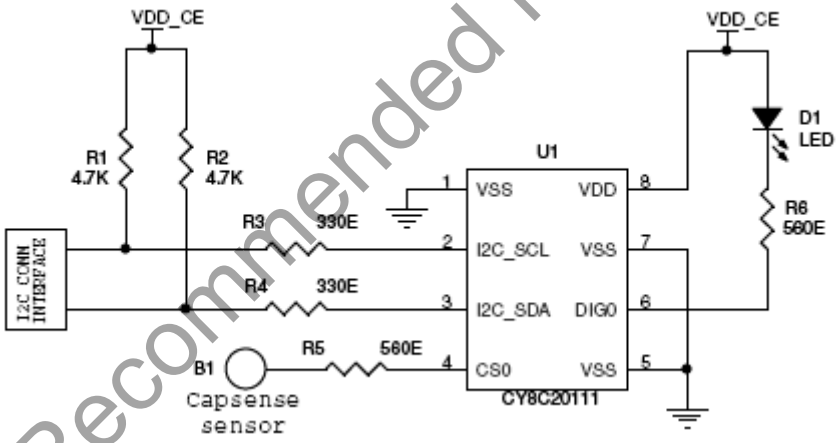


Figure 4. Circuit-2: One Button and One LED with I²C Interface



Note
1. The sensors are factory tuned to work with 1 mm plastic or glass overlay.

Typical Circuits *(continued)*

Figure 5. Circuit-3: Two Buttons and Two LEDs with I²C Interface

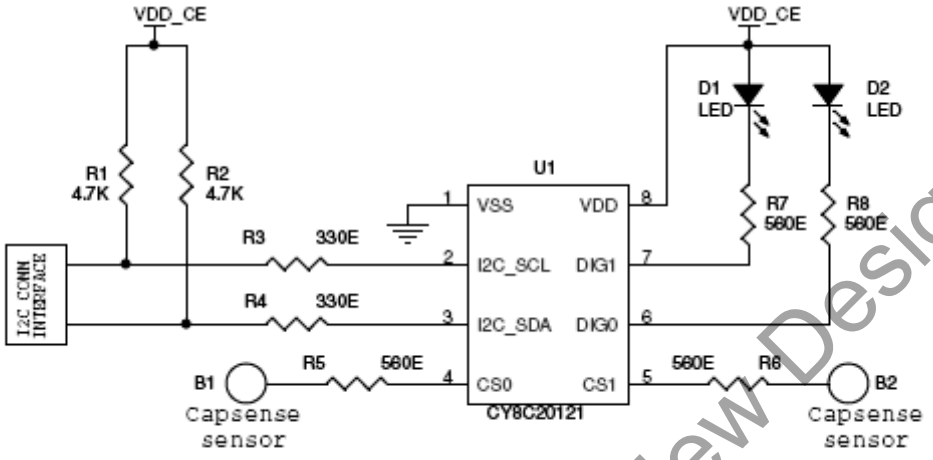
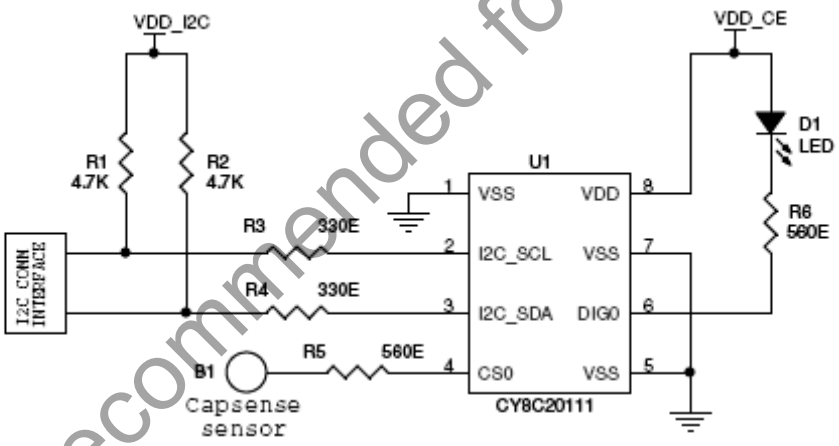


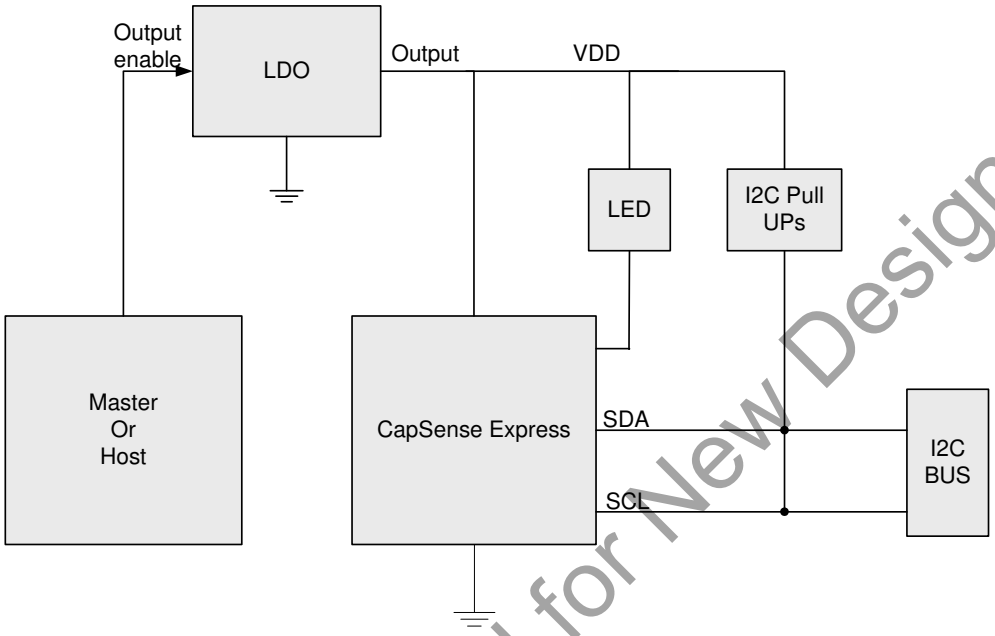
Figure 6. Circuit-4: Compatibility with 1.8 V I²C Signaling [2, 3]



Note
2. 1.8 V ≤ V_{DD}_I2C ≤ V_{DD}_CE and 2.4 V ≤ V_{DD}_CE ≤ 5.25 V.
3. The I2C drive mode of the CapSense device should be configured properly before using in an I2C environment with external pull-ups. Please refer to I2C_ADDR_DM register and its factory setting.

Typical Circuits *(continued)*

Figure 7. Circuit-5: Powering Down CapSense Express Device for Low Power Requirements [4]



Note

4. For low power requirements, if VDD is to be turned off, the above concept can be used. The VDDs of CapSense Express, I2C pull-ups, and LEDs must be from the same source. Turning off the VDD ensures that no signal is applied to the device while it is unpowered. The I2C signals should not be driven high by the master in this situation. If a port pin or group of port pins can cater to the power supply requirement of the circuit, the LDO can be avoided.

Operating Modes

Normal Mode

In normal mode of operation, the acknowledgment time is optimized. The timings remain approximately the same for different configurations of the slave. To reduce the acknowledgment times in normal mode, the registers 0x07, 0x08, 0x11, 0x50, 0x51, 0x5C, 0x5D are given only read access. Writing to these registers can be done only in setup mode.

Setup Mode

All registers have read and write access (except those which are read only) in this mode. The acknowledgment times are longer compared to normal mode. When CapSense scanning is disabled (command code 0x0A in command register 0xA0), the acknowledgment times can be improved to values similar to the normal mode of operation.

I²C Interface

The CapSense Express devices support the industry standard I²C protocol, which can be used to:

- Configure the device
- Read the status and data registers of the device
- Control device operation
- Execute commands

The I²C address can be modified during configuration.

I²C Device Addressing

The device uses a seven bit addressing protocol. The I²C data transfer is always initiated by the master sending one byte address; first 7-bit contains address and LSb indicates the data transfer direction. Zero in the LSb indicates the write transaction form master and one indicates read transfer by the master. Table 1 shows example for different I²C addresses.

Table 1. I²C Addresses

7-bit Slave Address (in Dec)	D7	D6	D5	D4	D3	D2	D1	D0	8-bit Slave Address (in Hex)
1	0	0	0	0	0	0	1	0(W)	02
1	0	0	0	0	0	0	1	1(R)	03
75	1	0	0	1	0	1	1	0(W)	96
75	1	0	0	1	0	1	1	1(W)	97

I²C Clock Stretching

"Clock stretching" or "bus stalling" in I²C communication protocol is a state in which the slave holds the SCL line low to indicate that it is busy. In this condition, the master is expected to wait until the SCL is released by the slave.

When an I²C master communicates with the CapSense Express device, the CapSense Express stalls the I²C bus after the reception of each byte (that is, just before the ACK/NAK bit) until processing of the byte is complete and critical internal functions are executed. Use a fully I²C compliant master to communicate with the CapSense Express device.

An I²C master which does not support clock stretching (a bit banged software I²C Master) must wait for a specific amount of time specified (as shown in the section Format for Register Write and Read) for each register write and read operation before the next bit is transmitted. It is mandatory to check the SCL status (it should be high) before I²C master initiates any data transfer with CapSense Express. If the master fails to do so and continues to communicate, the communication is erroneous.

The following diagrams represent the ACK time delays shown in the Register Map on page 7.

Also note that, while using CapSense Express Devices on an I2C bus, I2C master should not generate a start or stop condition in the I2C bus before CapSense Express device generating acknowledgement (ACK/NCK) for the previous transaction. An acknowledgement state produced by the CapSense Express Device for the previous data transfer after start condition for new data transfer by the master may produce unexpected behavior from CapSense Express I2C slave interface.

Figure 8. Write ACK Time Representation

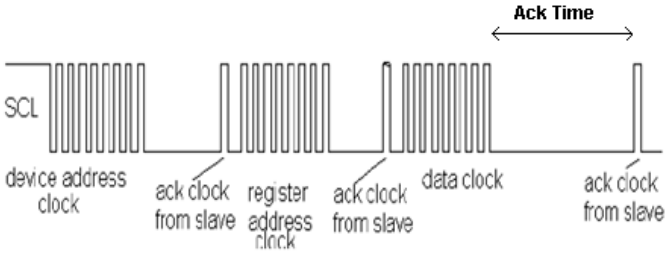
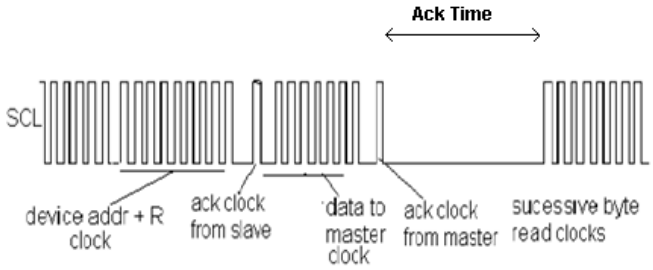


Figure 9. Read ACK Time Representation



Format for Register Write and Read

Register write format

Start	Slave Addr + W	A	Reg Addr	A	Data	A	Data	A	. . . .	Data	A	Stop

Register read format

Start	Slave Addr + W	A	Reg Addr	A	Stop							
Start	Slave Addr + R	A	Data	A	Data	A	. . . . .	Data	N	Stop		

Legends

Master	A – ACK
Slave	N – NAK

Registers

Register Conventions

Convention	Description
RW	Register have both read and write access
R	Register have only read access
WPR	Write register with pass code
FD	Factory defaults

Register Map

Name	Register Address (in Hex)	Access	Writable Only in Setup Mode [5]	Factory Default Values of Registers (in Hex)		I²C Max ACK Time in Normal Mode (ms) [6]	I²C Max ACK Time in Setup Mode (ms) [6]	Page No.
				1 Button	2 Button			
OUTPUT_PORT	04	W	–	01	03	0.10	–	13
CS_ENABLE	07	RW	Yes	01	03	–	11	13
DIG_ENABLE	08	RW	Yes	01	03	–	11	14
SET_STRONG_DM	11	RW	Yes	01	03	–	11	14
OP_SEL_0	1C	RW	–	82	82	0.12	11	15
LOGICAL_OPR_INPUT0	1E	RW	–	01	01	0.12	11	15
OP_SEL_1 [7]	21	RW	–		82	0.12	11	15
LOGICAL_OPR_INPUT1 [7]	23	RW	–		02	0.12	11	15
CS_NOISE_TH	4E	RW	–	28	28	0.11	11	16
CS_BL_UPD_TH	4F	RW	–	64	64	0.11	11	16
CS_SETL_TIME	50	RW	Yes	A0	A0	–	35	16
CS_OTH_SET	51	RW	Yes	00	00	–	35	17
CS_HYSTERISIS	52	RW	–	0A	0A	0.11	11	17
CS_DEBOUNCE	53	RW	–	03	03	0.11	11	18
CS_NEG_NOISE_TH	54	RW	–	14	14	0.11	11	18
CS_LOW_BL_RST	55	RW	–	14	14	0.11	11	18
CS_FILTERING	56	RW	–	20	20	0.11	11	19
CS_SCAN_POS_0	5C	RW	Yes	00	00	–	11	19
CS_SCAN_POS_1 [7]	5D	RW	Yes		01	–	11	19
CS_FINGER_TH_0	66	RW	–	64	64	0.14	11	20
CS_FINGER_TH_1 [7]	67	RW	–		64	0.14	11	20
CS_IDAC_0	70	RW	–	0A	0A	0.14	11	20
CS_IDAC_1 [7]	71	RW	–		0A	0.14	11	20
I2C_ADDR_LOCK	79	RW	–	01	01	0.11	11	20
DEVICE_ID	7A	R	–	11	21	0.11	11	21
DEVICE_STATUS	7B	R	–	03	03	0.11	11	21
I2C_ADDR_DM	7C	RW	–	80	80	0.11	11	22
CS_READ_BUTTON	81	RW	–	81	81	0.12	11	22
CS_READ_BLM	82	R	–	NA	NA	0.12	11	23
CS_READ_BLL	83	R	–	NA	NA	0.12	11	23
CS_READ_DIFFM	84	R	–	NA	NA	0.12	11	23
CS_READ_DIFFL	85	R	–	NA	NA	0.12	11	23
CS_READ_RAWM	86	R	–	NA	NA	0.12	11	23
CS_READ_RAWL	87	R	–	NA	NA	0.12	11	23

Notes
5. These registers are writable only after entering into setup mode. All other registers are available for read and write in normal and setup mode.
6. The Ack times specified are 1x I2C Ack times.
7. These registers are available only in CY8C20121 device.

Register Map *(continued)*

Name	Register Address (in Hex)	Access	Writable Only in Setup Mode [5]	Factory Default Values of Registers (in Hex)		I²C Max ACK Time in Normal Mode (ms) [6]	I²C Max ACK Time in Setup Mode (ms) [6]	Page No.
				1 Button	2 Button			
CS_READ_STATUS	88	R	–	NA	NA	0.12	11	24
COMMAND_REG	A0	W	–	00	00	0.10	11	24

CapSense Express Commands

Command [8]	Description	Executable Mode	Duration the Device is NOT Accessible after ACK (in ms) [9]
W 00 A0 00	Get firmware revision	Setup/Normal	0
W 00 A0 01	Store current configuration to NVM	Setup/Normal	120
W 00 A0 02	Restore factory configuration	Setup/Normal	120
W 00 A0 03	Write NVM POR defaults	Setup/Normal	120
W 00 A0 04	Read NVM POR defaults	Setup/Normal	5
W 00 A0 05	Read current configurations (RAM)	Setup/Normal	5
W 00 A0 06	Reconfigure device (POR)	Setup	5
W 00 A0 07	Set Normal mode of operation	Setup/Normal	0
W 00 A0 08	Set Setup mode of operation	Setup/Normal	0
W 00 A0 09	Start scan	Setup/Normal	10
W 00 A0 0A	Stop scan	Setup/Normal	5
W 00 A0 0B	Get CapSense scan status	Setup/Normal	0

Notes
8. 'W' indicates the write transfer. The next byte of data represents the 7-bit I²C address.
9. The Ack times specified are 1x I2C Ack times.

OUTPUT_STATUS

Output Status Register

OUTPUT_STATUS: 00h

1 Button	7	6	5	4	3	2	1	0
Access: FD								R:01
Bit Name								STS[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							R:03	
Bit Name							STS[1:0]	

The Output Status register represents the actual logical levels on the output pins.

Bit	Name	Description
1:0	STS [1:0]	Used to represent the output status 0 Output low 1 Output high

OUTPUT_PORT

Output Port Register

OUTPUT_PORT: 04h

1 Button	7	6	5	4	3	2	1	0
Access: FD								W:01
Bit Name								DIG[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							W:03	
Bit Name							DIG[1:0]	

This register is used to write data to DIG output port. Pins defined as output of combinational logic (in OP_SEL_x register) cannot be changed using this register.

Bit	Name	Description
1:0	DIG [1:0]	A bit set in this register sets the logic level of the output. 0 Logic ‘0’ 1 Logic ‘1’

CS_ENABLE

Select CapSense Input Register

CS_ENABLE: 07h

(Writable only in Setup mode)

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								CS[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:03	
Bit Name							CS[1:0]	

This register is used to enable CapSense inputs. **This register should be set before setting finger threshold (0x66, 0x67) and IDAC setting (0x70, 0x71) registers.**

Bit	Name	Description
1:0	CS [1:0]	These bits are used to enable CapSense inputs. 0 Disable CapSense input 1 Enable CapSense input

DIG_ENABLE

Select DIG Output Register

GPO_ENABLE: 08h

(Writable only in Setup mode)

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								DIG[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:03	
Bit Name							DIG [1:0]	

This register is used to enable DIG (Digital) outputs. If DIG output is enabled, the strong drive mode register (11h) should also be set. If DIG output is disabled the drive mode of these pins is High Z.

Bit	Name	Description
1:0	DIG [1:0]	These bits are used to enable DIG outputs. 0 Disable DIG output 1 Enable DIG output

SET_STRONG_DM

Sets Strong Drive Mode for DIG Outputs.

SET_STRONG_DM: 11h

(Writable only in Setup mode)

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								DM [0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:03	
Bit Name							DM [1:0]	

This register sets strong drive mode for DIG (Digital) outputs. To set strong drive mode the pin should be enabled as GP output.

Bit	Name	Description
1:0	DM [1:0]	These bits are used to set the strong drive mode to DIG outputs. 0 Strong drive mode not set 1 Strong drive mode set

OP_SEL_x

Logic Operation Selection Registers

OP_SEL_0: 1Ch OP_SEL_1: 21h (Not available for 1 Button)

1/2Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0						RW: 0	RW: 0
Bit Name	Op_En						InvOp	Operator

This register is used to enable logic operation on GP outputs. OP_SEL_0 should be configured to get the logic operation output on DIG0 output and OP_SEL_1 for DIG1 output. Write to these registers during the disable state of respective DIG output pins does not have any effect.

The input to the logic operation can be selected in LOGIC_OPRX registers. The selected inputs can be ORed or ANDed. The output of logic operation can also be inverted.

Bit	Name	Description
7	Op_En	This bit enables or disables logic operation. 0 Disable logic operation 1 Enable logic operation
1	InvOp	This bit enables or disables logic operation output inversion. 0 Logic operation output not inverted 1 Logic operation output inverted
0	Operator	This bit selects which operator should be used to compute logic operation. 0 Logic operator OR is used on inputs 1 Logic operator AND is used on inputs

LOGICAL_OPR_INPUTx

Selects Input for Logic Operation

LOGICAL_OPR_INPUT0: 1Eh LOGICAL_OPR_INPUT1: 23h (Not available for 1 button)

LOGICAL_OPR_INPUT0

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								CSL[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:01	
Bit Name							CSL [1:0]	

LOGICAL_OPR_INPUT1

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:02	
Bit Name							CSL [1:0]	

These registers are used to give the input to logic operation block. The inputs can be only CapSense input status.

Bit	Name	Description
1:0	CSL [1:0]	These bits selects the input for logic operation block.

CS_NOISE_TH

Noise Threshold Register

CS_NOISE_TH: 4Eh

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:28							
Bit Name	NT[7:0]							

This register sets the noise threshold value. For individual sensors, count values above this threshold do not update the baseline. This count is relative to baseline. This parameter is common for all sensors.

The range is 3 to 255 and it should satisfy the equation NT < Min (Finger Threshold – Hysteresis – 5). Recommended value is 40% of finger threshold.

Bit	Name	Description
7:0	NT [7:0]	These bits are used to set the noise threshold value.

CS_BL_UPD_TH

Baseline Update Threshold Register

CS_BL_UPD_TH: 4Fh

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:64							
Bit Name	BLUT[7:0]							

When the new raw count value is above the current baseline and the difference is below the noise threshold, the difference between the current baseline and the raw count is accumulated into a “bucket.” When the bucket fills, the baseline increments and the bucket is emptied. This parameter sets the threshold that the bucket must reach for the baseline to increment. In other words, lower value provides faster baseline update rate and vice versa. This parameter is common for all sensors.

The range is 0 to 255.

Bit	Name	Description
7:0	BLUT [7:0]	These bits set the threshold that the bucket must reach for baseline to increment.

CS_SETL_TIME

Settling Time Register

CS_SETL_TIME: 50h

(Writable only in Setup mode)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:A0							
Bit Name	STLNG_TM[7:0]							

The settling time parameter controls the duration of the capacitance-to-voltage conversion phase. The parameter setting controls a software delay that allows the voltage on the integrating capacitor to stabilize. This parameter is common for all sensors.

This register should be set before setting finger threshold (0x66, 0x67) and IDAC setting (0x70, 0x71) registers.

The range is 2 to 255.

Bit	Name	Description
7:0	STLNG_TM [7:0]	These bits are used to set the settling time value.

CS_OTH_SET

CapSense Clock Select, Sensor Auto Reset Register

CS_OTH_SET: 51h

(Writable only in Setup mode)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD		RW: 00			RW: 0			
Bit Name		CS_CLK[1:0]			Sns_Ar			

The registers set the CapSense module frequency of operation and enables or disables the sensor auto reset.

CS_CLK bits provides option to select variable clock input for the CapSense block. A sensor design having higher paratactic requires lower clock for better performance and vice versa.

Sensor Auto Reset determines whether the baseline is updated at all times or only when the signal difference is below the noise threshold. When set to '1' (enabled), the baseline is updated constantly. This setting limits the maximum time duration of the sensor, but it prevents the sensors from permanently turning on when the raw count suddenly rises without anything touching the sensor. This sudden rise can be caused by a large power supply voltage fluctuation, a high energy RF noise source, or a very quick temperature change. When the parameter is set to '0' (disabled), the baseline is updated only when raw count and baseline difference is below the noise threshold parameter. This parameter may be enabled unless there is a demand to keep the sensors in the on state for a long time. This parameter is common for all sensors.

Bit	Name	Description
6:5	CS_CLK[1:0]	These bits selects the CapSense clock. 00 IMO 01 IMO/2 10 IMO/4 11 IMO/8
3	Sns_Ar	This bit is used to enable or disable sensor auto reset. 0 Disable Sensor auto reset 1 Enable Sensor auto reset

CS_HYSTERISIS

Hysteresis Register

CS_HYSTERISIS: 52h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	HYS[7:0]							

The Hysteresis parameter adds to or subtracts from the finger threshold depending on whether the sensor is currently active or inactive. If the sensor is off, the difference count must overcome the 'finger threshold + hysteresis'. If the sensor is on, the difference count must go below the 'finger threshold – hysteresis'. It is used to add debouncing and "stickiness" to the finger detection algorithm. This parameter is common for all sensors.

Possible values are 0 to 255. However, the setting must be lower than the finger threshold parameter setting. Recommended value for hysteresis is 15 percent of finger threshold.

Bit	Name	Description
7:0	HYS [7:0]	These bits are used to set the hysteresis value.

CS_DEBOUNCE

Debounce Register.

CS_DEBOUNCE: 53h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	DB[7:0]							

The Debounce parameter adds a debounce counter to the 'sensor active transition'. For the sensor to transition from inactive to active, the consecutive samples of difference count value must stay above the 'finger threshold + hysteresis' for the number specified. This parameter is common for all sensors.

Possible values are 1 to 255. A setting of '1' provides no debouncing.

Bit	Name	Description
7:0	DB [7:0]	These bits are used to set the debounce value.

CS_NEG_NOISE_TH

Negative Noise Threshold Register

CS_NEG_NOISE_TH: 54h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	NNT[7:0]							

This parameter adds a negative difference count threshold. If the current raw count is below the baseline and the difference between them is greater than this threshold, the baseline is not updated. However, if the current raw count stays in the low state (difference greater than the threshold) for the number of samples specified by the Low Baseline Reset parameter, the baseline is reset. This parameter is common for all sensors.

Bit	Name	Description
7:0	NNT [7:0]	These bits are used to set the negative noise value.

CS_LOW_BL_RST

Low Baseline Reset Register

CS_LOW_BL_RST: 55h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	LBR[7:0]							

This parameter works together with the Negative Noise Threshold parameter. If the sample count values are below the baseline minus the negative noise threshold for the specified number of samples, the baseline is set to the new raw count value. It essentially counts the number of abnormally low samples required to reset the baseline. It is generally used to correct the finger-on-at-startup condition. This parameter is common for all sensors.

Bit	Name	Description
7:0	LBR [7:0]	These bits are used to set the Low Baseline Reset value.

CS_FILTERING

CapSense Filtering Register

CS_FILTERING: 56h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0		RW: 1	RW: 0			RW: 00	
Bit Name	RstBl		I2C_DS	Avg_En			Avg_Order[1:0]	

This register provides an option for forced baseline reset and to enable and configure two different types of software filters.

Bit	Name	Description
7	RstBl	This bit resets all the baselines and it is auto cleared to '0'. 0 All Baselines are not reset 1 All baselines are reset
5	I2C_DS	When this bit is set to '1' the CapSense scan sample is dropped if I^2C communication was active during scanning. 0 Disable the I^2C drop sample filer 1 Enable the I^2C drop sample filter
4	Avg_En	This bit enables average filter on raw counts. 0 Disable the average filter 1 Enable the average filter
[1:0]	Avg_Order[1:0]	These bits are used to select the number of CapSense samples to average:

Avg_Order[1:0] in Hex	Samples to Average
00	2
01	4
10	8
11	16

CS_SCAN_POS_x

Scan Position Registers

CS_SCAN_POS_0: 5Ch

(Writable only in Setup mode)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD								RW: 0
Bit Name								Scan_Pstn

CS_SCAN_POS_1: 5Dh (Not available for 1 Button)

(Writable only in Setup mode)

2 Button	7	6	5	4	3	2	1	0
Access: FD								RW: 1
Bit Name								Scan_Pstn

This register is used to set the position of the sensors in the switch table for proper scanning sequence because the CapSense sensors are scanned in sequence.

This register should be set after setting 0x07, 0x50, and 0x51 registers.

Bit	Name	Description
0	Scan_Pstn	This bit sets the scan position.

CS_FINGER_TH_x

Finger Threshold Registers

CS_FINGER_TH_0: 66h CS_FINGER_TH_1: 67h (Not available in 1 Button)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 64							
Bit Name	FT[7:0]							

This register sets the finger threshold value for CapSense inputs. Possible values are 3 to 255. This parameter should be configured individually for each CapSense inputs.

This register should be set after setting 0x07, 0x50, and 0x51 registers.

Bit	Name	Description
[7:0]	FT [7:0]	These bit set the finger threshold for CapSense inputs.

CS_IDAC_x

IDAC Setting Registers

CS_IDAC_0: 70h CS_IDAC_1: 71h (Not available in 1 Button)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0A							
Bit Name	IDAC[7:0]							

The IDAC register controls the sensitivity of the CapSense algorithm. This register is used to tune the CapSense input for specific design or overlays. Decreasing the value of this register increases the sensitivity of the CapSense buttons and vice versa. Decreasing the value of IDAC increases noise and vice versa.

Possible values are 1 to 255. If the value is set to 0 then the value is reset to default value 10.

The recommended value is greater than 4. Setting value ≤ 4 creates excessive amount of noise.

This register should be set after setting 0x07, 0x50, and 0x51 registers.

Bit	Name	Description
[7:0]	IDAC [7:0]	These bit set the IDAC values.

I2C_ADDR_LOCK

I2C Address Lock Registers

I2C_ADDR_LOCK: 79h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD								WPR: 0
Bit Name								I2CAL

This register is used to unlock and lock the I^2C address register (7Ch) access. The device I^2C address should be modified by writing new address to register 7Ch after unlocking the access using this register. Write to the 7C register during the locked state does not have any effect and the new address take effect only after the access is locked.

To lock or unlock the I^2C AL bit, the following three bytes must be written to register 79h:

- unlock I2CAL: 3Ch A5h 69h
- lock I2CAL: 96h 5Ah C3h

Reading the I2CAL bit from register 79h indicates the current access state.

Bit	Name	Description
0	I2CAL	This bit gives the lock/unlock status of I^2C address. 0 Unlocked 1 Locked

DEVICE_ID

Device ID Register

DEVICE_ID: 7Ah

1 Button	7	6	5	4	3	2	1	0
Access: FD	R: 11							
Bit Name	DEV_ID[7:0]							

2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 21							
Bit Name	DEV_ID[7:0]							

This register contains the device and product ID. The device and product ID corresponds to “xx” in CY8C201xx.

Bit	Name	Description
7:0	DEV_ID [7:0]	These bits contain the device and product ID.

Part No	Device/Product ID
CY8C20111	11
CY8C20121	21

DEVICE_STATUS

Device Status Register

DEVICE_STATUS: 7Bh

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R : 00		R: 0	R : 0	R: 0		R: 0	R: 0
Bit Name	Ip_Volt[1:0]		IRES	Load_FD	No_NVM_Wr		CSE	DIGE

This register contains the device status.

Bit	Name	Description
7:6	Ip_Volt [1:0]	Supply voltage is automatically detected and these bits are set accordingly.

Ip_Volt[1:0]	Supply Voltage
00	5
01	3.3
10	2.7
11	Reserved

5	IRES	When set to ‘1’, this bit indicates that an internal reset occurred. 0 indicates the last system reset was not internal reset 1 indicates the last system reset was internal reset
4	Load_FD	This bit indicates whether factory defaults are loaded during power-up. 0 User default configuration is loaded during power-up 1 Factory default configuration is loaded during power-up
3	No_NVM_Wr	When set to ‘1’, this bit indicates that the supply voltage applied to the device Is too low for a write to nonvolatile memory operation, and no write is performed. This bit must be checked before any Store or Write POR command.
1	CSE	This bit indicates whether CapSense function is enabled or disabled. 0 Functionality of CapSense block is disabled 1 Functionality of CapSense block is enabled
0	DIGE	This bit indicates whether GP Output function is enabled or disabled. 0 Functionality of Digital output block is disabled 1 Functionality of Digital output block is enabled

I2C_ADDR_DM

Device I²C Address and I²C Pin Drive Mode Register

I2C_ADDR_DM: 7Ch

1 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0	RW: 00						
Bit Name	I2CIP_EN	I2C_ADDR[6:0]						

This register sets the drive mode of I²C pins and I²C slave address. To write to this register, register 79h must first be unlocked. The value written to register 7Ch is applied only after locking register 79h again.

Bit	Name	Description
7	I2CIP_EN	This bit is used to set the I²C pins drive mode. 0 Internal pull-up enabled 1 Internal pull-up disabled
6:0	I2C_ADDR [6:0]	Used to set the device I²C address.

CS_READ_BUTTON

Button Select Register

CS_READ_BUTTON: 81h

1 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0							RW: 0
Bit Name	RD_EN							CSBN[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0						RW: 00	
Bit Name	RD_EN						CSBN[1:0]	

The scan result of a CapSense input (raw count, difference count, and baseline) can be read only for one input at a time using 82h–87h registers. This register is used to select a CapSense input to read the raw count, difference count, and baseline. Only the pins defined as CapSense inputs in register 07h can be used with this register. Trying to select other pins not defined as CapSense does not have any change.

Bit	Name	Description
7	RD_EN	This bit enables the CapSense raw data reading. 0 Disable CapSense scan result reading 1 Enable CapSense scan result reading
1:0	CSBN [1:0]	These bits decide which CapSense button scan result are read. When writing to this register, the bitmask must contain only one bit set to '1', otherwise the data is discarded.

CSBN [1:0]	CapSense Button No
01	1
10	2

CS_READ_BLx

Baseline Value MSB/LSB Registers

CS_READ_BLM: 82h CS_READ_BLL: 83h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	BL [7:0]							

Reading from this register returns the 2-byte current baseline value for the selected CapSense input.

Bit	Name	Description
7:0	BL [7:0]	These bits represent the baseline value.

CS_READ_DIFFx

Difference Count Value MSB/LSB Registers

CS_READ_DIFFM: 84h CS_READ_DIFFL: 85h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	DIF [7:0]							

Reading from this register returns the 2-byte current difference count for the selected CapSense input.

Bit	Name	Description
7:0	DIF [7:0]	These bits represent the sensor difference count.

CS_READ_RAWx

Difference Count Value MSB/LSB Registers

CS_READ_RAWM: 86h CS_READ_RAWL: 87h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	RC [7:0]							

Reading from this register returns the 2-byte current raw count value for the selected CapSense input.

Bit	Name	Description
7:0	RC [7:0]	These bits represent the raw count value.

CS_READ_STATUS

Sensor On Status Register

CS_READ_STATUS: 88h

1 Button	7	6	5	4	3	2	1	0
Access: FD								R: 0
Bit Name								BT_ST[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							R: 00	
Bit Name							BT_ST[1:0]	

This register gives the sensor ON/OFF status. A bit '1' indicates sensor is ON and '0' indicates sensor is OFF.

Bit	Name	Description
1:0	BT_ST [1:0]	These bits used to represent sensor status. 0 Sensor OFF 1 Sensor ON

COMMAND_REG

Command Register

COMMAND_REG: A0h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	W: 00							
Bit Name	Cmnd [7:0]							

Commands are executed by writing the command code to the command register.

Bit	Name	Description
7:0	Cmnd [7:0]	Refer to the following table for command register opcodes.

Table 2. Command Register Opcodes

Command Code	Name	Description
00h	Get Firmware Revision	The I^2C buffer is loaded with the one byte firmware revision value. Reading one byte after writing this command returns the firmware revision. The upper nibble of the firmware revision byte is the major revision number and the lower nibble is the minor revision number.
01h	Store Current Configuration to NVM	The current register settings are saved in nonvolatile memory (flash). This setting is automatically loaded after the next device reset/power-up or if the Reconfigure Device (06h) command is issued.
02h	Restore Factory Configuration	Replaces the saved user configuration with the factory default configuration. Current settings are unaffected by this command. New settings are loaded after the next device reset/power-up or if the 06h command is issued.

Table 2. Command Register Opcodes *(continued)*

Command Code	Name	Description
03h	Write POR Defaults	Sends new power-up defaults to the CapSense controller without changing current settings unless the 06h command is issued afterwards. This command is followed by 123 data bytes according to the POR Default Data Structure table. The CRC is calculated as the XOR of the 122 data bytes (00h-79h). If the CRC check fails or an incomplete block is sent, the slave responds with an ACK and the data is NOT saved to flash. To define new POR defaults: ■ Write command 03h ■ Write 122 data bytes with new values of registers (use the _flash.iic file generated from s/w tool) ■ Write one CRC byte calculated as XOR of previous 122 data bytes
04h	Read POR Defaults	Reads the POR settings stored in the nonvolatile memory. To read POR defaults: ■ Write command 04h ■ Read 122 data bytes ■ Read one CRC byte
05h	Read Device Configuration (RAM)	Reads the current device configuration. Gives the user “flat-address-space” access to all device settings. To read device configuration: ■ Write command 05h ■ Read 122 data bytes ■ Read one CRC byte
06h	Reconfigure Device (POR)	Immediately reconfigures the device with actual POR defaults from flash. Has the same effect on the registers as a POR. This command can only be executed in setup operation mode (command code 08).
07h	Set Normal Operation Mode	Sets the device in normal operation mode. In this mode, CapSense pin assignments cannot be modified; settling time, IDAC setting, external capacitor, and sensor auto-reset also cannot be modified.
08h	Set Setup Operation Mode	Sets the device in setup operation mode. In this mode, CapSense pin assignments can be changed along with other parameters.
09h	Start CapSense Scanning	Allows the user to start CSA scanning after it has been stopped using command 0x0A. Note that at POR, scanning is enabled and started by default if one or more sensors are enabled.
0Ah	Stop CapSense Scanning	Allows the user to stop CSA scanning. A system host controller might initiate this command before powering down the device to make sure that during power-down no CapSense touches are detected. When CSA scanning is stopped by the user and the device is still in the valid V_{CC} operating range, the following behavior is supported: ■ Any change to configuration can still be done (as long as V_{CC} is in operating range). ■ Command code 0x06 overrides the status of stop/scan by enabling and starting CSA scanning if one or more sensors are enabled. ■ CapSense read-back values return 0x00.
0Bh	Returns CapSense Scanning Status	The I^2C buffer is loaded with the one-byte CSA scanning status value. After writing the value 0Bh to the A0h register, reading one byte returns the CSA scanning status. It returns the LVD_STOP_SCAN and STOP_SCAN bits. LVD_STOP_SCAN is bit 3 - Set when CSA is stopped because V_{CC} is outside the valid operating range. STOP_SCAN is bit 2 - Set when CSA is stopped by the user by writing command 0x0A.