Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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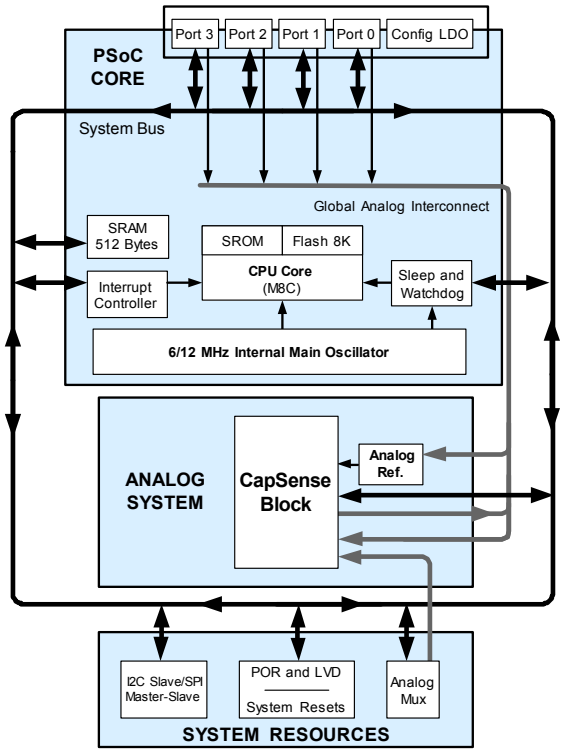
CY8C20134/CY8C20234/CY8C20334
CY8C20434/CY8C20534/CY8C20634

PSoC® Programmable System-on-Chip™

Features

- Low power CapSense® block
  - Configurable capacitive sensing elements
  - Supports combination of CapSense buttons, sliders, touchpads, and proximity sensors
- Powerful Harvard-architecture processor
  - M8C processor speeds running up to 12 MHz
  - Low power at high speed
  - Operating voltage: 2.4 V to 5.25 V
  - Industrial temperature range: –40 °C to +85 °C
- Flexible on-chip memory
  - 8 KB flash program storage 50,000 erase/write cycles
  - 512-Bytes SRAM data storage
  - Partial flash updates
  - Flexible protection modes
  - Interrupt controller
  - In-system serial programming (ISSP)
- Complete development tools
  - Free development tool (PSoC Designer™)
  - Full-featured, in-circuit emulator, and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- Precision, programmable clocking
  - Internal ±5.0% 6- / 12-MHz main oscillator
  - Internal low speed oscillator at 32 kHz for watchdog and sleep
- Programmable pin configurations
  - Pull-up, high Z, open-drain, and CMOS drive modes on all GPIOs
  - Up to 28 analog inputs on all GPIOs
  - Configurable inputs on all GPIOs
  - 20-mA sink current on all GPIOs
  - Selectable, regulated digital I/O on port 1
    - 3.0 V, 20 mA total port 1 source current
    - 5 mA strong drive mode on port 1 versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O combinations
  - Comparator noise immunity
  - Low-dropout voltage regulator for the analog array
- Additional system resources
  - Configurable communication speeds
    - I^2C: selectable to 50 kHz, 100 kHz, or 400 kHz
    - SPI: configurable between 46.9 kHz and 3 MHz
  - I^2C slave
  - SPI master and SPI slave
  - Watchdog and sleep timers
  - Internal voltage reference
  - Integrated supervisory circuit

Logic Block Diagram



More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

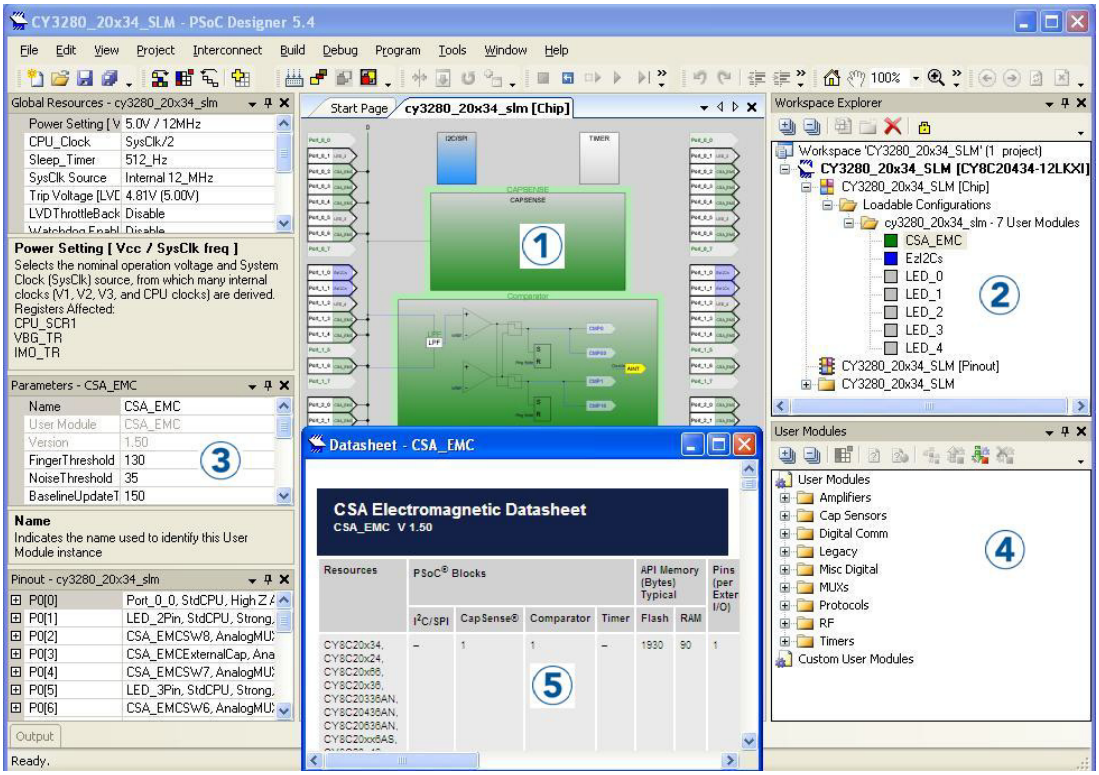
- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4. In addition, PSoC Designer offers a device selection tool at the time of creating a new project.
- Application Notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
  - AN64846 – Getting Started With CapSense
  - CY8C20x34 CapSense® Design Guide
  - AN2397 – CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
  - PSoC® CY8C20x24, CY8C20x34 Family Technical Reference Manual
- Development Kits:
  - CY3280-20x34 Universal CapSense Controller Kit features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
  - CY3280-SLM Linear Slider Module Kit consists of five CapSense buttons, one linear slider (with ten sensors) and five LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x34 kit.
  - CY3280-BBM Universal CapSense Prototyping Module Kit provides access to every signal routed to the 44-pin connector on the attached controller board including CY3280-20x34 kit.
- Programming
  - PSoC supports a number of different programming modes and tools. For more information see the General Programming page.

PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



Contents

PSoC Functional Overview

The PSoC family consists of many *Programmable System-on-Chips with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog and digital blocks and programmable interconnect. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture for this device family, as shown in Figure 2, consists of three main areas: the Core, the System Resources, and the CapSense Analog System. A common versatile bus enables connection between I/O and the analog system. Each CY8C20x34 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 general purpose I/O (GPIO) are also included. The GPIO provide access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, IMO, and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a two MIPS, 8-bit Harvard-architecture microprocessor.

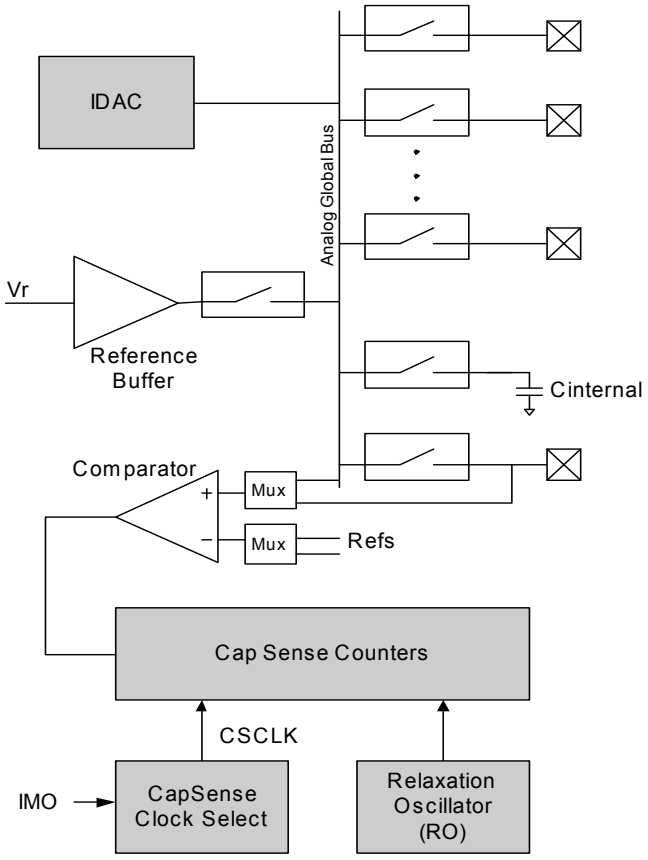
System Resources provide additional capability such as a configurable I^2C slave or SPI master-slave communication interface and various system resets supported by the M8C.

The Analog System consists of the CapSense PSoC block and an internal 1.8 V analog reference. Together they support capacitive sensing of up to 28 inputs.

CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple ports.

Figure 2. Analog System Block Diagram



Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces such as sliders and touch pads
- Chip-wide mux that enables analog input from any I/O pin
- Crosspoint connection between any I/O pin combinations

Additional System Resources

System Resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource follow:

- The I^2C slave or SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires run at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.8 V reference provides an absolute reference for capacitive sensing.
- The 5 V maximum input, 3 V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K

Notes
1. Limited analog functionality
2. Two analog blocks and one CapSense®.

Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

Pin Information

This section describes, lists, and illustrates the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC device pins and pinout configurations.

The CY8C20x34 PSoC device is available in a variety of packages that are listed and shown in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

8-Pin SOIC Pinout

Figure 3. CY8C20134-12SXI 8-Pin SOIC Pinout

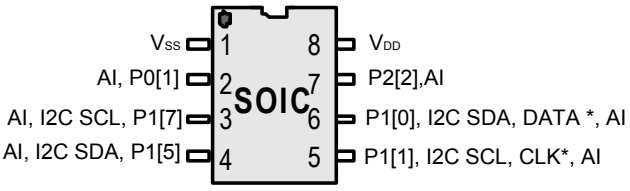


Table 2. Pin Definitions – CY8C20134 8-Pin (SOIC)

Pin No.	Digital	Analog	Name	Description
1	Power		V_{SS}	Ground connection
2	I/O	I	P0[1]	Analog column mux input, integrating input
3	I/O	I	P1[7]	I2C serial clock (SCL)
4	I/O	I	P1[5]	I2C serial data (SDA)
5	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK
6	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA
7	I/O	I	P2[2]	Analog column mux input
8	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

16-Pin SOIC Pinout

Figure 4. CY8C20234-12SXI 16-Pin SOIC Pinout

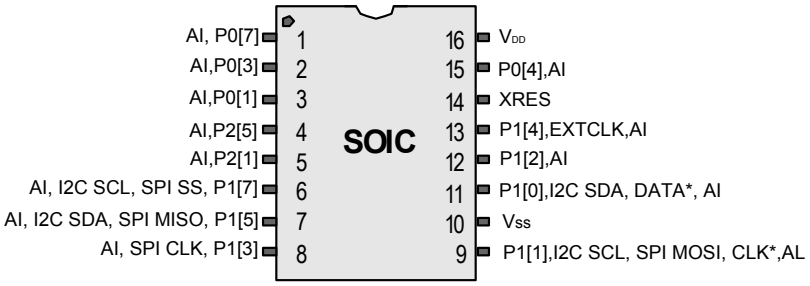


Table 3. Pin Definitions – CY8C20234 16-Pin (SOIC)

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[3]	Analog column mux input and column input, integrating input
3	I/O	I	P0[1]	Analog column mux input, integrating input
4	I/O	I	P2[5]	Analog column mux input
5	I/O	I	P2[1]	Analog column mux input
6	I/O	I	P1[7]	I2C serial clock (SCL), SPI SS
7	I/O	I	P1[5]	I2C serial data (SDA),SPI MISO
8	I/O	I	P1[3]	Analog column mux input, SPI CLK
9	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK,SPI MOSI
10	Power		V_{SS}	Ground connection
11	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA
12	I/O	I	P1[2]	Analog column mux input
13	I/O	I	P1[4]	Analog column mux input, optional external clock input (EXTCLK)
14	I/O	I	XRES	XRES
15	I/O	I	P0[4]	Analog column mux input
16	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

48-Pin OCD Part Pinout

The 48-Pin QFN part table and pin diagram is for the CY8C20000 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. It is NOT available for production.

Figure 5. CY8C20000 48-Pin OCD PSoC Device

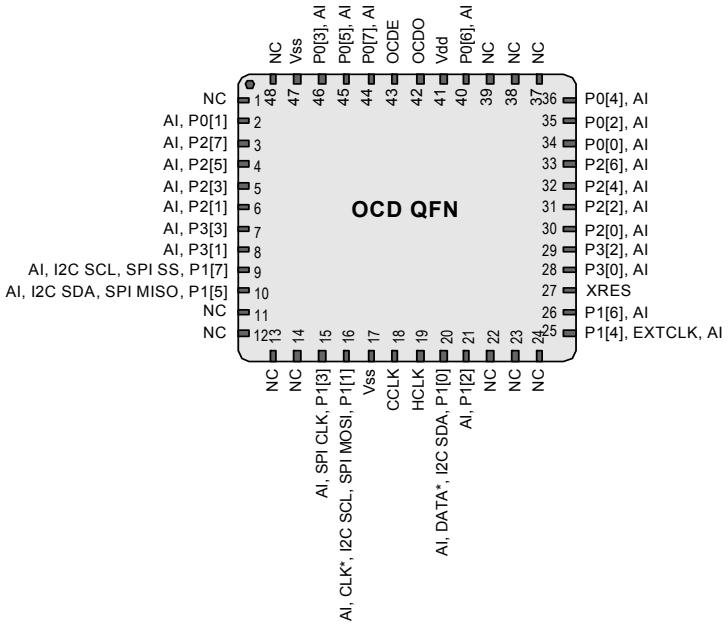


Table 4. Pin Definitions – CY8C20000 48-Pin OCD (QFN) [3]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P0[1]	
3	I/O	I	P2[7]	
4	I/O	I	P2[5]	
5	I/O	I	P2[3]	
6	I/O	I	P2[1]	
7	I/O	I	P3[3]	
8	I/O	I	P3[1]	
9	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
10	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
11	I/O	I	P0[1]	
12			NC	No connection
13			NC	No Connection
14			NC	No Connection
15			NC	SPI CLK
16	I_{OH}	I	P1[3]	CLK[4], I^2C SCL, SPI MOSI
17	I_{OH}	I	P1[1]	Ground connection

Notes
3. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
4. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

Table 4. Pin Definitions – CY8C20000 48-Pin OCD (QFN) [3]

Pin No.	Digital	Analog	Name	Description
18	Power		V_{SS}	OCD CPU clock output
19			CCLK	OCD high speed clock output
20			HCLK	DATA[5], I^2C SDA
21	I_{OH}	I	P1[0]	
22	I_{OH}	I	P1[2]	No connection
23			NC	No connection
24			NC	No connection
25			NC	Optional external clock input (EXTCLK)
26	I_{OH}	I	P1[4]	
27	I_{OH}	I	P1[6]	Active high external reset with internal pull-down
28	Input		XRES	
29	I/O	I	P3[0]	
30	I/O	I	P3[2]	
31	I/O	I	P2[0]	
32	I/O	I	P2[2]	
33	I/O	I	P2[4]	
34	I/O	I	P2[6]	
35	I/O	I	P0[0]	
36	I/O	I	P0[2]	
37			NC	No connection
38			NC	No connection
39			NC	No connection
40	I/O	I	P0[6]	Analog bypass
41	Power		V_{DD}	Supply voltage
42			OCDO	OCD odd data output
43			OCDE	OCD even data I/O
44	I/O	I	P0[7]	
45	I/O	I	P0[5]	
46	I/O	I	P0[3]	Integrating Input
47	Power		V_{SS}	Ground connection
48			NC	No connection
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive.

Note
5. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

16-Pin Part Pinout

Figure 6. CY8C20234 16-Pin PSoC Device

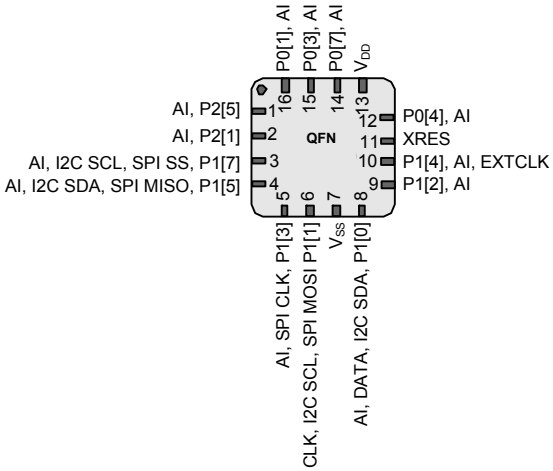


Table 5. Pin Definitions – CY8C20234 16-Pin (QFN no e-pad)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[1]	
3	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
5	I_{OH}	I	P1[3]	SPI CLK
6	I_{OH}	I	P1[1]	CLK[6], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection
8	I_{OH}	I	P1[0]	DATA[6], I^2C SDA
9	I_{OH}	I	P1[2]	
10	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	
15	I/O	I	P0[3]	Integrating Input
16	I/O	I	P0[1]	

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
6. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

24-Pin Part Pinout

Figure 7. CY8C20334 24-Pin PSoC Device

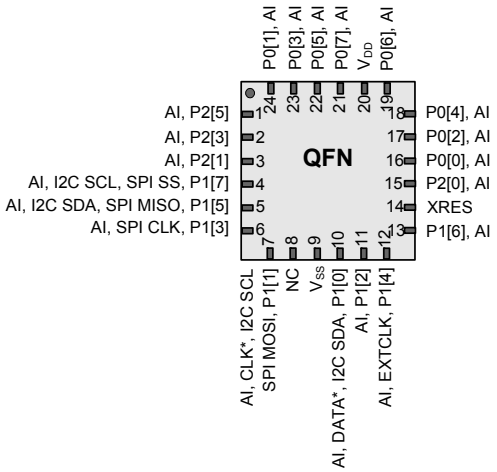


Table 6. Pin Definitions – CY8C20334 24-Pin (QFN) [7]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
5	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
6	I_{OH}	I	P1[3]	SPI CLK
7	I_{OH}	I	P1[1]	CLK[8], I^2C SCL, SPI MOSI
8			NC	No Connection
9	Power		V_{SS}	Ground Connection
10	I_{OH}	I	P1[0]	DATA[8], I^2C SDA
11	I_{OH}	I	P1[2]	
12	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
13	I_{OH}	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down
15	I/O	I	P2[0]	
16	I/O	I	P0[0]	
17	I/O	I	P0[2]	
18	I/O	I	P0[4]	
19	I/O	I	P0[6]	Analog bypass
20	Power		V_{DD}	Supply voltage
21	I/O	I	P0[7]	
22	I/O	I	P0[5]	
23	I/O	I	P0[3]	Integrating input
24	I/O	I	P0[1]	
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Notes
7. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
8. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

32-Pin Part Pinout

Figure 8. CY8C20434 32-Pin PSoC Device

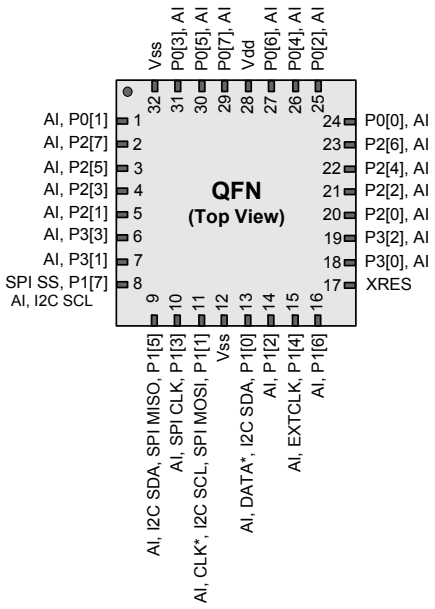


Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) [9]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[1]	
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	
4	I/O	I	P2[3]	
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
9	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
10	I_{OH}	I	P1[3]	SPI CLK
11	I_{OH}	I	P1[1]	CLK[10], I^2C SCL, SPI MOSI
12	Power		V_{SS}	Ground Connection[11]
13	I_{OH}	I	P1[0]	DATA[10], I^2C SDA
14	I_{OH}	I	P1[2]	
15	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
16	I_{OH}	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down

Notes
9. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
10. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.
11. All V_{SS} pins should be brought out to one common GND plane.

Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) [9]

Pin No.	Type		Name	Description
	Digital	Analog		
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	
25	I/O	I	P0[2]	
26	I/O	I	P0[4]	
27	I/O	I	P0[6]	Analog bypass
28	Power		V_{DD}	Supply voltage
29	I/O	I	P0[7]	
30	I/O	I	P0[5]	
31	I/O	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[12]
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA high output drive.

Note
12. All V_{SS} pins should be brought out to one common GND plane.

28-Pin Part Pinout

Figure 9. CY8C20534 28-Pin PSoC Device

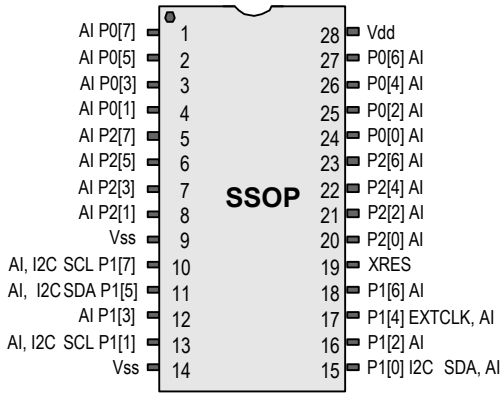


Table 8. Pin Definitions – CY8C20534 28-Pin (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input and column output
3	I/O	I	P0[3]	Analog column mux input and column output, integrating input
4	I/O	I	P0[1]	Analog column mux input, integrating input
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		V_{SS}	Ground connection[13]
10	I/O	I	P1[7]	I2C serial clock (SCL)
11	I/O	I	P1[5]	I2C serial data (SDA)
12	I/O	I	P1[3]	
13	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK[14]
14	Power		V_{SS}	Ground connection
15	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA[14]
16	I/O	I	P1[2]	
17	I/O	I	P1[4]	Optional external clock input (EXTCLK)
18	I/O	I	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I	P0[2]	Analog column mux input
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

Notes
13. All V_{SS} pins should be brought out to one common GND plane.
14. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

30-Ball Part Pinout

Figure 10. CY8C20634 30-Ball PSoC Device

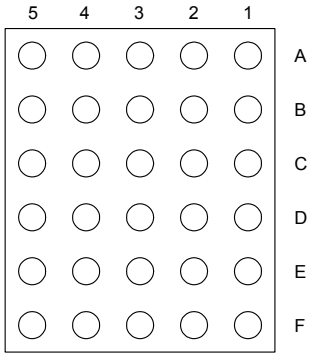


Table 9. 30-Ball Part Pinout (WLCSP)

Pin No.	Type		Name	Description
	Digital	Analog		
A1	Power		V_{DD}	Supply voltage
A2	I/O	I	P0[6]	Analog bypass
A3	I/O	I	P0[4]	
A4	I/O	I	P0[3]	Integrating input
A5	I/O	I	P2[7]	
B1	I/O	I	P0[2]	
B2	I/O	I	P0[0]	
B3	I/O	I	P2[6]	
B4	I/O	I	P0[5]	
B5	I/O	I	P0[1]	
C1	I/O	I	P2[4]	
C2	I/O	I	P2[2]	
C3	I/O	I	P3[1]	
C4	I/O	I	P0[7]	
C5	I/O	I	P2[1]	
D1	I/O	I	P2[0]	
D2	I/O	I	P3[0]	
D3	I/O	I	P3[2]	
D4	I_{OH}	I	P1[1]	CLK[15], I^2C SCL, SPI MOSI
D5	I/O	I	P2[3]	
E1	Input		XRES	Active high external reset with internal pull-down
E2	I_{OH}	I	P1[6]	
E3	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
E4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
E5	I/O	I	P2[5]	
F1	Power		V_{SS}	Ground connection[16]
F2	I_{OH}	I	P1[2]	
F3	I_{OH}	I	P1[0]	DATA[15], I^2C SDA
F4	I_{OH}	I	P1[3]	SPI CLK
F5	I_{OH}	I	P1[7]	I^2C SCL, SPI SS

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

Notes
15. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.
16. All V_{SS} pins should be brought out to one common GND plane.

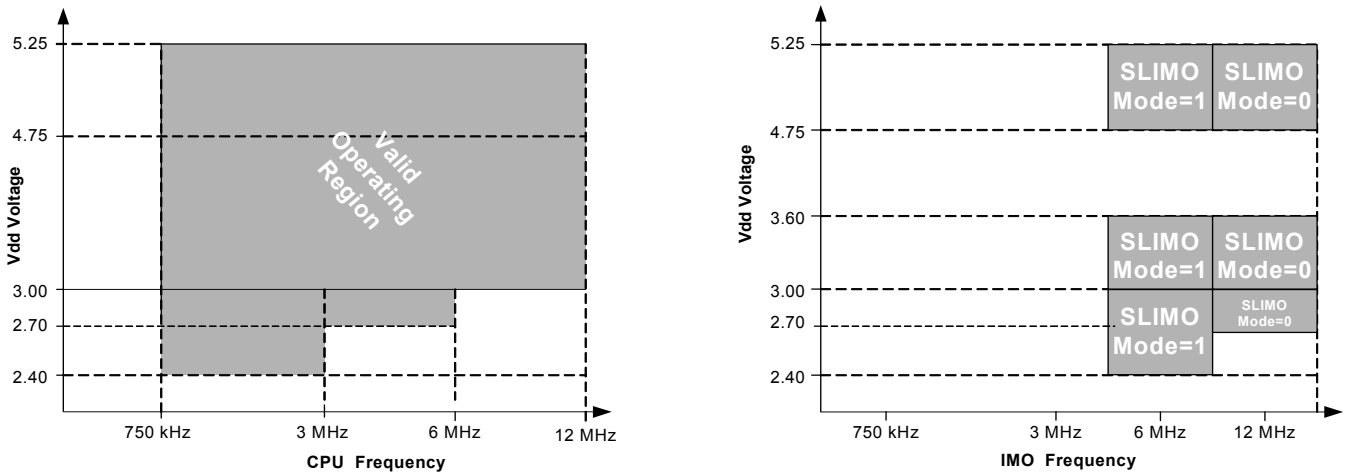
Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC devices. For the latest electrical specifications, check the most recent datasheet by visiting the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C as specified, except where mentioned.

Refer to Table 19 on page 25 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 11. Voltage versus CPU Frequency and IMO Frequency Trim Options



Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	–55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrades reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch-up current	–	–	200	mA	

Operating Temperature

Table 11. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 16 on page 23. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0V to 3.6V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 12. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See Table 16 on page 23.
I_{DD12}	Supply current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz.
I_{DD6}	Supply current, IMO = 6 MHz	–	1	1.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz
I_{SB27}	Sleep (mode) current with POR, LVD, Sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C
I_{SB}	Sleep (mode) current with POR, LVD, Sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C

DC GPIO Specifications

Unless otherwise noted, Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or Table 14 for 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only.

Table 13. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High output voltage Port 1 pins with 3.0 V LDO regulator enabled	2.7	3.0	3.3	V	I_{OH} < 10 µA, V_{DD} ≥ 3.1 V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High output voltage Port 1 pins with 3.0 V LDO regulator enabled	2.2	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os.

Table 13. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OH7}	High output voltage Port 1 pins with 2.4 V LDO regulator enabled	2.1	2.4	2.7	V	I_{OH} < 10 µA, $V_{DD} \geq$ 3.0 V , maximum of 20 mA source current in all I/Os.
V_{OH8}	High output voltage Port 1 pins with 2.4 V LDO regulator enabled	2.0	–	–	V	I_{OH} < 200 µA, $V_{DD} \geq$ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH9}	High output voltage Port 1 pins with 1.8 V LDO regulator enabled	1.6	1.8	2.0	V	I_{OH} < 10 µA 3.0V ≤ V_{DD} ≤ 3.6 V 0 °C ≤ T_A ≤ 85 °C Maximum of 20 mA source current in all I/Os.
V_{OH10}	High output voltage Port 1 pins with 1.8 V LDO regulator enabled	1.5	–	–	V	I_{OH} < 100 µA. 3.0V ≤ V_{DD} ≤ 3.6 V. 0 °C ≤ T_A ≤ 85 °C. Maximum of 20 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 20 mA, V_{DD} > 3.0 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH}	High level source current	–	–	20	mA	V_{OH} = V_{DD} – 0.9. See the limitations of the total current in the Notes for V_{OH}.
I_{OH2}	High level source current port 0, 2, or 3 pins	1	–	–	mA	V_{OH} = V_{DD} – 0.9, for the limitations of the total current and I_{OH} at other V_{OH} levels, see the Notes for V_{OH}.
I_{OH4}	High level source current port 1 Pins with LDO regulator disabled	5	–	–	mA	V_{OH} = V_{DD} – 0.9, for the limitations of the total current and I_{OH} at other V_{OH} levels, see the Notes for V_{OH}.
I_{OL}	Low level sink current	20	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the Notes for V_{OL}
V_{IL}	Input low voltage	–	–	0.8	V	3.6 V ≤ V_{DD} ≤ 5.25 V
V_{IH}	Input high voltage	2.0	–	–	V	3.6 V ≤ V_{DD} ≤ 5.25 V
V_H	Input hysteresis voltage	–	140	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C

Table 14. 2.7-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.
V_{OH2}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.5	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current port 1 Pins with LDO regulator disabled	2	–	–	mA	V_{OH} = V_{DD} – 0.5, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	10	–	–	mA	V_{OH} = .75 V, see the limitations of the total current in the note for V_{OL}
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	I_{OL} = 5 mA Maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]). 2.4 V ≤ V_{DD} < 3.6 V
V_{IL}	Input low voltage	–	–	0.75	V	2.4 V ≤ V_{DD} < 3.6 V
V_{IH1}	Input high voltage	1.4	–	–	V	2.4 V ≤ V_{DD} < 2.7 V
V_{IH2}	Input high voltage	1.6	–	–	V	2.7 V ≤ V_{DD} < 3.6 V
V_H	Input hysteresis voltage	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C

DC Analog Mux Bus Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 15. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω Ω	V_{DD} ≥ 2.7 V 2.4 V ≤ V_{DD} ≤ 2.7 V

DC POR and LVD Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively.
Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} is greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.39	2.45	2.51[17]	V	
V_{LVD1}	VM[2:0] = 001b	2.54	2.71	2.78[18]	V	
V_{LVD2}	VM[2:0] = 010b	2.75	2.92	2.99[19]	V	
V_{LVD3}	VM[2:0] = 011b	2.85	3.02	3.09	V	
V_{LVD4}	VM[2:0] = 100b	2.96	3.13	3.20	V	
V_{LVD5}	VM[2:0] = 101b	–	–	–	V	
V_{LVD6}	VM[2:0] = 110b	–	–	–	V	
V_{LVD7}	VM[2:0] = 111b	4.52	4.73	4.83	V	

Notes
17. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
18. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
19. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

DC Programming Specifications

Table 17 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM User Module are valid only within the range: 25 °C +/–20C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash write requirements outside of the 25 °C +/–20 °C temperature window.

Table 17. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[21]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[20]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

Notes
20. A maximum of 36 × 50,000 block endurance cycles is allowed. This is balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).
21. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V and 4.75 V to 5.25 V.

DC I²C Specifications

Table 18 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM user module are valid only within the range: 25 °C +/–20C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash Write requirements outside of the 25 °C +/–20 °C temperature window.

Table 18. DC I²C Specifications[22]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

AC Electrical Characteristics

AC Chip Level Specifications

Table 19, Table 20, and Table 21 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 19. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU frequency (3.3 V nominal)	0.75	–	12.6	MHz	12 MHz only for SLIMO Mode = 0.
F_{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	Internal main oscillator stability for 12 MHz (commercial temperature)[23]	11.4	12	12.6	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 0.
F_{IMO6}	Internal main oscillator stability for 6 MHz (commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	
t_{jit_IMO} [24]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1600	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	100	900	ps	

Notes
22. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the above specs.
23. 0 to 70 °C ambient, V_{DD} = 3.3 V.
24. Refer to Cypress Jitter Specifications Application Note – AN5054 at http://www.cypress.com for more information.