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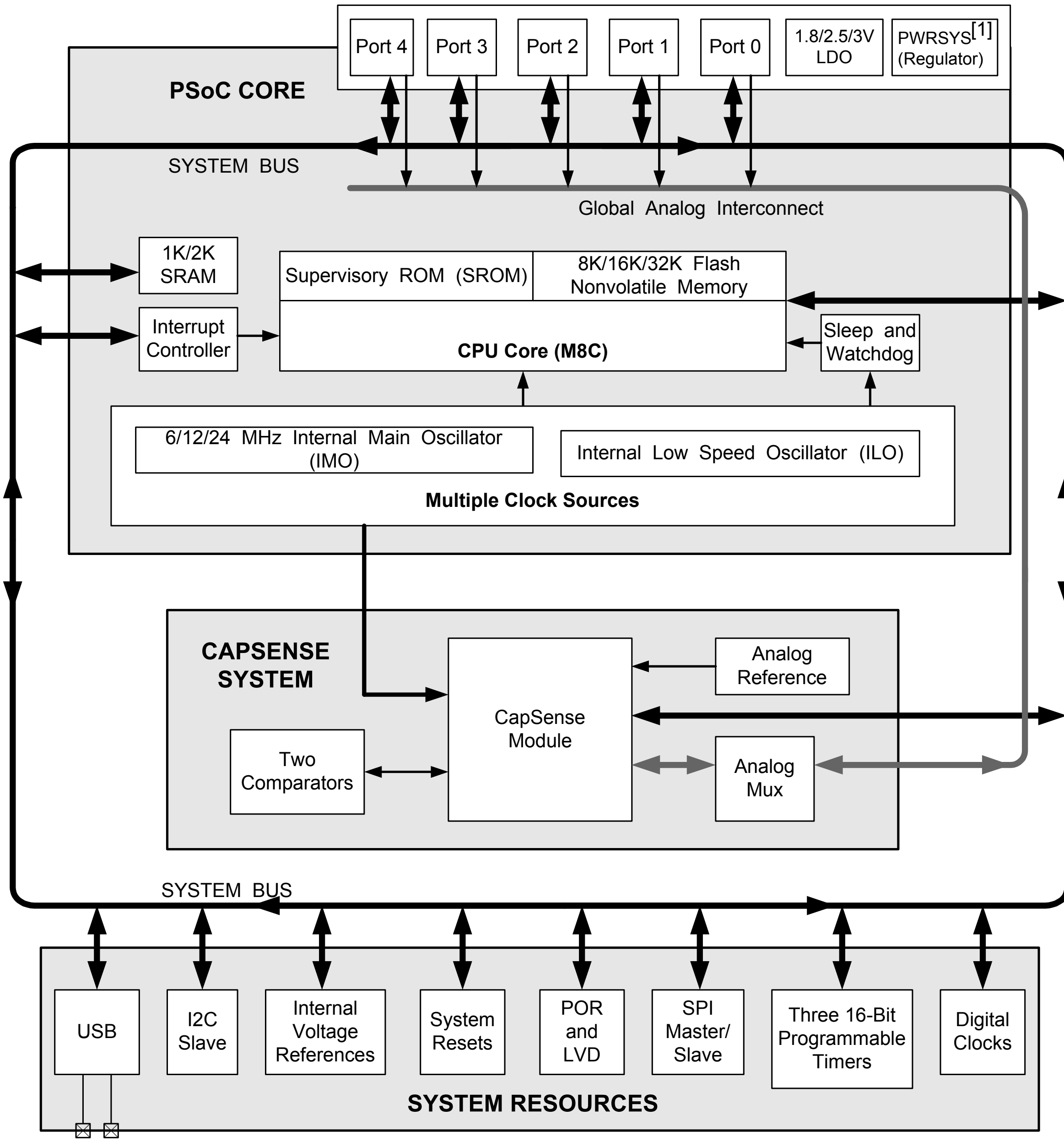
1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders

Features

- Low power CapSense® block with SmartSense Auto-tuning
  - Patented CSA_EMC, CSD sensing algorithms
  - SmartSense_EMC Auto-Tuning
    - Sets and maintains optimal sensor performance during run time
    - Eliminates system tuning during development and production
    - Compensates for variations in manufacturing process Low average power consumption – 28 µA/sensor in run time (wake-up and scan once every 125 ms)
- Powerful Harvard-architecture processor
  - M8C CPU with a max speed of 24 MHz
- Operating Range: 1.71 V to 5.5 V
  - Standby Mode 1.1 µA (Typ)
  - Deep Sleep 0.1 µA (Typ)
- Operating Temperature range: –40 °C to +85 °C
- Flexible on-chip memory
  - 8 KB flash, 1 KB SRAM
  - 16 KB flash, 2 KB SRAM
  - 32 KB flash, 2 KB SRAM
  - Read while Write with EEPROM emulation
  - 50,000 flash erase/write cycles
  - In-system programming simplifies manufacturing process
- Four Clock Sources
  - Internal main oscillator (IMO): 6/12/24 MHz
  - Internal low-speed oscillator (ILO) at 32 kHz for watchdog and sleep timers
  - External 32 KHz Crystal Oscillator
  - External Clock Input
- Programmable pin configurations
  - Up to 36 general-purpose I/Os (GPIOs) configurable as buttons or sliders
  - Dual mode GPIO (Analog inputs and Digital I/O supported)
  - High sink current of 25 mA per GPIO
    - Max sink current 120 mA for all GPIOs
  - Source Current
    - 5 mA on ports 0 and 1
    - 1 mA on ports 2,3 and 4
  - Configurable internal pull-up, high-Z and open drain modes
  - Selectable, regulated digital I/O on port 1
  - Configurable input threshold on port 1
- Versatile Analog functions
  - Internal analog bus supports connection of multiple sensors to form ganged proximity sensor
  - Internal Low-Dropout voltage regulator for high power supply rejection ratio (PSRR)
- Full-Speed USB
  - 12 Mbps USB 2.0 compliant
- Additional system resources
  - I2C Slave:
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
  - Configurable up to 12 MHz SPI master and slave
  - Three 16-bit timers
  - Watchdog and sleep timers
  - Integrated supervisory circuit
  - 10-bit incremental analog-to-digital converter (ADC) with internal voltage reference
  - Two general-purpose high speed, low power analog comparators
- Complete development tools
  - Free development tool (PSoC Designer™)
- Sensor and Package options
  - 10 Sensors – QFN 16, 24
  - 16 Sensors – QFN 24
  - 22 / 25 Sensors – QFN 32
  - 24 Sensors - WLCSP 30
  - 31 Sensors – SSOP 48
  - 33 Sensors – QFN 48

Errata: For information on silicon errata, see "Errata" on page 46. Details include trigger conditions, devices affected, and proposed workaround.

Logic Block Diagram



Note

1. Internal voltage regulator for internal circuitry

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4. In addition, PSoC Designer offers a device selection tool at the time of creating a new project.
- Application notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
  - AN64846: Getting Started With CapSense
  - AN73034: CY8C20xx6A/H/AS CapSense® Design Guide
  - AN2397: CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
  - PSoC® CY8C20xx6A/AS/L Family Technical Reference Manual
- Development Kits:
  - CY3280-20x66 Universal CapSense Controller Kit features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
  - CY3280-BMM Matrix Button Module Kit consists of eight CapSense sensors organized in a 4x4 matrix format to form 16 physical buttons and eight LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.
  - CY3280-BSM Simple Button Module Kit consists of ten CapSense buttons and ten LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.

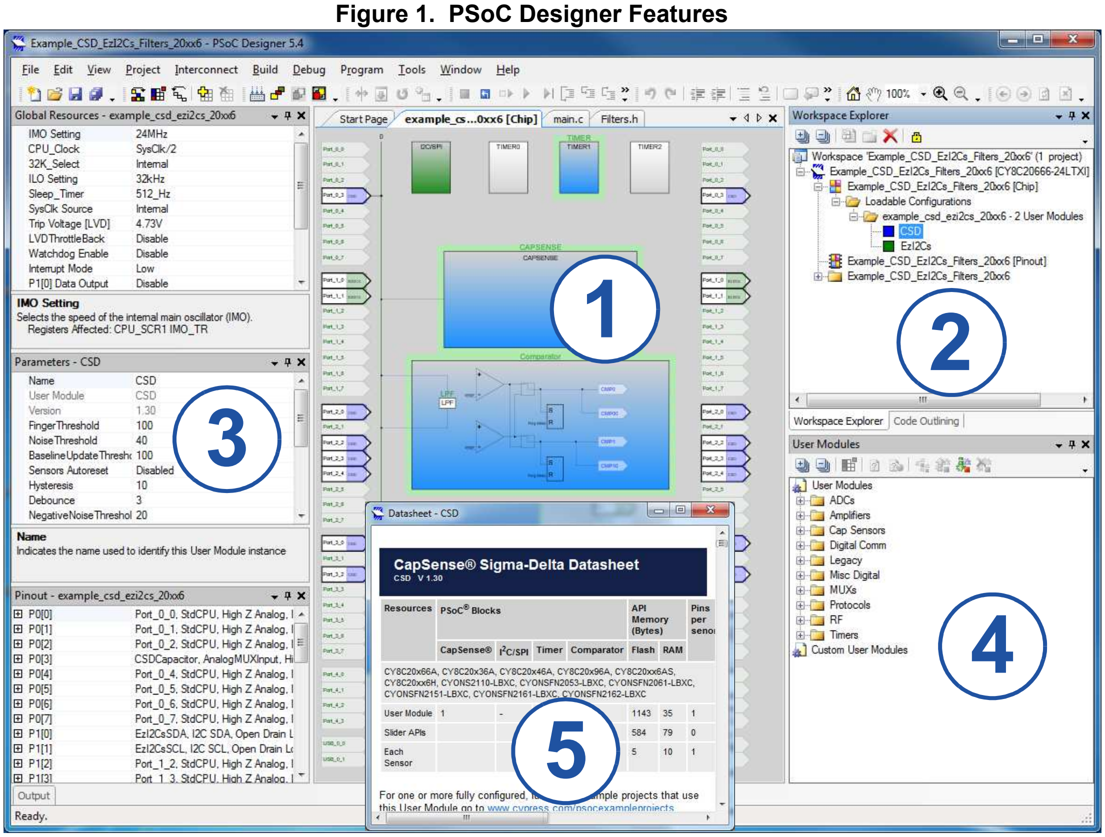
The CY3217-MiniProg1 and CY8CKIT-002 PSoC® MiniProg3 device provides an interface for flash programming.

PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



Contents

PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, consists of three main areas:

- The Core
- CapSense Analog System
- System Resources (including a full-speed USB port).

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20XX6A/S PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 GPIO are also included. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1 V or 1.2 V analog reference, which together support capacitive sensing of up to 33 inputs [2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

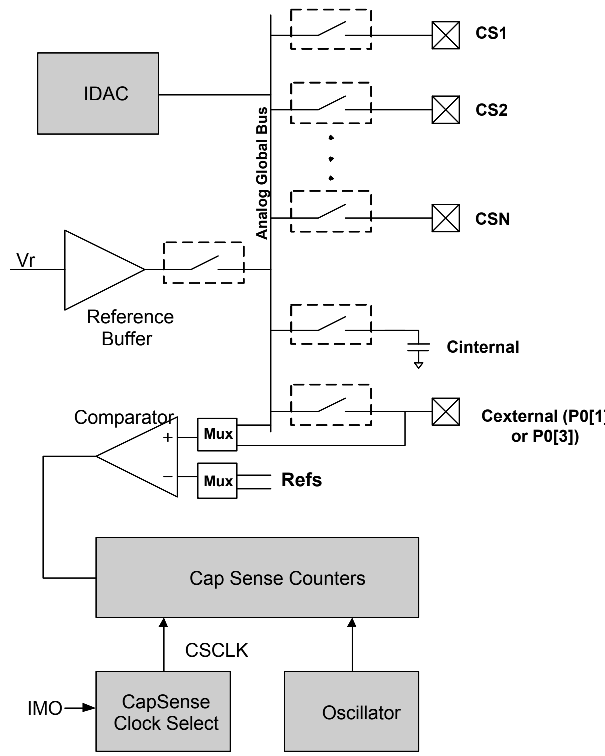
SmartSense

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides a robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

SmartSense_EMC

In addition to the SmartSense auto tuning algorithm to remove manual tuning of CapSense applications, SmartSense_EMC user module incorporates a unique algorithm to improve robustness of capacitive sensing algorithm/circuit against high frequency conducted and radiated noise. Every electronic device must comply with specific limits for radiated and conducted external noise and these limits are specified by regulatory bodies (for example, FCC, CE, U/L and so on). A very good PCB layout design, power supply design and system design is a mandatory for a product to pass the conducted and radiated noise tests. An ideal PCB layout, power supply design or system design is not often possible because of cost and form factor limitations of the product. SmartSense_EMC with superior noise immunity is well suited and handy for such applications to pass radiated and conducted noise test.

Figure 2. CapSense System Block Diagram



Note
2. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I^2C + 1 pin for modulator capacitor.

Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Additional System Resources

System resources provide additional capability, such as configurable USB and I^2C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I^2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20XX6A/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

CapSense Design Guides

Design Guides are an excellent introduction to the wide variety of possible CapSense designs. They are located at www.cypress.com/go/CapSenseDesignGuides.

Refer Getting Started with CapSense design guide for information on CapSense design and CY8C20XX6A/H/AS CapSense® Design Guide for specific information on CY8C20XX6A/AS CapSense controllers.

Silicon Errata

Errata documents known issues with silicon including errata trigger conditions, scope of impact, available workarounds and silicon revision applicability. Refer to Silicon Errata for the PSoC® CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families available at http://www.cypress.com/?rID=56239 for errata information on CY8C20xx6A/AS/H family of device. Compare errata document with datasheet for a complete functional description of device.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

6. Select user modules.
7. Configure user modules.
8. Organize and connect.
9. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pinouts

The CY8C20XX6A/S PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

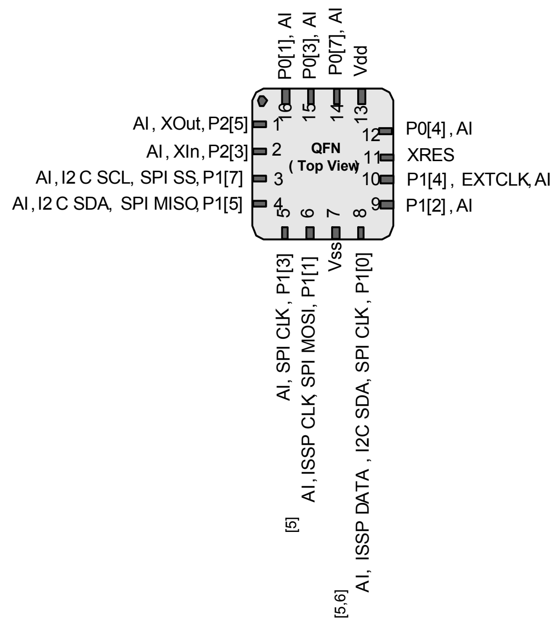
16-pin QFN (10 Sensing Inputs)[3, 4]

Table 1. Pin Definitions – CY8C20236A, CY8C20246A, CY8C20246AS PSoC Device

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I^2C SCL, SPI SS
4	IOHR	I	P1[5]	I^2C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK[5], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection[7]
8	IOHR	I	P1[0]	ISSP DATA[5], I^2C SDA, SPI CLK[6]
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	IOH	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 3. CY8C20236A, CY8C20246A, CY8C20246AS



Notes

3. 13 GPIOs = 10 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
4. No Center Pad.
5. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
6. Alternate SPI clock.
7. All VSS pins should be brought out to one common GND plane.

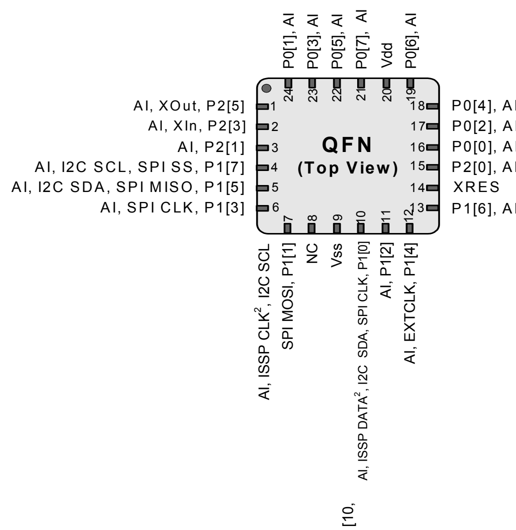
24-pin QFN (17 Sensing Inputs) [8]

Table 2. Pin Definitions – CY8C20336A, CY8C20346A, CY8C20346AS [9]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I^2C SCL, SPI SS
5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[10], I^2C SCL, SPI MOSI
8			NC	No connection
9	Power		V_{SS}	Ground connection[12]
10	IOHR	I	P1[0]	ISSP DATA[10], I^2C SDA, SPI CLK[11]
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down
15	I/O	I	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Power		V_{DD}	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 4. CY8C20336A, CY8C20346A, CY8C20346AS



Notes

8. 20 GPIOs = 17 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
9. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
10. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
11. Alternate SPI clock.
12. All VSS pins should be brought out to one common GND plane.

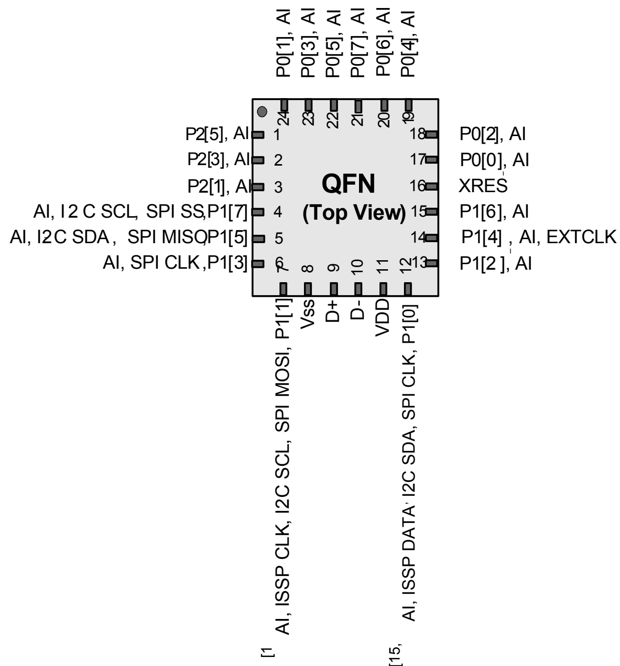
24-pin QFN (15 Sensing Inputs (With USB)) [13]

Table 3. Pin Definitions – CY8C20396A [14]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I^2C SCL, SPI SS
5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[15], I^2C SCL, SPI MOSI
8	Power		V_{SS}	Ground[17]
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Power		V_{DD}	Supply
12	IOHR	I	P1[0]	ISSP DATA[15], I^2C SDA, SPI CLK[16]
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET INPUT		XRES	Active high external reset with internal pull-down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V_{SS}	Center pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 5. CY8C20396A



Notes

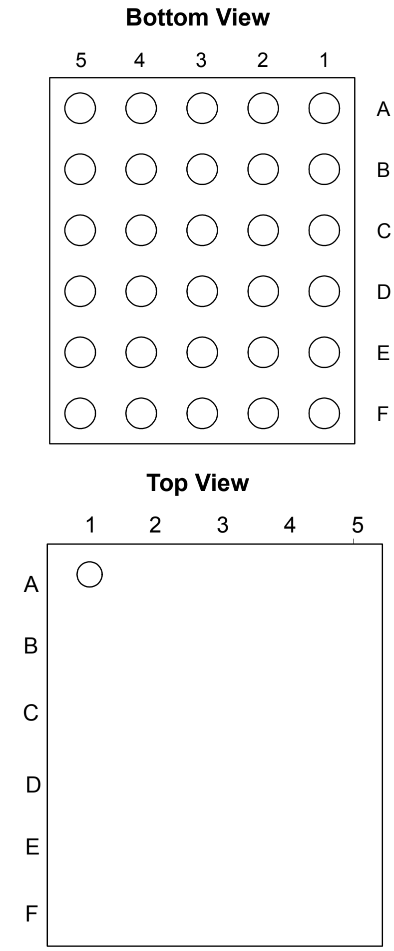
13. 20 GPIOs = 15 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
14. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
16. Alternate SPI clock.
17. All VSS pins should be brought out to one common GND plane.

30-ball WLCSP (24 Sensing Inputs) [18]

Table 4. Pin Definitions – CY8C20766A, CY8C20746A 30-ball WLCSP

Pin No.	Type		Name	Description
	Digital	Analog		
A1	IOH	I	P0[2]	
A2	IOH	I	P0[6]	
A3	Power		V_{DD}	Supply voltage
A4	IOH	I	P0[1]	Integrating Input
A5	I/O	I	P2[7]	
B1	I/O	I	P2[6]	
B2	IOH	I	P0[0]	
B3	IOH	I	P0[4]	
B4	IOH	I	P0[3]	Integrating Input
B5	I/O	I	P2[5]	Crystal Output (Xout)
C1	I/O	I	P2[2]	
C2	I/O	I	P2[4]	
C3	IOH	I	P0[7]	
C4	IOH	I	P0[5]	
C5	I/O	I	P2[3]	Crystal Input (Xin)
D1	I/O	I	P2[0]	
D2	I/O	I	P3[0]	
D3	I/O	I	P3[1]	
D4	I/O	I	P3[3]	
D5	I/O	I	P2[1]	
E1	Input		XRES	Active high external reset with internal pull-down
E2	IOHR	I	P1[6]	
E3	IOHR	I	P1[4]	Optional external clock input (EXT CLK)
E4	IOHR	I	P1[7]	I^2C SCL, SPI SS
E5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
F1	IOHR	I	P1[2]	
F2	IOHR	I	P1[0]	ISSP DATA[19], I^2C SDA, SPI CLK[20]
F3	Power		V_{SS}	Supply ground[21]
F4	IOHR	I	P1[1]	ISSP CLK[19], I^2C SCL, SPI MOSI
F5	IOHR	I	P1[3]	SPI CLK

Figure 6. CY8C20766A 30-ball WLCSP



Notes

18. 27 GPIOs = 24 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
19. On power-up , the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
20. Alternate SPI clock.
21. All VSS pins should be brought out to one common GND plane.

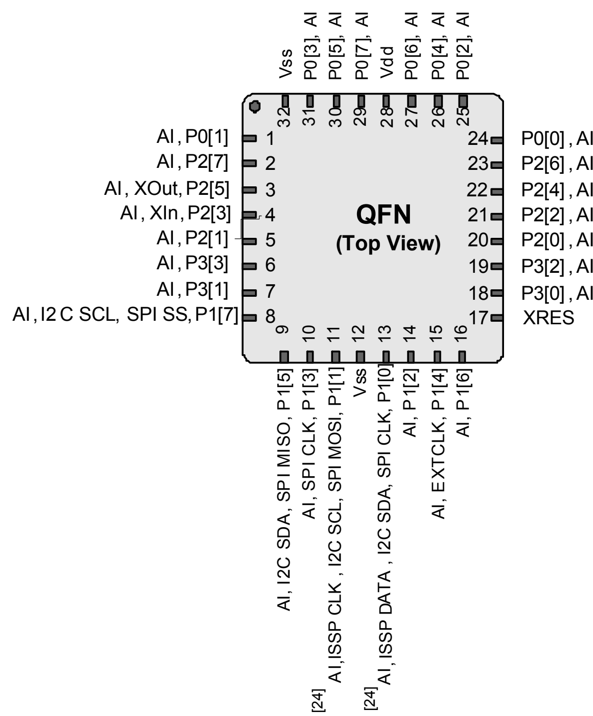
32-pin QFN (25 Sensing Inputs) [22]

Table 5. Pin Definitions – CY8C20436A, CY8C20446A, CY8C20446AS, CY8C20466A, CY8C20466AS[23]

Pin No.	Type: Digital	Type: Analog	Name	Description
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I^2C SCL, SPI SS
9	IOHR	I	P1[5]	I^2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK[24], I^2C SCL, SPI MOSI.
12	Power		V_{SS}	Ground connection[26]
13	IOHR	I	P1[0]	ISSP DATA[24], I^2C SDA, SPI CLK[25]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V_{DD}	Supply voltage
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[26]
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 7. CY8C20436A, CY8C20446A, CY8C20446AS, CY8C20466A, CY8C20466AS



Notes

22. 28 GPIOs = 25 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
23. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
24. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
25. Alternate SPI clock.
26. All VSS pins should be brought out to one common GND plane.

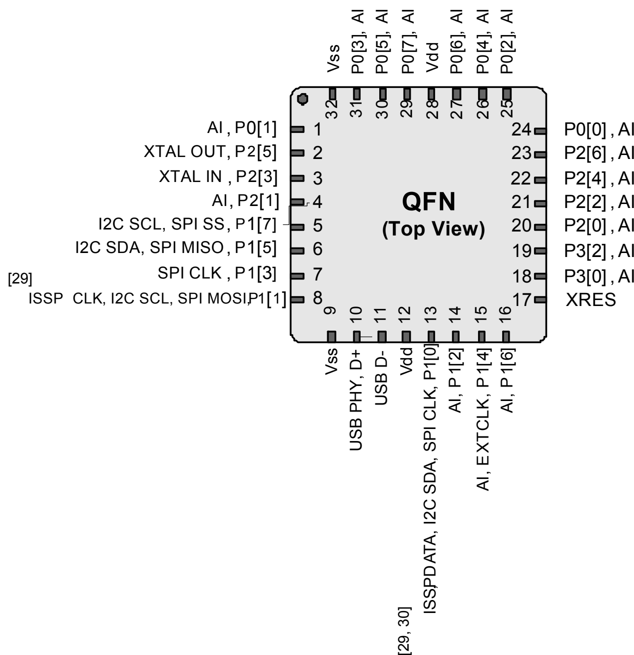
32-pin QFN (22 Sensing Inputs (With USB)) [27]

Table 6. Pin Definitions – CY8C20496A[28]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating Input
2	I/O	I	P2[5]	XTAL Out
3	I/O	I	P2[3]	XTAL In
4	I/O	I	P2[1]	
5	IOHR	I	P1[7]	I2C SCL, SPI SS
6	IOHR	I	P1[5]	I2C SDA, SPI MISO
7	IOHR	I	P1[3]	SPI CLK
8	IOHR	I	P1[1]	ISSP CLK[29], I2C SCL, SPI MOSI
9	Power		V_{SS}	Ground Pin[31]
10	I		D+	USB D+
11	I		D-	USB D-
12	Power		V_{DD}	Power pin
13	IOHR	I	P1[0]	ISSP DATA[29], I2C SDA, SPI CLKI[30]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V_{DD}	Power Pin
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating Input
32	Power		V_{SS}	Ground Pin[31]

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 8. CY8C20496A



Notes

27. 27 GPIOs = 22 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
28. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
29. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
30. Alternate SPI clock.
31. All VSS pins should be brought out to one common GND plane.

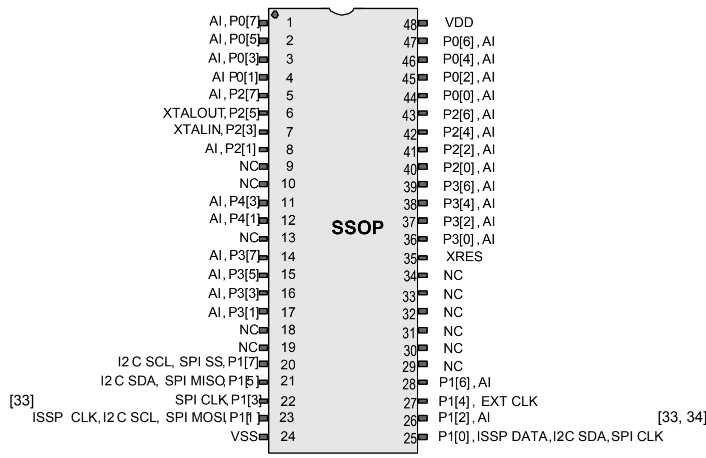
48-pin SSOP (31 Sensing Inputs) [32]

Table 7. Pin Definitions – CY8C20536A, CY8C20546A, and CY8C20566A[33]

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[7]	
2	IOH	I	P0[5]	
3	IOH	I	P0[3]	Integrating Input
4	IOH	I	P0[1]	Integrating Input
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	XTAL Out
7	I/O	I	P2[3]	XTAL In
8	I/O	I	P2[1]	
9			NC	No connection
10			NC	No connection
11	I/O	I	P4[3]	
12	I/O	I	P4[1]	
13			NC	No connection
14	I/O	I	P3[7]	
15	I/O	I	P3[5]	
16	I/O	I	P3[3]	
17	I/O	I	P3[1]	
18			NC	No connection
19			NC	No connection
20	IOHR	I	P1[7]	I^2C SCL, SPI SS
21	IOHR	I	P1[5]	I^2C SDA, SPI MISO
22	IOHR	I	P1[3]	SPI CLK
23	IOHR	I	P1[1]	ISSP CLK[33], I^2C SCL, SPI MOSI
24			V_{SS}	Ground Pin[35]
25	IOHR	I	P1[0]	ISSP DATA[33], I^2C SDA, SPI CLK[34]
26	IOHR	I	P1[2]	
27	IOHR	I	P1[4]	Optional external clock input (EXT CLK)
28	IOHR	I	P1[6]	
29			NC	No connection
30			NC	No connection
31			NC	No connection
32			NC	No connection
33			NC	No connection
34			NC	No connection
35			XRES	Active high external reset with internal pull-down
36	I/O	I	P3[0]	
37	I/O	I	P3[2]	
38	I/O	I	P3[4]	
39	I/O	I	P3[6]	
40	I/O	I	P2[0]	
41	I/O	I	P2[2]	
42	I/O	I	P2[4]	
43	I/O	I	P2[6]	
44	IOH	I	P0[0]	
45	IOH	I	P0[2]	
46	IOH	I	P0[4]	VREF
47	IOH	I	P0[6]	
48	Power		V_{DD}	Power Pin

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

Figure 9. CY8C20536A, CY8C20546A, and CY8C20566A



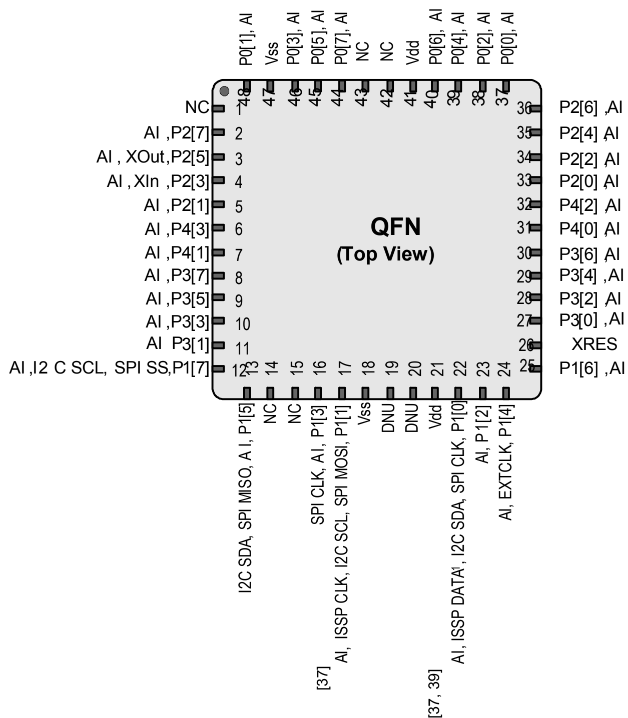
Notes

32. 34 GPIOs = 31 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
33. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
34. Alternate SPI clock.
35. All VSS pins should be brought out to one common GND plane.

48-pin QFN (33 Sensing Inputs) [36]

Table 8. Pin Definitions – CY8C20636A[37, 38]

Figure 10. CY8C20636A



Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[37], I^2C SCL, SPI MOSI
18	Power		V_{SS}	Ground connection[40]
19			DNU	
20			DNU	
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[37], I^2C SDA, SPI CLK[39]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection[40]
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Notes

36. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
37. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
38. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal
39. Alternate SPI clock.
40. All VSS pins should be brought out to one common GND plane.

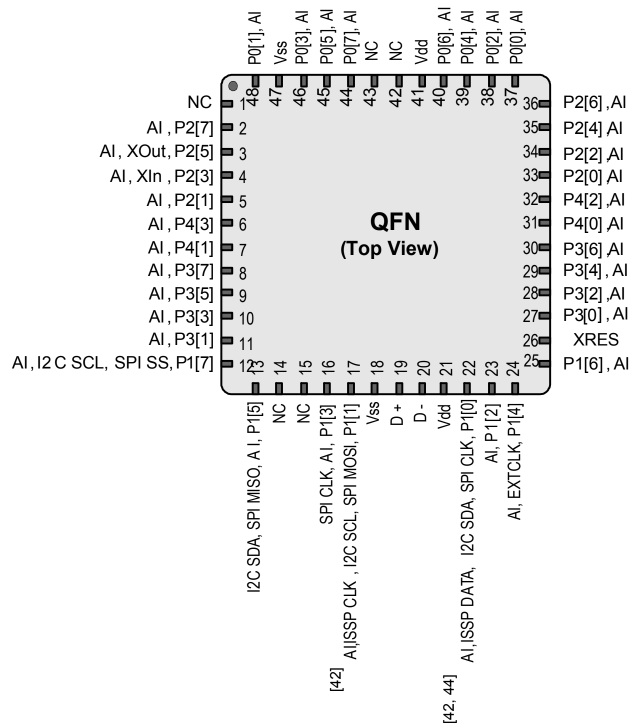
48-pin QFN (33 Sensing Inputs (With USB)) [41]

Table 9. Pin Definitions – CY8C20646A, CY8C20646AS, CY8C20666A, CY8C20666AS [42, 43]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[42], I^2C SCL, SPI MOSI
18	Power		V_{SS}	Ground connection[45]
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[42], I^2C SDA, SPI CLK[44]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection[45]
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 11. CY8C20646A, CY8C20646AS, CY8C20666A, CY8C20666AS



Notes

41. 38 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
42. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
43. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
44. Alternate SPI clock.
45. All VSS pins should be brought out to one common GND plane.

48-pin QFN (OCD) (33 Sensing Inputs) [46]

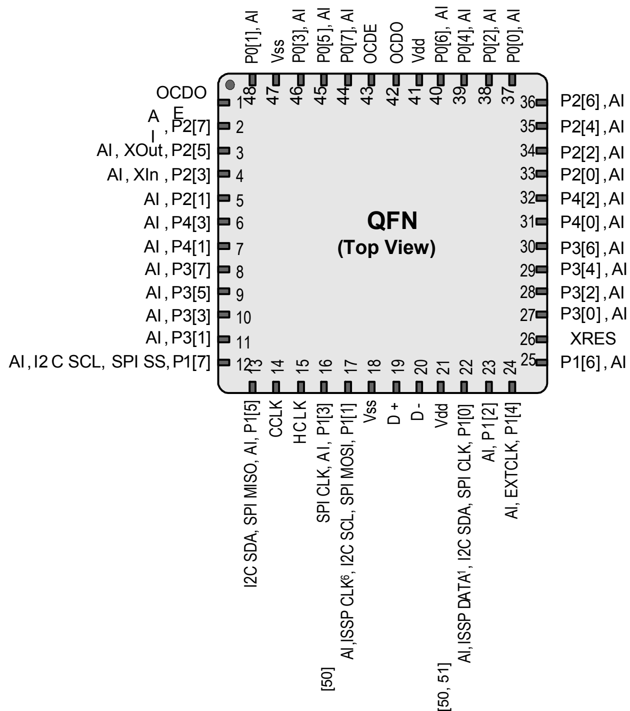
The 48-pin QFN part is for the CY8C20066A On-Chip Debug (OCD). Note that this part is only used for in-circuit debugging.

Table 10. Pin Definitions – CY8C20066A [47, 48]

Pin No.	Digital	Analog	Name	Description
1[49]			OCDOE	OCD mode direction pin
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14[49]			CCLK	OCD CPU clock output
15[49]			HCLK	OCD high speed clock output
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK[50], I^2C SCL, SPI MOSI
18	Power		V_{SS}	Ground connection[52]
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[50], I^2C SDA, SPI CLK[51]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42[49]			OCDO	OCD even data I/O
43[49]			OCDE	OCD odd data output
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection[52]
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 12. CY8C20066A



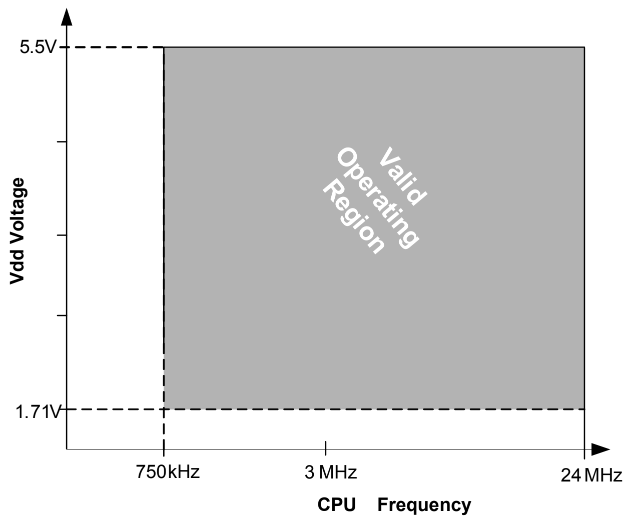
Notes

46. 38 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
47. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
48. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
49. This pin (associated with OCD part only) is required for connecting the device to ICE-Cube In-Circuit Emulator for firmware debugging purpose. To know more about the usage of ICE-Cube, refer to CY3215-DK PSoC® IN-CIRCUIT EMULATOR KIT GUIDE.
50. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
51. Alternate SPI clock.
52. All VSS pins should be brought out to one common GND plane.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20XX6A/S PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at http://www.cypress.com/psoc.

Figure 13. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	+25	+125	°C
V_{DD}	Supply voltage relative to V_{SS}	–	–0.5	–	+6.0	V
V_{IO}	DC input voltage	–	V_{SS} – 0.5	–	V_{DD} + 0.5	V
V_{IOZ}[53]	DC voltage applied to tristate	–	V_{SS} – 0.5	–	V_{DD} + 0.5	V
I_{MIO}	Maximum current into any port pin	–	–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	–	–	V
LU	Latch-up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 12. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature	–	–40	–	+85	°C
T_C	Commercial temperature range	–	0	–	70	°C
T_J	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the Thermal Impedances on page 38. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

Note

53. Port1 pins are hot-swap capable with I/O configured in High-Z mode, and pin input voltage above V_{DD}.

DC Chip-Level Specifications

Table 13 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD} [54, 55, 56, 57]	Supply voltage	No USB activity. Refer the table "DC POR and LVD Specifications" on page 26	1.71	–	5.50	V
V_{DDUSB} [54, 55, 56, 57]	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
		USB activity, USB regulator bypassed	3.15	3.3	3.60	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \le 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	2.88	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \le 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.71	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \le 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.16	1.80	mA
$I_{DDAVG10}$	Average supply current per sensor	One sensor scanned at 10 mS rate	–	250	–	µA
$I_{DDAVG100}$	Average supply current per sensor	One sensor scanned at 100 mS rate	–	25	–	µA
$I_{DDAVG500}$	Average supply current per sensor	One sensor scanned at 500 mS rate	–	7	–	µA
I_{SB0} [58, 59, 60, 61, 62, 63]	Deep sleep current	$V_{DD} \le 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.05	µA
I_{SB1} [58, 59, 60, 61, 62, 63]	Standby current with POR, LVD and sleep timer	$V_{DD} \le 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	µA
I_{SBI2C} [58, 59, 60, 61, 62, 63]	Standby current with I^2C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	µA

Notes

54. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
55. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that V_{DD} falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register.
    For the referenced registers, refer to the *CY8C20X36 Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1V/ms.
56. For USB mode, the V_{DD} supply for bus-powered application should be limited to 4.35 V–5.35 V. For self-powered application, V_{DD} should be 3.15 V–3.45 V.
57. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.
58. Errata: When the device is put to sleep in Standby or I2C_USB Mode and the bandgap circuit is refreshed less frequently than every 8 ms (default), the device may not come out of sleep when a sleep-ending input is received. For more information, see the "Errata" on page 46.
59. Errata: The I2C block exhibits occasional data and bus corruption errors when the I2C master initiates transactions while the device is in or out of transition of sleep mode. For more information, see the "Errata" on page 46.
60. Errata: When programmable timer 0 is used in "one-shot" mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the "Errata" on page 47.
61. Errata: When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the "Errata" on page 47.
62. Errata: If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the "Errata" on page 48.
63. Errata: Device wakes up from sleep when an analog interrupt is trigger. For more information, see the "Errata" on page 48.

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 C and are for design guidance only.

Table 14. 3.0 V to 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} ≤ 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH5}	High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out	I_{OH} < 10 µA, V_{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, V_{DD} > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.80	V
V_{IH}	Input high voltage	–	2.00	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (Absolute Value)	–	–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT3.3}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT3.3}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.4	–	–	V
$V_{ILLVT5.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT5.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.7	–	–	V

Table 15. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.40	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V_{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.72	V
V_{IH}	Input high voltage	–	1.40	–		V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT2.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	V	–	
$V_{IHLVT2.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2		–	V

Table 16. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 100 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OL}	Low output voltage	I_{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V_{IL}	Input low voltage	–	–	–	0.30 × V_{DD}	V

Table 16. 1.71 V to 2.4 V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input high voltage	–	0.65 × V_{DD}	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

Table 17. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{USBI}	USB D+ pull-up resistance	With idle bus	900	–	1575	Ω
R_{USBA}	USB D+ pull-up resistance	While receiving traffic	1425	–	3090	Ω
V_{OHUSB}	Static output high	–	2.8	–	3.6	V
V_{OLUSB}	Static output low	–	–	–	0.3	V
V_{DI}	Differential input sensitivity	–	0.2	–		V
V_{CM}	Differential input common mode range	–	0.8	–	2.5	V
V_{SE}	Single ended receiver threshold	–	0.8	–	2.0	V
C_{IN}	Transceiver capacitance	–	–	–	50	pF
I_{IO}	High Z state data line leakage	On D+ or D- line	–10	–	+10	µA
R_{PS2}	PS/2 pull-up resistance	–	3000	5000	7000	Ω
R_{EXT}	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus	–	–	–	800	Ω
R_{GND}	Resistance of initialization switch to V_{SS}	–	–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V_{DD}	0.0	–	1.8	V
I_{LPC}	LPC supply current	–	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	–	3	30	mV

Comparator User Module Electrical Specifications

Table 20 lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40 °C ≤ T_A ≤ 85 °C, 1.71 V ≤ V_{DD} ≤ 5.5 V.

Table 20. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to V_{DD} – 0.2 V	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	µA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range		–	0		1.5	V

ADC Electrical Specifications

Table 21. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	VREFADC	V
C_{IIN}	Input capacitance	–	–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^Resolution/Data Clock)	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^resolution/data clock)	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (V_{DD} > 3.0 V)	–	24	–	dB
		PSRR (V_{DD} < 3.0 V)	–	30	–	dB