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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

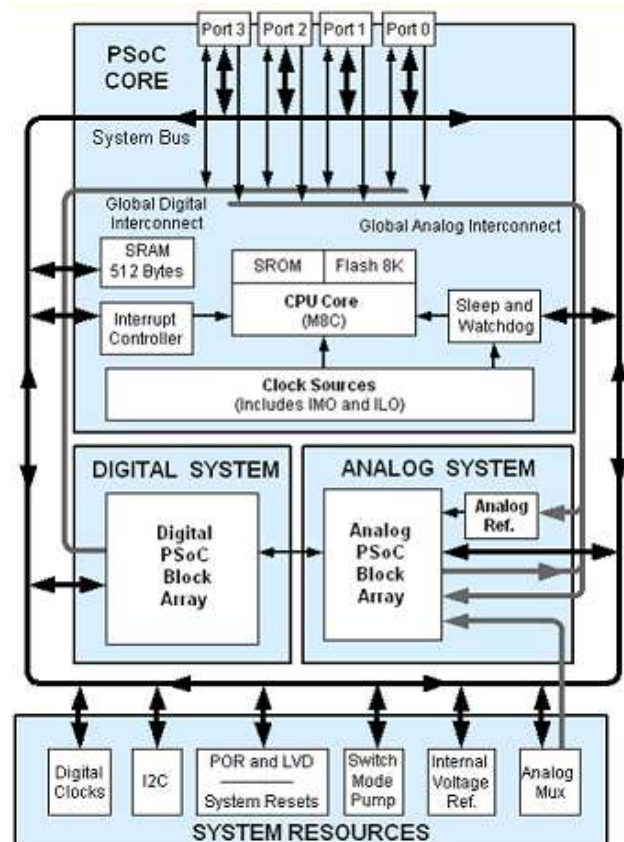


## Features

- Powerful Harvard-architecture processor
  - M8C processor speeds up to 24 MHz
  - Low power at high speed
  - Operating voltage: 2.4 V to 5.25 V
  - Operating voltages down to 1.0 V using on-chip switch mode pump (SMP)
  - Industrial temperature range: -40 °C to +85 °C
- Advanced peripherals (PSoC® blocks)
  - Four analog Type E PSoC blocks provide:
    - Two comparators with digital-to-analog converter (DAC) references
    - Single or dual 10-bit 28 channel analog-to-digital converters (ADC)
  - Four digital PSoC blocks provide:
    - 8- to 32-bit timers, counters, and pulse width modulators (PWMs)
    - Cyclical redundancy check (CRC) and pseudo random sequence (PRS) modules
    - Full-duplex universal asynchronous receiver transmitter (UART), serial peripheral interface (SPI) master or slave
    - Connectable to all general purpose I/O (GPIO) pins
  - Complex peripherals by combining blocks
- Flexible on-chip memory
  - 8 KB flash program storage 50,000 erase/write cycles
  - 512 bytes static random access memory (SRAM) data storage
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Complete development tools
  - Free development software (PSoC Designer™)
  - Full-featured, in-circuit emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128-KB trace memory
- Precision, programmable clocking
  - Internal ±2.5% 24- / 48-MHz main oscillator [1]
  - Internal oscillator for watchdog and sleep
- Programmable pin configurations
  - 25-mA sink, 10-mA source on all GPIOs
  - Pull-up, pull-down, high Z, strong, or open-drain drive modes on all GPIOs

- Up to eight analog inputs on GPIOs
- Configurable interrupt on all GPIOs
- Versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O combinations
  - Capacitive sensing application capability
- Additional system resources
  - I<sup>2</sup>C [2] master, slave, and multi-master to 400 kHz
  - Watchdog and sleep timers
  - User-configurable low-voltage detection (LVD)
  - Integrated supervisory circuit
  - On-chip precision voltage reference

## Logic Block Diagram



**Errata:** For information on silicon errata, see "Errata" on page 49. Details include trigger conditions, devices affected, and proposed workaround.

### Notes

1. **Errata:** The worst case IMO frequency deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
2. **Errata:** The I<sup>2</sup>C block exhibits occasional data and bus corruption errors when the I<sup>2</sup>C master initiates transactions while the device is transitioning in to or out of sleep mode.

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article, [How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292](#). Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
  - Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
  - In addition, PSoC Designer includes a device selection tool.
  - Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
    - [Getting Started with PSoC® 1 – AN75320](#)
    - [PSoC® 1 - Getting Started with GPIO – AN2094](#)
    - [PSoC® 1 Analog Structure and Configuration – AN74170](#)
    - [PSoC® 1 Switched Capacitor Analog Blocks – AN2041](#)
    - [Selecting Analog Ground and Reference – AN2219](#)
- Note:** For CY8C21x34B devices related Application note please click [here](#).
- Development Kits:
    - [CY3210-PSoCEval1](#) supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
    - [CY3214-PSoCEvalUSB](#) features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

**Note:** For CY8C21x34B devices related Development Kits please click [here](#).

The [MiniProg1](#) and [MiniProg3](#) devices provide interfaces for flash programming and debug.

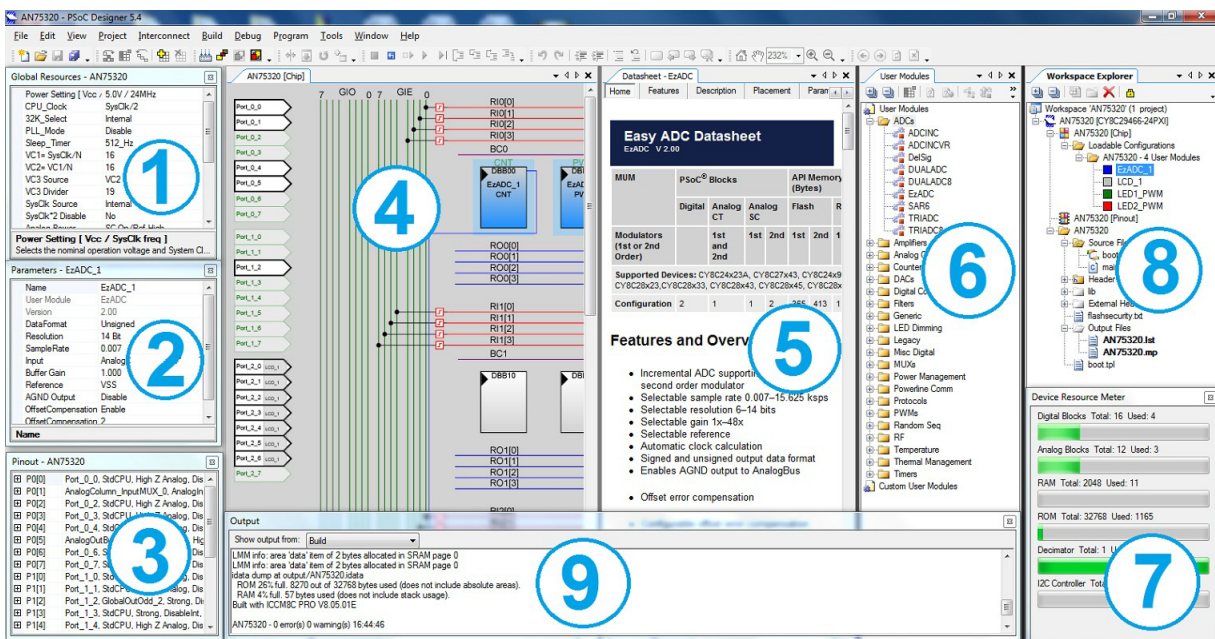
## PSoC Designer

[PSoC Designer](#) is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. [Figure 1](#) shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources** – all device hardware settings.
2. **Parameters** – the parameters of the currently selected User Modules.
3. **Pinout** – information related to device pins.
4. **Chip-Level Editor** – a diagram of the resources available on the selected chip.
5. **Datasheet** – the datasheet for the currently selected UM
6. **User Modules** – all available User Modules for the selected device.
7. **Device Resource Meter** – device resource usage for the current project configuration.
8. **Workspace** – a tree level diagram of files associated with the project.
9. **Output** – output from project build and debug operations.

**Note:** For detailed information on PSoC Designer, go to **PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide**.

**Figure 1. PSoC Designer Layout**



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## PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional MCU-based system components with one low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, shown in [Figure 2](#), consists of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow combining all of the device resources into a complete custom system. Each CY8C21x34 PSoC device includes four digital blocks and four analog blocks. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

### The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz [3]. The M8C is a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System resources provide these additional capabilities:

- Digital clocks for increased flexibility
- I<sup>2</sup>C [4] functionality to implement an I<sup>2</sup>C master and slave
- An internal voltage reference, multi-master, that provides an absolute value of 1.3 V to a number of PSoC subsystems
- A SMP that generates normal operating voltages from a single battery cell
- Various system resets supported by the M8C

The digital system consists of an array of digital PSoC blocks that may be configured into any number of digital peripherals. The digital blocks are connected to the GPIOs through a series of global buses. These buses can route any signal to any pin, freeing designs from the constraints of a fixed peripheral controller.

The analog system consists of four analog PSoC blocks, supporting comparators, and analog-to-digital conversion up to 10 bits of precision.

## The Digital System

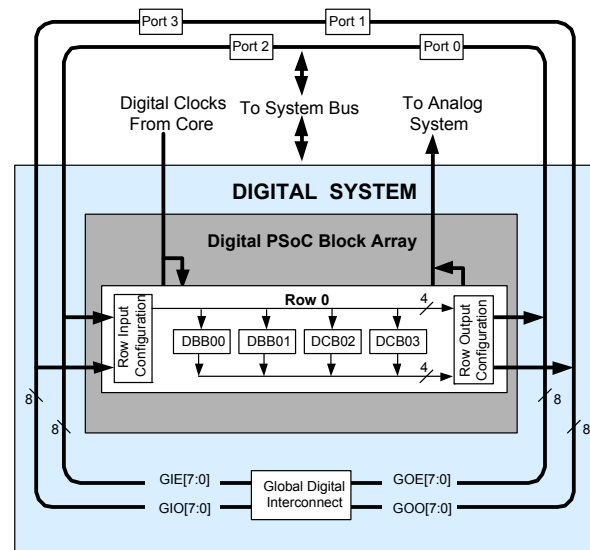
The digital system consists of four digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include:

- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8- with selectable parity
- Serial peripheral interface (SPI) master and slave
- I<sup>2</sup>C slave and multi-master [4]
- CRC/generator (8-bit)
- IrDA
- PRS generators (8-bit to 32-bit)

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in [Table 1 on page 6](#).

**Figure 2. Digital System Block Diagram**



### Notes

3. **Errata:** The worst case IMO frequency deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
4. **Errata:** The I<sup>2</sup>C block exhibits occasional data and bus corruption errors when the I<sup>2</sup>C master initiates transactions while the device is transitioning in to or out of sleep mode.

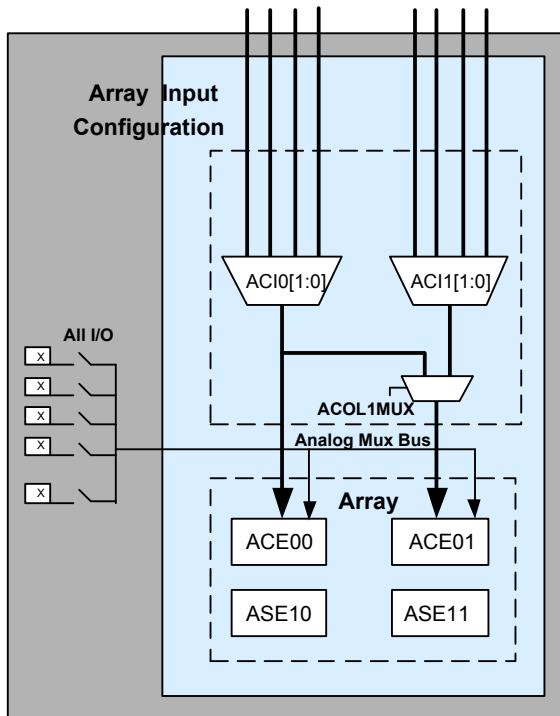
## The Analog System

The analog system consists of four configurable blocks that allow for the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are:

- ADCs (single or dual, with 8-bit or 10-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to two) with absolute (1.3 V) reference or 8-bit DAC reference
- 1.3-V reference (as a system resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. The CY8C21x34 devices provide limited functionality Type E analog blocks. Each column contains one CT Type E block and one SC Type E block. Refer to the *PSoC Technical Reference Manual* for detailed information on the CY8C21x34's Type E analog blocks.

**Figure 3. Analog System Block Diagram**



## The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins may be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Chip-wide mux that allows analog input from any I/O pin
- Crosspoint connection between any I/O pin combinations

## Additional System Resources

System resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch-mode pump, low-voltage detection, and power-on-reset (POR).

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I<sup>2</sup>C<sup>[5]</sup> module provides 100- and 400-kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch-mode pump generates normal operating voltages from a single 1.2-V battery cell, providing a low cost boost converter.
- Versatile analog multiplexer system.

### Note

5. **Errata:** The I<sup>2</sup>C block exhibits occasional data and bus corruption errors when the I2C master initiates transactions while the device is transitioning in to or out of sleep mode.

## PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. [Table 1](#) lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in [Table 1](#).

**Table 1. PSoC Device Characteristics**

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 <sup>[6]</sup>	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6 <sup>[6]</sup>	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6 <sup>[6]</sup>	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4 <sup>[6]</sup>	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4 <sup>[6]</sup>	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3 <sup>[6,7]</sup>	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3 <sup>[6,7]</sup>	up to 2 K	up to 32 K

## Getting Started

For in-depth information, along with detailed programming details, see the *PSoC<sup>®</sup> Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

## Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

## Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

## Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via [www.cypress.com](http://www.cypress.com),

covers a wide variety of topics and skill levels to assist you in your designs.

## CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

## Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

## Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

## Notes

- Limited analog functionality.
- Two analog blocks and one CapSense<sup>®</sup>.

## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I<sup>2</sup>C<sup>[8]</sup> slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

## PSoC Designer Software Subsystems

### Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

### Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers.** The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

### Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

### Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

### In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

#### Note

8. **Errata:** The I<sup>2</sup>C block exhibits occasional data and bus corruption errors when the I<sup>2</sup>C master initiates transactions while the device is transitioning in to or out of sleep mode.



## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select [User Modules](#).
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance

specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

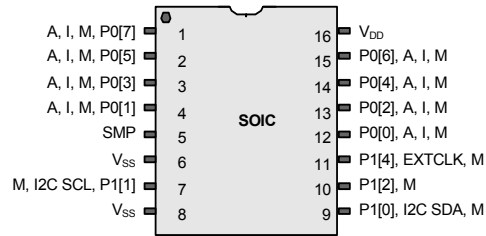
The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

## Pin Information

The CY8C21x34 PSoC device is available in a variety of packages which are listed in the following tables. Every port pin (labeled with a "P") is capable of Digital I/O and connection to the common analog bus. However, V<sub>SS</sub>, V<sub>DD</sub>, SMP, and XRES are not capable of Digital I/O.

### 16-pin Part Pinout

**Figure 4. CY8C21234 16-pin PSoC Device**



### CY8C21234 16-pin SOIC Pin Definitions

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	Power		SMP	Switch-mode pump (SMP) connection to required external components
6	Power		V <sub>SS</sub>	Ground connection <sup>[9]</sup>
7	I/O	M	P1[1]	I <sup>2</sup> C serial clock (SCL), ISSP-SCLK <sup>[10]</sup>
8	Power		V <sub>SS</sub>	Ground connection <sup>[9]</sup>
9	I/O	M	P1[0]	I <sup>2</sup> C serial data (SDA), ISSP-SDATA <sup>[10]</sup>
10	I/O	M	P1[2]	
11	I/O	M	P1[4]	Optional external clock input (EXTCLK)
12	I/O	I, M	P0[0]	Analog column mux input
13	I/O	I, M	P0[2]	Analog column mux input
14	I/O	I, M	P0[4]	Analog column mux input
15	I/O	I, M	P0[6]	Analog column mux input
16	Power		V <sub>DD</sub>	Supply voltage

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

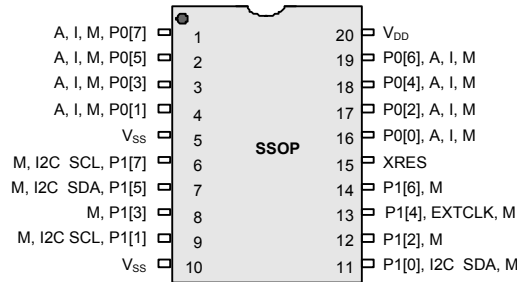
#### Notes

9. All V<sub>SS</sub> pins should be brought out to one common GND plane.

10. These are the ISSP pins, which are not High Z at POR. See the *PSoC Technical Reference Manual* for details.

**20-pin Part Pinout**

**Figure 5. CY8C21334 20-pin PSoC Device**



**CY8C21334 20-pin SSOP Pin Definitions**

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	Power		V <sub>SS</sub>	Ground connection <sup>[11]</sup>
6	I/O	M	P1[7]	I <sup>2</sup> C SCL
7	I/O	M	P1[5]	I <sup>2</sup> C SDA
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	I <sup>2</sup> C SCL, ISSP-SCLK <sup>[12]</sup>
10	Power		V <sub>SS</sub>	Ground connection <sup>[11]</sup>
11	I/O	M	P1[0]	I <sup>2</sup> C SDA, ISSP-SDATA <sup>[12]</sup>
12	I/O	M	P1[2]	
13	I/O	M	P1[4]	Optional external clock input (EXTCLK)
14	I/O	M	P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I, M	P0[0]	Analog column mux input
17	I/O	I, M	P0[2]	Analog column mux input
18	I/O	I, M	P0[4]	Analog column mux input
19	I/O	I, M	P0[6]	Analog column mux input
20	Power		V <sub>DD</sub>	Supply voltage

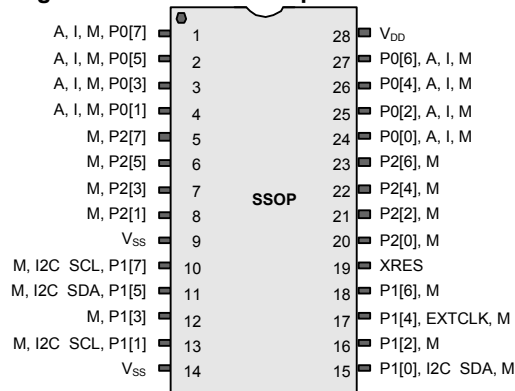
**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

**Notes**

- All V<sub>SS</sub> pins should be brought out to one common GND plane.
- These are the ISSP pins, which are not High Z at POR. See the *PSoC Technical Reference Manual* for details.

28-pin Part Pinout

Figure 6. CY8C21534 28-pin PSoC Device



CY8C21534 28-pin SSOP Pin Definitions

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input and column output
3	I/O	I, M	P0[3]	Analog column mux input and column output, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	I, M	P2[3]	Direct switched capacitor block input
8	I/O	I, M	P2[1]	Direct switched capacitor block input
9	Power		V <sub>SS</sub>	Ground connection <sup>[13]</sup>
10	I/O	M	P1[7]	I <sup>2</sup> C SCL
11	I/O	M	P1[5]	I <sup>2</sup> C SDA
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	I <sup>2</sup> C SCL, ISSP-SCLK <sup>[14]</sup>
14	Power		V <sub>SS</sub>	Ground connection <sup>[13]</sup>
15	I/O	M	P1[0]	I <sup>2</sup> C SDA, ISSP-SDATA <sup>[14]</sup>
16	I/O	M	P1[2]	
17	I/O	M	P1[4]	Optional external clock input (EXTCLK)
18	I/O	M	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I, M	P2[0]	Direct switched capacitor block input
21	I/O	I, M	P2[2]	Direct switched capacitor block input
22	I/O	M	P2[4]	
23	I/O	M	P2[6]	
24	I/O	I, M	P0[0]	Analog column mux input
25	I/O	I, M	P0[2]	Analog column mux input
26	I/O	I, M	P0[4]	Analog column mux input
27	I/O	I, M	P0[6]	Analog column mux input
28	Power		V <sub>DD</sub>	Supply voltage

LEGEND A: Analog, I: Input, O = Output, and M = Analog Mux Input.

Notes

13. All V<sub>SS</sub> pins should be brought out to one common GND plane.

14. These are the ISSP pins, which are not high Z at POR. See the *PSoC Technical Reference Manual* for details.

32-pin Part Pinout

Figure 7. CY8C21434 32-pin PSoC Device

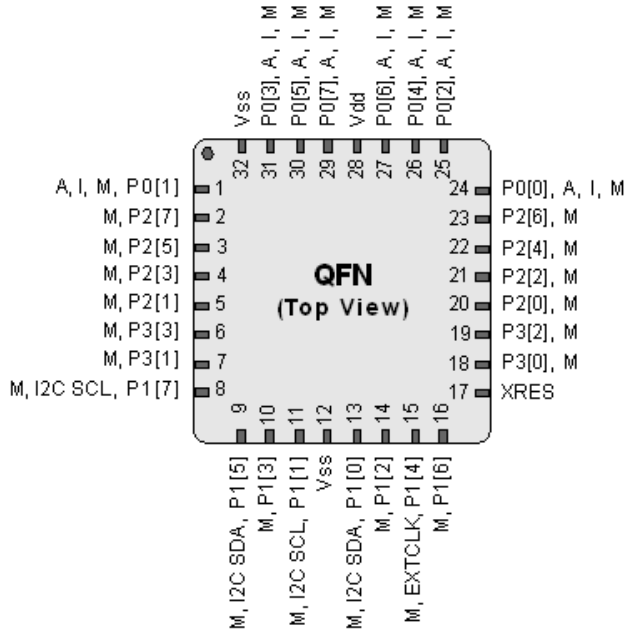


Figure 7. CY8C21634 32-pin PSoC Device

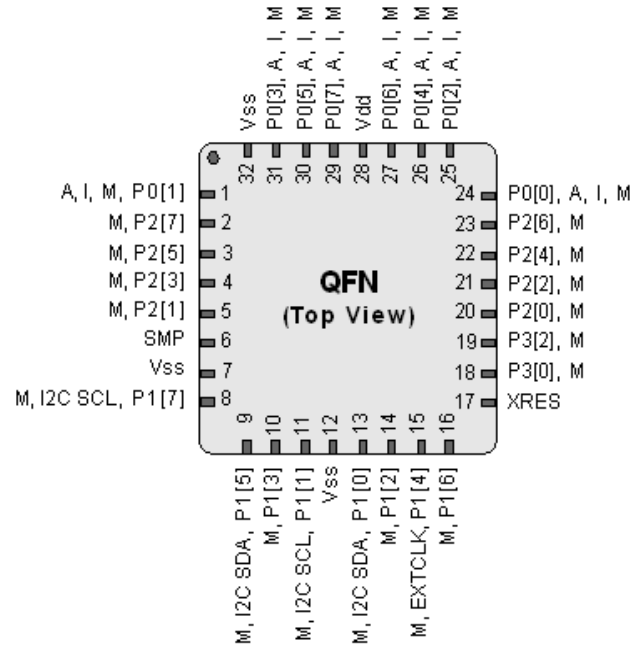


Figure 8. CY8C21434 32-pin Sawn PSoC Device Sawn

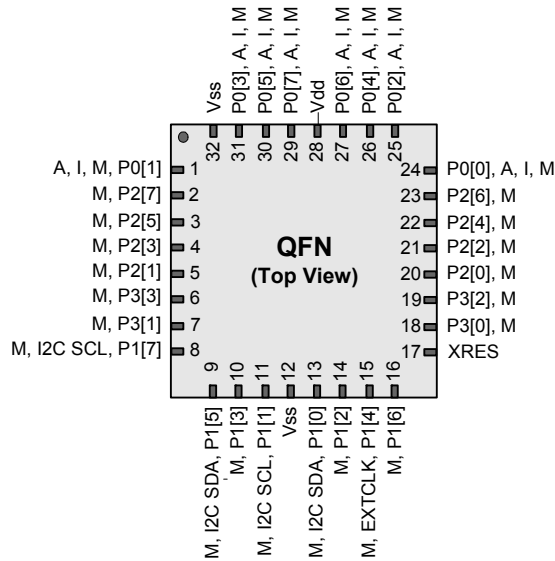
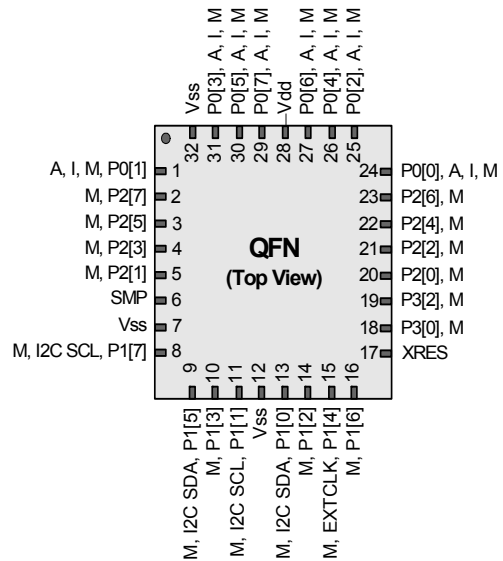


Figure 9. CY8C21634 32-pin Sawn PSoC Device Sawn



**CY8C21434/CY8C21634 32-pin QFN Pin Definitions**

Pin No. <sup>[15]</sup>	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[1]	Analog column mux input, integrating input
2	I/O	M	P2[7]	
3	I/O	M	P2[5]	
4	I/O	M	P2[3]	
5	I/O	M	P2[1]	
6	I/O	M	P3[3]	In CY8C21434 part
6	Power		SMP	SMP connection to required external components in CY8C21634 part
7	I/O	M	P3[1]	In CY8C21434 part
7	Power		V <sub>SS</sub>	Ground connection in CY8C21634 part <sup>[16]</sup>
8	I/O	M	P1[7]	I <sup>2</sup> C SCL
9	I/O	M	P1[5]	I <sup>2</sup> C SDA
10	I/O	M	P1[3]	
11	I/O	M	P1[1]	I <sup>2</sup> C SCL, ISSP-SCLK <sup>[17]</sup>
12	Power		V <sub>SS</sub>	Ground connection <sup>[16]</sup>
13	I/O	M	P1[0]	I <sup>2</sup> C SDA, ISSP-SDATA <sup>[17]</sup>
14	I/O	M	P1[2]	
15	I/O	M	P1[4]	Optional external clock input (EXTCLK)
16	I/O	M	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	M	P3[0]	
19	I/O	M	P3[2]	
20	I/O	M	P2[0]	
21	I/O	M	P2[2]	
22	I/O	M	P2[4]	
23	I/O	M	P2[6]	
24	I/O	I, M	P0[0]	Analog column mux input
25	I/O	I, M	P0[2]	Analog column mux input
26	I/O	I, M	P0[4]	Analog column mux input
27	I/O	I, M	P0[6]	Analog column mux input
28	Power		V <sub>DD</sub>	Supply voltage
29	I/O	I, M	P0[7]	Analog column mux input
30	I/O	I, M	P0[5]	Analog column mux input
31	I/O	I, M	P0[3]	Analog column mux input, integrating input
32	Power		V <sub>SS</sub>	Ground connection <sup>[16]</sup>

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

**Notes**

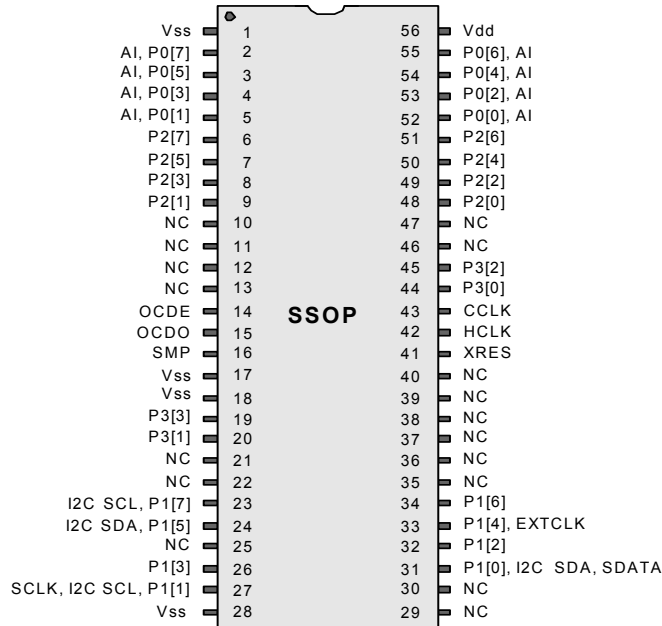
15. The center pad on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
16. All V<sub>SS</sub> pins should be brought out to one common GND plane.
17. These are the ISSP pins, which are not high Z at POR. See the *PSoC Technical Reference Manual* for details.

### 56-pin Part Pinout

The 56-pin SSOP part is for the CY8C21001 on-chip debug (OCD) PSoC device.

**Note** This part is only used for in-circuit debugging. It is NOT available for production.

Figure 10. CY8C21001 56-pin PSoC Device



### CY8C21001 56-pin SSOP Pin Definitions

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	Power		V <sub>SS</sub>	Ground connection <sup>[18]</sup>
2	I/O	I	P0[7]	Analog column mux input
3	I/O	I	P0[5]	Analog column mux input and column output
4	I/O	I	P0[3]	Analog column mux input and column output
5	I/O	I	P0[1]	Analog column mux input
6	I/O		P2[7]	
7	I/O		P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input
9	I/O	I	P2[1]	Direct switched capacitor block input
10			NC	No connection. Pin must be left floating
11			NC	No connection. Pin must be left floating
12			NC	No connection. Pin must be left floating
13			NC	No connection. Pin must be left floating
14	OCD		OCDE	OCD even data I/O
15	OCD		OCDO	OCD odd data output
16	Power		SMP	SMP connection to required external components
17	Power		V <sub>SS</sub>	Ground connection <sup>[18]</sup>
18	Power		V <sub>SS</sub>	Ground connection <sup>[18]</sup>
19	I/O		P3[3]	

**CY8C21001 56-pin SSOP Pin Definitions** (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
20	I/O		P3[1]	
21			NC	No connection. Pin must be left floating
22			NC	No connection. Pin must be left floating
23	I/O		P1[7]	I <sup>2</sup> C SCL
24	I/O		P1[5]	I <sup>2</sup> C SDA
25			NC	No connection. Pin must be left floating
26	I/O		P1[3]	I <sub>FMTEST</sub>
27	I/O		P1[1]	I <sup>2</sup> C SCL, ISSP-SCLK <sup>[19]</sup>
28	Power		V <sub>SS</sub>	Ground connection <sup>[18]</sup>
29			NC	No connection. Pin must be left floating
30			NC	No connection. Pin must be left floating
31	I/O		P1[0]	I <sup>2</sup> C SDA, ISSP-SDATA <sup>[19]</sup>
32	I/O		P1[2]	V <sub>FMTEST</sub>
33	I/O		P1[4]	Optional external clock input (EXTCLK)
34	I/O		P1[6]	
35			NC	No connection. Pin must be left floating
36			NC	No connection. Pin must be left floating
37			NC	No connection. Pin must be left floating
38			NC	No connection. Pin must be left floating
39			NC	No connection. Pin must be left floating
40			NC	No connection. Pin must be left floating
41	Input		XRES	Active high external reset with internal pull-down
42	OCD		HCLK	OCD high-speed clock output
43	OCD		CCLK	OCD CPU clock output
44	I/O		P3[0]	
45	I/O		P3[2]	
46			NC	No connection. Pin must be left floating
47			NC	No connection. Pin must be left floating
48	I/O	I	P2[0]	
49	I/O	I	P2[2]	
50	I/O		P2[4]	
51	I/O		P2[6]	
52	I/O	I	P0[0]	Analog column mux input
53	I/O	I	P0[2]	Analog column mux input and column output
54	I/O	I	P0[4]	Analog column mux input and column output
55	I/O	I	P0[6]	Analog column mux input
56	Power		V <sub>DD</sub>	Supply voltage

**LEGEND:** A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.

**Notes**

18. All V<sub>SS</sub> pins should be brought out to one common GND plane.
19. These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.



## Register Reference

This chapter lists the registers of the CY8C21x34 PSoC device. For detailed register information, see the [PSoC Technical Reference Manual](#).

### Register Conventions

The register conventions specific to this section are listed in [Table 2](#).

**Table 2. Register Conventions**

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

### Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XO1 bit in the Flag register (CPU\_F) determines which bank the user is currently in. When the XO1 bit is set to 1, the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are reserved and must not be accessed.

**Table 3. Register Map 0 Table: User Space**

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90		CUR_PP	D0	RW
	11			51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and must not be accessed.

# Access is bit specific.

**Table 4. Register Map 1 Table: Configuration Space**

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and must not be accessed.

# Access is bit specific.

## Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T <sub>STG</sub>	Storage temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrade reliability.
T <sub>BAKETEMP</sub>	Bake temperature	-	125	See package label	°C	
t <sub>BAKETIME</sub>	Bake time	See package label	-	72	Hours	
T <sub>A</sub>	Ambient temperature with power applied	-40	-	+85	°C	
V <sub>DD</sub>	Supply voltage on V <sub>DD</sub> relative to V <sub>SS</sub>	-0.5	-	+6.0	V	
V <sub>IO</sub>	DC input voltage	V <sub>SS</sub> - 0.5	-	V <sub>DD</sub> + 0.5	V	
V <sub>IOZ</sub>	DC voltage applied to tri-state	V <sub>SS</sub> - 0.5	-	V <sub>DD</sub> + 0.5	V	
I <sub>MIO</sub>	Maximum current into any port pin	-25	-	+50	mA	
ESD	Electrostatic discharge voltage	2000	-	-	V	Human body model ESD.
LU	Latch-up current	-	-	200	mA	

## Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T <sub>A</sub>	Ambient temperature	-40	-	+85	°C	
T <sub>J</sub>	Junction temperature	-40	-	+100	°C	The temperature rise from ambient to junction is package specific. See <a href="#">Table 29 on page 38</a> . You must limit the power consumption to comply with this requirement.

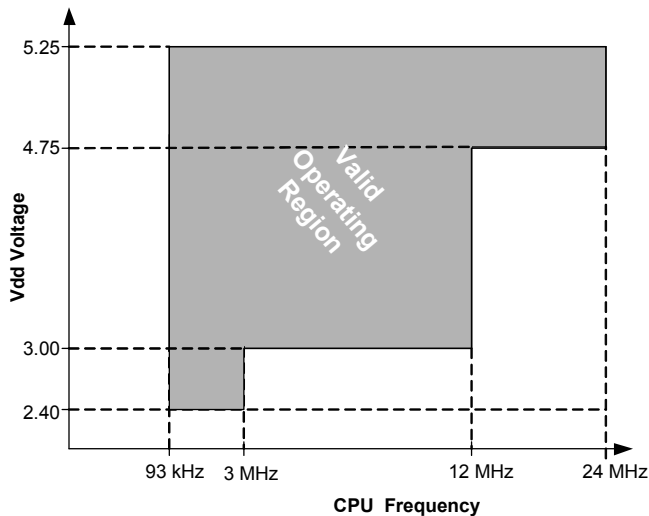
## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x34 PSoC device. For up-to-date electrical specifications, visit the Cypress web site at <http://www.cypress.com>.

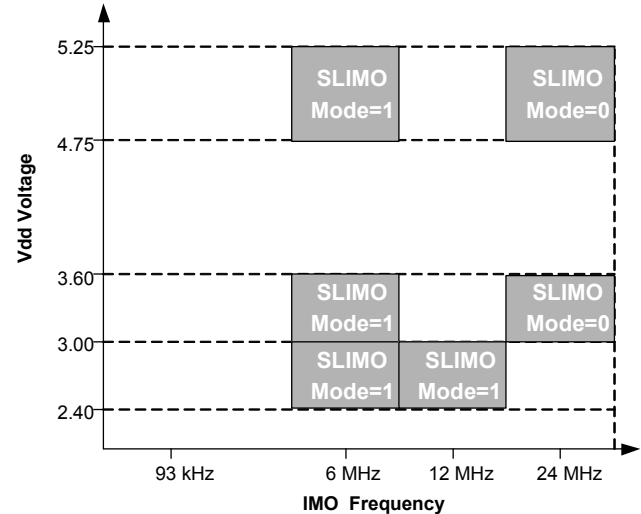
Specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$  and  $T_J \leq 100\text{ }^{\circ}\text{C}$  as specified, except where noted.

Refer to [Table 16 on page 26](#) for the electrical specifications for the IMO using SLIMO mode.

**Figure 11. Voltage versus CPU Frequency**



**Figure 14. IMO Frequency Trim Options**



## DC Electrical Characteristics

### DC Chip-Level Specifications

[Table 5](#) lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 5. DC Chip-level Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{DD}$	Supply voltage	2.40	–	5.25	V	See <a href="#">Table 13 on page 24</a>
$I_{DD}$	Supply current, IMO = 24 MHz	–	3	4	mA	Conditions are $V_{DD} = 5.0\text{ V}$ , $T_A = 25\text{ }^{\circ}\text{C}$ , CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz
$I_{DD3}$	Supply current, IMO = 6 MHz using SLIMO mode.	–	1.2	2	mA	Conditions are $V_{DD} = 3.3\text{ V}$ , $T_A = 25\text{ }^{\circ}\text{C}$ , CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz
$I_{DD27}$	Supply current, IMO = 6 MHz using SLIMO mode.	–	1.1	1.5	mA	Conditions are $V_{DD} = 2.55\text{ V}$ , $T_A = 25\text{ }^{\circ}\text{C}$ , CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz
$I_{SB27}$	Sleep (mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	$\mu\text{A}$	$V_{DD} = 2.55\text{ V}$ , $0\text{ }^{\circ}\text{C} \leq T_A \leq 40\text{ }^{\circ}\text{C}$
$I_{SB}$	Sleep (mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	2.8	5	$\mu\text{A}$	$V_{DD} = 3.3\text{ V}$ , $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$
$V_{REF}$	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate $V_{DD}$ $V_{DD} = 3.0\text{ V}$ to 5.25 V
$V_{REF27}$	Reference voltage (Bandgap)	1.16	1.30	1.33	V	Trimmed for appropriate $V_{DD}$ $V_{DD} = 2.4\text{ V}$ to 3.0 V
AGND	Analog ground	$V_{REF} - 0.003$	$V_{REF}$	$V_{REF} + 0.003$	V	

**DC General-Purpose I/O Specifications**

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

**Table 6. 5-V and 3.3-V DC GPIO Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
R <sub>PU</sub>	Pull-up resistor	4	5.6	8	kΩ	
R <sub>PD</sub>	Pull-down resistor	4	5.6	8	kΩ	
V <sub>OH</sub>	High output level	V <sub>DD</sub> - 1.0	–	–	V	I <sub>OH</sub> = 10 mA, V <sub>DD</sub> = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
V <sub>OL</sub>	Low output level	–	–	0.75	V	I <sub>OL</sub> = 25 mA, V <sub>DD</sub> = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
I <sub>OH</sub>	High level source current	10	–	–	mA	V <sub>OH</sub> = V <sub>DD</sub> - 1.0 V, see the limitations of the total current in the note for V <sub>OH</sub>
I <sub>OL</sub>	Low level sink current	25	–	–	mA	V <sub>OL</sub> = 0.75 V, see the limitations of the total current in the note for V <sub>OL</sub>
V <sub>IL</sub>	Input low level	–	–	0.8	V	V <sub>DD</sub> = 3.0 to 5.25
V <sub>IH</sub>	Input high level	2.1	–	–	V	V <sub>DD</sub> = 3.0 to 5.25
V <sub>H</sub>	Input hysteresis	–	60	–	mV	
I <sub>IL</sub>	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C <sub>IN</sub>	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C <sub>OUT</sub>	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

**Table 7. 2.7-V DC GPIO Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
R <sub>PU</sub>	Pull-up resistor	4	5.6	8	kΩ	
R <sub>PD</sub>	Pull-down resistor	4	5.6	8	kΩ	
V <sub>OH</sub>	High output level	V <sub>DD</sub> - 0.4	–	–	V	I <sub>OH</sub> = 2.5 mA (6.25 Typ), V <sub>DD</sub> = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I <sub>OH</sub> budget)
V <sub>OL</sub>	Low output level	–	–	0.75	V	I <sub>OL</sub> = 10 mA, V <sub>DD</sub> = 2.4 to 3.0 V (90 mA maximum combined I <sub>OL</sub> budget)
I <sub>OH</sub>	High level source current	2.5	–	–	mA	V <sub>OH</sub> = V <sub>DD</sub> - 0.4 V, see the limitations of the total current in the note for V <sub>OH</sub>
I <sub>OL</sub>	Low level sink current	10	–	–	mA	V <sub>OL</sub> = 0.75 V, see the limitations of the total current in the note for V <sub>OL</sub>
V <sub>IL</sub>	Input low level	–	–	0.75	V	V <sub>DD</sub> = 2.4 to 3.0
V <sub>IH</sub>	Input high level	2.0	–	–	V	V <sub>DD</sub> = 2.4 to 3.0
V <sub>H</sub>	Input hysteresis	–	90	–	mV	
I <sub>IL</sub>	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C <sub>IN</sub>	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C <sub>OUT</sub>	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

### DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 8. 5-V DC Operational Amplifier Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{\text{OSOA}}$	Input offset voltage (absolute value)	–	2.5	15	mV	
$\text{TCV}_{\text{OSOA}}$	Average input offset voltage drift	–	10	–	$\mu\text{V}/^{\circ}\text{C}$	
$I_{\text{EBOA}}$	Input leakage current (Port 0 analog pins 7-to-1)	–	200	–	pA	Gross tested to 1 $\mu\text{A}$
$I_{\text{EBOA00}}$	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 $\mu\text{A}$
$C_{\text{INOA}}$	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
$V_{\text{CMOA}}$	Common mode voltage range	0.0	–	$V_{\text{DD}} - 1.0$	V	
$G_{\text{OLOA}}$	Open loop gain	–	80	–	dB	
$I_{\text{SOA}}$	Amplifier supply current	–	10	30	$\mu\text{A}$	

**Table 9. 3.3-V DC Operational Amplifier Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{\text{OSOA}}$	Input offset voltage (absolute value)	–	2.5	15	mV	
$\text{TCV}_{\text{OSOA}}$	Average input offset voltage drift	–	10	–	$\mu\text{V}/^{\circ}\text{C}$	
$I_{\text{EBOA}}$	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 $\mu\text{A}$
$I_{\text{EBOA00}}$	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 $\mu\text{A}$
$C_{\text{INOA}}$	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
$V_{\text{CMOA}}$	Common mode voltage range	0	–	$V_{\text{DD}} - 1.0$	V	
$G_{\text{OLOA}}$	Open loop gain	–	80	–	dB	
$I_{\text{SOA}}$	Amplifier supply current	–	10	30	$\mu\text{A}$	

**Table 10. 2.7-V DC Operational Amplifier Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{\text{OSOA}}$	Input offset voltage (absolute value)	–	2.5	15	mV	
$\text{TCV}_{\text{OSOA}}$	Average input offset voltage drift	–	10	–	$\mu\text{V}/^{\circ}\text{C}$	
$I_{\text{EBOA}}$	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 $\mu\text{A}$
$I_{\text{EBOA00}}$	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 $\mu\text{A}$
$C_{\text{INOA}}$	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
$V_{\text{CMOA}}$	Common mode voltage range	0	–	$V_{\text{DD}} - 1.0$	V	
$G_{\text{OLOA}}$	Open loop gain	–	80	–	dB	
$I_{\text{SOA}}$	Amplifier supply current	–	10	30	$\mu\text{A}$	

DC Switch Mode Pump Specifications

Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Figure 12. Basic Switch Mode Pump Circuit

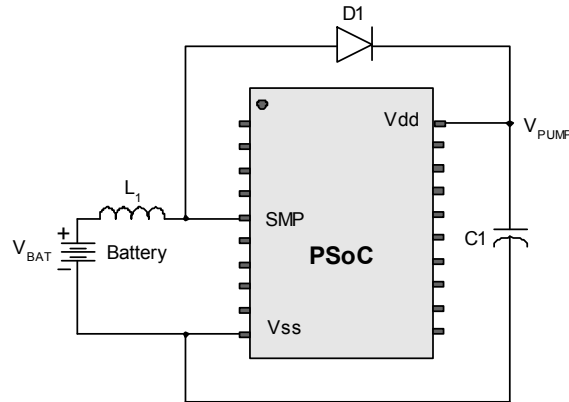


Table 11. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>PUMP5V</sub>	5 V output voltage from pump	4.75	5.0	5.25	V	Configured as in Note 20 Average, neglecting ripple SMP trip voltage is set to 5.0 V
V <sub>PUMP3V</sub>	3.3 V output voltage from pump	3.00	3.25	3.60	V	Configured as in Note 20 Average, neglecting ripple. SMP trip voltage is set to 3.25 V
V <sub>PUMP2V</sub>	2.6 V output voltage from pump	2.45	2.55	2.80	V	Configured as in Note 20 Average, neglecting ripple. SMP trip voltage is set to 2.55 V
I <sub>PUMP</sub>	Available output current V <sub>BAT</sub> = 1.8 V, V <sub>PUMP</sub> = 5.0 V V <sub>BAT</sub> = 1.5 V, V <sub>PUMP</sub> = 3.25 V V <sub>BAT</sub> = 1.3 V, V <sub>PUMP</sub> = 2.55 V	5 8 8	– – –	– – –	mA mA mA	Configured as in Note 20 SMP trip voltage is set to 5.0 V SMP trip voltage is set to 3.25 V SMP trip voltage is set to 2.55 V
V <sub>BAT5V</sub>	Input voltage range from battery	1.8	–	5.0	V	Configured as in Note 20 SMP trip voltage is set to 5.0 V
V <sub>BAT3V</sub>	Input voltage range from battery	1.0	–	3.3	V	Configured as in Note 20 SMP trip voltage is set to 3.25 V
V <sub>BAT2V</sub>	Input voltage range from battery	1.0	–	2.8	V	Configured as in Note 20 SMP trip voltage is set to 2.55 V
V <sub>BATSTART</sub>	Minimum input voltage from battery to start pump	1.2	–	–	V	Configured as in Note 20 0 °C ≤ T <sub>A</sub> ≤ 100. 1.25 V at T <sub>A</sub> = –40 °C
ΔV <sub>PUMP_Line</sub>	Line regulation (over V <sub>i</sub> range)	–	5	–	%V <sub>O</sub>	Configured as in Note 20 V <sub>O</sub> is the “V <sub>DD</sub> Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 13 on page 24
ΔV <sub>PUMP_Load</sub>	Load regulation	–	5	–	%V <sub>O</sub>	Configured as in Note 20 V <sub>O</sub> is the “V <sub>DD</sub> Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 13 on page 24
ΔV <sub>PUMP_Ripple</sub>	Output voltage ripple (depends on cap/load)	–	100	–	mVpp	Configured as in Note 20 Load is 5 mA
E <sub>3</sub>	Efficiency	35	50	–	%	Configured as in Note 20 Load is 5 mA. SMP trip voltage is set to 3.25 V

Note

20. L<sub>1</sub> = 2 mH inductor, C<sub>1</sub> = 10 mF capacitor, D<sub>1</sub> = Schottky diode. See Figure 12 on page 23.



**Table 11. DC Switch Mode Pump (SMP) Specifications** (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
E <sub>2</sub>	Efficiency	35	80	–	%	For I load = 1mA, V <sub>PUMP</sub> = 2.55 V, V <sub>BAT</sub> = 1.3 V, 10 μH inductor, 1 μF capacitor, and Schottky diode
F <sub>PUMP</sub>	Switching frequency	–	1.3	–	MHz	
DC <sub>PUMP</sub>	Switching duty cycle	–	50	–	%	

*DC Analog Mux Bus Specifications*

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 12. DC Analog Mux Bus Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
R <sub>SW</sub>	Switch resistance to common analog bus	–	–	400 800	Ω	V <sub>DD</sub> ≥ 2.7 V 2.4 V ≤ V <sub>DD</sub> ≤ 2.7 V
R <sub>VDD</sub>	Resistance of initialization switch to V <sub>DD</sub>	–	–	800	Ω	

*DC POR and LVD Specifications*

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 13. DC POR and LVD Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>PPOR0</sub>	V <sub>DD</sub> value for PPOR trip PORLEV[1:0] = 00b	–	2.36	2.40	V	V <sub>DD</sub> must be greater than or equal to 2.5 V during startup, the reset from the XRES pin, or reset from watchdog
V <sub>PPOR1</sub>	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V <sub>PPOR2</sub>	PORLEV[1:0] = 10b	–	4.55	4.70	V	
V <sub>LVD0</sub>	V <sub>DD</sub> value for LVD trip VM[2:0] = 000b	2.40	2.45	2.51 <sup>[21]</sup>	V	
V <sub>LVD1</sub>	VM[2:0] = 001b	2.85	2.92	2.99 <sup>[22]</sup>	V	
V <sub>LVD2</sub>	VM[2:0] = 010b	2.95	3.02	3.09	V	
V <sub>LVD3</sub>	VM[2:0] = 011b	3.06	3.13	3.20	V	
V <sub>LVD4</sub>	VM[2:0] = 100b	4.37	4.48	4.55	V	
V <sub>LVD5</sub>	VM[2:0] = 101b	4.50	4.64	4.75	V	
V <sub>LVD6</sub>	VM[2:0] = 110b	4.62	4.73	4.83	V	
V <sub>LVD7</sub>	VM[2:0] = 111b	4.71	4.81	4.95	V	
V <sub>PUMP0</sub>	V <sub>DD</sub> value for pump trip VM[2:0] = 000b	2.45	2.55	2.62 <sup>[23]</sup>	V	
V <sub>PUMP1</sub>	VM[2:0] = 001b	2.96	3.02	3.09	V	
V <sub>PUMP2</sub>	VM[2:0] = 010b	3.03	3.10	3.16	V	
V <sub>PUMP3</sub>	VM[2:0] = 011b	3.18	3.25	3.32 <sup>[24]</sup>	V	
V <sub>PUMP4</sub>	VM[2:0] = 100b	4.54	4.64	4.74	V	
V <sub>PUMP5</sub>	VM[2:0] = 101b	4.62	4.73	4.83	V	
V <sub>PUMP6</sub>	VM[2:0] = 110b	4.71	4.82	4.92	V	
V <sub>PUMP7</sub>	VM[2:0] = 111b	4.89	5.00	5.12	V	

**Notes**

21. Always greater than 50 mV above V<sub>PPOR</sub> (PORLEV = 00) for falling supply.
22. Always greater than 50 mV above V<sub>PPOR</sub> (PORLEV = 01) for falling supply.
23. Always greater than 50 mV above V<sub>LVD0</sub>.
24. Always greater than 50 mV above V<sub>LVD3</sub>.

### DC Programming Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 14. DC Programming Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>DDP</sub>	V <sub>DD</sub> for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V <sub>DDL</sub>	Low V <sub>DD</sub> for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V <sub>DDH</sub>	High V <sub>DD</sub> for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
V <sub>DDIWRITE</sub>	Supply voltage for flash write operation	2.7		5.25	V	This specification applies to this device when it is executing internal flash writes
I <sub>DDP</sub>	Supply current during programming or verify	–	5	25	mA	
V <sub>ILP</sub>	Input low voltage during programming or verify	–	–	0.8	V	
V <sub>IHP</sub>	Input high voltage during programming or verify	2.2	–	–	V	
I <sub>ILP</sub>	Input current when applying V <sub>ILP</sub> to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I <sub>IHP</sub>	Input current when applying V <sub>IHP</sub> to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V <sub>OLV</sub>	Output low voltage during programming or verify	–	–	V <sub>SS</sub> + 0.75	V	
V <sub>OHV</sub>	Output high voltage during programming or verify	V <sub>DD</sub> – 1.0	–	V <sub>DD</sub>	V	
Flash <sub>ENPB</sub>	Flash endurance (per block)	50,000 <sup>[25]</sup>	–	–	–	Erase/write cycles per block
Flash <sub>ENT</sub>	Flash endurance (total) <sup>[26]</sup>	1,800,000	–	–	–	Erase/write cycles
Flash <sub>DR</sub>	Flash data retention	10	–	–	Years	

### DC I<sup>2</sup>C Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 15. DC I<sup>2</sup>C Specifications<sup>[27]</sup>**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>IL2C</sub>	Input low level	–	–	0.3 × V <sub>DD</sub>	V	2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V
		–	–	0.25 × V <sub>DD</sub>	V	4.75 V ≤ V <sub>DD</sub> ≤ 5.25 V
V <sub>IH2C</sub>	Input high level	0.7 × V <sub>DD</sub>	–	–	V	2.4 V ≤ V <sub>DD</sub> ≤ 5.25 V

#### Notes

25. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
26. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and ensure that no single block ever sees more than 50,000 cycles). For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note AN2015 (Design Aids - Reading and Writing PSoC® Flash) for more information.
27. All GPIO meet the DC GPIO VIL and VIH specifications found in the DC GPIO Specifications sections. The I<sup>2</sup>C GPIO pins also meet the above specs.