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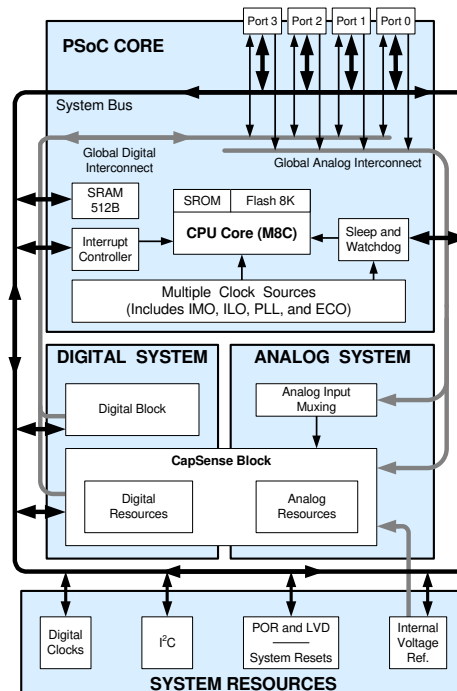


Automotive PSoC[®] Programmable System-on-Chip™

Features

- Automotive Electronics Council (AEC) Q100 qualified
- Powerful Harvard-architecture processor
 - M8C processor speeds up to 24 MHz
 - Low power at high speed
 - Operating voltage: 3.0 V to 5.25 V
 - Automotive temperature range: -40 °C to +85 °C
- Advanced peripherals
 - One CapSense[®] block:
 - Provides configurable capacitive sensing elements
 - Supports combination of CapSense buttons, sliders, touchpads, and proximity sensors
 - One limited digital PSoC[®] block provides:
 - 8-bit timer, counter, or pulse-width modulator (PWM)
 - Half-duplex UART
 - SPI slave
 - Connectable to all general purpose I/O (GPIO) pins
- Flexible on-chip memory
 - 8 KB flash program storage
 - 512 bytes SRAM data storage
 - In-system serial programming (ISSP)
 - Partial flash updates
 - Flexible protection modes
 - EEPROM emulation in flash
- Complete development tools
 - Free development software (PSoC Designer™)
 - Full-featured in-circuit emulator (ICE) and programmer
 - Full-speed emulation
 - Complex breakpoint structure
 - 128 KB trace memory
- Precision, programmable clocking
 - Internal ±5% 24 MHz oscillator
 - Internal low-speed, low-power oscillator for Watchdog and Sleep functionality
 - Optional external oscillator, up to 24 MHz
- Programmable pin configurations
 - 25 mA sink, 10 mA drive on all GPIOs
 - Pull-up, pull-down, high Z, strong, or open drain drive modes on all GPIOs
 - Analog input on all GPIOs
 - Configurable interrupt on all GPIOs
- Versatile analog mux
 - Common internal analog bus
 - Simultaneous connection of I/O combinations
- Additional system resources
 - Inter-Integrated Circuit (I²C™) master, slave, or multi-master operation up to 400 kHz
 - Watchdog and sleep timers
 - User-configurable low-voltage detection (LVD)
 - Integrated supervisory circuit
 - On-chip precision voltage reference

Logic Block Diagram



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PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, as illustrated in the “Logic Block Diagram” on page 1, comprises of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow all the device resources to be combined into a complete custom system. Each CY8C21x12 device includes one limited digital block and one CapSense block. Depending on the PSoC package, up to 24 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep, and watchdog timers, and an internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System Resources provide additional capability, such as digital clocks for increased flexibility, I²C functionality for implementing an I²C master, slave, or multi-master, an internal voltage reference that provides an absolute value of 1.3 V to a number of PSoC subsystems, and various system resets supported by the M8C.

The Digital System is composed of a programmable limited digital block and fixed-function digital resources inside the CapSense block. The limited digital block can be configured into a number of digital peripherals. The fixed-function digital resources in the CapSense block provide external modulation signals, measurement timing, and measurement conversion. The digital resources can be connected to the GPIO through a series of global buses that provide very flexible routing options.

The Analog System is composed of a comparator and a filter that are used in the CapSense block to implement capacitive sensing measurement.

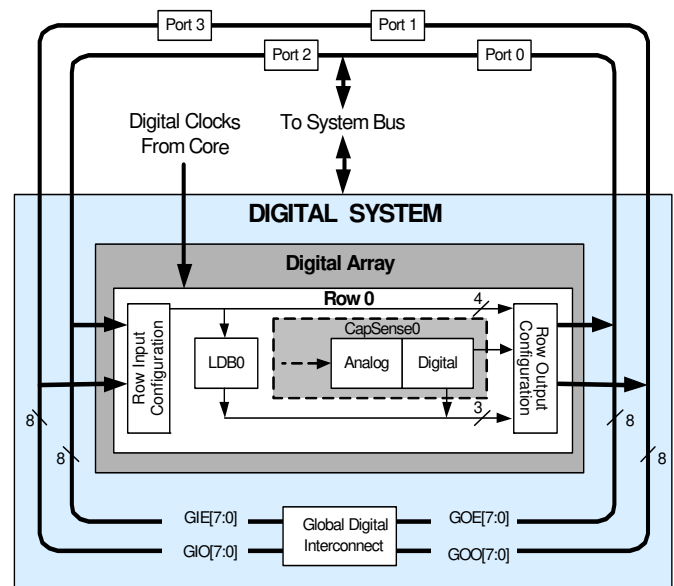
The Digital System

The Digital System is composed of one digital block. This block is an 8-bit resource that can implement various 8-bit digital peripherals. Digital peripheral configurations include those listed.

- PWM (8-bit)
- Counter (8-bit)
- Timer (8-bit)
- Half-duplex 8-bit UART with selectable parity
- SPI slave
- I²C master, slave, or multi-master (implemented in a dedicated I²C block)

The digital block can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Figure 1. Digital System Block Diagram

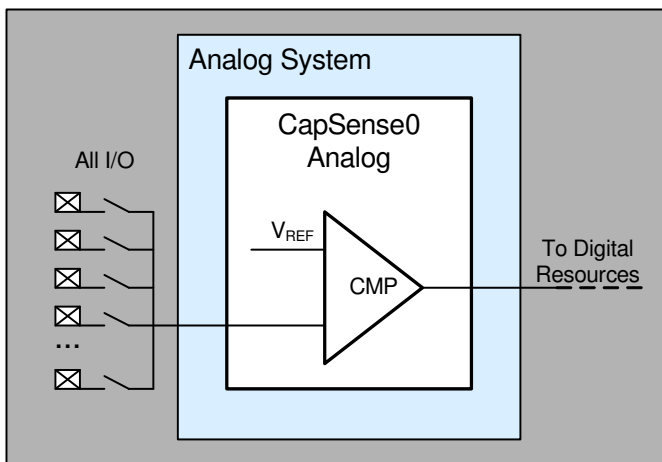


The Analog System

The Analog System is composed of analog resources inside of the CapSense block. These resources are used to implement a flexible capacitive sensing and measurement module. The analog resources in the CapSense block are listed.

- Comparator used in capacitance-to-digital conversion
- Fixed, absolute reference or adjustable, ratiometric reference can be used with the comparator
- Low-pass filter converts a digital bit stream into the adjustable, ratiometric analog reference

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system. Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combination.

Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful for complete systems. Brief statements describing the merits of each system resource are presented.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems.
- The I²C module provides communication up to 400 kHz over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3 V voltage reference provides an absolute reference for the analog system.
- Versatile analog multiplexer system.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. [Table 1](#) lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in [Table 1](#)

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66 ^[1]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 ^[2]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94 ^[1]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A ^[1]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45 ^[1]	up to 38	2	8	up to 38	0	4	6 ^[2]	1 K	16 K
CY8C21x45 ^[1]	up to 24	1	4	up to 24	0	4	6 ^[2]	512	8 K
CY8C21x34 ^[1]	up to 28	1	4	28	0	2	4 ^[2]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4 ^[2]	256	4 K
CY8C21x12 ^[1]	up to 24	1	1 ^[2]	24	0	0	1 ^[2]	512	8 K
CY8C20x34 ^[1]	up to 28	0	0	up to 28	0	0	3 ^[2,3]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3 ^[2,3]	up to 2 K	up to 32 K

Getting Started

For in-depth information, along with detailed programming details, see the [PSoC[®] Technical Reference Manual](#).

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Notes

1. Automotive qualified devices available in this group.
2. Limited analog functionality.
3. Two analog blocks and one CapSense[®] block.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select [User Modules](#)
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pinouts

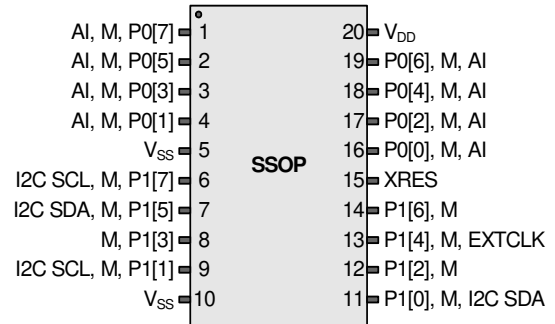
The CY8C21x12 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

20-Pin Part Pinout

Table 2. 20-Pin Part Pinout (shrink small-outline package (SSOP))

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, C _{MOD} capacitor pin
4	I/O	I, M	P0[1]	Analog column mux input, C _{MOD} capacitor pin
5	Power		V _{SS}	Ground connection
6	I/O	M	P1[7]	I ² C serial clock (SCL)
7	I/O	M	P1[5]	I ² C serial data (SDA)
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	I ² C SCL, ISSP-SCLK ^[4]
10	Power		V _{SS}	Ground connection
11	I/O	M	P1[0]	I ² C SDA, ISSP-SDATA ^[4]
12	I/O	M	P1[2]	
13	I/O	M	P1[4]	Optional external clock input (EXTCLK)
14	I/O	M	P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I, M	P0[0]	Analog column mux input
17	I/O	I, M	P0[2]	Analog column mux input
18	I/O	I, M	P0[4]	Analog column mux input
19	I/O	I, M	P0[6]	Analog column mux input
20	Power		V _{DD}	Supply voltage

Figure 3. CY8C21312 20-Pin PSoC Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note

4. These are the ISSP pins, which are not high Z when coming out of POR. See the [PSoC Technical Reference Manual](#) for details.

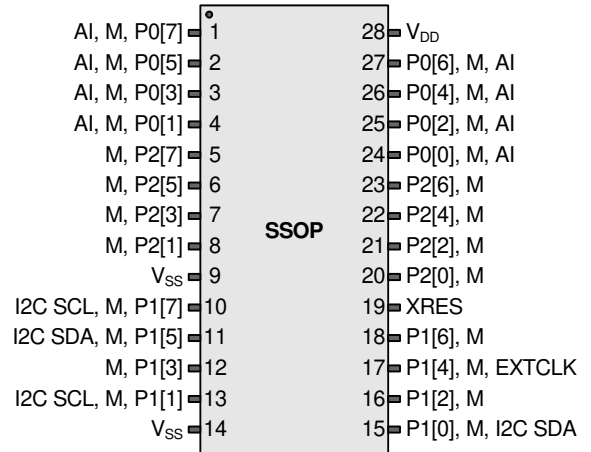
28-Pin Part Pinout

Table 3. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, C _{MOD} capacitor pin
4	I/O	I, M	P0[1]	Analog column mux input, C _{MOD} capacitor pin
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	M	P2[3]	
8	I/O	M	P2[1]	
9	Power		V _{SS}	Ground connection
10	I/O	M	P1[7]	I ² C SCL
11	I/O	M	P1[5]	I ² C SDA
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	I ² C SCL, ISSP-SCLK ^[5]
14	Power		V _{SS}	Ground connection
15	I/O	M	P1[0]	I ² C SDA, ISSP-SDATA ^[5]
16	I/O	M	P1[2]	
17	I/O	M	P1[4]	Optional EXTCLK
18	I/O	M	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	M	P2[0]	
21	I/O	M	P2[2]	
22	I/O	M	P2[4]	
23	I/O	M	P2[6]	
24	I/O	I, M	P0[0]	Analog column mux input
25	I/O	I, M	P0[2]	Analog column mux input
26	I/O	I, M	P0[4]	Analog column mux input
27	I/O	I, M	P0[6]	Analog column mux input
28	Power		V _{DD}	Supply voltage

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Figure 4. CY8C21512 28-Pin PSoC Device



Note

5. These are the ISSP pins, which are not high Z when coming out of POR. See the *PSoC Technical Reference Manual* for details.

Registers

Register Conventions

This section lists the registers of the CY8C21x12 PSoC device. For detailed register information, refer to the [PSoC Technical Reference Manual](#).

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, bank 0 and bank 1. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set to '1', the user is in bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 4. Register Map 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		CSREF_CR1	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		CUR_PP	D0	RW
	11			51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
CSCNT_DR0	20	#		60			A0		INT_MSK0	E0	RW
CSCNT_DR1	21	W	AMUX_CFG	61	RW		A1		INT_MSK1	E1	RW
CSCNT_DR2	22	RW	CSCMP_CR0	62	RW		A2		INT_VC	E2	RC
CSCNT_CR0	23	#		63			A3		RES_WDT	E3	W
CSMOD0_DR0	24	#	CSCMP_CR1	64	#		A4			E4	
CSMOD0_DR1	25	W		65			A5			E5	
CSMOD0_DR2	26	RW	CSCMP_CR2	66	RW		A6		CSCMP_CR5	E6	RW
CSMOD0_CR0	27	#		67			A7		CSCMP_CR6	E7	RW
CSMOD1_DR0	28	#		68			A8			E8	
CSMOD1_DR1	29	W	CSREF_CR0	69	#		A9			E9	
CSMOD1_DR2	2A	RW		6A			AA			EA	
CSMOD1_CR0	2B	#		6B			AB			EB	
LDB0_DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
LDB0_DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
LDB0_DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
LDB0_CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDIORI	B0	RW		F0	
	31			71		RDIOSYN	B1	RW		F1	
	32			72		RDIOIS	B2	RW		F2	
	33			73		RDIOILT0	B3	RW		F3	
	34			74		RDIOILT1	B4	RW		F4	
	35			75		RDIORO0	B5	RW		F5	
	36		CSCMP_CR3	76	RW	RDIORO1	B6	RW		F6	
	37		CSCMP_CR4	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Table 5. Register Map 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44			84			C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D			DD	
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
CSCNT_CR1	20	RW	CSCCLK_CR0	60	RW		A0		OSC_CR0	E0	RW
CSCNT_CR2	21	RW	CSCCLK_CR1	61	RW		A1		OSC_CR1	E1	RW
CSCNT_CR3	22	RW		62			A2		OSC_CR2	E2	RW
	23		CSREF_CR2	63	RW		A3		VLT_CR	E3	RW
CSMOD0_CR1	24	RW	CSCMP_CR7	64	RW		A4		VLT_CMP	E4	R
CSMOD0_CR2	25	RW		65			A5			E5	
CSMOD0_CR3	26	RW	CSREF_CR3	66	RW		A6		CSREF_CR4	E6	RW
	27		CSCMP_CR8	67	RW		A7			E7	
CSMOD1_CR1	28	RW		68			A8		IMO_TR	E8	W
CSMOD1_CR2	29	RW		69			A9		ILO_TR	E9	W
CSMOD1_CR3	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CSCCLK_CR2	6B	RW		AB		ECO_TR	EB	W
LDB0_FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
LDB0_IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
LDB0_OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDIORI	B0	RW		F0	
	31			71		RDIOSYN	B1	RW		F1	
	32			72		RDIOIS	B2	RW		F2	
	33			73		RDIOILT0	B3	RW		F3	
	34			74		RDIOILT1	B4	RW		F4	
	35			75		RDIORO0	B5	RW		F5	
	36			76		RDIORO1	B6	RW		F6	
	37			77			B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x12 PSoC device. For the most up-to-date electrical specifications, visit the Cypress website at <http://www.cypress.com>.

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$ as specified, except where noted. Refer to Table 12 on page 18 for the electrical specifications for the IMO using slow IMO (SLIMO) mode.

Figure 5. Voltage versus CPU Frequency

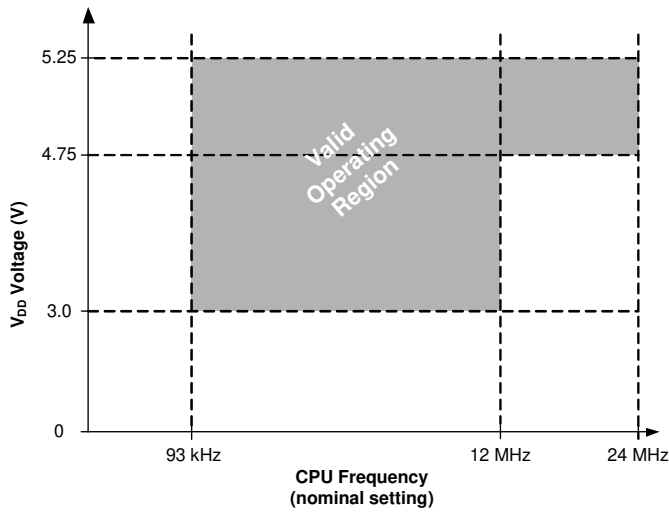
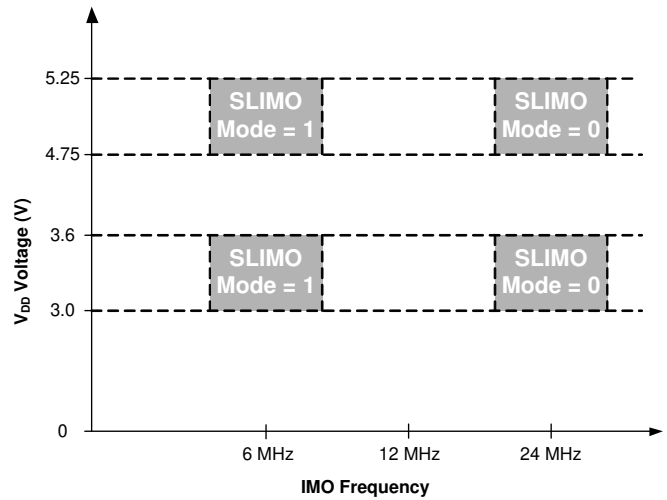


Figure 6. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested

Symbol	Description	Min	Typ	Max	Units	Notes
T _{STG}	Storage temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Time spent in storage at a temperature greater than 65 °C counts toward the Flash _{DR} electrical specification in Table 11 on page 17.
T _{BAKETEMP}	Bake temperature	-	125	See package label	°C	
t _{BAKETIME}	Bake time	See package label	-	72	Hours	
T _A	Ambient temperature with power applied	-40	-	+85	°C	
V _{DD}	Supply voltage on V _{DD} relative to V _{SS}	-0.5	-	+6.0	V	
V _{IO}	DC input voltage	V _{SS} - 0.5	-	V _{DD} + 0.5	V	
V _{IOZ}	DC voltage applied to tri-state	V _{SS} - 0.5	-	V _{DD} + 0.5	V	
I _{MIO}	Maximum current into any port pin	-25	-	+50	mA	
ESD	Electrostatic discharge voltage	2000	-	-	V	Human Body Model ESD
LU	Latch up current	-	-	200	mA	

Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T _A	Ambient temperature	-40	-	+85	°C	
T _J	Junction temperature	-40	-	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 24. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics
DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 6. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{DD}	Supply voltage	3.0	–	5.25	V	See table titled DC POR and LVD Specifications on page 16
I _{DD}	Supply current, IMO = 24 MHz	–	4	6	mA	Conditions are V _{DD} = 5.25 V, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz
I _{DD3}	Supply current, IMO = 6 MHz using SLIMO mode	–	2	4	mA	Conditions are V _{DD} = 3.3 V, CPU = 3 MHz, 48 MHz disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz
I _{SB1}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and ILO active	–	2.8	7	μA	V _{DD} = 3.3 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$
I _{SB2}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and ILO active	–	5	15	μA	V _{DD} = 5.25 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$
V _{REF}	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V _{DD} range

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 7. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R _{PU}	Pull-up resistor	4	5.6	8	kΩ	
R _{PD}	Pull-down resistor	4	5.6	8	kΩ	Also applies to the internal pull-down resistor on the XRES pin
V _{OH}	High output level	V _{DD} – 1.0	–	–	V	I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
V _{OL}	Low output level	–	–	0.75	V	I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
I _{OH}	High level source current	10	–	–	mA	V _{OH} ≥ V _{DD} – 1.0 V, see the limitations of the total current in the note for V _{OH}
I _{OL}	Low level sink current	25	–	–	mA	V _{OL} ≤ 0.75 V, see the limitations of the total current in the note for V _{OL}
V _{IL}	Input low level	–	–	0.8	V	
V _{IH}	Input high level	2.1	–	–	V	
V _H	Input hysteresis	–	60	–	mV	
I _{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C _{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C _{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

DC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

These comparator electrical specifications apply to the comparator in the CapSense block.

Table 8. DC Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSCMP}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSCMP}	Average input offset voltage drift	–	10	–	$\mu\text{V}/^{\circ}\text{C}$	
$I_{EBCMP}^{[6]}$	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA
C_{INCMP}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent Temp = 25 °C
V_{CMCMP}	Common mode voltage range	0.0	–	$V_{DD} - 1$	V	
G_{OLCMP}	Open loop gain	–	80	–	dB	
I_{SCMP}	Supply current					
	$3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	–	30	–	μA	
	$4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$	–	35	–	μA	

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 9. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400	Ω	
R_{VDD}	Resistance of initialization switch to V_{DD}	–	–	800	Ω	

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 10. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR0}	V_{DD} value for precision POR (PPOR) trip PORLEV[1:0] = 00b	–	2.36	2.40	V	V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR1}		–	2.82	2.95	V	
V_{PPOR2}		–	4.55	4.70	V	
V_{LVD1}	V_{DD} value for LVD trip VM[2:0] = 001b	2.85	2.92	2.99 ^[7]	V	
V_{LVD2}		2.95	3.02	3.09	V	
V_{LVD3}		3.06	3.13	3.20	V	
V_{LVD4}		4.37	4.48	4.55	V	
V_{LVD5}		4.50	4.64	4.75	V	
V_{LVD6}		4.62	4.73	4.83	V	
V_{LVD7}		4.71	4.81	4.95	V	

Notes

- Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 pA.
- Always greater than 50 mV above V_{PPOR1} (PORLEV[1:0] = 01b) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 11. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{DDP}	V _{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V _{DDL}	Low V _{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V _{DDHV}	High V _{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
V _{DDWRITE}	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I _{DDP}	Supply current during programming or verify	–	5	25	mA	
V _{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V _{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I _{ILP}	Input current when applying V _{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I _{IHP}	Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V _{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V _{OHV}	Output high voltage during programming or verify	V _{DD} – 1.0	–	V _{DD}	V	
Flash _{ENPB}	Flash endurance (per block) ^[8, 9]	1,000	–	–	–	Erase/write cycles per block
Flash _{ENT}	Flash endurance (total) ^[9, 10]	128,000	–	–	–	Erase/write cycles
Flash _{DR}	Flash data retention	15	–	–	Years	

Notes

8. The erase/write cycle limit per block (Flash_{ENPB}) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs [Application Note AN2015](#) for more information.
10. The maximum total number of allowed erase/write cycles is the minimum Flash_{ENPB} value multiplied by the number of flash blocks in the device.

AC Electrical Characteristics

AC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 12. AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{IMO24}	IMO frequency for 24 MHz	22.8 ^[11]	24	25.2 ^[11]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 0.
F _{IMO6}	IMO frequency for 6 MHz	5.5 ^[11]	6	6.5 ^[11]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1.
F _{CPU1}	CPU frequency (5 V V _{DD} nominal)	0.089 ^[11]	24	25.2 ^[11]	MHz	24 MHz only for SLIMO mode = 0
F _{CPU2}	CPU frequency (3.3 V V _{DD} nominal)	0.089 ^[11]	12	12.6 ^[11]	MHz	
F _{BLK5}	Digital PSoC block frequency (5 V V _{DD} nominal)	0	48	50.4 ^[11,12]	MHz	Refer to the AC Digital Block Specifications below
F _{BLK33}	Digital PSoC block frequency (3.3 V V _{DD} nominal)	0	24	25.2 ^[11,12]	MHz	Refer to the AC Digital Block Specifications below
F _{32K1}	ILO frequency	15	32	64	kHz	This specification applies when the ILO has been trimmed
F _{32KU}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
t _{XRST}	External reset pulse width	10	–	–	μs	
DC _{24M}	24 MHz duty cycle	40	50	60	%	
DC _{ILO}	ILO duty cycle	20	50	80	%	
Step _{24M}	24 MHz trim step size	–	50	–	kHz	
F _{out48M}	48 MHz output frequency	45.6 ^[11]	48.0	50.4 ^[11]	MHz	
F _{MAX}	Maximum frequency of signal on row input or row output	–	–	12.6	MHz	
SR _{POWERUP}	Power supply slew rate	–	–	250	V/ms	V _{DD} slew rate during power-up
t _{POWERUP}	Time between end of POR state and CPU code execution	–	16	100	ms	Power-up from 0 V.
t _{JIT_IMO} ^[13]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	

Notes

11. Accuracy derived from IMO with appropriate trim for V_{DD} range.

12. See the individual user module datasheets for information on maximum frequencies for user modules.

13. Refer to Cypress Jitter Specifications application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information.

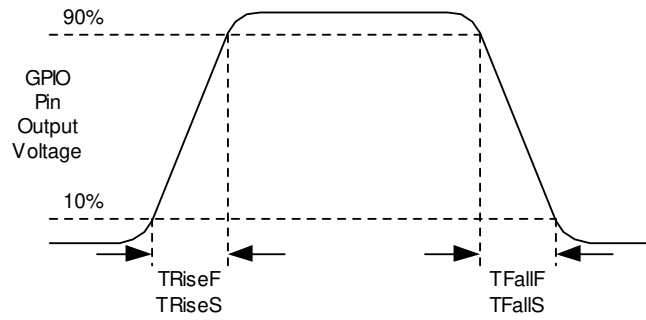
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 13. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.6	MHz	Normal Strong Mode
T_{RiseF}	Rise time, normal strong mode, Clload = 50 pF	2	6	18	ns	$V_{DD} = 4.75$ to 5.25 V, 10% to 90%
T_{FallF}	Fall time, normal strong mode, Clload = 50 pF	2	6	18	ns	$V_{DD} = 4.75$ to 5.25 V, 10% to 90%
T_{RiseS}	Rise time, slow strong mode, Clload = 50 pF	7	27	–	ns	$V_{DD} = 3$ to 5.25 V, 10% to 90%
T_{FallS}	Fall time, slow strong mode, Clload = 50 pF	7	22	–	ns	$V_{DD} = 3$ to 5.25 V, 10% to 90%

Figure 7. GPIO Timing Diagram



AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

These comparator electrical specifications apply to the comparator in the CapSense block.

Table 14. AC Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Response time, 50 mV overdrive	–	75	100	ns	

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 15. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Input clock frequency					
	No capture, $V_{\text{DD}} \geq 4.75\text{ V}$	–	–	50.4 ^[15]	MHz	
	No capture, $V_{\text{DD}} < 4.75\text{ V}$	–	–	25.2 ^[15]	MHz	
	With capture	–	–	25.2 ^[15]	MHz	
	Capture pulse width	50 ^[14]	–	–	ns	
Counter	Input clock frequency					
	No enable input, $V_{\text{DD}} \geq 4.75\text{ V}$	–	–	50.4 ^[15]	MHz	
	No enable input, $V_{\text{DD}} < 4.75\text{ V}$	–	–	25.2 ^[15]	MHz	
	With enable input	–	–	25.2 ^[15]	MHz	
	Enable input pulse width	50 ^[14]	–	–	ns	
SPIS	Input clock (SCLK) frequency	–	–	4.2 ^[15]	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated between transmissions	50 ^[14]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{\text{DD}} \geq 4.75\text{ V}$, 2 stop bits	–	–	50.4 ^[15]	MHz	
	$V_{\text{DD}} \geq 4.75\text{ V}$, 1 stop bit	–	–	25.2 ^[15]	MHz	
	$V_{\text{DD}} < 4.75\text{ V}$	–	–	25.2 ^[15]	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{\text{DD}} \geq 4.75\text{ V}$, 2 stop bits	–	–	50.4 ^[15]	MHz	
	$V_{\text{DD}} \geq 4.75\text{ V}$, 1 stop bit	–	–	25.2 ^[15]	MHz	
	$V_{\text{DD}} < 4.75\text{ V}$	–	–	25.2 ^[15]	MHz	

Notes

14. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

15. Accuracy derived from IMO with appropriate trim for V_{DD} range.

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 16. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	μs	

Table 17. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F _{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	μs	

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 18. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t _{RSCLK}	Rise time of SCLK	1	–	20	ns	
t _{FSCLK}	Fall time of SCLK	1	–	20	ns	
t _{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t _{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
t _{SCLK}	Frequency of SCLK	0	–	8	MHz	
t _{ERASEB}	Flash block erase time	–	10	40 ^[16]	ms	
t _{WRITE}	Flash block write time	–	40	160 ^[16]	ms	
t _{DSCLK}	Data out delay from falling edge of SCLK	–	38	45	ns	3.6 < V _{DD}
t _{DSCLK3}	Data out delay from falling edge of SCLK	–	44	50	ns	3.0 ≤ V _{DD} ≤ 3.6
t _{PRGH}	Total flash block program time (t _{ERASEB} + t _{WRITE}), hot	–	–	100 ^[16]	ms	T _J ≥ 0 °C
t _{PRGC}	Total flash block program time (t _{ERASEB} + t _{WRITE}), cold	–	–	200 ^[16]	ms	T _J < 0 °C

Note

16. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs [Application Note AN2015](#) for more information.

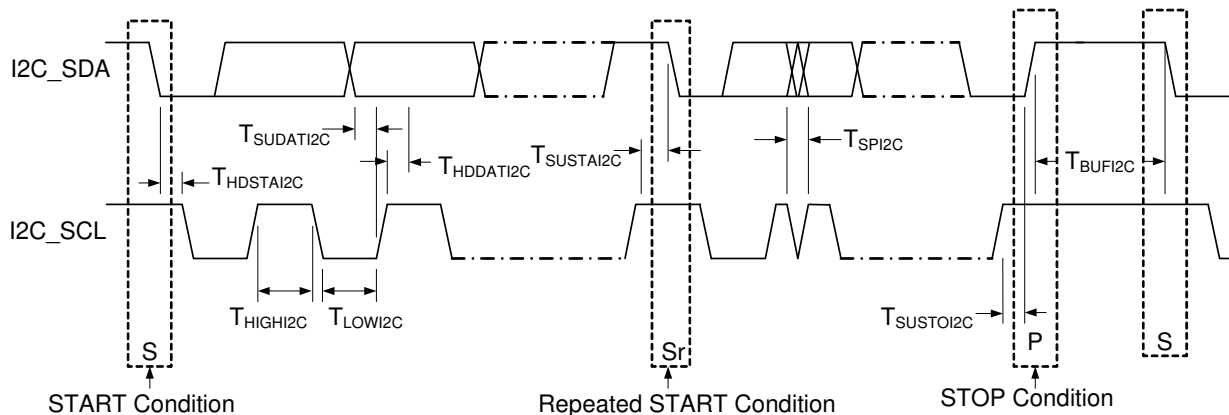
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 19. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F _{SCLi2C}	SCL clock frequency	0	100 ^[17]	0	400 ^[17]	kHz	
t _{HDSTAI2C}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs	
t _{LOWi2C}	LOW period of the SCL clock	4.7	–	1.3	–	μs	
t _{HIGHi2C}	HIGH period of the SCL clock	4.0	–	0.6	–	μs	
t _{SUSTAI2C}	Setup time for a repeated START condition	4.7	–	0.6	–	μs	
t _{HDDATI2C}	Data hold time	0	–	0	–	μs	
t _{SUDATI2C}	Data setup time	250	–	100 ^[18]	–	ns	
t _{SUSTOI2C}	Setup time for STOP condition	4.0	–	0.6	–	μs	
t _{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	μs	
t _{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 8. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

- 17. F_{SCLi2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLi2C} specification adjusts accordingly
- 18. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement t_{SUDATI2C} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SUDATI2C} = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

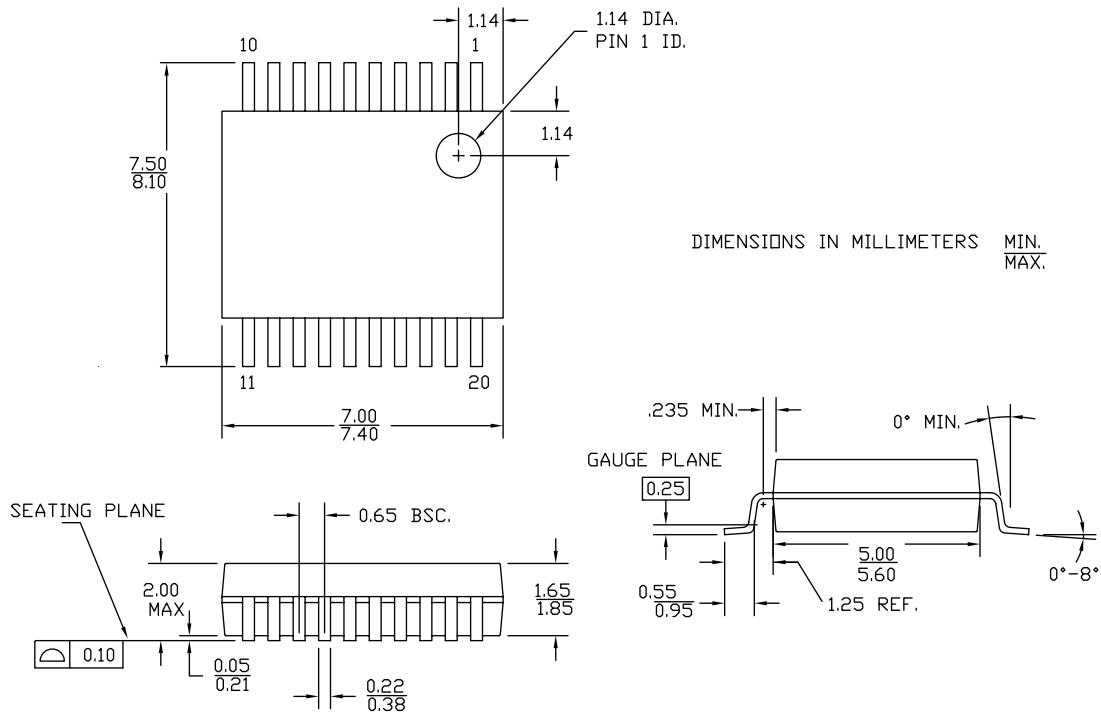
Packaging Information

This section illustrates the packaging specifications for the CY8C21x12 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at <http://www.cypress.com>.

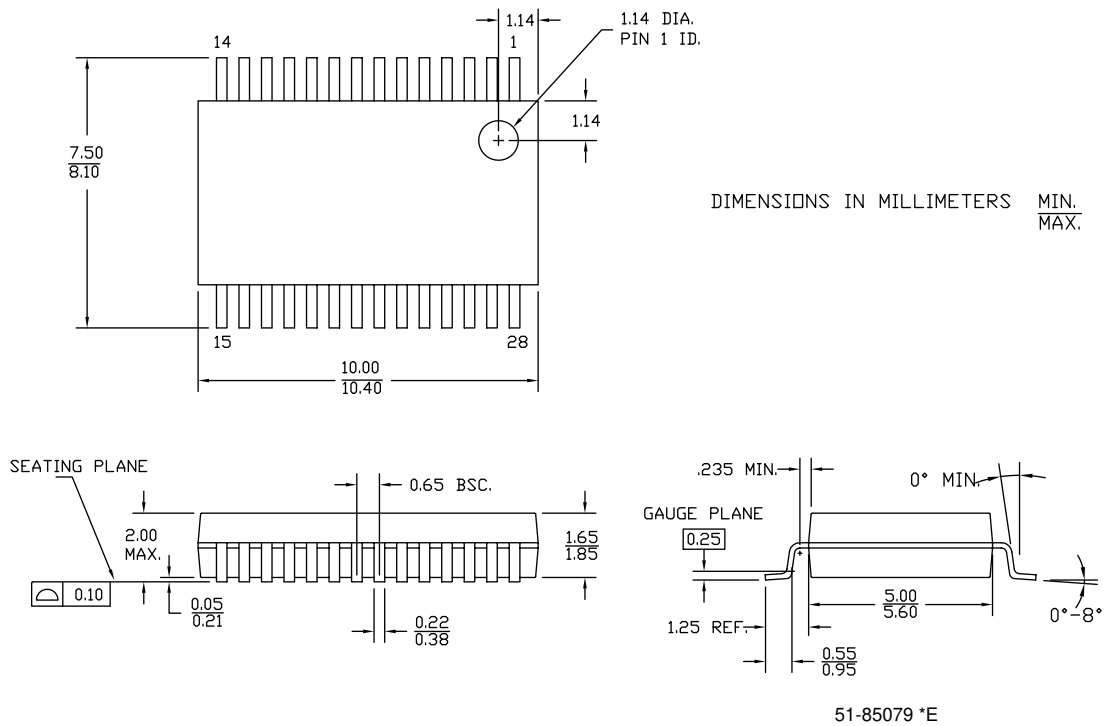
Packaging Dimensions

Figure 9. 20-Pin (210-Mil) SSOP



51-85077 *E

Figure 10. 28-Pin (210-Mil) SSOP



Thermal Impedances

Table 20. Thermal Impedances per Package

Package	Typical θ_{JA} [19]	Typical θ_{JC}
20-Pin SSOP	117 °C/W	41 °C/W
28-Pin SSOP	96 °C/W	39 °C/W

Solder Reflow Specifications

Table 21 shows the solder reflow temperature limits that must not be exceeded.

Table 21. Solder Reflow Specifications

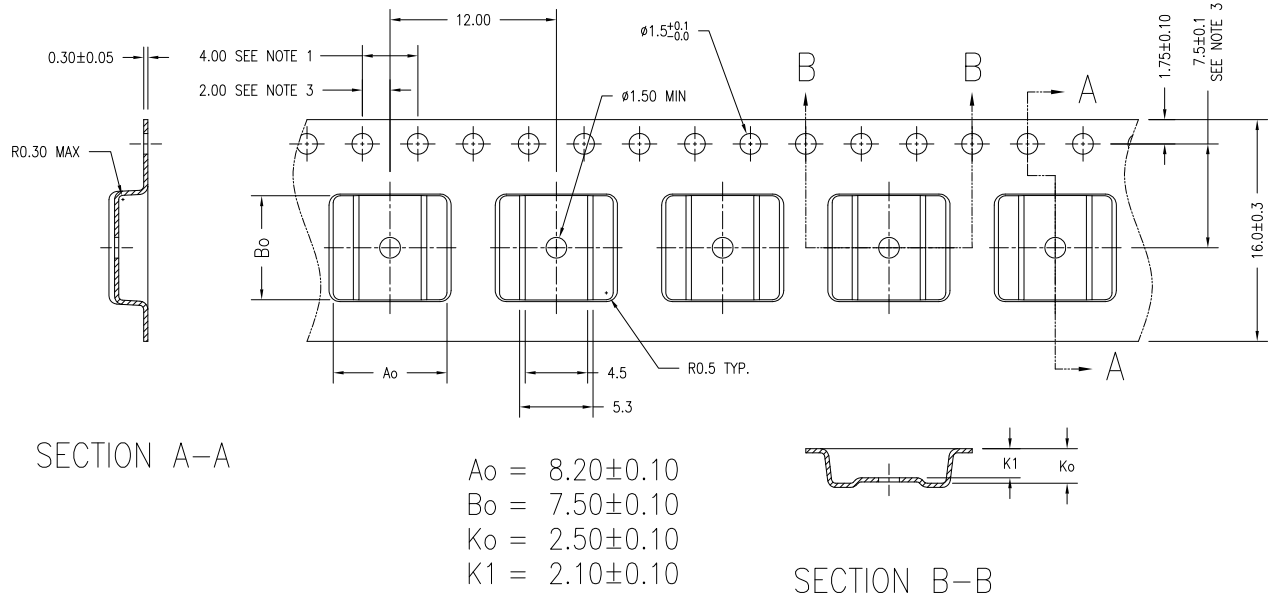
Package	Maximum Peak Temperature (T_C)	Maximum Time above $T_C - 5$ °C
20-Pin SSOP	260 °C	30 seconds
28-Pin SSOP	260 °C	30 seconds

Note

19. $T_J = T_A + \text{Power} \times \theta_{JA}$

Tape and Reel Information

Figure 11. 20-Pin SSOP Carrier Tape Drawing



- NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
 2. CAMBER IN COMPLIANCE WITH EIA 481
 3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

51-51101 *C