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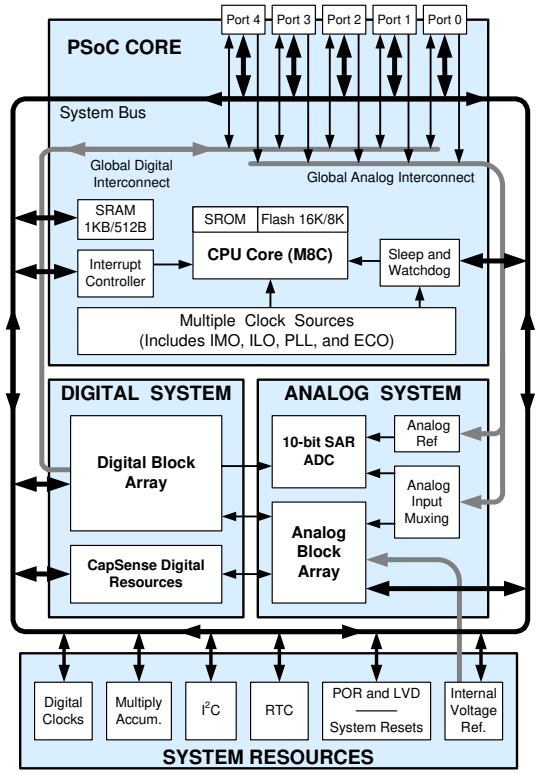
CY8C21345/CY8C21645
CY8C22345/CY8C22345H/CY8C22645

Automotive PSoC® Programmable System-on-Chip™

Features

- Automotive Electronics Council (AEC) Q100 qualified
- Powerful Harvard-architecture processor
  - M8C processor speeds up to 24 MHz
  - 8 × 8 multiply, 32-bit accumulate
  - Low power at high speed
  - Automotive A-grade: 3.0 V to 5.25 V operation at –40 °C to +85 °C temperature range
  - Automotive E-grade: 4.75 V to 5.25 V operation at –40 °C to +125 °C temperature range
- Advanced peripherals (PSoC® blocks)
  - Six analog Type 'E' PSoC blocks provide:
    - Up to four comparators with digital-to-analog converters (DAC) references
    - Up to 10-bit single or dual analog-to-digital converters (ADCs)
  - Up to eight digital PSoC blocks provide:
    - 8 to 32-bit timers, counters, and pulse width modulators (PWMs)
    - One-shot, multi-shot mode in timers and PWMs
    - PWM with deadband in one digital block
    - Shift register, cyclical redundancy check (CRC), and pseudo random sequence (PRS) modules
    - Full- or half-duplex UARTs
    - SPI masters or slaves, 8- to 16-bit variable data length
    - Connectable to all general-purpose I/O (GPIO) pins
  - Complex peripherals by combining blocks
  - Powerful synchronization support, analog module operations can be synchronized by digital blocks or external signals.
- High-speed 10-bit successive approximation register (SAR) ADC with sample and hold optimized for embedded control
- CY8C22345H devices Integrate Immersion® TouchSense® Haptics Technology for ERM drive control
- Precision, programmable clocking
  - Internal oscillator up to 24 MHz
  - High accuracy 24 MHz with optional 32-kHz crystal and phase locked loop (PLL)
  - Optional external oscillator, up to 24 MHz
  - Internal low speed, low-power oscillator for watchdog and sleep functionality
- Flexible on-chip memory
  - Up to 16 KB flash program storage, 1000 erase/write cycles
  - Up to 1 KB SRAM data storage
  - In-System Serial Programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Optimized CapSense® resource
  - Supports two CapSense channels with simultaneous scanning
  - Two current DACs provide programmable sensor tuning in firmware
  - Two dedicated clock resources for CapSense
  - Two dedicated 16-bit timers/counters for CapSense scanning
- Versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O combinations
- Programmable pin configurations
  - 25 mA sink, 10 mA drive on all GPIOs
  - Pull-up, pull-down, high Z, strong, or open-drain drive modes on all GPIOs
  - Analog input on all GPIOs
  - Configurable interrupt on all GPIOs
- Additional system resources:
  - I^2C master, slave, or multi-master
    - Operation up to 400 kHz
    - Hardware address detection feature
  - Watchdog and sleep timers
  - User-configurable low voltage detection
  - Integrated supervisory circuit
  - On-chip precision voltage reference
  - Hardware real time clock (RTC) block

Block Diagram



Contents

PSoC Functional Overview

The PSoC programmable system-on-chip series of products consists of many devices. These devices are designed to replace multiple traditional MCU-based system components with one low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, shown in the Block Diagram on page 1, consists of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global busing allows the combining of all the device resources into a complete custom system. The PSoC family can have up to five I/O ports connecting to the global digital and analog interconnects, providing access to eight digital blocks [1] and six analog blocks.

PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO.

The M8C CPU core is a powerful processor with speeds up to 24 MHz (up to 12 MHz for E-grade devices), providing four MIPS (two MIPS for E-grade devices) 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller to simplify the programming of real time embedded events.

Program execution is timed and protected using the included Sleep Timer and watchdog timer (WDT).

Memory encompasses 16 KB of flash (8 KB for CY8C21x45 devices) for program storage, 1 KB of SRAM (512 bytes for CY8C21x45 devices) for data storage, and EEPROM emulation using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

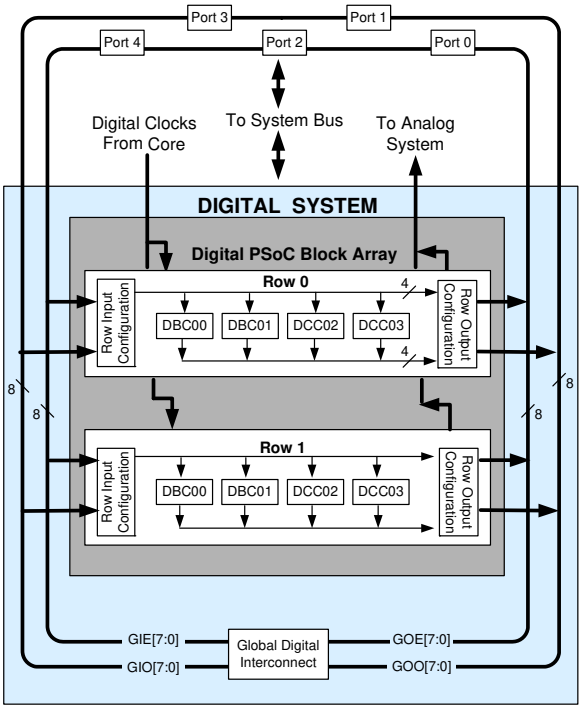
The PSoC device incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO). For A-grade devices the 24-MHz IMO can also be doubled to 48 MHz for use by the digital system. A low-power 32-kHz internal low-speed oscillator (ILO) is provided for the Sleep Timer and WDT. If crystal accuracy is required, the 32.768 kHz external crystal oscillator (ECO) is available for use as a RTC, and can optionally generate a crystal-accurate 24-MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Each pin can also generate a system interrupt.

Digital System

The digital system is composed of eight digital PSoC blocks. Each block is an 8-bit resource that may be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules.

Figure 1. Digital System Block Diagram [1]



Digital peripheral configurations are:

- PWMs (8- to 16-bit)
- PWMs with deadband (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- One-shot and multi-shot modules
- Full or half-duplex 8-bit UART with selectable parity (up to two full-duplex or four half-duplex)
- SPI master and slave (up to four total) with programmable data length from 8 to 16 bits.
- Shift register (1- to 32-bit)
- I^2C master, slave, or multi-master (one available)
- CRC/generator (16-bit)
- IrDA (up to two)
- PRS generators (8- to 32-bit)

Note
1. CY8C22x45 devices have 2 digital rows with 8 digital blocks. CY8C21x45 devices only have 1 digital row with 4 digital blocks.

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides a choice of system resources for your application. Family resources are shown in Table 1 on page 5.

Analog System

The Analog System of CY8C21x45 and CY8C22x45 PSoC devices consists of a 10-bit SAR ADC and six configurable analog blocks.

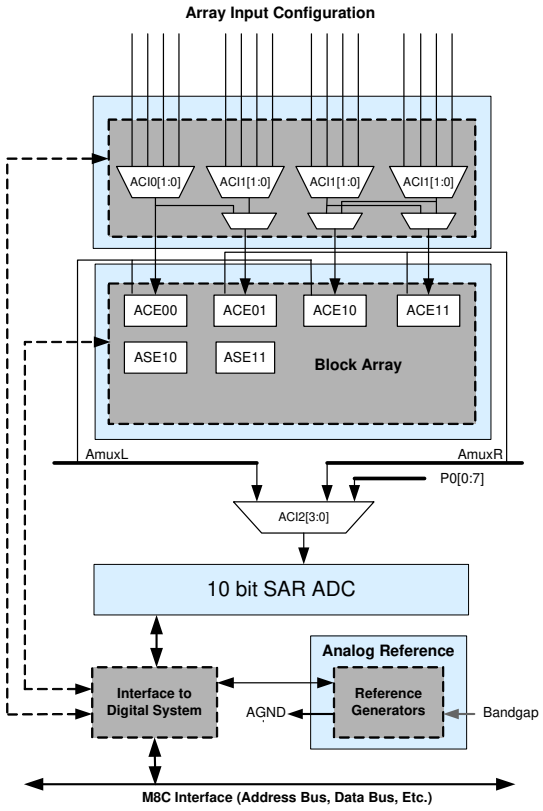
The programmable 10-bit SAR ADC is an optimized ADC with a fast maximum sample rate. External filters are required on ADC input channels for antialiasing. This ensures that any out-of-band content is not folded into the input signal band.

Reconfigurable analog resources allow creating complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with up to 10-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to four) with absolute (1.3 V) reference or DAC reference
- Precision voltage reference (1.3 V nominal)

CY8C21x45 and CY8C22x45 devices have six limited-functionality Type 'E' analog blocks. These analog blocks are arranged in four columns. Each column contains one continuous time (CT) Type E block. The first two columns also have a switched capacitor (SC) type E block. Refer to the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for detailed information on the Type E analog blocks.

Figure 2. Analog System Block Diagram



Haptics TS2000 Controller

The CY8C22x45H family of devices features an easy-to-use Haptics controller resource with up to 14 different effects. These effects are available for use with three different, selectable ERM modules.

Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful for complete systems. Additional resources include a MAC, low voltage detection, and power on reset. The merits of each system resource are:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Additional digital resources and clocks dedicated to and optimized for CapSense.
- RTC hardware block.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The I^2C module provides 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power on reset (POR) circuit eliminates the need for a system supervisor.
- An internal voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have varying numbers of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC families covered by this datasheet are highlighted in the table.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66 [2]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 [3]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94 [2]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A [2]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45 [2]	up to 38	2	8	up to 38	0	4	6 [3]	1 K	16 K
CY8C21x45 [2]	up to 24	1	4	up to 24	0	4	6 [3]	512	8 K
CY8C21x34 [2]	up to 28	1	4	up to 28	0	2	4 [3]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4 [3]	256	4 K
CY8C20x34 [2]	up to 28	0	0	up to 28	0	0	3 [3, 4]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3 [3, 4]	up to 2 K	up to 32 K

Notes
2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense® block.

Getting Started

For in depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pinouts

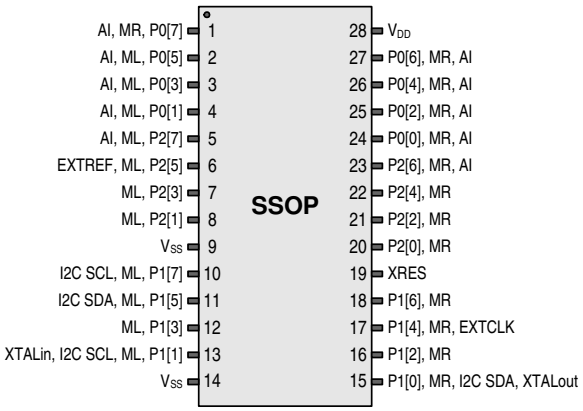
The automotive CY8C21x45 and CY8C22x45 PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog mux bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

28-pin Part Pinout

Table 2. 28-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, MR	P0[7]	Analog column mux input, C_{MOD} capacitor pin
2	I/O	I, ML	P0[5]	Analog column mux input, C_{MOD} capacitor pin
3	I/O	I, ML	P0[3]	Analog column mux input
4	I/O	I, ML	P0[1]	Analog column mux input
5	I/O	I, ML	P2[7]	Direct input to analog block
6	I/O	ML	P2[5]	Optional SAR ADC external reference (EXTREF)
7	I/O	ML	P2[3]	
8	I/O	ML	P2[1]	
9	Power		V_{SS}	Ground connection
10	I/O	ML	P1[7]	I^2C serial clock (SCL)
11	I/O	ML	P1[5]	I^2C serial data (SDA)
12	I/O	ML	P1[3]	
13	I/O	ML	P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[5]
14	Power		V_{SS}	Ground connection
15	I/O	MR	P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[5]
16	I/O	MR	P1[2]	
17	I/O	MR	P1[4]	Optional external clock input (EXTCLK)
18	I/O	MR	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	MR	P2[0]	
21	I/O	MR	P2[2]	
22	I/O	MR	P2[4]	
23	I/O	I, MR	P2[6]	Direct input to analog block
24	I/O	I, MR	P0[0]	Analog column mux input
25	I/O	I, MR	P0[2]	Analog column mux input
26	I/O	I, MR	P0[4]	Analog column mux input
27	I/O	I, MR	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

Figure 3. CY8C21345 and CY8C22345 28-pin PSoC Device



LEGEND: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input.

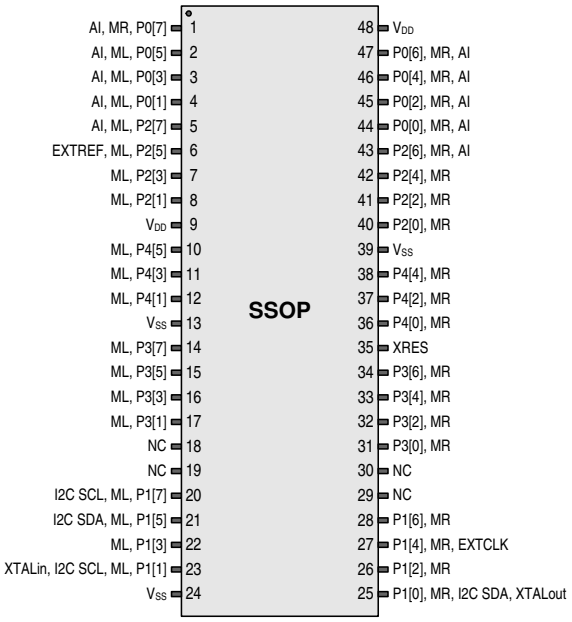
Note
5. These are the ISSP pins, which are not High Z after exiting a reset state. See the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for details.

48-pin Part Pinout

Table 3. 48-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, MR	P0[7]	Analog column mux input, C_{MOD} capacitor pin
2	I/O	I, ML	P0[5]	Analog column mux input, C_{MOD} capacitor pin
3	I/O	I, ML	P0[3]	Analog column mux input
4	I/O	I, ML	P0[1]	Analog column mux input
5	I/O	I, ML	P2[7]	Direct input to analog block
6	I/O	ML	P2[5]	Optional SAR ADC external reference
7	I/O	ML	P2[3]	
8	I/O	ML	P2[1]	
9	Power		V_{DD}	Supply voltage
10	I/O	ML	P4[5]	
11	I/O	ML	P4[3]	
12	I/O	ML	P4[1]	
13	Power		V_{SS}	Ground connection
14	I/O	ML	P3[7]	
15	I/O	ML	P3[5]	
16	I/O	ML	P3[3]	
17	I/O	ML	P3[1]	
18			NC	Not connected
19			NC	Not connected
20	I/O	ML	P1[7]	I^2C serial clock
21	I/O	ML	P1[5]	I^2C serial data
22	I/O	ML	P1[3]	
23	I/O	ML	P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[6]
24	Power		V_{SS}	
25	I/O	MR	P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[6]
26	I/O	MR	P1[2]	
27	I/O	MR	P1[4]	Optional external clock input
28	I/O	MR	P1[6]	
29			NC	Not connected
30			NC	Not connected
31	I/O	MR	P3[0]	
32	I/O	MR	P3[2]	
33	I/O	MR	P3[4]	
34	I/O	MR	P3[6]	
35	Input		XRES	Active high external reset with internal pull-down
36	I/O	MR	P4[0]	
37	I/O	MR	P4[2]	
38	I/O	MR	P4[4]	
39	Power		V_{SS}	Ground connection
40	I/O	MR	P2[0]	
41	I/O	MR	P2[2]	
42	I/O	MR	P2[4]	

Figure 4. CY8C21645 and CY8C22645 48-pin PSoC Device



Note
6. These are the ISSP pins, which are not High Z after exiting a reset state. See the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for details.

Table 3. 48-pin Part Pinout (SSOP) (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
43	I/O	I, MR	P2[6]	Direct input to analog block
44	I/O	I, MR	P0[0]	Analog column mux input
45	I/O	I, MR	P0[2]	Analog column mux input
46	I/O	I, MR	P0[4]	Analog column mux input
47	I/O	I, MR	P0[6]	Analog column mux input
48	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input

Registers

This section lists the registers of this PSoC device family by mapping tables. For detailed register information, refer to the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 4. Abbreviations

Convention	Description
RW	Read and write register or bit(s)
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
PRT2DR	08	RW		48			88		PWMVREF0	C8	#
PRT2IE	09	RW		49			89		PWMVREF1	C9	#
PRT2GS	0A	RW		4A			8A		IDAC_MODE	CA	RW
PRT2DM2	0B	RW		4B			8B		PWM_SRC	CB	#
PRT3DR	0C	RW		4C			8C		TS_CR0	CC	RW
PRT3IE	0D	RW		4D			8D		TS_CMPH	CD	RW
PRT3GS	0E	RW		4E			8E		TS_CMPL	CE	RW
PRT3DM2	0F	RW		4F			8F		TS_CR1	CF	RW
PRT4DR	10	RW	CSD0_DR0_L	50	R		90		CUR PP	D0	RW
PRT4IE	11	RW	CSD0_DR1_L	51	W		91		STK_PP	D1	RW
PRT4GS	12	RW	CSD0_CNT_L	52	R		92			D2	
PRT4DM2	13	RW	CSD0_CR0	53	#		93		IDX_PP	D3	RW
	14		CSD0_DR0_H	54	R		94		MVR_PP	D4	RW
	15		CSD0_DR1_H	55	W		95		MVW_PP	D5	RW
	16		CSD0_CNT_H	56	R		96		I2C0_CFG	D6	RW
	17		CSD0_CR1	57	RW		97		I2C0_SCR	D7	#
	18		CSD1_DR0_L	58	R		98		I2C0_DR	D8	RW
	19		CSD1_DR1_L	59	W		99		I2C0_MSCR	D9	#
	1A		CSD1_CNT_L	5A	R		9A		INT_CLR0	DA	RW
	1B		CSD1_CR0	5B	#		9B		INT_CLR1	DB	RW
	1C		CSD1_DR0_H	5C	R		9C		INT_CLR2	DC	RW
	1D		CSD1_DR1_H	5D	W		9D		INT_CLR3	DD	RW
	1E		CSD1_CNT_H	5E	R		9E		INT_MSK3	DE	RW
	1F		CSD1_CR1	5F	RW		9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW		A1		INT_MSK1	E1	RW
DBC00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4				
DBC01DR1	25	W	ASY_CR	65	#		A5				
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC _CR0	E6	RW
DBC01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCC02DR0	28	#	ADC0_CR	68	#		A8		MUL0_X	E8	W
DCC02DR1	29	W	ADC1_CR	69	#		A9		MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW		AA		MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW		AB		MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW		AC		ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW		AD		ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW		AE		ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW		AF		ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RDI0RI	B0	RW		F0	
DBC10DR1	31	W		71		RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#		74		RDI0LT1	B4	RW		F4	
DBC11DR1	35	W		75		RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACE01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW	IDACR_D	FC	RW
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW	IDACL_D	FD	RW
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. **# Access is bit specific.**

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	CMP0CR1	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	CMP0CR2	51	RW		91		GDI_E_IN	D1	RW
PRT4IC0	12	RW		52			92		GDI_O_OU	D2	RW
PRT4IC1	13	RW	VDAC50CR0	53	RW		93		GDI_E_OU	D3	RW
	14		CMP1CR1	54	RW		94			D4	
	15		CMP1CR2	55	RW		95			D5	
	16			56			96			D6	
	17		VDAC51CR0	57	RW		97			D7	
	18		CSCMPCR0	58	#		98		MUX_CR0	D8	RW
	19		CSCMPGOEN	59	RW		99		MUX_CR1	D9	RW
	1A		CSLUTCR0	5A	RW		9A		MUX_CR2	DA	RW
	1B		CMPCOLMUX	5B	RW		9B		MUX_CR3	DB	RW
	1C		CMPPWMCR	5C	RW		9C		DAC_CR1#	DC	RW
	1D		CMPFLTCR	5D	RW		9D		OSC_GO_EN	DD	RW
	1E		CMPCLK1	5E	RW		9E		OSC_CR4	DE	RW
	1F		CMPCLK0	5F	RW		9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	V2BG_TR	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	W
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	W
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DBC02CR1	2B	RW	CLK_CR3	6B	RW	SADC_CR3TRIM	AB	RW	ECO_TR	EB	W
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_AD	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DBC03CR1	2F	RW	TMP_DR3	6F	RW		AF			EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW		71		RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DBC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW	DAC_CR0#	FD	RW
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DBC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. **# Access is bit specific.**

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+150	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ±25 °C. Time spent in storage at a temperature greater than 65 °C counts toward the $Flash_{DR}$ electrical specification in Table 16 on page 20.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied A-grade devices E-grade devices	 –40 –40	 – –	 +85 +125	 °C °C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOz}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature A-grade devices E-grade devices	 –40 –40	 – –	 +85 +125	 °C °C	
T_J	Junction temperature A-grade devices E-grade devices	 –40 –40	 – –	 +100 +135	 °C °C	The temperature rise from ambient to junction is package specific. See Table 27 on page 34. The user must limit the power consumption to comply with this requirement.

Electrical Specifications

This section presents the DC and AC electrical specifications for automotive CY8C21x45 and CY8C22x45 PSoC devices. For the latest electrical specifications, check the most recent data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for A-grade devices at –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and for E-grade devices at –40 °C ≤ T_A ≤ 125 °C, T_J ≤ 135 °C, unless noted otherwise.

Figure 5. Voltage vs. CPU Frequency for A-grade Devices

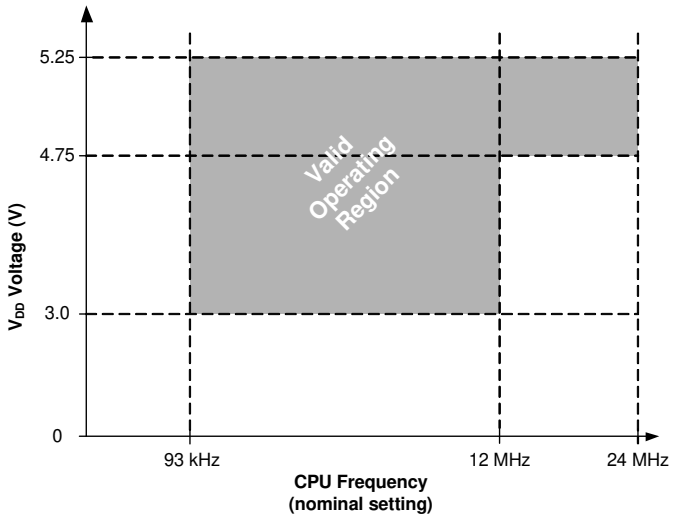


Figure 6. Voltage vs. CPU Frequency for E-grade Devices

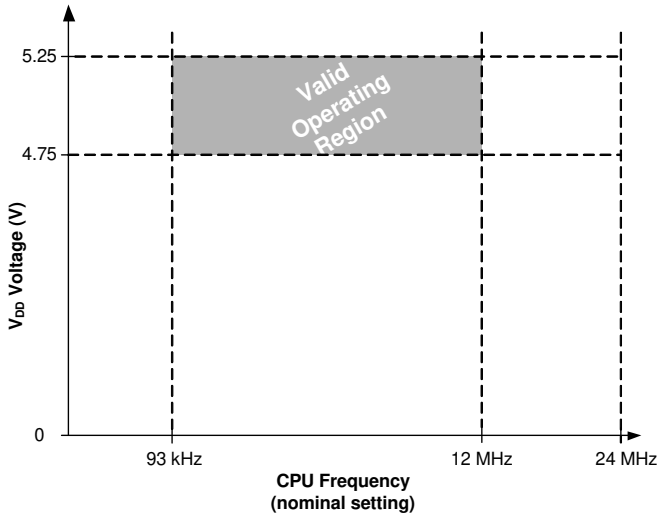
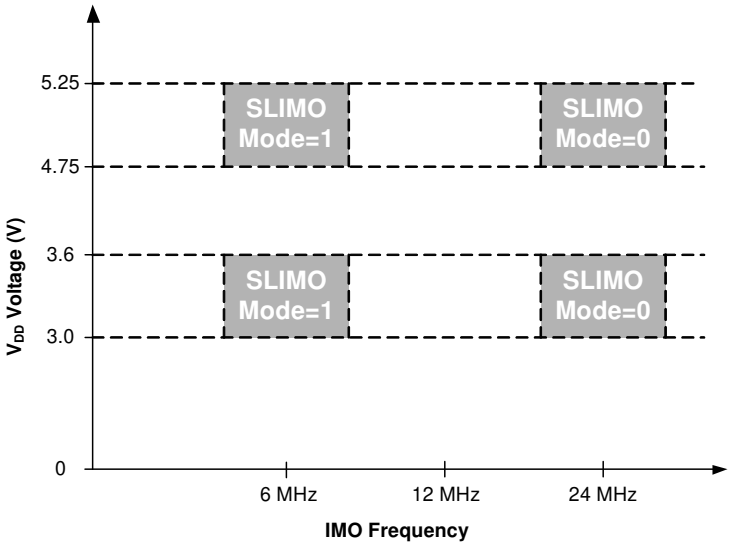


Figure 7. IMO Frequency Trim Options (A-grade Devices Only)



DC Electrical Characteristics

DC Chip Level Specifications

Table 9 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 9. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage A-grade devices E-grade devices	 3.0 4.75	 – –	 5.25 5.25	 V V	See Table 15 on page 19
I_{DD}	Supply current A-grade devices, 3.0 V ≤ V_{DD} ≤ 3.6 V A-grade devices, 4.75 V ≤ V_{DD} ≤ 5.25 V E-grade devices	 – – –	 4 7 8	 7 12 15	 mA mA mA	CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog blocks disabled
I_{SB}	Sleep (mode) current A-grade devices, 3.0 V ≤ V_{DD} ≤ 3.6 V A-grade devices, 4.75 V ≤ V_{DD} ≤ 5.25 V E-grade devices	 – – –	 3 4 4	 12 25 25	 µA µA µA	Everything disabled except ILO, POR, LVD, Sleep Timer, and WDT circuits
I_{SBXTL}	Sleep (mode) current with ECO A-grade devices, 3.0 V ≤ V_{DD} ≤ 3.6 V A-grade devices, 4.75 V ≤ V_{DD} ≤ 5.25 V E-grade devices	 – – –	 4 5 5	 13 26 26	 µA µA µA	Everything disabled except ECO, POR, LVD, Sleep Timer, and WDT circuits
V_{REF}	Reference voltage (Bandgap)	1.275	1.30	1.325	V	Trimmed for appropriate V_{DD} setting.

DC GPIO Specifications

Table 10 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 10. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	Also applies to the internal pull-down resistor on the XRES pin
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (80 mA maximum combined I_{OH} budget)
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (100 mA maximum combined I_{OL} budget)
		–	–	0.65	V	I_{OL} = 5 mA, V_{DD} = 3.0 to 3.6 V
I_{OH}	High-level source current	10	–	–	mA	$V_{OH} \geq V_{DD}$ – 1.0 V, see the limitations of the total current in the note for V_{OH}.
I_{OL}	Low-level sink current	25	–	–	mA	$V_{OL} \leq 0.75$ V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input low level	–	–	0.8	V	
V_{IH}	Input high level	2.1	–		V	
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C

DC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25°C, unless specified otherwise, and are for design guidance only.

Table 11. DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
I_{SOA}	Supply current (absolute value) A-grade devices E-grade devices	 – –	 – –	 30 35	 µA µA	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}[7]	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. T_A = 25 °C
V_{CMOA}	Common mode voltage range	0.5	–	V_{DD} – 1	V	

DC IDAC Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 12. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$IDAC_{GAIN}$	IDAC gain	–	75.4	218	nA/bit	IDAC gain at 1x current gain
		–	335	693	nA/bit	IDAC gain at 4x current gain
		–	1160	2410	nA/bit	IDAC gain at 16x current gain
		–	2340	5700	nA/bit	IDAC gain at 32x current gain
	Monotonicity	No	–	–	–	IDAC gain is non-monotonous at step intervals of (0x10)
$IDAC_{GAIN\_VAR}$	IDAC gain variation over temperature –40 °C to 85 °C	–	3.22	–	nA	at 1x current gain
		–	18.1	–	nA	at 4x current gain
		–	59.9	–	nA	at 16x current gain
		–	120	–	nA	at 32x current gain
I_{IDAC}	IDAC current at maximum code (0xFF)	–	19.2	–	µA	at 1x current gain
		–	85.4	–	µA	at 4x current gain
		–	295	–	µA	at 16x current gain
		–	596	–	µA	at 32x current gain

Note
7. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1 – 7 for the lowest leakage of 200 nA.

DC SAR10 ADC Specifications

Table 13 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 13. DC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ADCREF}	Reference voltage at pin P2[5] when configured as ADC reference voltage	3.0	–	5.25	V	When V_{REF} is buffered inside ADC, the voltage level at P2[5] (when configured as ADC reference voltage) must be always maintained to be at least 300 mV less than the chip supply voltage level on V_{DD} pin. ($V_{ADCREF} < V_{DD}$)
I_{ADCREF}	Current into P2[5] when configured as ADC V_{REF}	–	–	100	µA	Disables the internal voltage reference buffer
INL_{ADC}	Integral nonlinearity A-grade devices E-grade devices	 –3.0 –5.0	 – –	 3.0 5.0	 LSbit LSbit	10-bit resolution
DNL_{ADC}	Differential nonlinearity A-grade devices E-grade devices	 –1.5 –4.0	 – –	 1.5 4.0	 LSbit LSbit	10-bit resolution

DC Analog Mux Bus Specifications

Table 14 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 14. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400	Ω	
R_{GND}	Resistance of initialization switch to GND	–	–	800	Ω	

DC POR and LVD Specifications

Table 15 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 15. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 3.0 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.73	V	
	V_{DD} value for LVD trip					
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

DC Programming Specifications

Table 16 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 16. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify A-grade devices E-grade devices	 3.0 4.7	 3.1 4.8	 3.2 4.9	 V V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation A-grade devices E-grade devices	 3.0 4.75	 – –	 5.25 5.25	 V V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block) [8, 9] A-grade devices E-grade devices	 1,000 100	 – –	 – –	 – –	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total) [9, 10] CY8C21x45 A-grade devices CY8C22x45 A-grade devices CY8C21x45 E-grade devices CY8C22x45 E-grade devices	 128,000 256,000 12,800 25,600	 – – – –	 – – – –	 – – – –	Erase/write cycles
$Flash_{DR}$	Flash data retention [9] A-grade devices E-grade devices	 10 10	 – –	 – –	 Years Years	

Notes

8. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

AC Electrical Characteristics

AC Chip Level Specifications

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 17. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal main oscillator frequency for 24 MHz A-grade devices, 4.75 V ≤ V_{DD} ≤ 5.25 V A-grade devices, 3.0 V ≤ V_{DD} ≤ 3.6 V E-grade devices	 22.8 22.5 22.3	 24 24 24	 25.2 [11] 25.5 [11] 25.7 [11]	 MHz MHz MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 7 on page 14.
F_{IMO6}	Internal main oscillator frequency for 6 MHz A-grade devices E-grade devices	 5.5 5.5	 6 6	 6.5 [11] 6.5 [11]	 MHz MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 7 on page 14.
F_{CPU1}	CPU frequency (5 V V_{DD} operation) A-grade devices E-grade devices	 0.089 0.089	 – –	 25.2 [11] 12.6 [11]	 MHz MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V V_{DD} operation)	0.089	–	12.6 [11]	MHz	A-grade devices only. SLIMO mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V V_{DD} operation) A-grade devices E-grade devices	 0 0	 48 24	 50.4 [11, 12] 25.2 [11, 12]	 MHz MHz	Refer to Table 20 on page 24.
F_{BLK33}	Digital PSoC block frequency (3.3 V V_{DD} operation)	0	24	24.6 [11]	MHz	A-grade devices only
F_{32K1}	ILO frequency	15	32	75	kHz	This specification applies when the ILO has been trimmed.
F_{32KU}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Fout48M	48 MHz output frequency	45.6	48.0	50.4 [11]	MHz	
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.6	MHz	
$SR_{POWERUP}$	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time between end of POR state and CPU code execution	–	16	100	ms	Power-up from 0 V.

Notes
11. Accuracy derived from IMO with appropriate trim for V_{DD} range
12. Refer to the individual user module data sheets for information on maximum frequencies for user modules.

Table 17. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
t_{JIT_IMO}[13]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{JIT_PLL} [13]	PLL cycle-to-cycle jitter (RMS)	–	200	800	ps	
	PLL long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	PLL period jitter (RMS)	–	100	700	ps	

Note
13. Refer to Cypress Jitter Specifications document, Understanding Datasheet Jitter Specifications for Cypress Timing Products for more information.

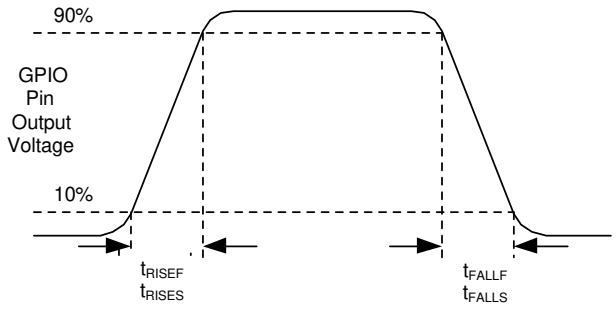
AC GPIO Specifications

Table 18 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 18. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.6	MHz	Normal strong mode
t_{RISEF}	Rise time, normal strong mode, Cload = 50 pF A-grade devices E-grade devices	 3 3	 – –	 18 24	 ns ns	Refer to Figure 8
t_{FALLF}	Fall time, normal strong mode, Cload = 50 pF A-grade devices E-grade devices	 2 2	 – –	 18 28	 ns ns	Refer to Figure 8
t_{RISES}	Rise time, slow strong mode, Cload = 50 pF A-grade devices E-grade devices	 7 7	 27 32	 – –	 ns ns	Refer to Figure 8
t_{FALLS}	Fall time, slow strong mode, Cload = 50 pF A-grade devices E-grade devices	 7 7	 22 28	 – –	 ns ns	Refer to Figure 8

Figure 8. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 19 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 19. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator mode response time, 50 mV	–	–	100	ns	

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 20. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block Input Clock Frequency					
	$V_{DD} \geq 4.75$ V	–	–	50.4 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	
Timer	Input Clock Frequency					
	No Capture, $V_{DD} \geq 4.75$ V	–	–	50.4 [15]	MHz	
	No Capture, $V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	
	With Capture	–	–	25.2 [15]	MHz	
	Capture Pulse Width	50 [14]	–	–	ns	
Counter	Input Clock Frequency					
	No Enable Input, $V_{DD} \geq 4.75$ V	–	–	50.4 [15]	MHz	
	No Enable Input, $V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	
	With Enable Input	–	–	25.2 [15]	MHz	
	Enable Input Pulse Width	50 [14]	–	–	ns	
Dead Band	Kill Pulse Width					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50 [14]	–	–	ns	
	Disable Mode	50 [14]	–	–	ns	
	Input Clock Frequency					
	$V_{DD} \geq 4.75$ V	–	–	50.4 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	
CRCPRS (PRS Mode)	Input Clock Frequency					
	$V_{DD} \geq 4.75$ V	–	–	50.4 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	
CRCPRS (CRC Mode)	Input Clock Frequency	–	–	25.2 [15]	MHz	
SPIM	Input Clock Frequency	–	–	8.4 [15]	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.2 [15]	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated Between Transmissions	50 [14]	–	–	ns	

Note
14. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 20. AC Digital Block Specifications (continued)

Function	Description	Min	Typ	Max	Units	Notes
Transmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 Stop Bits	–	–	50.4 [15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 Stop Bit	–	–	25.2 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 Stop Bits	–	–	50.4 [15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 Stop Bit	–	–	25.2 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	

Note
15. Accuracy derived from IMO with appropriate trim for V_{DD} range.