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PSoC Functional Overview

The PSoC family consists of many programmable system-on-chips with on-chip Controller devices. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture makes it possible for the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in the [Logic Block Diagram](#) on page 1, is comprised of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global buses allow all the device resources to be combined into a complete custom system. Each CY8C24x23A PSoC device includes four digital blocks and six analog blocks. Depending on the PSoC package, up to 24 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with multiple vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included sleep timer and watchdog timer (WDT).

Memory includes 4 KB of flash for program storage and 256 bytes of SRAM for data storage. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

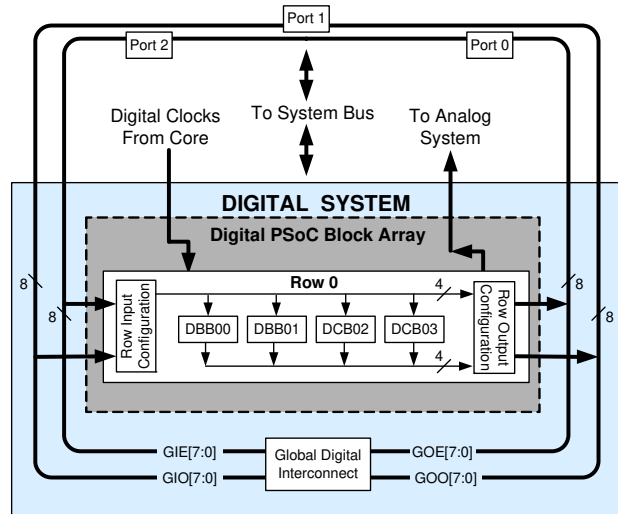
The PSoC device incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO) accurate to ±5% over temperature and voltage. A low-power 32-kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. If crystal accuracy is desired, the 32.768-kHz external crystal oscillator (ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24-MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt.

Digital System

The digital system is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules.

Figure 1. Digital System Block Diagram



Digital peripheral configurations include:

- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 24-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- Full- or half-duplex 8-bit UART with selectable parity
- SPI master and slave
- I²C master, slave, or multimaster (implemented in a dedicated I²C block)
- Cyclical redundancy checker/generator (16-bit)
- Infrared Data Association (IrDA)
- PRS generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in [Table 1](#) on page 5.

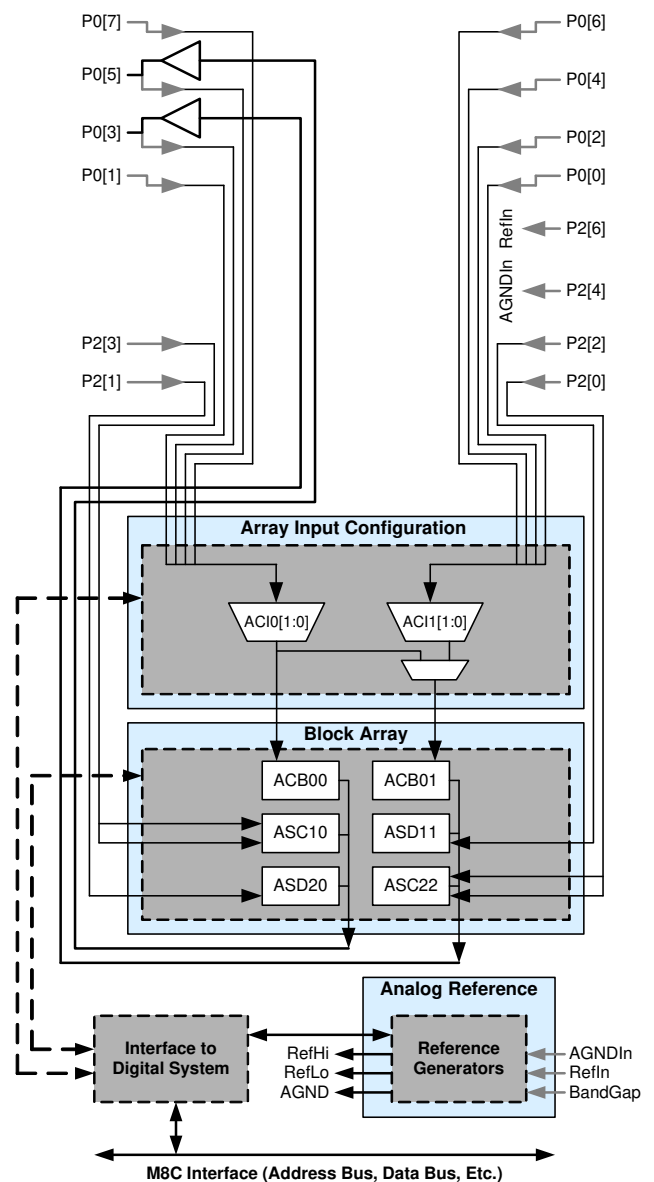
Analog System

The analog system is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are:

- ADCs (up to two, with 6- to 14-bit resolution, selectable as incremental, delta-sigma, or successive approximation register (SAR))
- Filters (two- and four-pole band pass, low pass, and notch)
- Amplifiers (up to two, with selectable gain up to 48x)
- Instrumentation amplifiers (one with selectable gain up to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6- to 9-bit resolution)
- Multiplying DACs (up to two, with 6- to 9-bit resolution)
- High current output drivers (two with 30-mA drive)
- 1.3 V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful for complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power-on reset (POR). Brief statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math as well as digital filters.

- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta-sigma ADCs.
- The I²C module provides 0 to 400 kHz communication over two wires. Slave, master, and multimaster modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have varying numbers of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The device covered by this data sheet is shown in the highlighted row of the table.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66 ^[2]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 ^[3]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94 ^[2]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A ^[2]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45 ^[2]	up to 38	2	8	up to 38	0	4	6 ^[3]	1 K	16 K
CY8C21x45 ^[2]	up to 24	1	4	up to 24	0	4	6 ^[3]	512	8 K
CY8C21x34 ^[2]	up to 28	1	4	up to 28	0	2	4 ^[3]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4 ^[3]	256	4 K
CY8C20x34 ^[2]	up to 28	0	0	up to 28	0	0	3 ^[3,4]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3 ^[3,4]	up to 2 K	up to 32 K

Notes

2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense[®] block.

Getting Started

For in-depth information, along with detailed programming details, see the *PSoC[®] Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits

- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional

subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select [User Modules](#)
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their

precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition

to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pinouts

The automotive CY8C24x23A PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

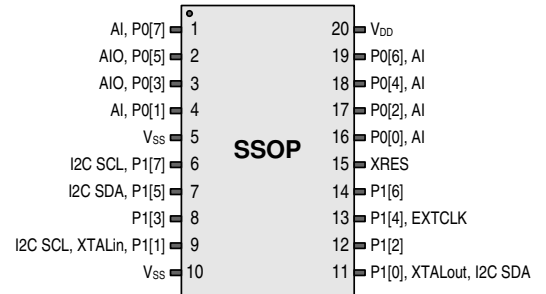
20-Pin Part Pinout

Table 2. 20-Pin Part Pinout (Shrink Small-Outline Package (SSOP))

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	Power		V _{SS}	Ground connection
6	I/O		P1[7]	I ² C serial clock (SCL)
7	I/O		P1[5]	I ² C serial data (SDA)
8	I/O		P1[3]	
9	I/O		P1[1]	Crystal input (XTALin), I ² C serial clock (SCL), ISSP-SCLK ^[5]
10	Power		V _{SS}	Ground connection
11	I/O		P1[0]	Crystal output (XTALout), I ² C serial data (SDA), ISSP-SDATA ^[5]
12	I/O		P1[2]	
13	I/O		P1[4]	Optional external clock input (EXTCLK)
14	I/O		P1[6]	
15	Input		XRES	Active high external reset with internal pull down
16	I/O	I	P0[0]	Analog column mux input
17	I/O	I	P0[2]	Analog column mux input
18	I/O	I	P0[4]	Analog column mux input
19	I/O	I	P0[6]	Analog column mux input
20	Power		V _{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C24223A 20-Pin PSoC Device



Note

5. These are the ISSP pins, which are not high Z when coming out of POR. See the [PSoC Technical Reference Manual](#) for details.

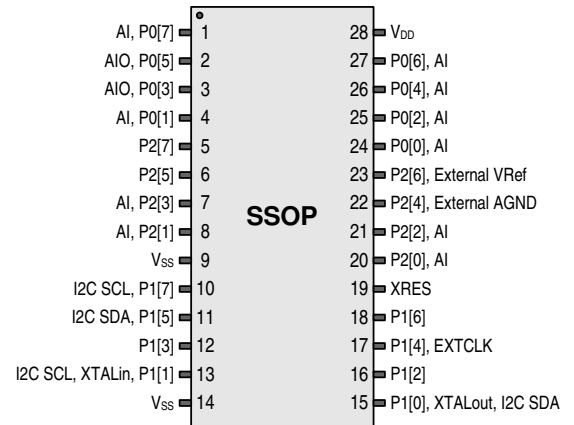
28-Pin Part Pinout

Table 3. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		V _{SS}	Ground connection
10	I/O		P1[7]	I ² C serial clock (SCL)
11	I/O		P1[5]	I ² C serial data (SDA)
12	I/O		P1[3]	
13	I/O		P1[1]	Crystal input (XTALin), I ² C serial clock (SCL), ISSP-SCLK ^[6]
14	Power		V _{SS}	Ground connection
15	I/O		P1[0]	Crystal output (XTALout), I ² C serial data (SDA), ISSP-SDATA ^[6]
16	I/O		P1[2]	
17	I/O		P1[4]	Optional external clock input (EXTCLK)
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O		P2[4]	External analog ground (AGND)
23	I/O		P2[6]	External voltage reference (VRef)
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I	P0[2]	Analog column mux input
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		V _{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 4. CY8C24423A 28-Pin PSoc Device



Note

6. These are the ISSP pins, which are not high Z when coming out of POR. See the *PSoc Technical Reference Manual* for details.

Registers

Register Conventions

This section lists the registers of the automotive CY8C24x23A PSoC device. For detailed register information, refer to the [PSoC Technical Reference Manual](#).

The register conventions specific to this section are listed in the following table.

Table 4. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, bank 0 and bank 1. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set to '1', the user is in bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW		D0	
	11			51		ASD20CR1	91	RW		D1	
	12			52		ASD20CR2	92	RW		D2	
	13			53		ASD20CR3	93	RW		D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the automotive CY8C24x23A PSoC devices. For the latest electrical specifications, visit <http://www.cypress.com>.

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted.

Refer to [Table 21](#) on page 27 for the electrical specifications of the IMO using slow IMO (SLIMO) mode.

Figure 5. Voltage versus CPU Frequency

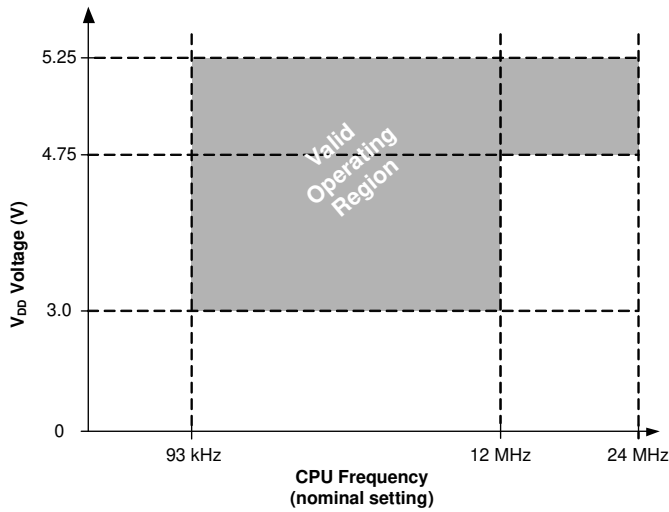
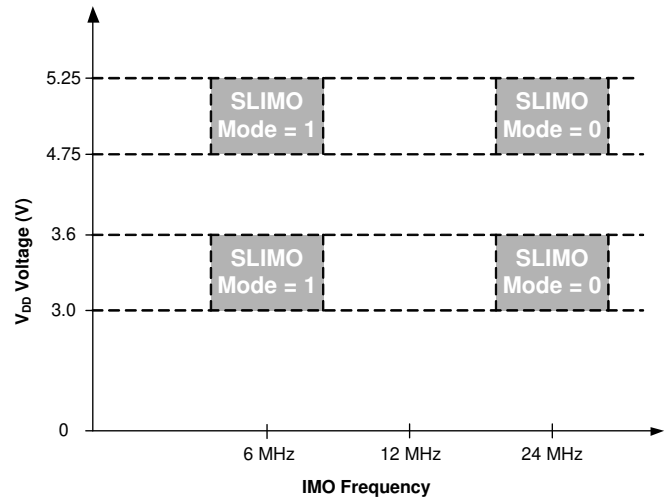


Figure 6. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T _{STG}	Storage temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Time spent in storage at a temperature greater than 65 °C counts toward the Flash _{DR} electrical specification in Table 20 on page 26.
T _{BAKETEMP}	Bake temperature	-	125	See package label	°C	
t _{BAKETIME}	Bake time	See package label	-	72	Hours	
T _A	Ambient temperature with power applied	-40	-	+85	°C	
V _{DD}	Supply voltage on V _{DD} relative to V _{SS}	-0.5	-	+6.0	V	
V _{IO}	DC input voltage	V _{SS} - 0.5	-	V _{DD} + 0.5	V	
V _{IOZ}	DC voltage applied to tristate	V _{SS} - 0.5	-	V _{DD} + 0.5	V	
I _{MIO}	Maximum current into any port pin	-25	-	+50	mA	
ESD	Electrostatic discharge voltage	2000	-	-	V	Human body model ESD.
LU	Latch up current	-	-	200	mA	

Operating Temperature
Table 8. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T _A	Ambient temperature	-40	-	+85	°C	
T _J	Junction temperature	-40	-	+100	°C	The temperature rise from ambient to junction is package specific. See Table 33 on page 37. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

Table 9 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 9. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{DD}	Supply voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 19 on page 25.
I _{DD}	Supply current	–	5	8	mA	Conditions are V _{DD} = 5.0 V, CPU = 3 MHz, 48 MHz disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. IMO = 24 MHz.
I _{DD3}	Supply current	–	3.3	6.0	mA	Conditions are V _{DD} = 3.3 V, CPU = 3 MHz, 48 MHz disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog power = off. IMO = 24 MHz.
I _{SB}	Sleep (mode) current with POR, LVD, sleep timer, and WDT. ^[7]	–	3	6.5	μA	V _{DD} = 3.3 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 55\text{ }^{\circ}\text{C}$, Analog power = off.
I _{SBH}	Sleep (mode) current with POR, LVD, sleep timer, and WDT at high temperature. ^[7]	–	4	25	μA	V _{DD} = 3.3 V, $55\text{ }^{\circ}\text{C} < T_A \leq 85\text{ }^{\circ}\text{C}$, Analog power = off.
I _{SBXTL}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and external crystal. ^[7]	–	4	7.5	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 55\text{ }^{\circ}\text{C}$, Analog power = off.
I _{SBXTLH}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and external crystal at high temperature. ^[7]	–	5	26	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3 V, $55\text{ }^{\circ}\text{C} < T_A \leq 85\text{ }^{\circ}\text{C}$, Analog power = off.
V _{REF}	Reference voltage (bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V _{DD} .

Note

7. Standby current includes all functions (POR, LVD, WDT, sleep timer) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

DC GPIO Specifications

Table 10 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 10. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R _{PU}	Pull-up resistor	4	5.6	8	kΩ	
R _{PD}	Pull-down resistor	4	5.6	8	kΩ	Also applies to the internal pull-down resistor on the XRES pin.
V _{OH}	High output level	V _{DD} - 1.0	–	–	V	I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25 V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I _{OH} budget.
V _{OL}	Low output level	–	–	0.75	V	I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25 V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I _{OL} budget.
I _{OH}	High-level source current	10	–	–	mA	V _{OH} ≥ V _{DD} - 1.0 V, see the limitations of the total current in the note for V _{OH} .
I _{OL}	Low-level sink current	25	–	–	mA	V _{OL} ≤ 0.75 V, see the limitations of the total current in the note for V _{OL} .
V _{IL}	Input low level	–	–	0.8	V	
V _{IH}	Input high level	2.1	–	–	V	
V _H	Input hysteresis	–	60	–	mV	
I _{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C _{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. T _A = 25 °C
C _{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. T _A = 25 °C

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog CT PSoC blocks and the analog SC PSoC blocks. The guaranteed specifications are measured in the analog CT PSoC block.

Table 11. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{OSO A}$	Input offset voltage (absolute value) Power = low, Opamp bias = high	–	1.6	10	mV	
	Power = medium, Opamp bias = high	–	1.3	8	mV	
	Power = high, Opamp bias = high	–	1.2	7.5	mV	
$TCV_{OSO A}$	Average input offset voltage drift	–	7.0	35.0	$\mu\text{V}/^{\circ}\text{C}$	
$I_{EBO A}$	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 μA .
$C_{INO A}$	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. $T_A = 25\text{ }^{\circ}\text{C}$.
$V_{CMO A}$	Common mode voltage range	0.0	–	V_{DD}	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common mode voltage range (high power or high opamp bias)	0.5	–	$V_{DD} - 0.5$	V	
$G_{OLO A}$	Open loop gain					Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = low, Opamp bias = high	60	–	–	dB	
	Power = medium, Opamp bias = high	60	–	–	dB	
$V_{OHIGHO A}$	High output voltage swing (internal signals)					
	Power = low, Opamp bias = high	$V_{DD} - 0.2$	–	–	V	
	Power = medium, Opamp bias = high	$V_{DD} - 0.2$	–	–	V	
$V_{OLOWO A}$	Low output voltage swing (internal signals)					
	Power = low, Opamp bias = high	–	–	0.2	V	
	Power = medium, Opamp bias = high	–	–	0.2	V	
$I_{SO A}$	Supply current (including associated AGND buffer)					
	Power = low, Opamp bias = high	–	150	200	μA	
	Power = low, Opamp bias = high	–	300	400	μA	
	Power = medium, Opamp bias = high	–	600	800	μA	
	Power = medium, Opamp bias = high	–	1200	1600	μA	
	Power = high, Opamp bias = high	–	2400	3200	μA	
$PSRR_{O A}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \leq V_{IN} \leq (V_{DD} - 2.25\text{ V})$ or $(V_{DD} - 1.25\text{ V}) \leq V_{IN} \leq V_{DD}$.

Table 12. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{OSOA}	Input offset voltage (absolute value)	–	1.65	10	mV	Power = high, Opamp bias = high is not allowed.
	Power = low, Opamp bias = high	–	1.32	8	mV	
	Power = medium, Opamp bias = high	–	–	–	mV	
	Power = high, Opamp bias = high	–	–	–	mV	
TCV _{OSOA}	Average input offset voltage drift	–	7.0	35.0	μV/°C	
I _{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 μA.
C _{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. T _A = 25 °C
V _{CMOA}	Common mode voltage range	0.2	–	V _{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G _{OLOA}	Open loop gain	60	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = low, Opamp bias = low	60	–	–		
	Power = medium, Opamp bias = low	60	–	–		
	Power = high, Opamp bias = low	80	–	–		
V _{OHIGHOA}	High output voltage swing (internal signals)	V _{DD} – 0.2	–	–	V	
	Power = low, Opamp bias = low	V _{DD} – 0.2	–	–	V	
	Power = medium, Opamp bias = low	V _{DD} – 0.2	–	–	V	
	Power = high, Opamp bias = low	V _{DD} – 0.2	–	–	V	
V _{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.2	V	
	Power = low, Opamp bias = low	–	–	0.2	V	
	Power = medium, Opamp bias = low	–	–	0.2	V	
	Power = high, Opamp bias = low	–	–	0.2	V	
I _{SOA}	Supply current (including associated AGND buffer)	–	–	–	–	Power = high, Opamp bias = high is not allowed.
	Power = low, Opamp bias = low	–	150	200	μA	
	Power = low, Opamp bias = high	–	300	400	μA	
	Power = medium, Opamp bias = low	–	600	800	μA	
	Power = medium, Opamp bias = high	–	1200	1600	μA	
	Power = high, Opamp bias = low	–	2400	3200	μA	
	Power = high, Opamp bias = high	–	–	–	μA	
PSRR _{OA}	Supply voltage rejection ratio	64	80	–	dB	V _{SS} ≤ VIN ≤ (V _{DD} – 2.25) or (V _{DD} – 1.25 V) ≤ VIN ≤ V _{DD} .

DC Low Power Comparator Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 13. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V _{DD} – 1	V	
I _{SLPC}	LPC supply current	–	10	40	μA	
V _{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 14. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	$\mu\text{V}/^{\circ}\text{C}$	
V_{CMOB}	Common mode input voltage range	0.5	–	$V_{DD} - 1.0$	V	
R_{OUTOB}	Output resistance	–	1	–	Ω	
	Power = low Power = high	– –	1 1	– –	Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = $32\ \Omega$ to $V_{DD}/2$)	Power = low	$0.5 \times V_{DD} + 1.1$	–	V	
		Power = high	$0.5 \times V_{DD} + 1.1$	–	V	
V_{OLOWOB}	Low output voltage swing (Load = $32\ \Omega$ to $V_{DD}/2$)	Power = low	–	$0.5 \times V_{DD} - 1.3$	V	
		Power = high	–	$0.5 \times V_{DD} - 1.3$	V	
I_{SOB}	Supply current including bias cell (no load)	Power = low	–	5.1	mA	
		Power = high	–	2.6 8.8	mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	$V_{OUT} > (V_{DD} - 1.25)$.
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.

Table 15. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	$\mu\text{V}/^{\circ}\text{C}$	
V_{CMOB}	Common mode input voltage range	0.5	–	$V_{DD} - 1.0$	V	
R_{OUTOB}	Output resistance	–	1	–	Ω	
	Power = low Power = high	– –	1 1	– –	Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = $1\ \text{k}\Omega$ to $V_{DD}/2$)	Power = low	$0.5 \times V_{DD} + 1.0$	–	V	
		Power = high	$0.5 \times V_{DD} + 1.0$	–	V	
V_{OLOWOB}	Low output voltage swing (Load = $1\ \text{k}\Omega$ to $V_{DD}/2$)	Power = low	–	$0.5 \times V_{DD} - 1.0$	V	
		Power = high	–	$0.5 \times V_{DD} - 1.0$	V	
I_{SOB}	Supply current including bias cell (no load)	Power = low	–	0.8 2.0	mA	
		Power = high	–	2.0 4.3	mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	$V_{OUT} > (V_{DD} - 1.25)$.
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.

DC Analog Reference Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLO are measured through the analog continuous time PSoC blocks. The power levels for RefHI and RefLO refer to the analog reference control register. AGND is measured at P2[4] in AGND bypass mode. Each analog continuous time PSoC block adds a maximum of 10 mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the analog reference. Some coupling of the digital signal may appear on the AGND.

Table 16. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.136	V _{DD} /2 + 1.288	V _{DD} /2 + 1.409	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.138	V _{DD} /2 + 0.003	V _{DD} /2 + 0.132	V
		V _{REFLO}	Ref Low	V _{DD} /2 - Bandgap	V _{DD} /2 - 1.417	V _{DD} /2 - 1.289	V _{DD} /2 - 1.154	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.202	V _{DD} /2 + 1.290	V _{DD} /2 + 1.358	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.055	V _{DD} /2 + 0.001	V _{DD} /2 + 0.055	V
		V _{REFLO}	Ref Low	V _{DD} /2 - Bandgap	V _{DD} /2 - 1.369	V _{DD} /2 - 1.295	V _{DD} /2 - 1.218	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.211	V _{DD} /2 + 1.292	V _{DD} /2 + 1.357	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.055	V _{DD} /2	V _{DD} /2 + 0.052	V
		V _{REFLO}	Ref Low	V _{DD} /2 - Bandgap	V _{DD} /2 - 1.368	V _{DD} /2 - 1.298	V _{DD} /2 - 1.224	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.215	V _{DD} /2 + 1.292	V _{DD} /2 + 1.353	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.040	V _{DD} /2 - 0.001	V _{DD} /2 + 0.033	V
		V _{REFLO}	Ref Low	V _{DD} /2 - Bandgap	V _{DD} /2 - 1.368	V _{DD} /2 - 1.299	V _{DD} /2 - 1.225	V
0b001	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] + P2[6] - 0.076	P2[4] + P2[6] - 0.021	P2[4] + P2[6] + 0.041	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] - P2[6] - 0.025	P2[4] - P2[6] + 0.011	P2[4] - P2[6] + 0.085	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] + P2[6] - 0.069	P2[4] + P2[6] - 0.014	P2[4] + P2[6] + 0.043	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] - P2[6] - 0.029	P2[4] - P2[6] + 0.005	P2[4] - P2[6] + 0.052	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] + P2[6] - 0.072	P2[4] + P2[6] - 0.011	P2[4] + P2[6] + 0.048	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] - P2[6] - 0.031	P2[4] - P2[6] + 0.002	P2[4] - P2[6] + 0.057	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] + P2[6] - 0.070	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.047	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] - P2[6] - 0.033	P2[4] - P2[6] + 0.001	P2[4] - P2[6] + 0.039	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b010	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	V _{DD}	V _{DD} - 0.121	V _{DD} - 0.003	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.040	V _{DD} /2	V _{DD} /2 + 0.034	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.019	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	V _{DD}	V _{DD} - 0.083	V _{DD} - 0.002	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.040	V _{DD} /2 - 0.001	V _{DD} /2 + 0.033	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.016	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	V _{DD}	V _{DD} - 0.075	V _{DD} - 0.002	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.040	V _{DD} /2 - 0.001	V _{DD} /2 + 0.032	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.015	V
RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	V _{DD}	V _{DD} - 0.074	V _{DD} - 0.002	V _{DD}	V	
	V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.040	V _{DD} /2 - 0.001	V _{DD} /2 + 0.032	V	
	V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.014	V	
0b011	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	3 × Bandgap	3.753	3.874	3.979	V
		V _{AGND}	AGND	2 × Bandgap	2.511	2.590	2.657	V
		V _{REFLO}	Ref Low	Bandgap	1.243	1.297	1.333	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	3 × Bandgap	3.767	3.881	3.974	V
		V _{AGND}	AGND	2 × Bandgap	2.518	2.592	2.652	V
		V _{REFLO}	Ref Low	Bandgap	1.241	1.295	1.330	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	3 × Bandgap	2.771	3.885	3.979	V
		V _{AGND}	AGND	2 × Bandgap	2.521	2.593	2.649	V
		V _{REFLO}	Ref Low	Bandgap	1.240	1.295	1.331	V
RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	3 × Bandgap	3.771	3.887	3.977	V	
	V _{AGND}	AGND	2 × Bandgap	2.522	2.594	2.648	V	
	V _{REFLO}	Ref Low	Bandgap	1.239	1.295	1.332	V	
0b100	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.481 + P2[6]	2.569 + P2[6]	2.639 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.511	2.590	2.658	V
		V _{REFLO}	Ref Low	2 × Bandgap - P2[6] (P2[6] = 1.3 V)	2.515 - P2[6]	2.602 - P2[6]	2.654 - P2[6]	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.498 + P2[6]	2.579 + P2[6]	2.642 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.518	2.592	2.652	V
		V _{REFLO}	Ref Low	2 × Bandgap - P2[6] (P2[6] = 1.3 V)	2.513 - P2[6]	2.598 - P2[6]	2.650 - P2[6]	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.504 + P2[6]	2.583 + P2[6]	2.646 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.521	2.592	2.650	V
		V _{REFLO}	Ref Low	2 × Bandgap - P2[6] (P2[6] = 1.3 V)	2.513 - P2[6]	2.596 - P2[6]	2.649 - P2[6]	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 + P2[6]	2.586 + P2[6]	2.648 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.521	2.594	2.648	V
		V _{REFLO}	Ref Low	2 × Bandgap - P2[6] (P2[6] = 1.3 V)	2.513 - P2[6]	2.595 - P2[6]	2.648 - P2[6]	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.228	P2[4] + 1.284	P2[4] + 1.332	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.358	P2[4] – 1.293	P2[4] – 1.226	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.236	P2[4] + 1.289	P2[4] + 1.332	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.357	P2[4] – 1.297	P2[4] – 1.229	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.237	P2[4] + 1.291	P2[4] + 1.337	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.356	P2[4] – 1.299	P2[4] – 1.232	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.237	P2[4] + 1.292	P2[4] + 1.337	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.357	P2[4] – 1.300	P2[4] – 1.233	V
0b110	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap	2.512	2.594	2.654	V
		V _{AGND}	AGND	Bandgap	1.250	1.303	1.346	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.011	V _{SS} + 0.027	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap	2.515	2.592	2.654	V
		V _{AGND}	AGND	Bandgap	1.253	1.301	1.340	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.02	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap	2.518	2.593	2.651	V
		V _{AGND}	AGND	Bandgap	1.254	1.301	1.338	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap	2.517	2.594	2.650	V
		V _{AGND}	AGND	Bandgap	1.255	1.300	1.337	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.015	V
0b111	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	3.2 × Bandgap	4.011	4.143	4.203	V
		V _{AGND}	AGND	1.6 × Bandgap	2.020	2.075	2.118	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.011	V _{SS} + 0.026	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	3.2 × Bandgap	4.022	4.138	4.203	V
		V _{AGND}	AGND	1.6 × Bandgap	2.023	2.075	2.114	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	3.2 × Bandgap	4.026	4.141	4.207	V
		V _{AGND}	AGND	1.6 × Bandgap	2.024	2.075	2.114	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.015	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	3.2 × Bandgap	4.030	4.143	4.206	V
		V _{AGND}	AGND	1.6 × Bandgap	2.024	2.076	2.112	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.013	V

Table 17. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.170	V _{DD} /2 + 1.288	V _{DD} /2 + 1.376	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.098	V _{DD} /2 + 0.003	V _{DD} /2 + 0.097	V
		V _{REFLO}	Ref Low	V _{DD} /2 - Bandgap	V _{DD} /2 - 1.386	V _{DD} /2 - 1.287	V _{DD} /2 - 1.169	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.210	V _{DD} /2 + 1.290	V _{DD} /2 + 1.355	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.055	V _{DD} /2 + 0.001	V _{DD} /2 + 0.054	V
		V _{REFLO}	Ref Low	V _{DD} /2 - Bandgap	V _{DD} /2 - 1.359	V _{DD} /2 - 1.292	V _{DD} /2 - 1.214	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.198	V _{DD} /2 + 1.292	V _{DD} /2 + 1.368	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.041	V _{DD} /2	V _{DD} /2 + 0.04	V
		V _{REFLO}	Ref Low	V _{DD} /2 - Bandgap	V _{DD} /2 - 1.362	V _{DD} /2 - 1.295	V _{DD} /2 - 1.220	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.202	V _{DD} /2 + 1.292	V _{DD} /2 + 1.364	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.033	V _{DD} /2	V _{DD} /2 + 0.030	V
		V _{REFLO}	Ref Low	V _{DD} /2 - Bandgap	V _{DD} /2 - 1.364	V _{DD} /2 - 1.297	V _{DD} /2 - 1.222	V
0b001	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] - 0.072	P2[4] + P2[6] - 0.017	P2[4] + P2[6] + 0.041	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] - P2[6] - 0.029	P2[4] - P2[6] + 0.010	P2[4] - P2[6] + 0.048	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] - 0.066	P2[4] + P2[6] - 0.010	P2[4] + P2[6] + 0.043	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] - P2[6] - 0.024	P2[4] - P2[6] + 0.004	P2[4] - P2[6] + 0.034	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] - 0.073	P2[4] + P2[6] - 0.007	P2[4] + P2[6] + 0.053	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] - P2[6] - 0.028	P2[4] - P2[6] + 0.002	P2[4] - P2[6] + 0.033	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] - 0.073	P2[4] + P2[6] - 0.006	P2[4] + P2[6] + 0.056	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	-
		V _{REFLO}	Ref Low	P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] - P2[6] - 0.030	P2[4] - P2[6]	P2[4] - P2[6] + 0.032	V
0b010	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	V _{DD}	V _{DD} - 0.102	V _{DD} - 0.003	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.040	V _{DD} /2 + 0.001	V _{DD} /2 + 0.039	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.005	V _{SS} + 0.020	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	V _{DD}	V _{DD} - 0.082	V _{DD} - 0.002	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.031	V _{DD} /2	V _{DD} /2 + 0.028	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.015	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	V _{DD}	V _{DD} - 0.083	V _{DD} - 0.002	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.032	V _{DD} /2 - 0.001	V _{DD} /2 + 0.029	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.014	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	V _{DD}	V _{DD} - 0.081	V _{DD} - 0.002	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 - 0.033	V _{DD} /2 - 0.001	V _{DD} /2 + 0.029	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.013	V
0b011	All power settings Not allowed at 3.3 V	-	-	-	-	-	-	-

Table 17. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b100	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–
0b101	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.211	P2[4] + 1.285	P2[4] + 1.348	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.354	P2[4] – 1.290	P2[4] – 1.197	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.209	P2[4] + 1.289	P2[4] + 1.353	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.352	P2[4] – 1.294	P2[4] – 1.222	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.218	P2[4] + 1.291	P2[4] + 1.351	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.351	P2[4] – 1.296	P2[4] – 1.224	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.215	P2[4] + 1.292	P2[4] + 1.354	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.352	P2[4] – 1.297	P2[4] – 1.227	V
0b110	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap	2.460	2.594	2.695	V
		V _{AGND}	AGND	Bandgap	1.257	1.302	1.335	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.01	V _{SS} + 0.029	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap	2.462	2.592	2.692	V
		V _{AGND}	AGND	Bandgap	1.256	1.301	1.332	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.005	V _{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap	2.473	2.593	2.682	V
		V _{AGND}	AGND	Bandgap	1.257	1.301	1.330	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.014	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap	2.470	2.594	2.685	V
		V _{AGND}	AGND	Bandgap	1.256	1.300	1.332	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.012	V
0b111	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	

DC Analog PSoC Block Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R _{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C _{SC}	Capacitor unit value (switched capacitor)	–	80	–	fF	

DC POR and LVD Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the [PSoC Programmable System-on-Chip Technical Reference Manual](#) for more information on the VLT_CR register.

Table 19. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR0}	V_{DD} value for PPOR trip PORLEV[1:0] = 00b	–	2.36	2.40	V	V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51 ^[8]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99 ^[9]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

Notes

8. Always greater than 50 mV above V_{PPOR} (PORLEV=00) for falling supply.
9. Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply.