



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an ARM® Cortex™-M0+ CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC 4100S product family is a member of the PSoC 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CapSense) with best-in-class performance, programmable general-purpose continuous-time and switched-capacitor analog blocks, and programmable connectivity. PSoC 4100S products will be upward compatible with members of the PSoC 4 platform for new applications and design needs.

## Features

### 32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0+ CPU
- Up to 64 KB of flash with Read Accelerator
- Up to 8 KB of SRAM

### Programmable Analog

- Two opamps with reconfigurable high-drive external and high-bandwidth internal drive and Comparator modes and ADC input buffering capability. Opamps can operate in Deep Sleep low-power mode.
- 12-bit 1-Msps SAR ADC with differential and single-ended modes, and Channel Sequencer with signal averaging
- Single-slope 10-bit ADC function provided by a capacitance sensing block
- Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
- Two low-power comparators that operate in Deep Sleep low-power mode

### Programmable Digital

- Programmable logic blocks allowing Boolean operations to be performed on port inputs and outputs

### Low-Power 1.71-V to 5.5-V Operation

- Deep Sleep mode with operational analog and 2.5- $\mu$ A digital system current

### Capacitive Sensing

- Cypress CapSense Sigma-Delta (CSD) provides best-in-class signal-to-noise ratio (SNR) (>5:1) and water tolerance
- Cypress-supplied software component makes capacitive sensing design easy
- Automatic hardware tuning (SmartSense™)

### LCD Drive Capability

- LCD segment drive capability on GPIOs

### Serial Communication

- Three independent run-time reconfigurable Serial Communication Blocks (SCBs) with re-configurable I<sup>2</sup>C, SPI, or UART functionality

### Timing and Pulse-Width Modulation

- Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

### Up to 36 Programmable GPIO Pins

- 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball WLCSP packages
- Any GPIO pin can be CapSense, analog, or digital
- Drive modes, strengths, and slew rates are programmable

### PSoC Creator Design Environment

- Integrated Development Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
- Applications Programming Interface (API) component for all fixed-function and programmable peripherals

### Industry-Standard Tool Compatibility

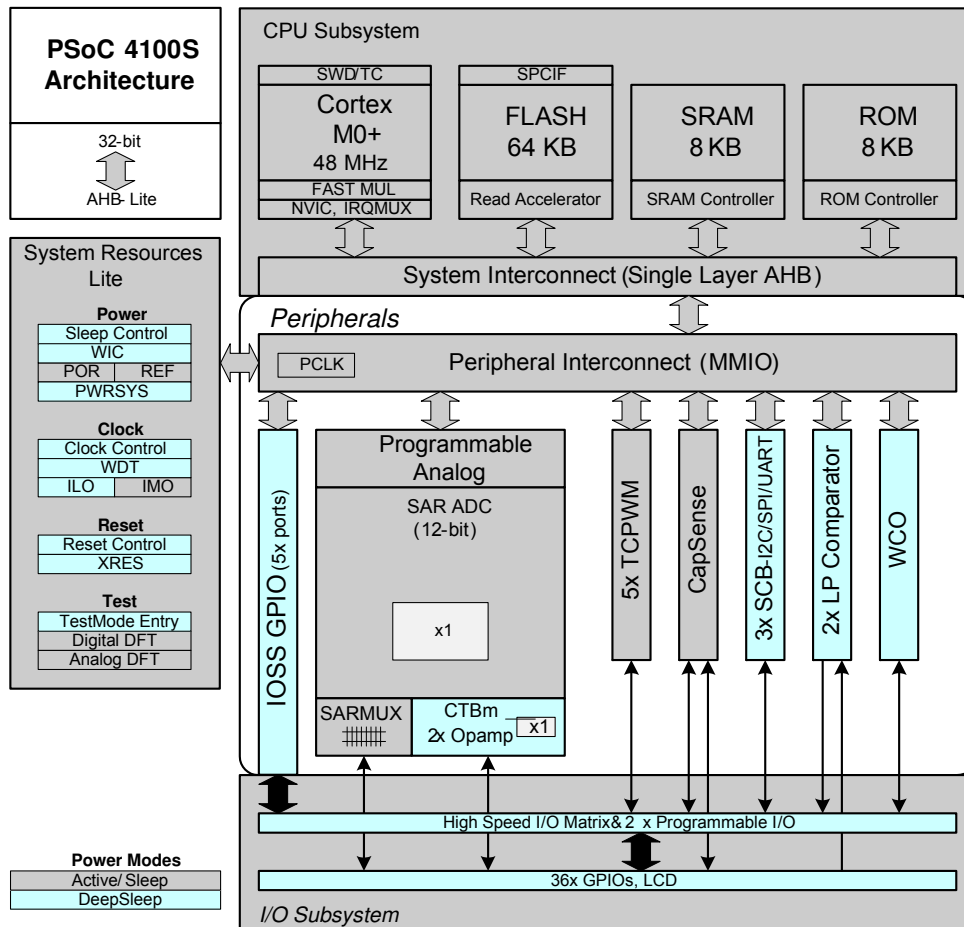
- After schematic entry, development can be done with ARM-based industry-standard development tools

## Contents

<b>Functional Definition</b> .....	<b>4</b>	Digital Peripherals .....	25
CPU and Memory Subsystem .....	4	Memory .....	28
System Resources .....	4	System Resources .....	28
Analog Blocks .....	5	<b>Ordering Information</b> .....	<b>31</b>
Fixed Function Digital .....	5	<b>Packaging</b> .....	<b>34</b>
GPIO .....	6	Package Diagrams .....	35
Special Function Peripherals.....	6	<b>Acronyms</b> .....	<b>38</b>
<b>Pinouts</b> .....	<b>7</b>	<b>Document Conventions</b> .....	<b>40</b>
Alternate Pin Functions .....	9	Units of Measure .....	40
<b>Power</b> .....	<b>11</b>	<b>Revision History</b> .....	<b>41</b>
Mode 1: 1.8 V to 5.5 V External Supply .....	11	<b>Sales, Solutions, and Legal Information</b> .....	<b>42</b>
Mode 2: 1.8 V ±5% External Supply.....	11	Worldwide Sales and Design Support.....	42
<b>Development Support</b> .....	<b>12</b>	Products .....	42
Documentation .....	12	PSoC® Solutions .....	42
Online .....	12	Cypress Developer Community.....	42
Tools.....	12	Technical Support .....	42
<b>Electrical Specifications</b> .....	<b>13</b>		
Absolute Maximum Ratings.....	13		
Device Level Specifications.....	13		
Analog Peripherals .....	17		



**Figure 1. Block Diagram**



PSoC 4100S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S allows the customer to make.

## Functional Definition

### CPU and Memory Subsystem

#### CPU

The Cortex-M0+ CPU in the PSoC 4100S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S has four breakpoint (address) comparators and two watchpoint (data) comparators.

#### Flash

The PSoC 4100S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

#### SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

#### SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

## System Resources

#### Power System

The power system is described in detail in the section [Power on page 11](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4100S operates with a single external supply over the range of either 1.8 V  $\pm$ 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4100S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35  $\mu$ s. The opamps can remain operational in Deep Sleep mode.

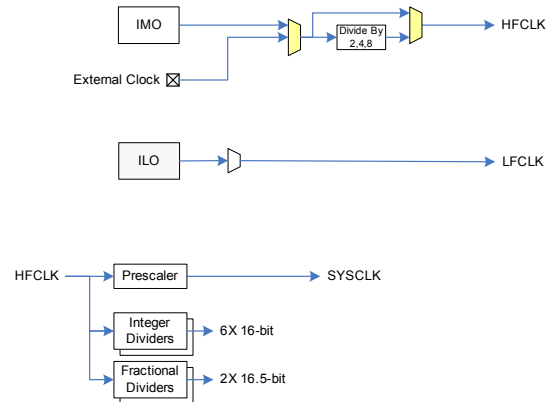
#### Clock System

The PSoC 4100S clock system is responsible for providing clocks to all subsystems that require clocks and for switching

between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

**Figure 2. PSoC 4100S MCU Clocking Architecture**



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4100S; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

#### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is  $\pm$ 2%.

#### ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

#### Watch Crystal Oscillator (WCO)

The PSoC 4100S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

#### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

### Reset

The PSoc 4100S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

### Analog Blocks

#### 12-bit SAR ADC

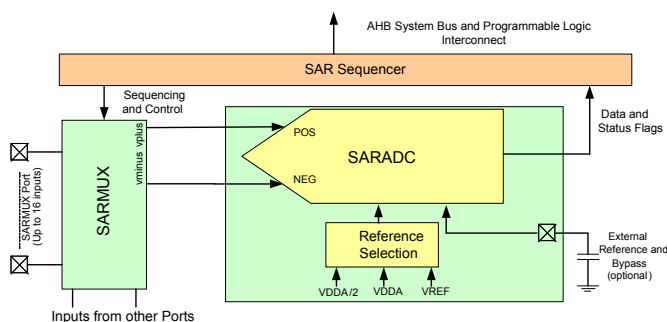
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

**Figure 3. SAR ADC**



#### Two Opamps (Continuous-Time Block; CTB)

The PSoc 4100S has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage

Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives, saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

#### Low-power Comparators (LPC)

The PSoc 4100S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

#### Current DACs

The PSoc 4100S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

#### Analog Multiplexed Buses

The PSoc 4100S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

### Programmable Digital Blocks

The Programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

### Fixed Function Digital

#### Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoc 4100S.

#### Serial Communication Block (SCB)

The PSoc 4100S has three serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

**I<sup>2</sup>C Mode:** The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also

supports EZI2C that creates a mailbox address range in the memory of the PSoC 4100S and effectively reduces I<sup>2</sup>C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode and Fast-mode devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4100S is not completely compliant with the I<sup>2</sup>C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system.

**UART Mode:** This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

**SPI Mode:** The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codex), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

## GPIO

The PSoC 4100S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100S).

## Special Function Peripherals

### CapSense

CapSense is supported in the PSoC 4100S through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

### LCD Segment Drive

The PSoC 4100S has an LCD controller, which can drive up to 4 commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

## Pinouts

The following table provides the pin list for PSoC 4100S for the 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 32-pin QFN, and 35-ball CSP packages. All port pins support GPIO.

**Table 1. Pin List**

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
28	P0.0	24	P0.0	22	P0.0	17	P0.0	C3	P0.0
29	P0.1	25	P0.1	23	P0.1	18	P0.1	A5	P0.1
30	P0.2	26	P0.2	24	P0.2	19	P0.2	A4	P0.2
31	P0.3	27	P0.3	25	P0.3	20	P0.3	A3	P0.3
32	P0.4	28	P0.4	26	P0.4	21	P0.4	B3	P0.4
33	P0.5	29	P0.5	27	P0.5	22	P0.5	A6	P0.5
34	P0.6	30	P0.6	28	P0.6	23	P0.6	B4	P0.6
35	P0.7	31	P0.7	29	P0.7			B5	P0.7
36	XRES	32	XRES	30	XRES	24	XRES	B6	XRES
37	VCCD	33	VCCD	31	VCCD	25	VCCD	A7	VCCD
38	VSSD			DN	VSSD	26	VSSD	B7	VSS
39	VDDD	34	VDDD	32	VDDD			C7	VDD
40	VDDA	35	VDDA	33	VDDA	27	VDD	C7	VDD
41	VSSA	36	VSSA	34	VSSA	28	VSSA	B7	VSS
42	P1.0	37	P1.0	35	P1.0	29	P1.0	C4	P1.0
43	P1.1	38	P1.1	36	P1.1	30	P1.1	C5	P1.1
44	P1.2	39	P1.2	37	P1.2	31	P1.2	C6	P1.2
45	P1.3	40	P1.3	38	P1.3	32	P1.3	D7	P1.3
46	P1.4	41	P1.4	39	P1.4			D4	P1.4
47	P1.5	42	P1.5					D5	P1.5
48	P1.6	43	P1.6					D6	P1.6
1	P1.7/VREF	44	P1.7/VREF	40	P1.7/VREF	1	P1.7/VREF	E7	P1.7/VREF
		1	VSSD						
2	P2.0	2	P2.0	1	P2.0	2	P2.0		
3	P2.1	3	P2.1	2	P2.1	3	P2.1		
4	P2.2	4	P2.2	3	P2.2	4	P2.2	D3	P2.2
5	P2.3	5	P2.3	4	P2.3	5	P2.3	E4	P2.3
6	P2.4	6	P2.4	5	P2.4			E5	P2.4
7	P2.5	7	P2.5	6	P2.5	6	P2.5	E6	P2.5
8	P2.6	8	P2.6	7	P2.6	7	P2.6	E3	P2.6
9	P2.7	9	P2.7	8	P2.7	8	P2.7	E2	P2.7
10	VSSD	10	VSSD	9	VSSD				
12	P3.0	11	P3.0	10	P3.0	9	P3.0	E1	P3.0
13	P3.1	12	P3.1	11	P3.1	10	P3.1	D2	P3.1
14	P3.2	13	P3.2	12	P3.2	11	P3.2	D1	P3.2
16	P3.3	14	P3.3	13	P3.3	12	P3.3	C1	P3.3
17	P3.4	15	P3.4	14	P3.4			C2	P3.4
18	P3.5	16	P3.5	15	P3.5				



**Table 1. Pin List** (continued)

48-TQFP		44-TQFP		40-QFN		32-QFN		35-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
19	P3.6	17	P3.6	16	P3.6				
20	P3.7	18	P3.7	17	P3.7				
21	VDDD	19	VDDD						
22	P4.0	20	P4.0	18	P4.0	13	P4.0	B1	P4.0
23	P4.1	21	P4.1	19	P4.1	14	P4.1	B2	P4.1
24	P4.2	22	P4.2	20	P4.2	15	P4.2	A2	P4.2
25	P4.3	23	P4.3	21	P4.3	16	P4.3	A1	P4.3

**Notes:** Pins 11, 15, 26, and 27 are No Connects (NC) on the 48-pin TQFP.

**Descriptions of the Power pins are as follows:**

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ±5%)

VDD: Power supply to all sections of the chip

VSS: Ground for all sections of the chip

### Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

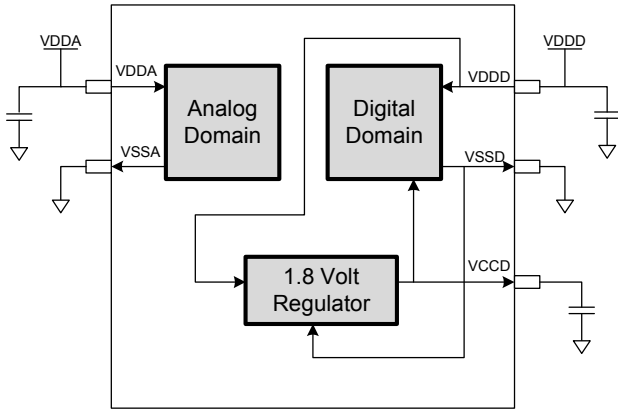
Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						scb[2].spi_select0
P0.4	wco.wco_in			scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1		scb[1].spi_clk:1
P0.7			tcpwm.line[0]:2	scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0	ctb0_oa0+		tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0_oa0-		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0_oa0_out		tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	ctb0_oa1_out		tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.4	ctb0_oa1-						scb[0].spi_select1:1
P1.5	ctb0_oa1+						scb[0].spi_select2:1
P1.6	ctb0_oa0+						scb[0].spi_select3:1
P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1						scb[2].spi_clk
P2.0	sarmux[0]	prgio[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	prgio[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux[2]	prgio[0].io[2]					scb[1].spi_clk:2
P2.3	sarmux[3]	prgio[0].io[3]					scb[1].spi_select0:2

Port/Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P2.4	sarmux[4]	prgio[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux[5]	prgio[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux[6]	prgio[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux[7]	prgio[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		prgio[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		prgio[1].io[6]	tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		prgio[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

## Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4100S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the  $V_{DD}$  input.

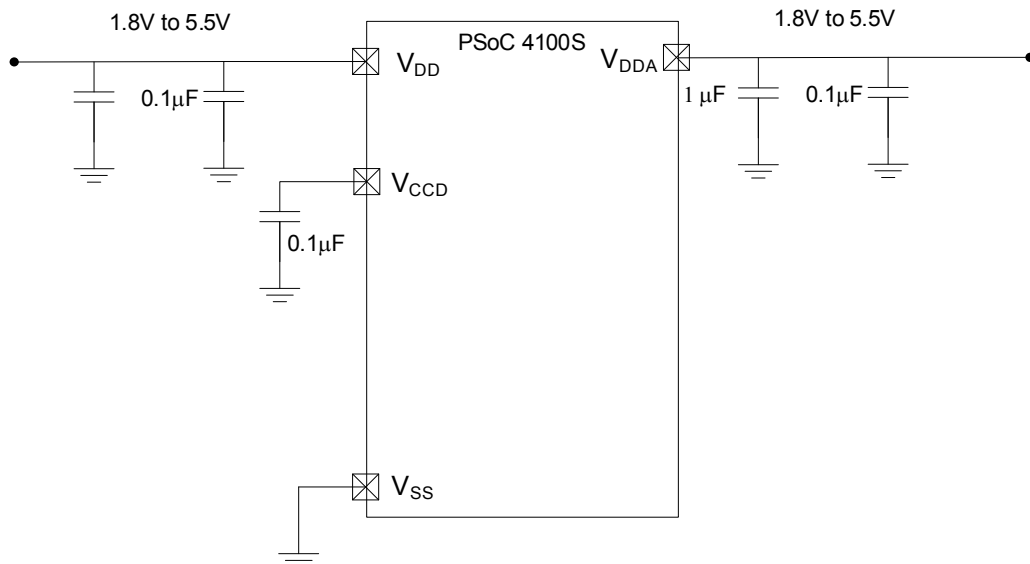
**Figure 4. Power Supply Connections**



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is 1.8 V  $\pm$ 5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

**Figure 5. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active**

Power supply bypass connections example



### Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC 4100S is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4100S supplies the internal logic and its output is connected to the  $V_{CCD}$  pin. The  $V_{CCD}$  pin must be bypassed to ground via an external capacitor (0.1  $\mu$ F; X5R ceramic or better) and must not be connected to anything else.

### Mode 2: 1.8 V $\pm$ 5% External Supply

In this mode, the PSoC 4100S is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the  $V_{DD}$  and  $V_{CCD}$  pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from  $V_{DDD}$  to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- $\mu$ F range, in parallel with a smaller capacitor (0.1  $\mu$ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.



## Development Support

The PSoC 4100S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit [www.cypress.com/go/psoc4](http://www.cypress.com/go/psoc4) to find out more.

### Documentation

A suite of documentation supports the PSoC 4100S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide:** A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets:** The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes:** PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual:** The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at [www.cypress.com/psoc4](http://www.cypress.com/psoc4).

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100S family is part of a development tool ecosystem. Visit us at [www.cypress.com/go/psoccreator](http://www.cypress.com/go/psoccreator) for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

## Electrical Specifications

### Absolute Maximum Ratings

**Table 2. Absolute Maximum Ratings<sup>[1]</sup>**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID1	V <sub>DDD_ABS</sub>	Digital supply relative to V <sub>SS</sub>	-0.5	-	6	V	-
SID2	V <sub>CDD_ABS</sub>	Direct digital core voltage input relative to V <sub>SS</sub>	-0.5	-	1.95		-
SID3	V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5	-	V <sub>DD</sub> +0.5		-
SID4	I <sub>GPIO_ABS</sub>	Maximum current per GPIO	-25	-	25	mA	-
SID5	I <sub>GPIO_injection</sub>	GPIO injection current, Max for V <sub>IH</sub> > V <sub>DDD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	-	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	-	-	V	-
BID45	ESD_CDM	Electrostatic discharge charged device model	500	-	-		-
BID46	LU	Pin current for latch-up	-140	-	140	mA	-

### Device Level Specifications

All specifications are valid for -40 °C ≤ T<sub>A</sub> ≤ 85 °C and T<sub>J</sub> ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 3. DC Specifications**

Typical values measured at V<sub>DD</sub> = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID53	V <sub>DD</sub>	Power supply input voltage	1.8	-	5.5	V	Internally regulated supply
SID255	V <sub>DD</sub>	Power supply input voltage (V <sub>CDD</sub> = V <sub>DDD</sub> = V <sub>DDA</sub> )	1.71	-	1.89		Internally unregulated supply
SID54	V <sub>CDD</sub>	Output voltage (for core logic)	-	1.8	-		-
SID55	C <sub>EFC</sub>	External regulator voltage bypass	-	0.1	-	μF	X5R ceramic or better
SID56	C <sub>EXC</sub>	Power supply bypass capacitor	-	1	-		X5R ceramic or better

**Active Mode, V<sub>DD</sub> = 1.8 V to 5.5 V. Typical values measured at V<sub>DD</sub> = 3.3 V and 25 °C.**

SID10	I <sub>DD5</sub>	Execute from flash; CPU at 6 MHz	-	1.8	2.7	mA	Max is at 85 °C and 5.5 V
SID16	I <sub>DD8</sub>	Execute from flash; CPU at 24 MHz	-	3.0	4.75		Max is at 85 °C and 5.5 V
SID19	I <sub>DD11</sub>	Execute from flash; CPU at 48 MHz	-	5.4	6.85		Max is at 85 °C and 5.5 V

#### Note

- Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 3. DC Specifications** (continued)

Typical values measured at  $V_{DD} = 3.3\text{ V}$  and  $25\text{ }^\circ\text{C}$ .

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
<b>Sleep Mode, <math>V_{DDD} = 1.8\text{ V to }5.5\text{ V}</math> (Regulator on)</b>							
SID22	IDD17	I <sup>2</sup> C wakeup WDT, and Comparators on	–	1.7	2.2	mA	6 MHz. Max is at $85\text{ }^\circ\text{C}$ and $5.5\text{ V}$ .
SID25	IDD20	I <sup>2</sup> C wakeup, WDT, and Comparators on.	–	2.2	2.5		12 MHz. Max is at $85\text{ }^\circ\text{C}$ and $5.5\text{ V}$ .
<b>Sleep Mode, <math>V_{DDD} = 1.71\text{ V to }1.89\text{ V}</math> (Regulator bypassed)</b>							
SID28	IDD23	I <sup>2</sup> C wakeup, WDT, and Comparators on	–	0.7	0.9	mA	6 MHz. Max is at $85\text{ }^\circ\text{C}$ and $5.5\text{ V}$ .
SID28A	IDD23A	I <sup>2</sup> C wakeup, WDT, and Comparators on	–	1	1.2	mA	12 MHz. Max is at $85\text{ }^\circ\text{C}$ and $5.5\text{ V}$ .
<b>Deep Sleep Mode, <math>V_{DD} = 1.8\text{ V to }3.6\text{ V}</math> (Regulator on)</b>							
SID31	I <sub>DD26</sub>	I <sup>2</sup> C wakeup and WDT on	–	2.5	60	μA	Max is at $3.6\text{ V}$ and $85\text{ }^\circ\text{C}$ .
<b>Deep Sleep Mode, <math>V_{DD} = 3.6\text{ V to }5.5\text{ V}</math> (Regulator on)</b>							
SID34	I <sub>DD29</sub>	I <sup>2</sup> C wakeup and WDT on	–	2.5	60	μA	Max is at $5.5\text{ V}$ and $85\text{ }^\circ\text{C}$ .
<b>Deep Sleep Mode, <math>V_{DD} = V_{CCD} = 1.71\text{ V to }1.89\text{ V}</math> (Regulator bypassed)</b>							
SID37	I <sub>DD32</sub>	I <sup>2</sup> C wakeup and WDT on	–	2.5	65	μA	Max is at $1.89\text{ V}$ and $85\text{ }^\circ\text{C}$ .
<b>XRES Current</b>							
SID307	I <sub>DD_XR</sub>	Supply current while XRES asserted	–	2	5	mA	–

**Table 4. AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F <sub>CPU</sub>	CPU frequency	DC	–	48	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49 <sup>[3]</sup>	T <sub>SLEEP</sub>	Wakeup from Sleep mode	–	0	–	μs	
SID50 <sup>[3]</sup>	T <sub>DEEPSLEEP</sub>	Wakeup from Deep Sleep mode	–	35	–		

**Note**

2. Guaranteed by characterization.

GPIO

**Table 5. GPIO DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions	
SID57	$V_{IH}^{[3]}$	Input voltage high threshold	$0.7 \times V_{DDD}$	–	–	V	CMOS Input	
SID58	$V_{IL}$	Input voltage low threshold	–	–	$0.3 \times V_{DDD}$		CMOS Input	
SID241	$V_{IH}^{[3]}$	LVTTL input, $V_{DDD} < 2.7 V$	$0.7 \times V_{DDD}$	–	–		–	
SID242	$V_{IL}$	LVTTL input, $V_{DDD} < 2.7 V$	–	–	$0.3 \times V_{DDD}$		–	
SID243	$V_{IH}^{[3]}$	LVTTL input, $V_{DDD} \geq 2.7 V$	2.0	–	–		–	
SID244	$V_{IL}$	LVTTL input, $V_{DDD} \geq 2.7 V$	–	–	0.8		–	
SID59	$V_{OH}$	Output voltage high level	$V_{DDD} - 0.6$	–	–		$I_{OH} = 4 mA$ at $3 V V_{DDD}$	
SID60	$V_{OH}$	Output voltage high level	$V_{DDD} - 0.5$	–	–		$I_{OH} = 1 mA$ at $1.8 V V_{DDD}$	
SID61	$V_{OL}$	Output voltage low level	–	–	0.6		$I_{OL} = 4 mA$ at $1.8 V V_{DDD}$	
SID62	$V_{OL}$	Output voltage low level	–	–	0.6		$I_{OL} = 10 mA$ at $3 V V_{DDD}$	
SID62A	$V_{OL}$	Output voltage low level	–	–	0.4		$I_{OL} = 3 mA$ at $3 V V_{DDD}$	
SID63	$R_{PULLUP}$	Pull-up resistor	3.5	5.6	8.5		k $\Omega$	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5			–
SID65	$I_{IL}$	Input leakage current (absolute value)	–	–	2		nA	25 °C, $V_{DDD} = 3.0 V$
SID66	$C_{IN}$	Input capacitance	–	–	7	pF	–	
SID67 <sup>[4]</sup>	$V_{HYSTTL}$	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7 V$	
SID68 <sup>[4]</sup>	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDD}$	–	–		$V_{DD} < 4.5 V$	
SID68A <sup>[4]</sup>	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		$V_{DD} > 4.5 V$	
SID69 <sup>[4]</sup>	$I_{DIODE}$	Current through protection diode to $V_{DD}/V_{SS}$	–	–	100	$\mu A$	–	
SID69A <sup>[4]</sup>	$I_{TOT\_GPIO}$	Maximum total source or sink chip current	–	–	200	mA	–	

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	$T_{RISEF}$	Rise time in fast strong mode	2	–	12	ns	3.3 V $V_{DDD}$ , Load = 25 pF
SID71	$T_{FALLF}$	Fall time in fast strong mode	2	–	12		3.3 V $V_{DDD}$ , Load = 25 pF
SID72	$T_{RISES}$	Rise time in slow strong mode	10	–	60	–	3.3 V $V_{DDD}$ , Load = 25 pF

**Notes**

- $V_{IH}$  must not exceed  $V_{DDD} + 0.2 V$ .
- Guaranteed by characterization.



**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID73	T <sub>FALLS</sub>	Fall time in slow strong mode	10	–	60	–	3.3 V V <sub>DDD</sub> , Cload = 25 pF
SID74	F <sub>GPIOOUT1</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DDD</sub> ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	F <sub>GPIOOUT2</sub>	GPIO F <sub>OUT</sub> ; 1.71 V ≤ V <sub>DDD</sub> ≤ 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	F <sub>GPIOOUT3</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DDD</sub> ≤ 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	F <sub>GPIOOUT4</sub>	GPIO F <sub>OUT</sub> ; 1.71 V ≤ V <sub>DDD</sub> ≤ 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F <sub>GPIOIN</sub>	GPIO input operating frequency; 1.71 V ≤ V <sub>DDD</sub> ≤ 5.5 V	–	–	48		90/10% V <sub>IO</sub>

XRES

**Table 7. XRES DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V <sub>IH</sub>	Input voltage high threshold	0.7 × V <sub>DDD</sub>	–	–	V	CMOS Input
SID78	V <sub>IL</sub>	Input voltage low threshold	–	–	0.3 × V <sub>DDD</sub>		
SID79	R <sub>PULLUP</sub>	Pull-up resistor	–	60	–	kΩ	–
SID80	C <sub>IN</sub>	Input capacitance	–	–	7	pF	–
SID81 <sup>[5]</sup>	V <sub>HYSXRES</sub>	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V <sub>DD</sub> > 4.5 V
SID82	I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	–	–	100	μA	

**Table 8. XRES AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83 <sup>[5]</sup>	T <sub>RESETWIDTH</sub>	Reset pulse width	1	–	–	μs	–
BID194 <sup>[5]</sup>	T <sub>RESETWAKE</sub>	Wake-up time from reset release	–	–	2.7	ms	–

**Note**

5. Guaranteed by characterization.

## Analog Peripherals

**Table 9. CTBm Opamp Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions	
	I <sub>DD</sub>	Opamp block current, External load						
SID269	I <sub>DD_HI</sub>	power=hi	–	1100	1850	μA	–	
SID270	I <sub>DD_MED</sub>	power=med	–	550	950		–	
SID271	I <sub>DD_LOW</sub>	power=lo	–	150	350		–	
	G <sub>BW</sub>	Load = 20 pF, 0.1 mA V <sub>DDA</sub> = 2.7 V						
SID272	G <sub>BW_HI</sub>	power=hi	6	–	–	MHz	Input and output are 0.2 V to V <sub>DDA</sub> -0.2 V	
SID273	G <sub>BW_MED</sub>	power=med	3	–	–		Input and output are 0.2 V to V <sub>DDA</sub> -0.2 V	
SID274	G <sub>BW_LO</sub>	power=lo	–	1	–		Input and output are 0.2 V to V <sub>DDA</sub> -0.2 V	
	I <sub>OUT_MAX</sub>	V <sub>DDA</sub> = 2.7 V, 500 mV from rail						
SID275	I <sub>OUT_MAX_HI</sub>	power=hi	10	–	–	mA	Output is 0.5 V V <sub>DDA</sub> -0.5 V	
SID276	I <sub>OUT_MAX_MID</sub>	power=mid	10	–	–		Output is 0.5 V V <sub>DDA</sub> -0.5 V	
SID277	I <sub>OUT_MAX_LO</sub>	power=lo	–	5	–		Output is 0.5 V V <sub>DDA</sub> -0.5 V	
	I <sub>OUT</sub>	V <sub>DDA</sub> = 1.71 V, 500 mV from rail						
SID278	I <sub>OUT_MAX_HI</sub>	power=hi	4	–	–	mA	Output is 0.5 V V <sub>DDA</sub> -0.5 V	
SID279	I <sub>OUT_MAX_MID</sub>	power=mid	4	–	–		Output is 0.5 V V <sub>DDA</sub> -0.5 V	
SID280	I <sub>OUT_MAX_LO</sub>	power=lo	–	2	–		Output is 0.5 V V <sub>DDA</sub> -0.5 V	
	I <sub>DD_Int</sub>	Opamp block current Internal Load						
SID269_I	I <sub>DD_HI_Int</sub>	power=hi	–	1500	1700	μA	–	
SID270_I	I <sub>DD_MED_Int</sub>	power=med	–	700	900		–	
SID271_I	I <sub>DD_LOW_Int</sub>	power=lo	–	–	–		–	
	G <sub>BW</sub>	V <sub>DDA</sub> = 2.7 V	–	–	–	–		
SID272_I	G <sub>BW_HI_Int</sub>	power=hi	8	–	–	MHz	Output is 0.25 V to V <sub>DDA</sub> -0.25 V	

**Table 9. CTBm Opamp Specifications (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
		General opamp specs for both internal and external modes					
SID281	V <sub>IN</sub>	Charge-pump on, V <sub>DDA</sub> = 2.7 V	-0.05	-	V <sub>DDA</sub> -0.2	V	-
SID282	V <sub>CM</sub>	Charge-pump on, V <sub>DDA</sub> = 2.7 V	-0.05	-	V <sub>DDA</sub> -0.2		-
	V <sub>OUT</sub>	V <sub>DDA</sub> = 2.7 V					
SID283	V <sub>OUT_1</sub>	power=hi, Iload=10 mA	0.5	-	V <sub>DDA</sub> -0.5	V	-
SID284	V <sub>OUT_2</sub>	power=hi, Iload=1 mA	0.2	-	V <sub>DDA</sub> -0.2		-
SID285	V <sub>OUT_3</sub>	power=med, Iload=1 mA	0.2	-	V <sub>DDA</sub> -0.2		-
SID286	V <sub>OUT_4</sub>	power=lo, Iload=0.1 mA	0.2	-	V <sub>DDA</sub> -0.2		-
SID288	V <sub>OS_TR</sub>	Offset voltage, trimmed	-1.0	±0.5	1.0	mV	High mode, input 0 V to V <sub>DDA</sub> -0.2 V
SID288A	V <sub>OS_TR</sub>	Offset voltage, trimmed	-	±1	-		Medium mode, input 0 V to V <sub>DDA</sub> -0.2 V
SID288B	V <sub>OS_TR</sub>	Offset voltage, trimmed	-	±2	-		Low mode, input 0 V to V <sub>DDA</sub> -0.2 V
SID290	V <sub>OS_DR_TR</sub>	Offset voltage drift, trimmed	-10	±3	10	μV/C	High mode
SID290A	V <sub>OS_DR_TR</sub>	Offset voltage drift, trimmed	-	±10	-	μV/C	Medium mode
SID290B	V <sub>OS_DR_TR</sub>	Offset voltage drift, trimmed	-	±10	-		Low mode
SID291	CMRR	DC	70	80	-	dB	Input is 0 V to V <sub>DDA</sub> -0.2 V, Output is 0.2 V to V <sub>DDA</sub> -0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	-		V <sub>DDD</sub> = 3.6 V, high-power mode, input is 0.2 V to V <sub>DDA</sub> -0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power=Hi	-	72	-	nV/rtHz	3
SID295	VN3	Input-referred, 10 kHz, power=Hi	-	28	-		Input and output are at 0.2 V to V <sub>DDA</sub> -0.2 V
SID296	VN4	Input-referred, 100 kHz, power=Hi	-	15	-		Input and output are at 0.2 V to V <sub>DDA</sub> -0.2 V
SID297	C <sub>LOAD</sub>	Stable up to max. load. Performance specs at 50 pF.	-	-	125	pF	-
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V <sub>DDA</sub> = 2.7 V	6	-	-	V/μs	-

**Table 9. CTBm Opamp Specifications** (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions	
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB		
	COMP_MODE	Comparator mode; 50 mV drive, T <sub>rise</sub> =T <sub>fall</sub> (approx.)						
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to V <sub>DDA</sub> -0.2 V	
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to V <sub>DDA</sub> -0.2 V	
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to V <sub>DDA</sub> -0.2 V	
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–	
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–	
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.						
SID_DS_1	I <sub>DD_HI_M1</sub>	Mode 1, High current	–	1400	–	µA	25 °C	
SID_DS_2	I <sub>DD_MED_M1</sub>	Mode 1, Medium current	–	700	–		25 °C	
SID_DS_3	I <sub>DD_LOW_M1</sub>	Mode 1, Low current	–	200	–		25 °C	
SID_DS_4	I <sub>DD_HI_M2</sub>	Mode 2, High current	–	120	–		25 °C	
SID_DS_5	I <sub>DD_MED_M2</sub>	Mode 2, Medium current	–	60	–		25 °C	
SID_DS_6	I <sub>DD_LOW_M2</sub>	Mode 2, Low current	–	15	–		25 °C	



**Table 9. CTBm Opamp Specifications (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_7	$G_{BW\_HI\_M1}$	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_8	$G_{BW\_MED\_M1}$	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_9	$G_{BW\_LOW\_M1}$	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_10	$G_{BW\_HI\_M2}$	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_11	$G_{BW\_MED\_M2}$	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_12	$G_{BW\_LOW\_M2}$	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_13	$V_{OS\_HI\_M1}$	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_14	$V_{OS\_MED\_M1}$	Mode 1, Medium current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_15	$V_{OS\_LOW\_M2}$	Mode 1, Low current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_16	$V_{OS\_HI\_M2}$	Mode 2, High current	–	5	–		With trim 25 °C, 0.2V to $V_{DDA}-0.2$ V
SID_DS_17	$V_{OS\_MED\_M2}$	Mode 2, Medium current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_18	$V_{OS\_LOW\_M2}$	Mode 2, Low current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_19	$I_{OUT\_HI\_M1}$	Mode 1, High current	–	10	–	mA	Output is 0.5 V to $V_{DDA}-0.5$ V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, Medium current	–	10	–		Output is 0.5 V to $V_{DDA}-0.5$ V
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, Low current	–	4	–		Output is 0.5 V to $V_{DDA}-0.5$ V
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, High current	–	1	–		
SID_DS_23	$I_{OU\_MED\_M2}$	Mode 2, Medium current	–	1	–		
SID_DS_24	$I_{OU\_LOW\_M2}$	Mode 2, Low current	–	0.5	–		

**Note**

6. Guaranteed by characterization.

**Table 10. Comparator DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID84	V <sub>OFFSET1</sub>	Input offset voltage, Factory trim	–	–	±10	mV	
SID85	V <sub>OFFSET2</sub>	Input offset voltage, Custom trim	–	–	±4		
SID86	V <sub>HYST</sub>	Hysteresis when enabled	–	10	35		
SID87	V <sub>ICM1</sub>	Input common mode voltage in normal mode	0	–	V <sub>DDD</sub> -0.1	V	Modes 1 and 2
SID247	V <sub>ICM2</sub>	Input common mode voltage in low power mode	0	–	V <sub>DDD</sub>		
SID247A	V <sub>ICM3</sub>	Input common mode voltage in ultra low power mode	0	–	V <sub>DDD</sub> -1.15		V <sub>DDD</sub> ≥ 2.2 V at –40 °C
SID88	C <sub>MRR</sub>	Common mode rejection ratio	50	–	–	dB	V <sub>DDD</sub> ≥ 2.7V
SID88A	C <sub>MRR</sub>	Common mode rejection ratio	42	–	–		V <sub>DDD</sub> ≤ 2.7V
SID89	I <sub>CMP1</sub>	Block current, normal mode	–	–	400	µA	
SID248	I <sub>CMP2</sub>	Block current, low power mode	–	–	100		
SID259	I <sub>CMP3</sub>	Block current in ultra low-power mode	–	–	6		V <sub>DDD</sub> ≥ 2.2 V at –40 °C
SID90	Z <sub>CMP</sub>	DC Input impedance of comparator	35	–	–	MΩ	

**Table 11. Comparator AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	µs	V <sub>DDD</sub> ≥ 2.2 V at –40 °C

**Table 12. Temperature Sensor Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID93	TSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

**Table 13. SAR Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
<b>SAR ADC DC Specifications</b>							
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes.
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.

**Table 13. SAR Specifications (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	
SID102	A_VIND	Input voltage range - differential[	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	TBD	V	
<b>SAR ADC AC Specifications</b>							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F <sub>IN</sub> = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A_samp/2	kHz	
SID111	A_INL	Integral non linearity. V <sub>DD</sub> = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	V <sub>REF</sub> = 1 to V <sub>DD</sub>
SID111A	A_INL	Integral non linearity. V <sub>DD</sub> = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	V <sub>REF</sub> = 1.71 to V <sub>DD</sub>
SID111B	A_INL	Integral non linearity. V <sub>DD</sub> = 1.71 to 5.5, 500 ksps	–1.5	–	1.7	LSB	V <sub>REF</sub> = 1 to V <sub>DD</sub>
SID112	A_DNL	Differential non linearity. V <sub>DD</sub> = 1.71 to 5.5, 1 Msps	–1	–	2.2	LSB	V <sub>REF</sub> = 1 to V <sub>DD</sub>
SID112A	A_DNL	Differential non linearity. V <sub>DD</sub> = 1.71 to 3.6, 1 Msps	–1	–	2	LSB	V <sub>REF</sub> = 1.71 to V <sub>DD</sub>
SID112B	A_DNL	Differential non linearity. V <sub>DD</sub> = 1.71 to 5.5, 500 ksps	–1	–	2.2	LSB	V <sub>REF</sub> = 1 to V <sub>DD</sub>
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F <sub>in</sub> = 10 kHz
SID261	FSARINTRE F	SAR operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution

CSD

**Table 14. CSD and IDAC Specifications**

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	$V_{DD} > 2\text{ V}$ (with ripple), $25^\circ\text{C}$ $T_A$ , Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	$V_{DD} > 1.75\text{V}$ (with ripple), $25^\circ\text{C}$ $T_A$ , Parasitic Capacitance ( $C_p$ ) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	μA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
SID.CSD#15	V <sub>REF</sub>	Voltage reference for CSD and Comparator	0.6	1.2	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	μA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	μA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	
SID310	IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA} > 2\text{ V}$ .
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5-nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34	–	41	μA	LSB = 300-nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1(7 bits) in high range	275	–	330	μA	LSB = 2.4-μA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75-nA typ.
SID314D	IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600-nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8-μA typ.
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5-nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	μA	LSB = 300-nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	μA	LSB = 2.4-μA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75-nA typ.
SID315D	IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600-nA typ.
SID315E	IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8-μA typ.
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	μA	LSB = 37.5-nA typ.



**Table 14. CSD and IDAC Specifications (continued)**

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	µA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

**Table 15. 10-bit CapSense ADC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus.
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	
SIDA98	A_GAINERR	Gain error	–	–	±2	%	In V <sub>REF</sub> (2.4 V) mode with V <sub>DDA</sub> bypass capacitance of 10 µF
SIDA99	A_OFFSET	Input offset voltage	–	–	3	mV	In V <sub>REF</sub> (2.4 V) mode with V <sub>DDA</sub> bypass capacitance of 10 µF
SIDA100	A_ISAR	Current consumption	–	–	0.25	mA	
SIDA101	A_VINS	Input voltage range - single ended	V <sub>SSA</sub>	–	V <sub>DDA</sub>	V	
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	
SIDA106	A_PSRR	Power supply rejection ratio	–	60	–	dB	In V <sub>REF</sub> (2.4 V) mode with V <sub>DDA</sub> bypass capacitance of 10 µF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = F <sub>clk</sub> /(2 <sup>N</sup> (N+2)). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = F <sub>clk</sub> /(2 <sup>N</sup> (N+2)). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.

**Table 15. 10-bit CapSense ADC Specifications (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V <sub>REF</sub> (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	V <sub>REF</sub> = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	–	–	1	LSB	

## Digital Peripherals

### Timer Counter Pulse-Width Modulator (TCPWM)

**Table 16. TCPWM Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	TCPWM <sub>FREQ</sub>	Operating frequency	–	–	F <sub>c</sub>	MHz	F <sub>c</sub> max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	TPWM <sub>ENEXT</sub>	Input trigger pulse width	2/F <sub>c</sub>	–	–	ns	For all trigger events <sup>[7]</sup>
SID.TCPWM.5	TPWM <sub>EXT</sub>	Output trigger pulse widths	2/F <sub>c</sub>	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC <sub>RES</sub>	Resolution of counter	1/F <sub>c</sub>	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM <sub>RES</sub>	PWM resolution	1/F <sub>c</sub>	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q <sub>RES</sub>	Quadrature inputs resolution	1/F <sub>c</sub>	–	–		Minimum pulse width between Quadrature phase inputs

<sup>2</sup>C

**Table 17. Fixed I<sup>2</sup>C DC Specifications<sup>[8]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I <sub>I2C1</sub>	Block current consumption at 100 kHz	–	–	50	μA	–
SID150	I <sub>I2C2</sub>	Block current consumption at 400 kHz	–	–	135		–
SID151	I <sub>I2C3</sub>	Block current consumption at 1 Mbps	–	–	310		–
SID152	I <sub>I2C4</sub>	I <sup>2</sup> C enabled in Deep Sleep mode	–	–	1.4		

**Table 18. Fixed I<sup>2</sup>C AC Specifications<sup>[8]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F <sub>I2C1</sub>	Bit rate	–	–	1	Msp/s	–

**Notes**

7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

**Note**

8. Guaranteed by characterization.