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PSoC® 4: PSoC 4100 Family Datasheet

Programmable System-on-Chip (PSoC®)

General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of mixed-signal programmable embedded system controllers with an ARM® Cortex™-M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC 4100 product family, based on this platform, is a combination of a microcontroller with digital programmable logic, high-performance analog-to-digital conversion, opamps with Comparator mode, and standard communication and timing peripherals. The PSoC 4100 products will be fully upward compatible with members of the PSoC 4 platform for new applications and design needs. The programmable analog and digital sub-systems allow flexibility and in-field tuning of the design.

Features

32-bit MCU Sub-system

- 24-MHz ARM Cortex-M0 CPU with single-cycle multiply
- Up to 32 kB of flash with Read Accelerator
- Up to 4 kB of SRAM

Programmable Analog

- Two opamps with reconfigurable high-drive external and high-bandwidth internal drive and Comparator modes and ADC input buffering capability
- 12-bit 806 ksps SAR ADC with differential and single-ended modes and Channel Sequencer with signal averaging
- Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
- Two low-power comparators that operate in Deep Sleep

Low Power 1.71-V to 5.5-V operation

- 20-nA Stop Mode with GPIO pin wakeup
- Hibernate and Deep Sleep modes allow wakeup-time versus power trade-offs

Capacitive Sensing

- Cypress CapSense Sigma-Delta (CSD) provides best-in-class SNR (>5:1) and water tolerance
- Cypress supplied software component makes capacitive sensing design easy
- Automatic hardware tuning (SmartSense™)

Segment LCD Drive

- LCD drive supported on all pins (common or segment)
- Operates in Deep Sleep mode with 4 bits per pin memory

Serial Communication

- Two independent run-time reconfigurable serial communication blocks (SCBs) with reconfigurable I^2C, SPI, or UART functionality

Timing and Pulse-Width Modulation

- Four 16-bit timer/counter pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals for motor drive and other high reliability digital logic applications

Up to 36 Programmable GPIOs

- Any GPIO pin can be CapSense, LCD, analog, or digital
- Drive modes, strengths, and slew rates are programmable

Five different packages

- 48-pin TQFP, 44-pin TQFP, 40-pin QFN, 35-ball WLCSP, and 28-pin SSOP package
- 35-ball WLCSP package is shipped with I^2C Bootloader in Flash

Extended Industrial Temperature Operation

- –40 °C to + 105 °C operation

PSoC Creator Design Environment

- Integrated Development Environment provides schematic design entry and build (with analog and digital automatic routing)
- Applications Programming Interface (API Component) for all fixed-function and programmable peripherals

Industry Standard Tool Compatibility

- After schematic entry, development can be done with ARM-based industry-standard development tools

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
  - AN90071: CY8CMBRxxx CapSense Design Guide
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

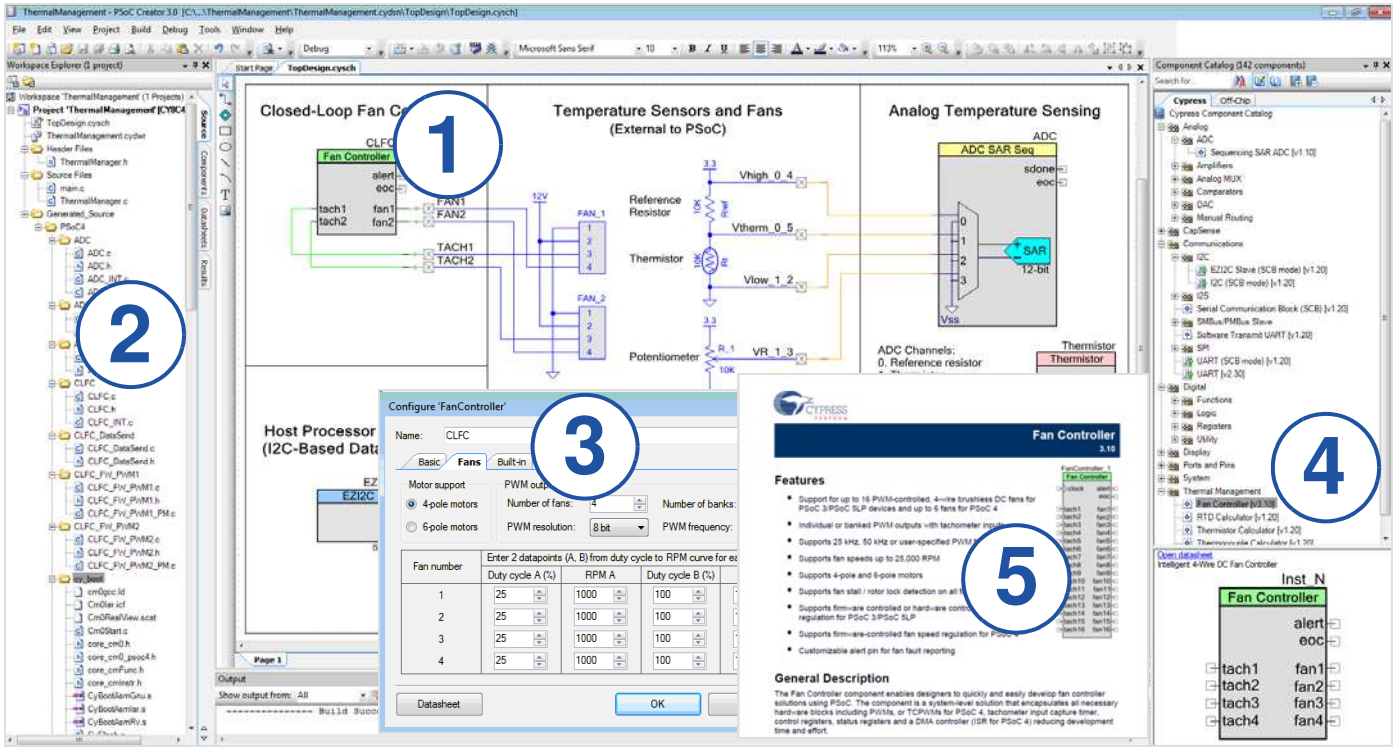
The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

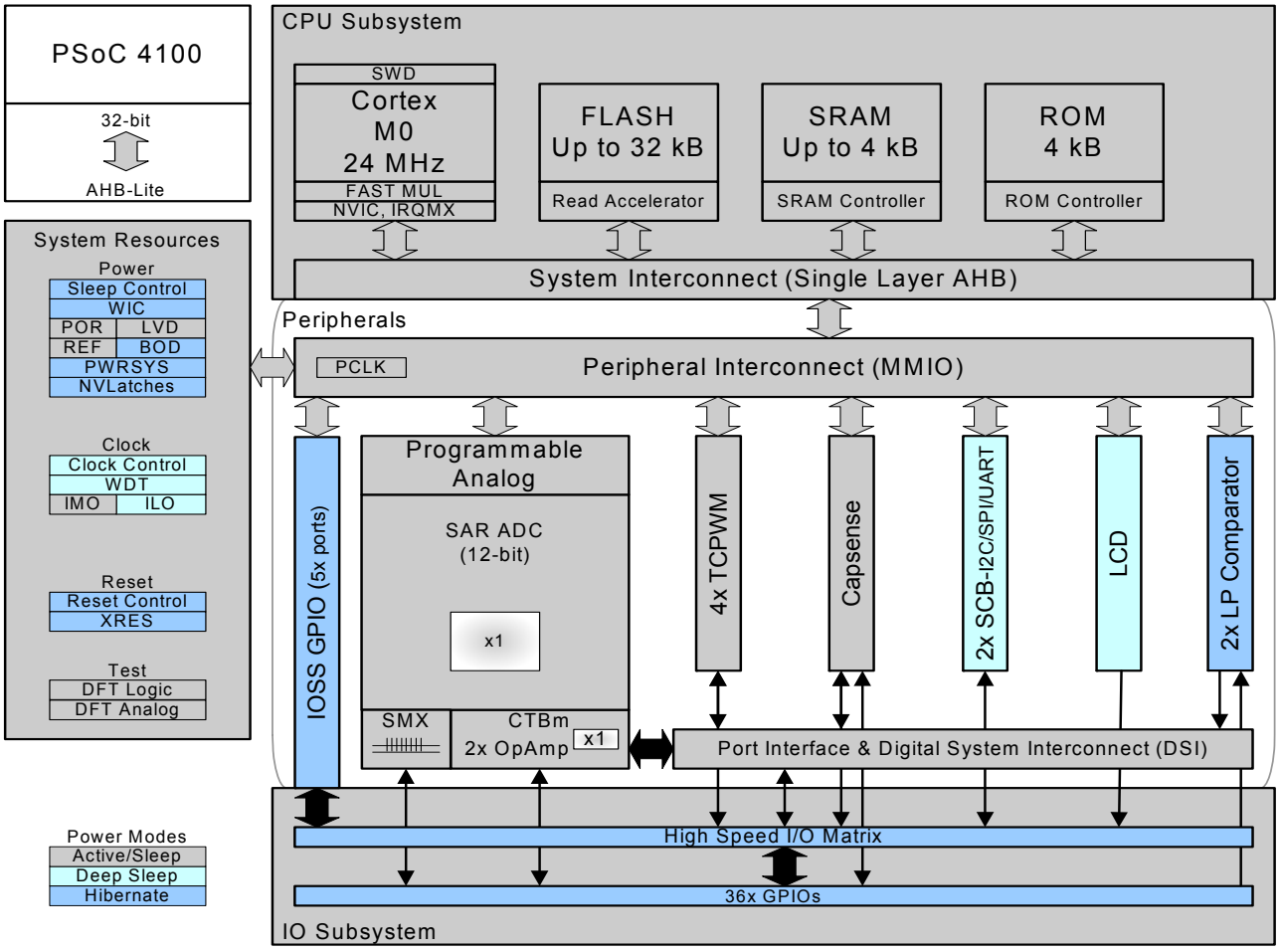
1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



Contents

Figure 2. Block Diagram



The PSoC 4100 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for the PSoC 4100 devices. The SWD interface is fully compatible with industry standard third party tools. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 4100 family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4100 with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4100 allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in PSoC 4100 is part of the 32-bit MCU subsystem, which is optimized for low power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from Deep Sleep mode allowing power to be switched off to the main processor when the chip is in Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt input (NMI), which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG; the debug configuration used for PSoC 4100 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

PSoC 4100 has a flash module with a flash accelerator tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 0 wait-state (WS) access time at 24 MHz. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4200 Flash supports the following flash protection modes at the memory subsystem level:

- **Open: No Protection.** Factory default mode in which the product is shipped.
- **Protected: User may change from Open to Protected.** This mode disables Debug interface accesses. The mode can be set back to Open but only after completely erasing the Flash.
- **Kill: User may change from Open to Kill.** This mode disables all Debug accesses. The part cannot be erased externally, thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrecvocable mode.

In addition, row-level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

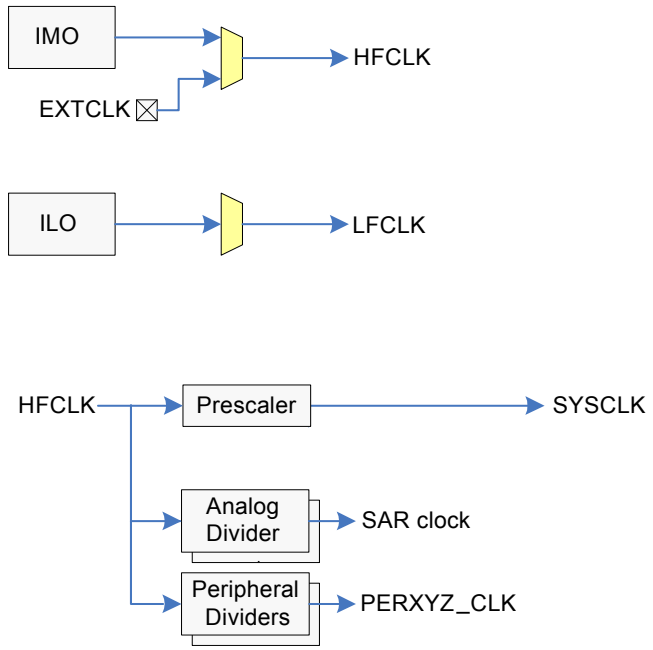
The power system is described in detail in the section Power on page 15. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4100 operates with a single external supply over the range of 1.71 V to 5.5 V and has five different power modes, transitions between which are managed by the power system. PSoC 4100 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4100 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4100 consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO) and provision for an external clock.

Figure 3. PSoC 4100 MCU Clocking Architecture



The HFCLK signal can be divided down (see PSoC 4100 MCU Clocking Architecture) to generate synchronous clocks for the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4100, each with 16-bit divide capability. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 MHz to 24 MHz in steps of 1 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low power oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Reset

PSoC 4100 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4100 reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal to noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the SAR.

Analog Blocks

12-bit SAR ADC

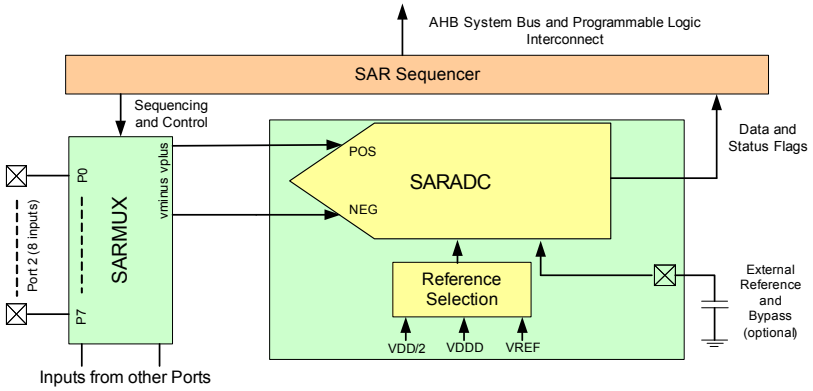
The 12-bit 806 ksps SAR ADC can operate at a maximum clock rate of 14.5 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice (for the PSoC 4100 case) of three internal voltage references: V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The sample-and-hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision providing appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, aggregate sampling bandwidth is equal to 806 ksps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 4. SAR ADC System Diagram



Two Opamps (CTBm Block)

PSoC 4100 has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the S/H circuit of the ADC without requiring external buffering.

Temperature Sensor

PSoC 4100 has one on-chip temperature sensor This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress supplied software that includes calibration and linearization.

Low-power Comparators

PSoC 4100 has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

Fixed Function Digital

Timer/Counter/PWM Block (TCPWM)

The TCPWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

Serial Communication Blocks (SCB)

The PSoC 4100 has two SCBs, which can each implement an I^2C, UART, or SPI interface.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes. The I^2C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. The required Rise and Fall times for different I^2C speeds are guaranteed by using appropriate pull-up resistor values depending on VDD, Bus Capacitance, and resistor tolerance. For detailed information on how to calculate the optimum pull-up resistor value for your design, refer to the UM10204 I2C bus specification and user manual (the latest revision is available at www.nxp.com).

PSoC 4100 is not completely compliant with the I^2C spec in the following respects:

- GPIO cells are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I^2C master, it interposes an IDLE state between NACK and Repeated Start; the I^2C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in I^2C slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its I^2C address must be even.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

GPIO

PSoC 4100 has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100 since it has 4.5 ports).

Special Function Peripherals

LCD Segment Drive

PSoC 4100 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

CapSense

CapSense is supported on all pins in the PSoC 4100 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

WLCSP Package Bootloader

The WLCSP package is supplied with an I^2C Bootloader installed in flash. The bootloader is compatible with PSoC Creator bootloadable project files and has the following default settings:

- I^2C SCL and SDA connected to port pins P4.0 and P4.1 respectively (external pull-up resistors required)
- I^2C Slave mode, address 8, data rate = 100 kbps
- Single application
- Wait two seconds for bootload command
- Other bootloader options are as set by the PSoC Creator Bootloader Component default
- Occupies the bottom 4.5 K of flash

For more information on this bootloader, see the following Cypress application notes:

AN73854 - Introduction to Bootloaders

Note that a PSoC Creator bootloadable project must be associated with *.hex* and *.elf* files for a bootloader project that is configured for the target device. Bootloader *.hex* and *.elf* files can be found at http://www.cypress.com/?rID=78805. The factory-installed bootloader can be overwritten using JTAG or SWD programming.

Pinouts

The following is the pin-list for PSoC 4100 (44-TQFP, 40-QFN, 28-SSOP, and 48-TQFP). Port 2 comprises of the high-speed Analog inputs for the SAR Mux. P1.7 is the optional external input and bypass for the SAR reference. Ports 3 and 4 contain the Digital Communication channels. All pins support CSD CapSense and analog mux bus connections.

44-TQFP		40-QFN		28-SSOP		48-TQFP		Alternate Functions for Pins					Pin Description
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
1	VSS	–	–	–	–	–	–	–	–	–	–	–	Ground
2	P2.0	1	P2.0	–	–	2	P2.0	sarmux.0	–	–	–	–	Port 2 Pin 0: gpio, lcd, csd, sarmux
3	P2.1	2	P2.1	–	–	3	P2.1	sarmux.1	–	–	–	–	Port 2 Pin 1: gpio, lcd, csd, sarmux
4	P2.2	3	P2.2	5	P2.2	4	P2.2	sarmux.2	–	–	–	–	Port 2 Pin 2: gpio, lcd, csd, sarmux
5	P2.3	4	P2.3	6	P2.3	5	P2.3	sarmux.3	–	–	–	–	Port 2 Pin 3: gpio, lcd, csd, sarmux
6	P2.4	5	P2.4	7	P2.4	6	P2.4	sarmux.4	tcpwm0_p[1]	–	–	–	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
7	P2.5	6	P2.5	8	P2.5	7	P2.5	sarmux.5	tcpwm0_n[1]	–	–	–	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
8	P2.6	7	P2.6	9	P2.6	8	P2.6	sarmux.6	tcpwm1_p[1]	–	–	–	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
9	P2.7	8	P2.7	10	P2.7	9	P2.7	sarmux.7	tcpwm1_n[1]	–	–	–	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
10	VSS	9	VSS	–	–	–	–	–	–	–	–	–	Ground
–	–	–	–	–	–	10	NC	–	–	–	–	–	No Connect
–	–	–	–	–	–	11	NC	–	–	–	–	–	No Connect
11	P3.0	10	P3.0	11	P3.0	12	P3.0	–	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
12	P3.1	11	P3.1	12	P3.1	13	P3.1	–	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
13	P3.2	12	P3.2	13	P3.2	14	P3.2	–	tcpwm1_p[0]	–	swd_io[0]	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
–	–	–	–	–	–	15	VSSD	–	–	–	–	–	Ground
14	P3.3	13	P3.3	14	P3.3	16	P3.3	–	tcpwm1_n[0]	–	swd_clk[0]	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
15	P3.4	14	P3.4	–	–	17	P3.4	–	tcpwm2_p[0]	–	–	scb1_spi_ssel_1	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1
16	P3.5	15	P3.5	–	–	18	P3.5	–	tcpwm2_n[0]	–	–	scb1_spi_ssel_2	Port 3 Pin 5: gpio, lcd, csd, pwm, scb1
17	P3.6	16	P3.6	–	–	19	P3.6	–	tcpwm3_p[0]	–	swd_io[1]	scb1_spi_ssel_3	Port 3 Pin 6: gpio, lcd, csd, pwm, scb1, swd
18	P3.7	17	P3.7	–	–	20	P3.7	–	tcpwm3_n[0]	–	swd_clk[1]	–	Port 3 Pin 7: gpio, lcd, csd, pwm, swd
19	VDDD	–	–	–	–	21	VDDD	–	–	–	–	–	Digital Supply, 1.8 - 5.5V
20	P4.0	18	P4.0	15	P4.0	22	P4.0	–	–	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
21	P4.1	19	P4.1	16	P4.1	23	P4.1	–	–	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
22	P4.2	20	P4.2	17	P4.2	24	P4.2	csd_c_mod	–	–	–	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
23	P4.3	21	P4.3	18	P4.3	25	P4.3	csd_c_sh_tank	–	–	–	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
–	–	–	–	–	–	26	NC	–	–	–	–	–	No Connect
–	–	–	–	–	–	27	NC	–	–	–	–	–	No Connect

44-TQFP		40-QFN		28-SSOP		48-TQFP		Alternate Functions for Pins					Pin Description
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
24	P0.0	22	P0.0	19	P0.0	28	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
25	P0.1	23	P0.1	20	P0.1	29	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
26	P0.2	24	P0.2	21	P0.2	30	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
27	P0.3	25	P0.3	22	P0.3	31	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
28	P0.4	26	P0.4	–	–	32	P0.4	–	–	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
29	P0.5	27	P0.5	–	–	33	P0.5	–	–	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
30	P0.6	28	P0.6	23	P0.6	34	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
31	P0.7	29	P0.7	24	P0.7	35	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
32	XRES	30	XRES	25	XRES	36	XRES	–	–	–	–	–	Chip reset, active low
33	VCCD	31	VCCD	26	VCCD	37	VCCD	–	–	–	–	–	Regulated supply, connect to 1µF cap or 1.8V
–	–	–	–	–	–	38	VSSD	–	–	–	–	–	Digital Ground
34	VDDD	32	VDDD	27	VDD	39	VDDD	–	–	–	–	–	Digital Supply, 1.8 - 5.5V
35	VDDA	33	VDDA	27	VDD	40	VDDA	–	–	–	–	–	Analog Supply, 1.8 - 5.5V, equal to VDDD
36	VSSA	34	VSSA	28	VSS	41	VSSA	–	–	–	–	–	Analog Ground
37	P1.0	35	P1.0	1	P1.0	42	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
38	P1.1	36	P1.1	2	P1.1	43	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
39	P1.2	37	P1.2	3	P1.2	44	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
40	P1.3	38	P1.3	–	–	45	P1.3	ctb.oa1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
41	P1.4	39	P1.4	–	–	46	P1.4	ctb.oa1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
42	P1.5	–	–	–	–	47	P1.5	ctb.oa1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
43	P1.6	–	–	–	–	48	P1.6	ctb.oa0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
44	P1.7/VREF	40	P1.7/VREF	4	P1.7/VREF	1	P1.7/VREF	ctb.oa1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Notes:

1. tcpwm_p and tcpwm_n refer to tcpwm non-inverted and inverted outputs respectively.
2. P3.2 and P3.3 are SWD pins after boot (reset).

The following is the pin-list for the PSoC 4100 (35-WLCSP).

35-Ball CSP		Alternate Functions for Pins					Pin Description
Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
D3	P2.2	sarmux.2	–	–	–	–	Port 2 Pin 2: gpio, lcd, csd, sarmux
E4	P2.3	sarmux.3	–	–	–	–	Port 2 Pin 3: gpio, lcd, csd, sarmux
E5	P2.4	sarmux.4	tcpwm0_p[1]	–	–	–	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
E6	P2.5	sarmux.5	tcpwm0_n[1]	–	–	–	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
E3	P2.6	sarmux.6	tcpwm1_p[1]	–	–	–	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
E2	P2.7	sarmux.7	tcpwm1_n[1]	–	–	–	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
E1	P3.0	–	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
D2	P3.1	–	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
D1	P3.2	–	tcpwm1_p[0]	–	swd_io[0]	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
B7	VSS	–	–	–	–	–	Ground
C1	P3.3	–	tcpwm1_n[0]	–	swd_clk[0]	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
C2	P3.4	–	tcpwm2_p[0]	-	–	scb1_spi_ssel_1	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1
B1	P4.0	–	–	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
B2	P4.1	–	–	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
A2	P4.2	csd_c_mod	–	–	–	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
A1	P4.3	csd_c_sh_tank	–	–	–	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
C3	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
A5	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
A4	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
A3	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
B3	P0.4	–	–	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
A6	P0.5	–	–	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
B4	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
B5	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
B6	XRES	–	–	–	–	–	Chip reset, active low
A7	VCCD	–	–	–	–	–	Regulated supply, connect to 1µF cap or 1.8V
C7	VDD	–	–	–	–	–	Supply, 1.8 - 5.5V
C4	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
C5	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm

35-Ball CSP		Alternate Functions for Pins					Pin Description
Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
C6	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
D7	P1.3	ctb.oa1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
D4	P1.4	ctb.oa1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
D5	P1.5	ctb.oa1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
D6	P1.6	ctb.oa0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
E7	P1.7/VREF	ctb.oa1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Descriptions of the Pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin).

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

VCCD: Regulated Digital supply (1.8 V ±5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following packages are supported: 48-pin TQFP, 44-pin TQFP, 40-pin QFN, and 28-pin SSOP.

Figure 5. 48-Pin TQFP Pinout

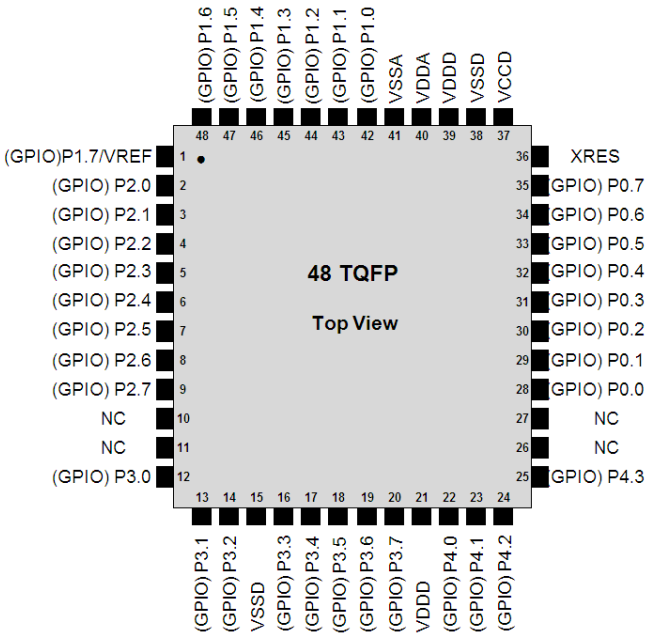


Figure 6. 44-pin TQFP Part Pinout

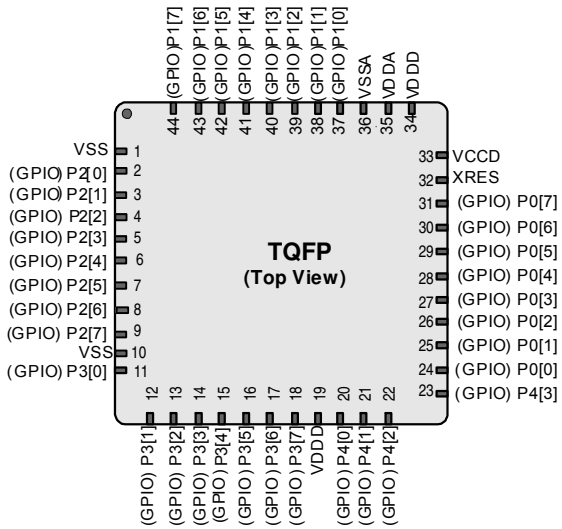


Figure 7. 40-Pin QFN Pinout

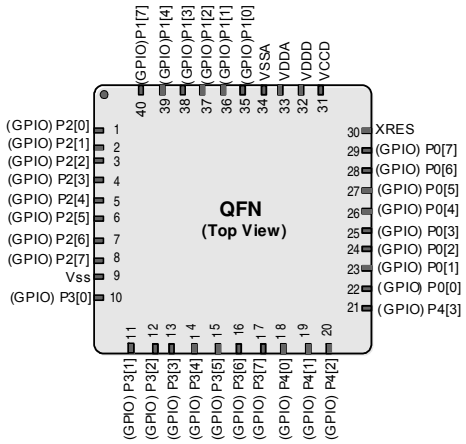
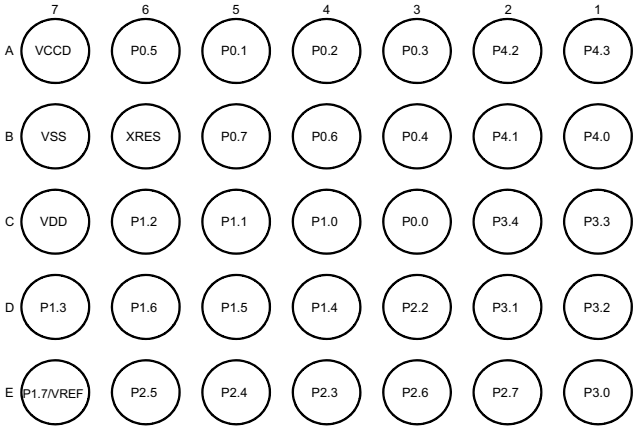
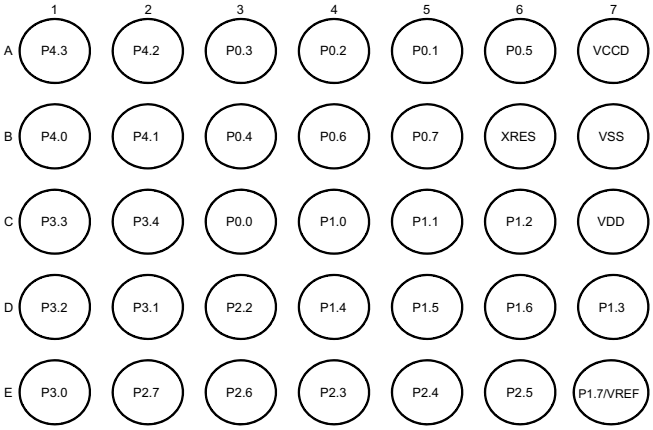


Figure 8. 35-Ball WLCSP

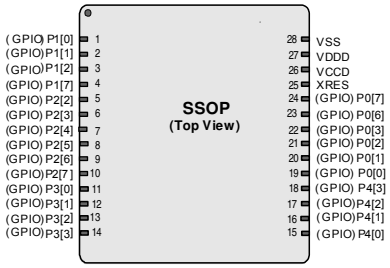


Balls Up View



Top View

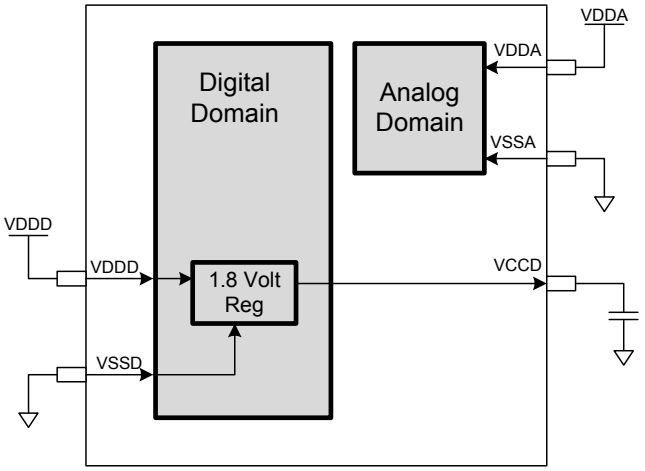
Figure 9. 28-Pin SSOP Pinout



Power

The following power system diagrams show the minimum set of power supply pins as implemented for PSoC 4100. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DDA} input. There are separate regulators for the Deep Sleep and Hibernate (lowered power supply and retention) modes. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.71 V to 5.5 V with all functions and circuits operating over that range.

Figure 10. PSoC 4 Power Supply



The PSoC 4100 family allows two distinct modes of power supply operation: Unregulated External Supply, and Regulated External Supply modes.

Unregulated External Supply

In this mode, PSoC 4100 is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC 4100 supplies the internal logic and the V_{CCD} output of the PSoC 4100 must be bypassed to ground via an external Capacitor (in the range of 1 µF to 1.6 µF; X5R ceramic or better).

V_{DDA} and V_{DDD} must be shorted together; the grounds, VSSA and V_{SS} must also be shorted together. Bypass capacitors must be used from V_{DDD} to ground, typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (0.1 µF for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 11. 48-TQFP Package Example

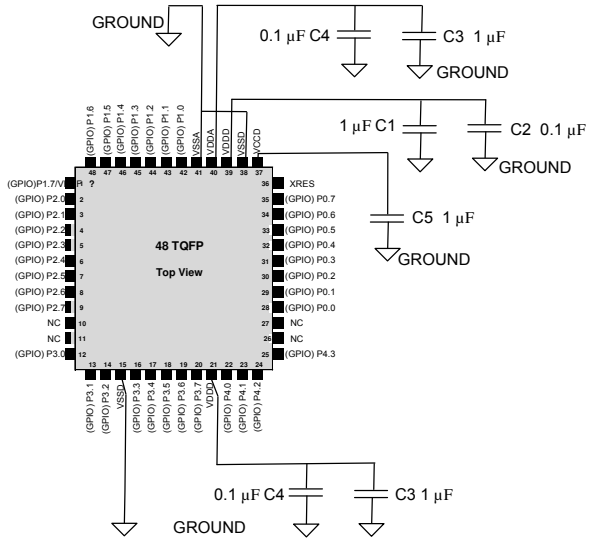
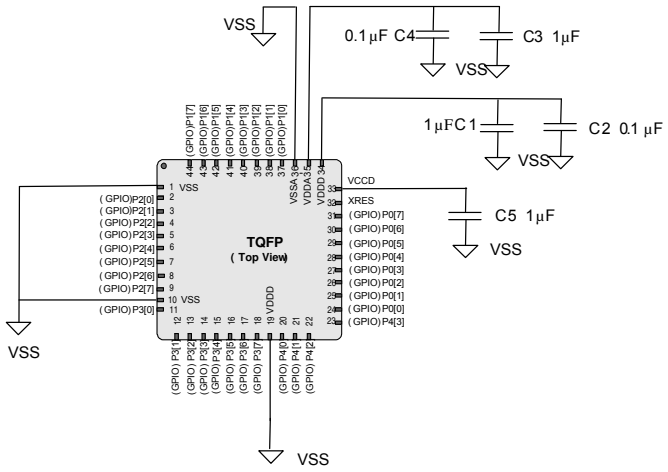


Figure 12. 44-TQFP Package Example



Power Supply	Bypass Capacitors
VDDD–VSS	0.1 µF ceramic at each pin (C2, C6) plus bulk capacitor 1 to 10 µF (C1). Total capacitance may be greater than 10 µF.
VDDA–VSSA	0.1 µF ceramic at pin (C4). Additional 1 µF to 10 µF (C3) bulk capacitor. Total capacitance may be greater than 10 µF.
VCCD–VSS	1 µF ceramic capacitor at the VCCD pin (C5)
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 µF to 10 µF capacitor. Total capacitance may be greater than 10 µF.

Note It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (V_{DDA}, V_{DDD}, or V_{CCD}) is a significant percentage of the rated working voltage. V_{DDA} must be equal to or higher than the V_{DDD} supply when powering up.

Figure 13. 40-pin QFN Example

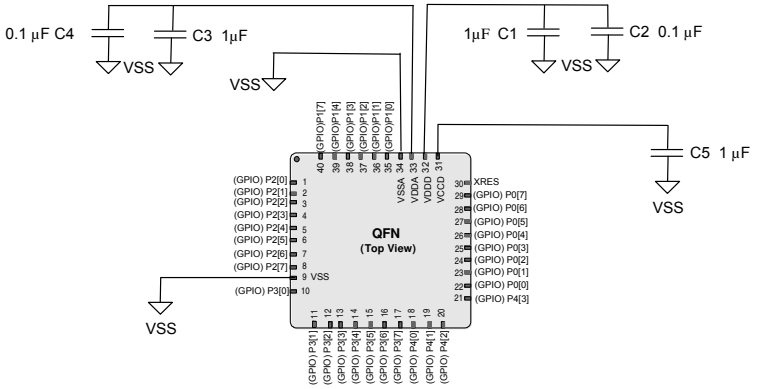
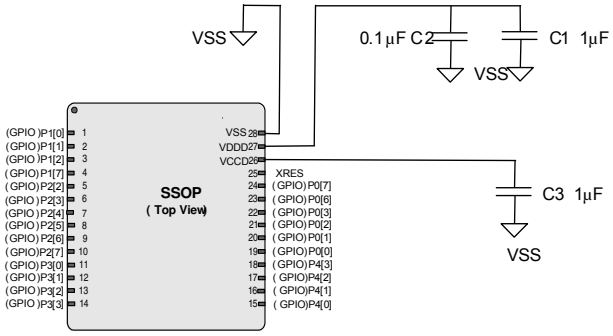


Figure 14. 28-SSOP Example



Regulated External Supply

In this mode, the PSoC 4100 is powered by an external power supply that must be within the range of 1.71 V to 1.89 V (1.8 ±5%); note that this range needs to include power supply ripple too. In this mode, VCCD, VDDA, and VDDD pins are all shorted together and bypassed. The internal regulator is disabled in firmware.

Development Support

The PSoC 4100 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4100 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SSD}	–0.5	–	6	V	Absolute max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to Vssd	–0.5	–	1.95	V	Absolute max
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5	V	Absolute max
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–200	–	200	mA	

Device-Level Specifications

All specifications are valid for -40 °C ≤ TA ≤ 105 °C and TJ ≤ 125 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DD}	Power Supply Input Voltage (V_{DDA} = V_{DDD} = V_{DD})	1.8	–	5.5	V	With regulator enabled
SID255	V_{DDD}	Power Supply Input Voltage unregulated	1.71	1.8	1.89	V	Internally unregulated Supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	
SID55	CEFC	External Regulator voltage bypass	1	1.3	1.6	µF	X5R ceramic or better
SID56	CEXC	Power supply decoupling capacitor	–	1	–	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V. Typical Values measured at V_{DD} = 3.3 V							
SID9	IDD4	Execute from Flash; CPU at 6 MHz	–	–	2.8	mA	
SID10	IDD5	Execute from Flash; CPU at 6 MHz	–	2.2	–	mA	T = 25 °C
SID12	IDD7	Execute from Flash; CPU at 12 MHz,	–	–	4.2	mA	
SID13	IDD8	Execute from Flash; CPU at 12 MHz	–	3.7	–	mA	T = 25 °C
SID16	IDD11	Execute from Flash; CPU at 24 MHz	–	6.7	–	mA	T = 25 °C
SID17	IDD12	Execute from Flash; CPU at 24 MHz	–	–	7.2	mA	
Sleep Mode, V_{DD} = 1.7 V to 5.5 V							
SID25	IDD20	I^2C wakeup, WDT, and Comparators on. 6 MHz.	–	1.3	1.8	mA	V_{DD} = 1.71 to 5.5 V
SID25A	IDD20A	I^2C wakeup, WDT, and Comparators on. 12 MHz.	–	1.7	2.2	mA	V_{DD} = 1.71 to 5.5 V
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID31	IDD26	I^2C wakeup and WDT on.	–	1.3	–	µA	T = 25 °C
SID32	IDD27	I^2C wakeup and WDT on.	–	–	45	µA	T = 85 °C

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 2. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V							
SID34	IDD29	I^2C wakeup and WDT on	–	1.5	15	µA	Typ at 25 °C Max at 85 °C
Deep Sleep Mode, V_{DD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	IDD32	I^2C wakeup and WDT on.	–	1.7	–	µA	T = 25 °C
SID38	IDD33	I^2C wakeup and WDT on	–	–	60	µA	T = 85 °C
Deep Sleep Mode, +105 °C							
SID33Q	IDD28Q	I^2C wakeup and WDT on. Regulator Off.	–	–	135	µA	V_{DD} = 1.71 to 1.89
SID34Q	IDD29Q	I^2C wakeup and WDT on.	–	–	180	µA	V_{DD} = 1.8 to 3.6
SID35Q	IDD30Q	I^2C wakeup and WDT on.	–	–	140	µA	V_{DD} = 3.6 to 5.5
Hibernate Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID40	IDD35	GPIO and Reset active	–	150	–	nA	T = 25 °C
SID41	IDD36	GPIO and Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, V_{DD} = 3.6 V to 5.5 V							
SID43	IDD38	GPIO and Reset active	–	150	–	nA	T = 25 °C
Hibernate Mode, V_{DD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID46	IDD41	GPIO and Reset active	–	150	–	nA	T = 25 °C
SID47	IDD42	GPIO and Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, +105 °C							
SID42Q	IDD37Q	Regulator Off	–	–	19.4	µA	V_{DD} = 1.71 to 1.89
SID43Q	IDD38Q		–	–	17	µA	V_{DD} = 1.8 to 3.6
SID44Q	IDD39Q		–	–	16	µA	V_{DD} = 3.6 to 5.5
Stop Mode							
SID304	IDD43A	Stop Mode current; V_{DD} = 3.3 V	–	20	80	nA	Typ at 25 °C Max at 85 °C
Stop Mode, +105 °C							
SID304Q	IDD43AQ	Stop Mode current; V_{DD} = 3.6 V	–	–	5645	nA	
XRES current							
SID307	IDD_XR	Supply current while XRES asserted	–	2	5	mA	

Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	24	MHz	$1.71 \le V_{DD} \le 5.5$
SID49	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	Guaranteed by characterization
SID50	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization
SID51	$T_{HIBERNATE}$	Wakeup from Hibernate and Stop modes	–	–	2	ms	Guaranteed by characterization
SID52	$T_{RESETWIDTH}$	External reset pulse width	1	–	–	µs	Guaranteed by characterization

GPIO

Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[2]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID241	V_{IH}[2]	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	
SID243	V_{IH}[2]	LVTTL input, $V_{DDD} \geq 2.7$ V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq 2.7$ V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 8 mA at 3-V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3-V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0-V
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	
SID66	C_{IN}	Input capacitance	–	–	7	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7$ V. Guaranteed by characterization
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DD}/Vss	–	–	100	µA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 5. GPIO AC Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	24	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout;1.7 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout;1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	24	MHz	90/10% V_{IO}

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Analog Peripherals

Opamp

Table 8. Opamp Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I_{DD_HI}	Power = high	–	1100	1850	µA	
SID270	I_{DD_MED}	Power = medium	–	550	950	µA	
SID271	I_{DD_LOW}	Power = low	–	150	350	µA	
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	V_{DDA} – 0.2	V	
SID282	V_{CM}	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	V_{DDA} – 0.2	V	
	V_{OUT}	$V_{DDA} \geq 2.7$ V	–	–	–		
SID283	V_{OUT_1}	Power = high, Iload=10 mA	0.5	–	V_{DDA} – 0.5	V	
SID284	V_{OUT_2}	Power = high, Iload=1 mA	0.2	–	V_{DDA} – 0.2	V	
SID285	V_{OUT_3}	Power = medium, Iload=1 mA	0.2	–	V_{DDA} – 0.2	V	
SID286	V_{OUT_4}	Power = low, Iload=0.1 mA	0.2	–	V_{DDA} – 0.2	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode. $T_A \leq 85$ °C
SID290Q	VOS_DR_TR	Offset voltage drift, trimmed	15	±3	15	µV/°C	High mode. $T_A \leq 105$ °C
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC	70	80	–	dB	V_{DDD} = 3.6 V
SID292	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V_{DDD} = 3.6 V
	Noise		–	–	–	–	
SID293	V_{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	µVrms	
SID294	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID295	V_{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	
SID296	V_{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	

Table 8. Opamp Specifications (Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V	6	–	–	V/µs	
SID299	T_op_wake	From disable to enable, no external RC dominating	–	300	–	µs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	Guaranteed by design
	Comp_mode	Comparator mode; 50-mV drive, Trise = Tfall (approx)	–	–	–		
SID300	T_{PD1}	Response time; power = high	–	150	–	ns	
SID301	T_{PD2}	Response time; power = medium	–	400	–	ns	
SID302	T_{PD3}	Response time; power = low	–	2000	–	ns	
SID303	Vhyst_op	Hysteresis	–	10	–	mV	

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	$V_{OFFSET2}$	Input offset voltage, Common Mode voltage range from 0 to V_{DD}-1	–	–	±4	mV	
SID85A	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode ($V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C)	–	±12	–	mV	
SID86	V_{HYST}	Hysteresis when enabled, Common Mode voltage range from 0 to V_{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} – 0.1	V	Modes 1 and 2.
SID247	V_{ICM2}	Input common mode voltage in low power mode ($V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C)	0	–	V_{DDD}	V	
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} – 1.15	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq 2.7$ V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	$V_{DDD} < 2.7$ V. Guaranteed by characterization
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	Guaranteed by characterization
SID248	I_{CMP2}	Block current, low power mode	–	–	100	µA	Guaranteed by characterization
SID259	I_{CMP3}	Block current, ultra low power mode ($V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C)	–	6	28	µA	Guaranteed by characterization
SID90	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	Guaranteed by characterization

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T_{RESP1}	Response time, normal mode	–	–	110	ns	50-mV overdrive
SID258	T_{RESP2}	Response time, low power mode	–	–	200	ns	50-mV overdrive
SID92	T_{RESP3}	Response time, ultra low power mode (V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C)	–	–	15	µs	200-mV overdrive

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	8		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference. Guaranteed by characterization
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V $V_{REF.}$ Guaranteed by characterization
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID111	A_INL	Integral non linearity	–1.7	–	+2	LSB	V_{DD} = 1.71 to 5.5, 806 ksps, V_{REF} = 1 to 5.5.
SID111A	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	V_{DDD} = 1.71 to 3.6, 806 ksps, V_{REF} = 1.71 to V_{DDD}.

Table 12. SAR ADC DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID111B	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	V_{DDD} = 1.71 to 5.5, 500 ksps, V_{REF} = 1 to 5.5.
SID112	A_DNL	Differential non linearity	–1	–	+2.2	LSB	V_{DDD} = 1.71 to 5.5, 806 ksps, V_{REF} = 1 to 5.5.
SID112A	A_DNL	Differential non linearity	–1	–	+2	LSB	V_{DDD} = 1.71 to 3.6, 806 ksps, V_{REF} = 1.71 to V_{DDD}.
SID112B	A_DNL	Differential non linearity	–1	–	+2.2	LSB	V_{DDD} = 1.71 to 5.5, 500 ksps, V_{REF} = 1 to 5.5.

Table 13. SAR ADC AC Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	806	ksps	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	ksps	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	ksps	
SID109	A_SNDR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz.