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# CY8CKIT-030 PSoC<sup>®</sup> 3 Development Kit Guide

Doc. # 001-61038 Rev. \*\*

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# Contents



<b>1. Introduction</b>	<b>5</b>
1.1 Kit Contents .....	5
1.2 PSoC Creator .....	5
1.3 Additional Learning Resources .....	6
1.4 Document History .....	6
1.5 Documentation Conventions .....	6
<b>2. Getting Started</b>	<b>7</b>
2.1 Introduction .....	7
2.2 CD Installation .....	7
2.3 Install Hardware .....	8
2.4 Install Software .....	8
2.5 Uninstall Software .....	8
<b>3. Kit Operation</b>	<b>9</b>
3.1 Introduction .....	9
3.2 Programming PSoC 3 Device .....	9
<b>4. Hardware</b>	<b>11</b>
4.1 System Block Diagram .....	11
4.2 Functional Description .....	12
4.2.1 Power Supply .....	12
4.2.1.1 Power Supply Jumper Settings .....	14
4.2.1.2 Grounding Scheme .....	14
4.2.1.3 Low Power Functionality .....	15
4.2.2 Programming Interface .....	15
4.2.2.1 On-board Programming Interface .....	15
4.2.2.2 JTAG/SWD Programming .....	16
4.2.3 USB Communication .....	17
4.2.4 Boost Converter .....	18
4.2.5 32-kHz and 24-MHz Crystal .....	19
4.2.6 PSoC 3 Development Kit Expansion Ports .....	19
4.2.6.1 Port D .....	19
4.2.6.2 Port E .....	21
4.2.7 RS-232 Interface .....	22
4.2.8 Prototyping Area .....	22
4.2.9 Character LCD .....	23
4.2.10 CapSense Sensors .....	24
<b>5. Example Projects</b>	<b>27</b>
5.1 Voltage Display .....	28
5.1.1 Project Description .....	28

5.1.2	Hardware Connections .....	28
5.1.3	Del-Sig ADC Configuration .....	28
5.1.4	Verify Output .....	29
5.2	Intensity LED .....	29
5.2.1	Project Description.....	29
5.2.2	Hardware Connections .....	29
5.2.3	Verify Output .....	30
5.3	Low Power Demonstration .....	30
5.3.1	Project Description.....	30
5.3.2	Hardware Connections .....	30
5.3.3	Verify Output .....	30
5.4	CapSense Example.....	31
5.4.1	Project Description.....	31
5.4.2	Hardware Connections .....	31
5.4.3	Verify Output .....	32
5.5	ADC and DMA-DAC Example .....	33
5.5.1	Project Description.....	33
5.5.2	Hardware Connections .....	33
5.5.3	Verify Output .....	33
<b>A. Appendix</b>		<b>35</b>
A.1	Schematic.....	35
A.2	Board Layout .....	40
A.2.1	PDC-09589 Top.....	40
A.2.2	PDC-09589 Power .....	41
A.2.3	PDC-09589 Ground .....	42
A.2.4	PDC-09589 Bottom.....	43
A.3	BOM .....	44

# 1. Introduction



Thank you for your interest in the CY8CKIT-030 PSoC<sup>®</sup> 3 Development Kit. This kit allows you to develop precision analog and low power designs using PSoC 3. You can design your own projects with PSoC Creator<sup>™</sup> or by altering sample projects provided with this kit.

The CY8CKIT-030 PSoC 3 Development Kit is based on the PSoC 3 family of devices. PSoC 3 is a Programmable System-on-Chip<sup>™</sup> platform for 8- and 16-bit applications. It combines precision analog and digital logic with a high-performance CPU. With PSoC, you can create the exact combination of peripherals and integrated proprietary IP to meet your application requirements.

## 1.1 Kit Contents

The PSoC 3 Development Kit contains:

- Development board
- Kit CD
- Quick Start Guide
- USB A to Mini B cable
- 3.3 V LCD module

Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help.

## 1.2 PSoC Creator

Cypress's PSoC Creator software is a state-of-the-art, easy-to-use integrated development environment (IDE) that introduces a game-changing, hardware and software design environment based on classic schematic entry and revolutionary embedded design methodology.

With PSoC Creator, you can:

- Create and share user-defined, custom peripherals using hierarchical schematic design.
- Automatically place and route select components and integrate simple glue logic, normally located in discrete muxes.
- Trade-off hardware and software design considerations allowing you to focus on what matters and getting to market faster.

PSoC Creator also enables you to tap into an entire tools ecosystem with integrated compiler tool chains, RTOS solutions, and production programmers to support both PSoC 3 and PSoC 5.

## 1.3 Additional Learning Resources

Visit [www.cypress.com](http://www.cypress.com) for additional learning resources in the form of data sheets, technical reference manual, and application notes.

## 1.4 Document History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	01/06/11	QVS	Initial version of kit guide

## 1.5 Documentation Conventions

Table 1-1. Document Conventions for Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\ . . .cd\icc\
<i>Italics</i>	Displays file names and reference documentation: Read about the <i>sourcefile.hex</i> file in the <i>PSoC Designer User Guide</i> .
[Bracketed, Bold]	Displays keyboard commands in procedures: [Enter] or [Ctrl] [C]
File > Open	Represents menu paths: File > Open > New Project
<b>Bold</b>	Displays commands, menu paths, and icon names in procedures: Click the <b>File</b> icon and then click <b>Open</b> .
Times New Roman	Displays an equation: $2 + 2 = 4$
Text in gray boxes	Describes cautions or unique functionality of the product.

## 2. Getting Started



### 2.1 Introduction

This chapter describes how to install and configure the PSoC 3 Development Kit. Chapter 3 describes the kit operation. It explains how to program a PSoC 3 device with PSoC Programmer and use the kit with the help of an example project. To reprogram the PSoC device with PSoC Creator, refer to the CD installation instructions for PSoC Creator. Chapter 4 details the hardware operation. Chapter 5 provides instructions to create a simple example project. The Appendix section provides the schematics and BOM associated with the PSoC 3 Development Kit.

### 2.2 CD Installation

Follow these steps to install the PSoC 3 Development Kit software:

1. Insert the kit CD into the CD drive of your PC. The CD is designed to auto-run and the kit menu appears.

Figure 2-1. Kit Menu



**Note** If auto-run does not execute, double-click **AutoRun** on the root directory of the CD.





After the installation is complete, the kit contents are available at the following location:

C:\Program Files\Cypress\PSoC 3 Development Kit\1.0

## 2.3 Install Hardware

No hardware installation is required for this kit.

## 2.4 Install Software

When installing the PSoC 3 Development Kit, the installer checks if your system has the required software. These include PSoC Creator, PSoC Programmer, Windows Installer, .NET, Acrobat Reader, and KEIL Compiler. If these applications are not installed, then the installer prompts you to download and install them.

Install the following software from the kit CD:

1. PSoC Creator
2. PSoC Programmer 3.12.3 or later  
**Note** When installing PSoC Programmer, select **Typical** on the Installation Type page.
3. Example projects (provided in the Firmware folder)

## 2.5 Uninstall Software

The software can be uninstalled using one of the following methods:

- Go to **Start > Control Panel > Add or Remove Programs**; select the **Remove** button.
- Go to **Start > All Programs > Cypress > Cypress Update Manager > Cypress Update Manager**; select the **Uninstall** button.
- Insert the installation CD and click **Install PSoC 3 Development Kit** button. In the **CyInstaller for PSoC 3 Development Kit 1.0** window, select **Remove** from the Installation Type drop-down menu. Follow the instructions to uninstall.

# 3. Kit Operation



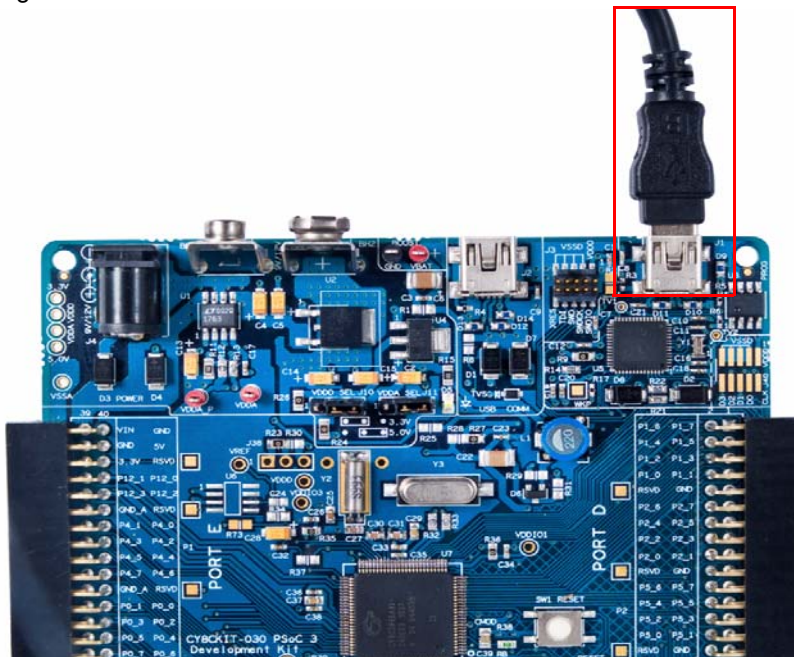
## 3.1 Introduction

The example projects in the PSoC 3 Development Kit help you develop precision analog applications using the PSoC 3 family of devices. The board also has hooks to enable low power measurements for low power application development and evaluation.

## 3.2 Programming PSoC 3 Device

The default programming interface for the board is a USB based on-board programming interface. To program the device, plug the USB cable to the programming USB connector J1, as shown in the following figure.

Figure 3-1. Connect USB Cable to J1



When plugged in, the board enumerates as DVKProg. After enumeration, initiate, build, and then program using PSoC Creator.

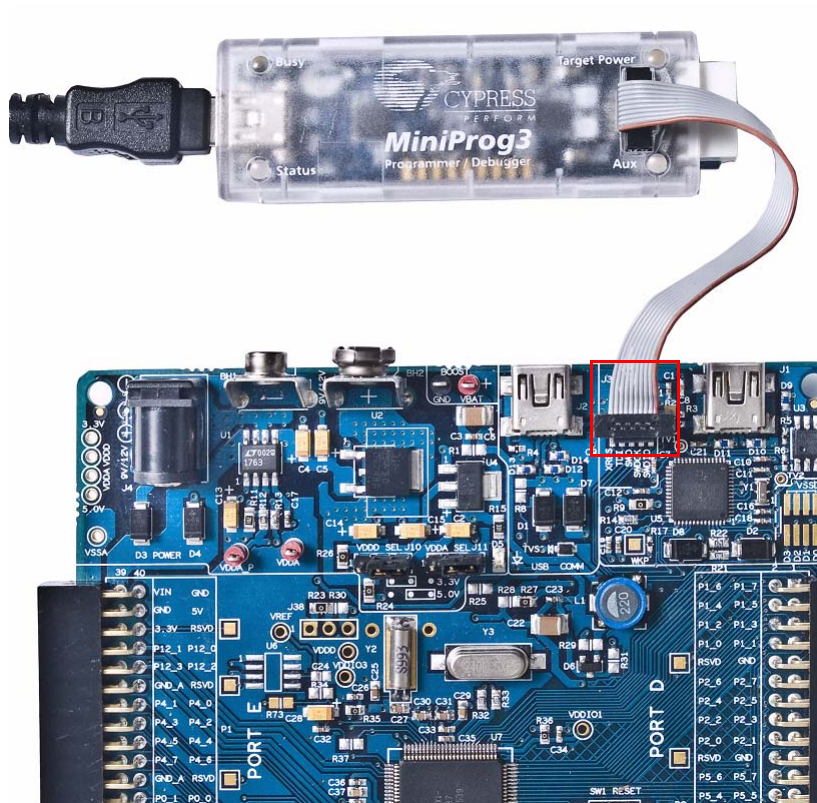
When using on-board programming, it is not necessary to power the board from the 12-V or 9-V DC supply or a battery. The USB power to the programming section can be used.

If the board is already powered from another source, plugging in the programming USB does not damage the board.

The PSoC 3 device on the board can also be programmed using a MiniProg3 (CY8CKIT-002). To use MiniProg3 for programming, use the connector J3 on the board as shown in the following figure.

**Note** The MiniProg3 (CY8CKIT-002) is not part of the PSoC 3 Development Kit contents. It can be purchased from the Cypress Online Store.

Figure 3-2. Connect MiniProg



With the MiniProg3, programming is similar to the on-board programmer; however, the setup enumerates as a MiniProg3.

# 4. Hardware

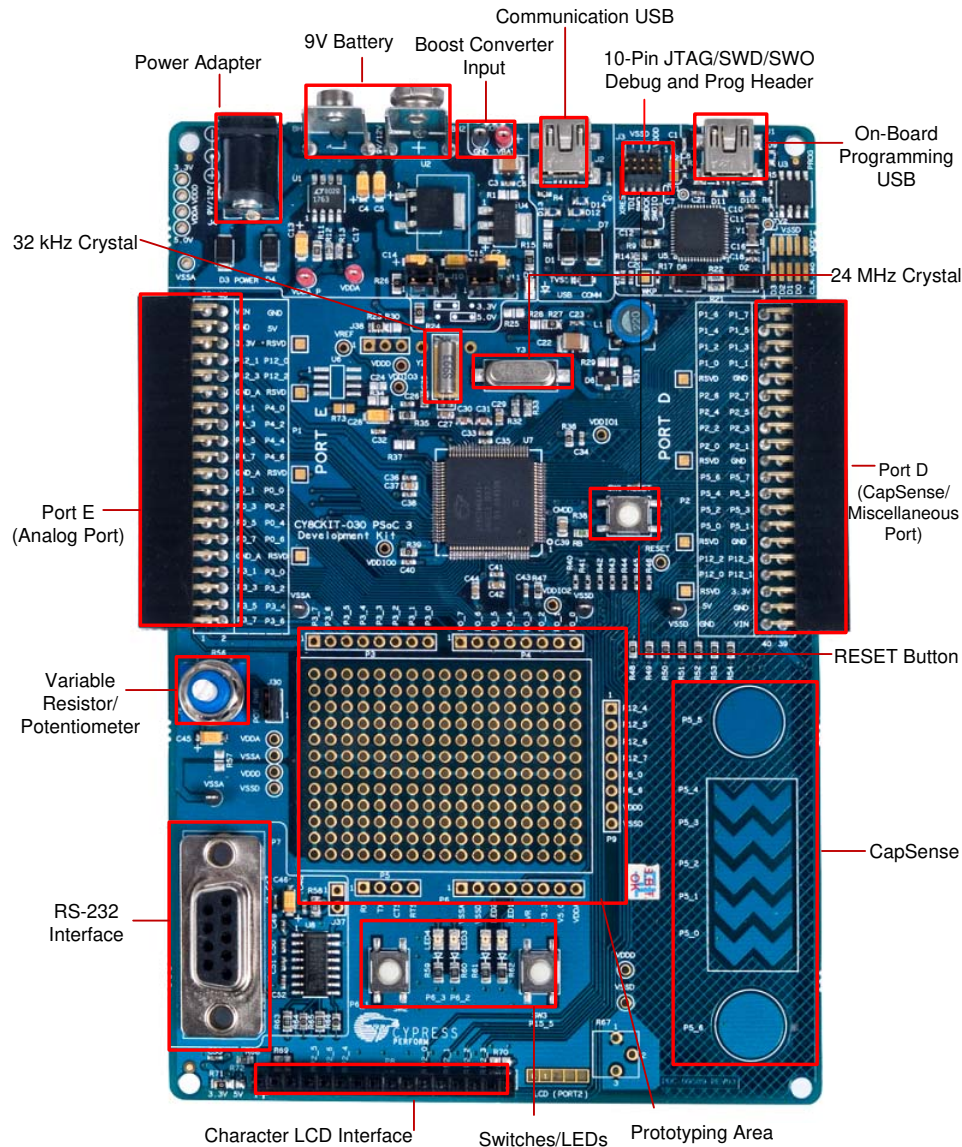


## 4.1 System Block Diagram

The PSoC 3 Development Kit has the following sections:

- Power supply system
- Programming interface
- USB communications
- Boost convertor
- PSoC 3 and related circuitry
- 32-kHz crystal
- 24-MHz crystal
- Port E (analog performance port) and port D (CapSense® or generic port)
- RS232 communications interface
- Prototyping area
- Character LCD interface
- CapSense buttons and sliders

Figure 4-1. PSoC 3 Development Kit Details



## 4.2 Functional Description

### 4.2.1 Power Supply

The power supply system on this board is versatile; input supply can be from the following sources:

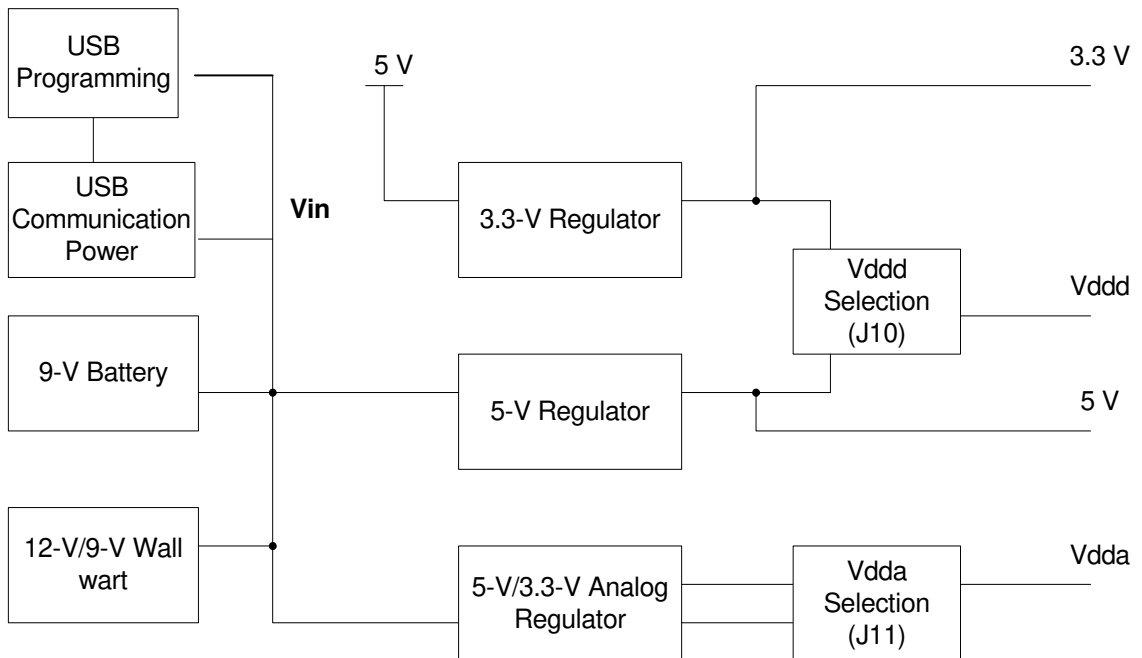
- 9-V or 12-V wall wart supply using connector J4
- 9-V battery connector using connectors BH1 and BH2
- USB power from communications section using connector J2
- USB power from the on-board programming section using connector J1
- Power from JTAG/SWD programming interface using connector J3
- Power through boost convertor that uses the input test points VBAT and GND

The board power domain has five rails:

- **Vin rail:** This is where the input of the on-board regulators are connected. This domain is powered through protection diodes.
- **5-V rail:** This is the output of the 5-V regulator U2. The rail is a fixed 5 V output regardless of jumper settings. The voltage in this rail can be less than 5 V only when the board is powered by the USB. This 5-V rail powers the circuits that require fixed 5 V supply.
- **3.3-V rail:** This is the output of the 3.3-V regulator U4. This rail remains 3.3 V regardless of jumper settings or power source changes. It powers the circuits requiring fixed 3.3 V supply such as the on-board programming section.
- **Vddd rail:** This rail provides power to the digital supply for the PSoC device. It can be derived from either the 5 V or 3.3 V rail. The selection is made using J10 (3-pin jumper).
- **Vdda rail:** This rail provides power to the analog supply of the PSoC device. It is the output of a low noise regulator U1. The regulator is a variable output voltage and can be either 3.3 V or 5 V. This is done by changing the position on J11 (3-pin jumper).

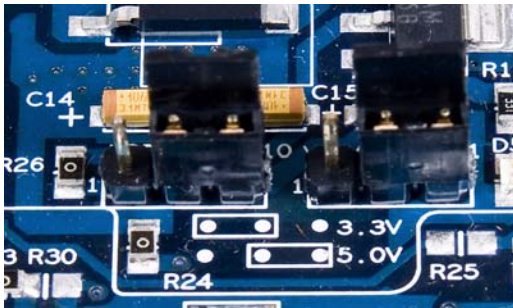
The following block diagram shows the structure of the power system on the board.

Figure 4-2. Power System Structure



#### 4.2.1.1 Power Supply Jumper Settings

Figure 4-3. Jumper Settings



Two jumpers govern the power rails on the board. J10 is responsible for the selection of V<sub>ddd</sub> (digital power) and J11 selects V<sub>dda</sub> (analog power).

The jumper settings for each power scheme are as follows.

Powering Scheme	Jumper Settings
V <sub>dda</sub> = 5 V, V <sub>ddd</sub> = 5 V	J10 in 5 V setting and J11 in 5 V setting.
V <sub>dda</sub> = 3.3 V, V <sub>ddd</sub> = 3.3 V	J10 in 3.3 V setting and J11 in 3.3 V setting.
V <sub>dda</sub> = 5 V, V <sub>ddd</sub> = 3.3 V	J10 in 3.3 V setting and J11 in 5 V setting.
V <sub>dda</sub> = 3.3 V, V <sub>ddd</sub> = 5 V	Can be achieved, but is an invalid condition because the PSoC 3 silicon performance cannot be guaranteed.

**Warning:**

- The PSoC device performance is guaranteed when V<sub>dda</sub> is greater than or equal to V<sub>ddd</sub>. Failure to meet this condition can have implications on the silicon performance.
- When USB power is used, ensure a 3.3 V setting on both analog and digital supplies. This is because, the 5 V rail of the USB power is not accurate and is not recommended.

#### 4.2.1.2 Grounding Scheme

The board is designed considering analog designs as major target applications. Therefore, the grounding scheme in the board is unique to ensure precision analog performance.

There are three types of ground on this board:

- GND - This is the universal ground where all the regulators are referred. Both V<sub>ssd</sub> and V<sub>ssa</sub> connect to this ground through a star connection.
- V<sub>ssd</sub> - This is the digital ground and covers the digital circuitry present on the board, such as RS232 and LCD.
- V<sub>ssa</sub> - This is the analog ground and covers the grounding for analog circuitry present on the board, such as the reference block.

When creating custom circuitry in the prototyping area provided on the board, remember to use the V<sub>ssa</sub> for the sensitive analog circuits and V<sub>ssd</sub> for the digital ones.

Port E on the board is the designated analog expansion connector. This connector brings out ports 0, 3, and 4, which are the best performing analog ports on PSoC 3 and PSoC 5 devices. The expansion connector, port E, has two types of grounds. One is the analog ground (GND\_A in silk

screen, Vssa in the schematic), which connects directly to the analog ground on the board. The other ground known simply as GND, is used for the digital and high current circuitry on the expansion board. This differentiation on the connector grounds helps the expansion board designer to separate the analog and digital ground on any high precision analog boards being designed for port E.

#### 4.2.1.3 *Low Power Functionality*

The kit also facilitates application development, which requires low power consumption. Low power functions require a power measurement capability, also available in this kit.

The analog supply is connected to the device through the zero-ohm resistor (R23). By removing this resistor and connecting an ammeter in series using the test points, Vdda\_p and Vdda, you can measure the analog power used by the system.

The digital supply can be monitored by removing connection on the jumper J10 and connecting an ammeter in place of the short. This allows to measure the digital power used by the system.

The board provides the ability to measure analog and digital power separately. To measure power at a single point, rather than at analog and digital separately, remove the resistor R23 to disconnect the analog regulator from powering the Vdda and short Vdda and Vddd through R30. Now, the net power can be measured at the J10 jumper similar to the digital power measurement. To switch repeatedly between R23 and R30, moving around the zero-ohm resistors can be discomfoting. Hence, a J38 (unpopulated) is provided to populate a male 3-pin header and have a shorting jumper in the place of R23/R30.

While measuring device power, make the following changes in the board to avoid leakage through other components that are connected to the device power rails.

- Disconnect the RS232 power by disconnecting R58. An additional jumper capability is available as J37 if you populate it with a 2-pin male header.
- Disconnect the potentiometer by disconnecting J30.
- Ground the boost pins if boost operation is not used by populating R1, R28, and R29. Also make sure R25 and R31 are not populated.

## 4.2.2 Programming Interface

This kit allows programming in two modes:

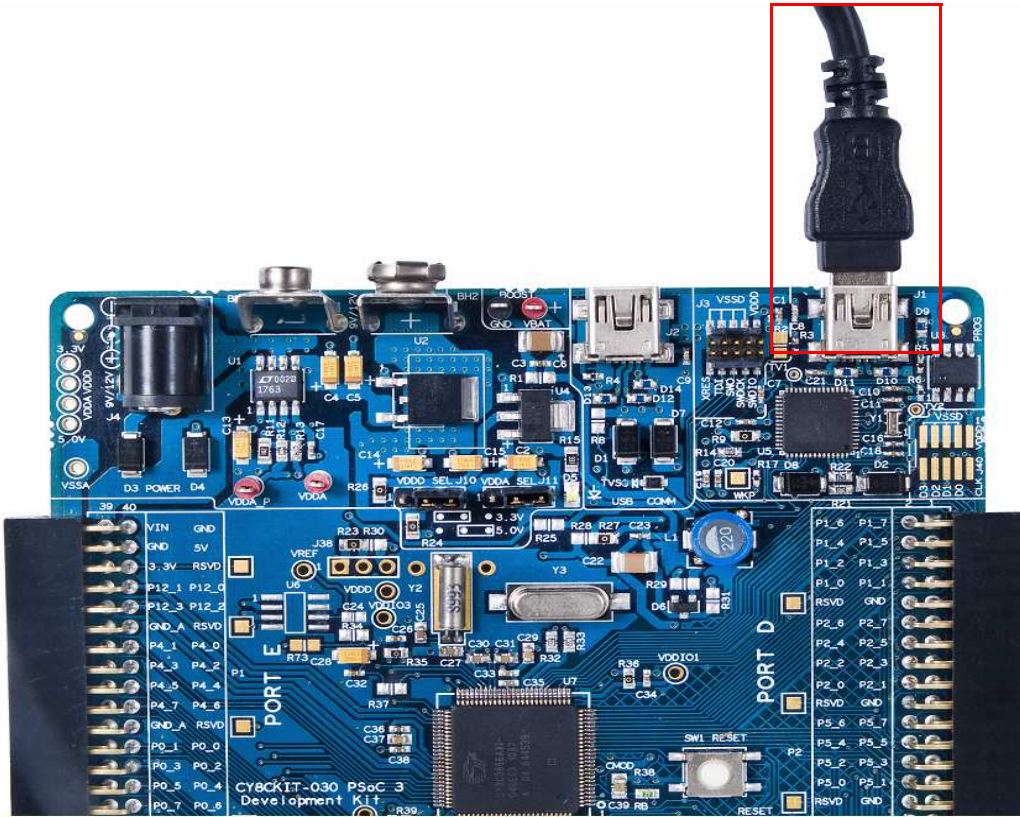
- Using the on-board programming interface
- Using the JTAG/SWD programming interface that uses a MiniProg3

### 4.2.2.1 *On-board Programming Interface*

The on-board programmer interfaces with your PC through a USB connector marked as USB programming.



Figure 4-4. On-board Programming Interface



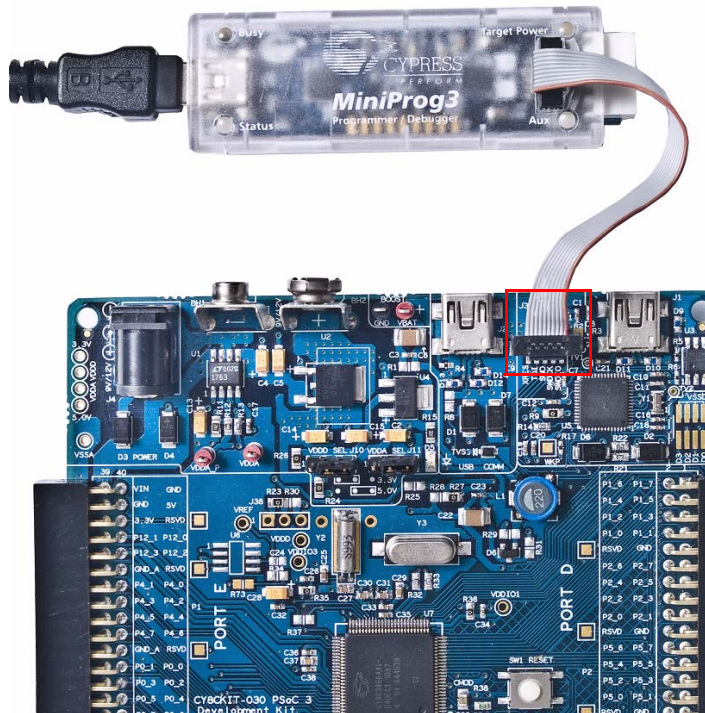
When the USB programming is plugged into the PC, it enumerates as DVKProg and you can use the normal programming interface from PSoC Creator to program this board through the on-board programmer.

A zero-ohm resistor R9 is provided on the board to disconnect power to the on-board programmer.

#### 4.2.2.2 JTAG/SWD Programming

Apart from the on-board programming interface, the board also provides the option of using the MiniProg3. This interface is much faster than the on-board program interface. The JTAG/SWD programming is done through the 10-pin connector, J3.

Figure 4-5. JTAG/SWD Programming

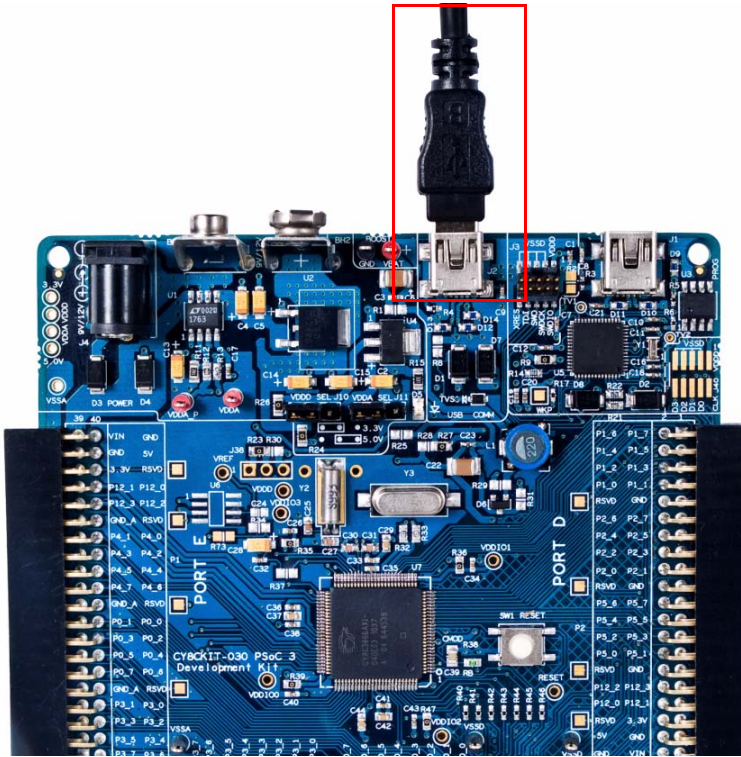


The JTAG/SWD programming using J3 requires the MiniProg3 programmer, which can be purchased from <http://www.cypress.com>.

### 4.2.3 USB Communication

The board has a USB communications interface that uses the connector, as shown in Figure 4-6. The USB connector connects to the D+ and D– lines on the PSoC to enable development of USB applications using the board. This USB interface can also supply power to the board as discussed in [Power Supply on page 12](#).

Figure 4-6. USB Interface



#### 4.2.4 Boost Convertor

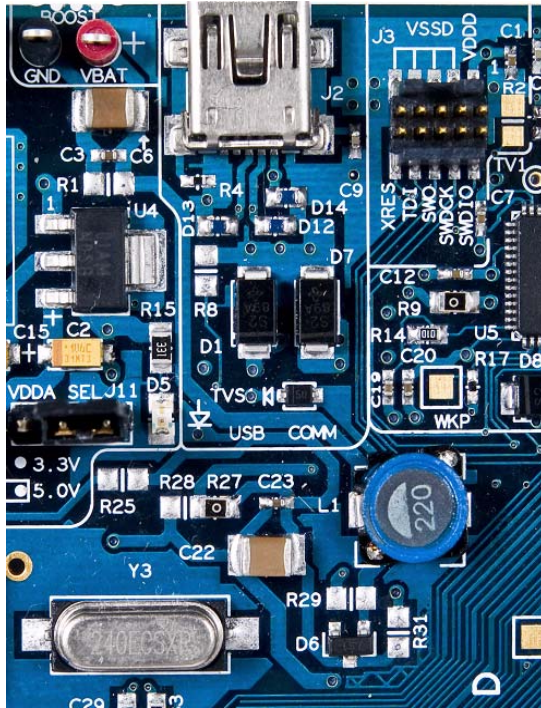
The PSoC 3 device has a unique capability of working from a voltage supply as low as 0.5 V. This is possible using the boost convertor. The boost convertor uses an external inductor and a diode. These components are pre-populated on the board. [Figure 4-7](#) shows the boost convertor.

To enable the boost convertor functionality, make the following hardware changes on the board.

- Populate resistors R25, R27, R29, and R31
- Ensure that R1 and R28 are not populated

After making these changes, you can make a boost convertor based design by making the appropriate configurations in the project. The input power supply to the boost convertor must be provided through the test points marked Vbat and GND.

Figure 4-7. Boost Converter



#### 4.2.5 32-kHz and 24-MHz Crystal

PSoC 3 has an on-chip Real Time Clock (RTC), which can function in sleep. This requires an external 32-kHz crystal, which is provided on board to facilitate RTC based designs. The PSoC 3 also has an option for an external MHz crystal in applications where the IMO tolerance is not satisfactory. In these applications, the board has a 24-MHz crystal to provide an accurate main oscillator.

#### 4.2.6 PSoC 3 Development Kit Expansion Ports

The PSoC 3 Development Kit has two expansion ports, Port D and Port E, each with their own unique features.

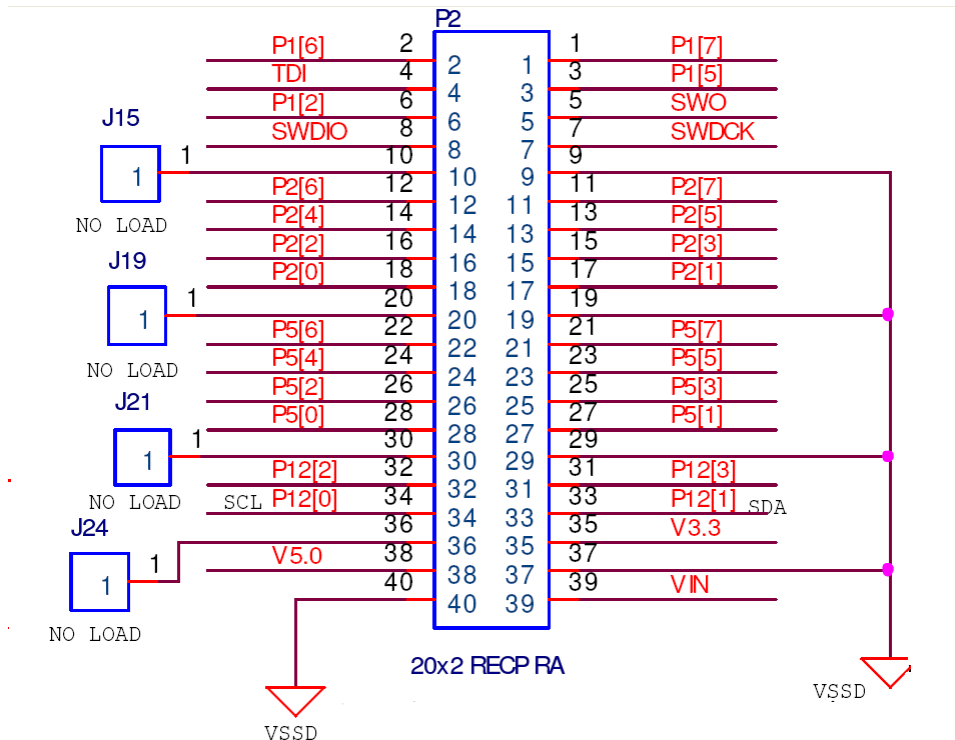
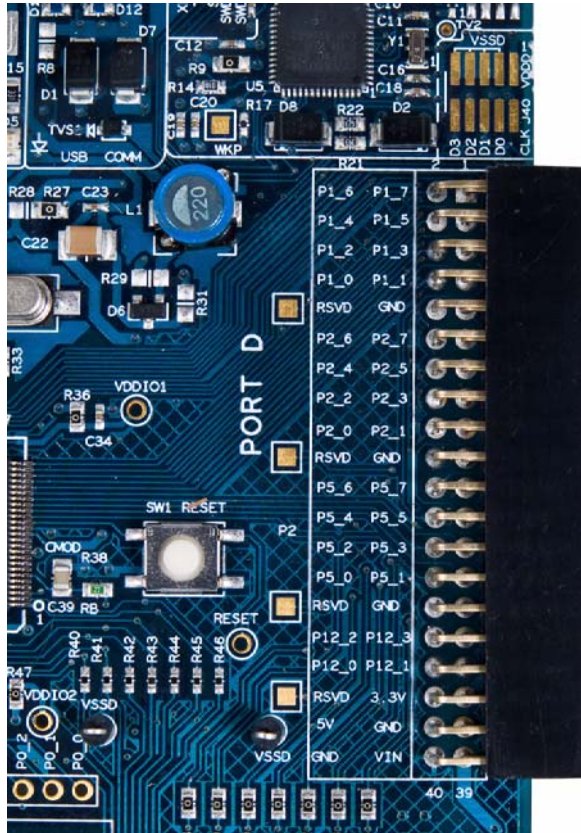
##### 4.2.6.1 Port D

This is the miscellaneous port on the board. It is designed to handle CapSense based application boards and digital application boards. The signal routing to this port adheres to the stringent requirements posed to provide good performance CapSense. This port can also be used for other functions and Expansion Board Kits (EBKs).

This port is not designed for precision analog performance. The pins on the port are functionally compatible to port B of the PSoC Development Kit. So any project made to function on port B of the PSoC Development Kit can be easily ported over to port D on this board. A caveat to this is that there is no opamp available on this port; therefore, opamp based designs are not recommended for use on this port.

The following figure shows the pin mapping for the port.

Figure 4-8. Port D

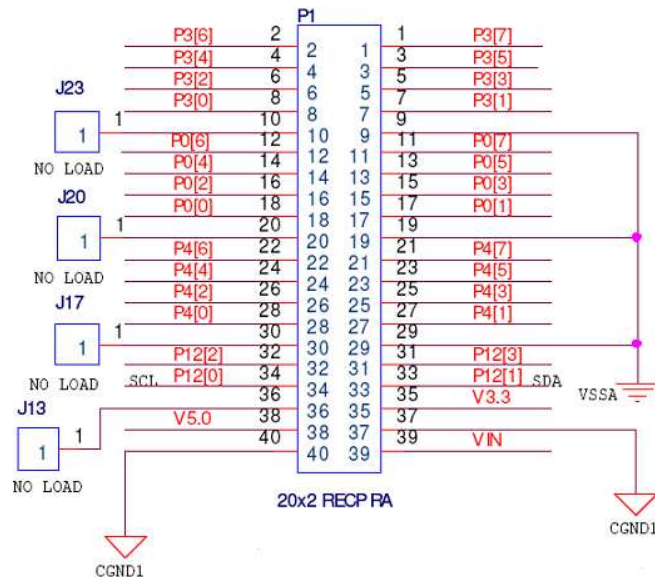
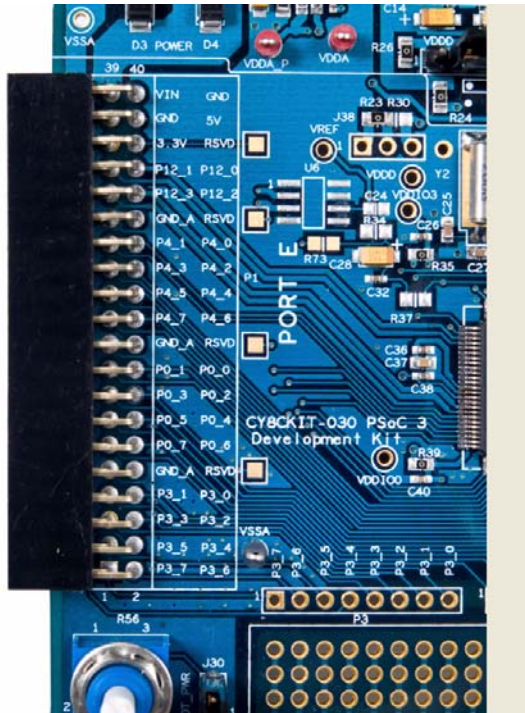


### 4.2.6.2 Port E

This is the analog port on this kit and has special layout considerations. It also brings out all analog resources such as dedicated opamps to a single connect. Therefore, this port is ideal for precision analog design development. This port is functionally compatible to port A of the PSoC Development Kit and it is easy to port application developed on port A.

There are two types of grounds on this port, CGND1 and CGND2. The two grounds are connected to the GND on the board, but are provided for expansion boards designed for analog performance. The expansion boards have an analog and digital ground. The two grounds on this port help to keep it distinct even on this board until it reaches the GND plane.

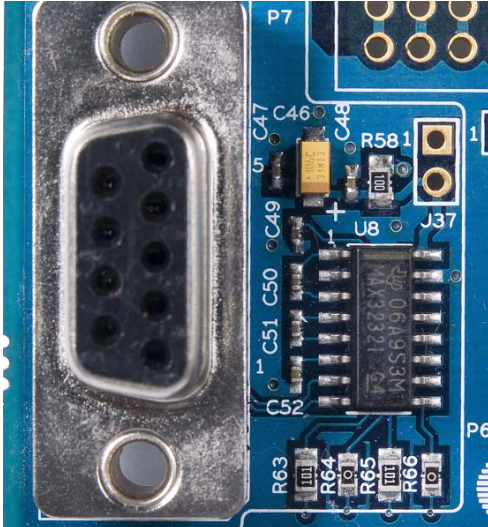
Figure 4-9. Port E



#### 4.2.7 RS-232 Interface

The board has an RS-232 transceiver on board for designs using RS-232 (UART). The RS-232 section power can be disconnected through a single resistor R58. This is useful for low-power designs.

Figure 4-10. RS-232 Interface

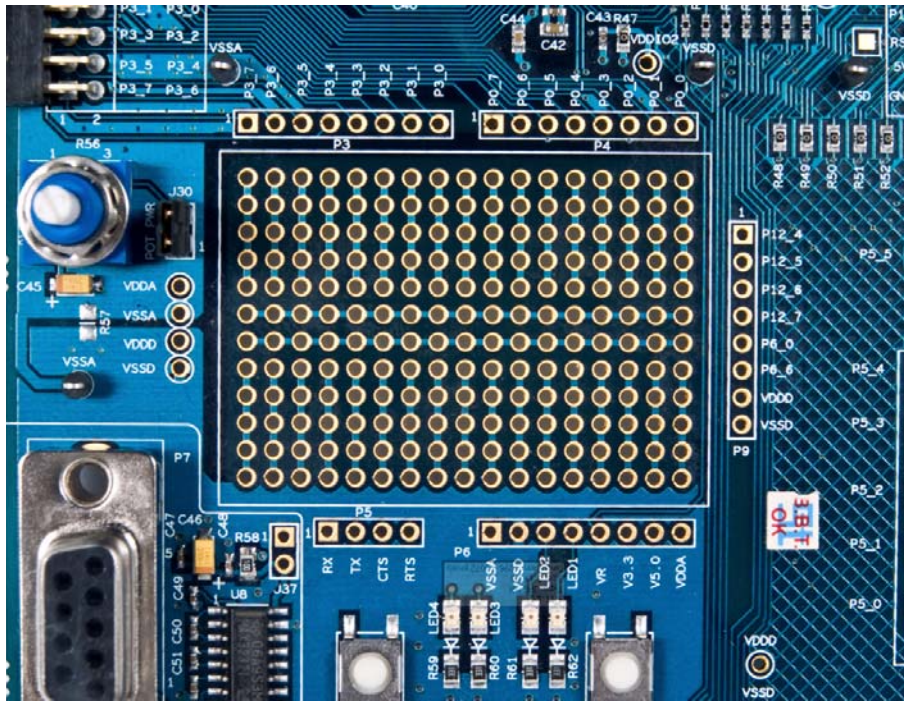


#### 4.2.8 Prototyping Area

The prototyping area on the board has two complete ports of the device for simple custom circuit development. The ports in the area are port 0 and port 3, which bring out the four dedicated opamp pins on the device. Therefore, these ports can be used with the prototyping area to create simple yet elegant analog designs. It also brings SIOs such as port 12[4], port 12[5], port 12[6], and port 12[7] and GPIOs such as port P6[0] and port P6[6]. There is power and ground connections close to the prototyping space for convenience.

The area also has four LEDs and two switches for applications development. The two switches on the board are hard-wired to port 15[5] and port 6[1]. Two LEDs out of the four are hard-wired to port 6[2] and port 6[3] and the other two are brought out on pads closer to the prototyping area.

Figure 4-11. Prototyping Area



This area also comprises of a potentiometer to be used for analog system development work. The potentiometer connects from Vdda, which is a noise free supply and is hence capable of being used for low noise analog applications. Potentiometer output is available on P6[5] and VR on header P6 in prototyping area.

#### 4.2.9 Character LCD

The kit has a character LCD module, which goes into the character LCD header, P8. The LCD runs on a 3.3-V supply and can function regardless of the voltage on which PSoC is powered. There is a zero-ohm resistor setting available on the LCD section (R71/72), making it possible to convert it to a 3.3 V LCD.

**CAUTION:** When the resistor is shifted to support a 5 V LCD module, plugging in a 3.3 V LCD module into the board can damage the LCD module.

Figure 4-12. Pin 1 Indication

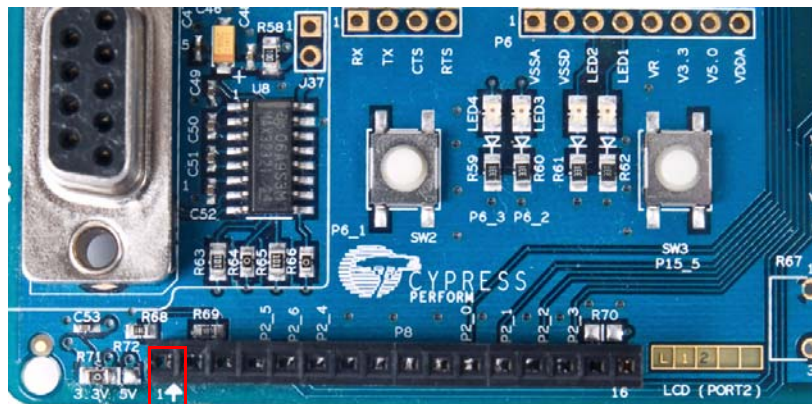
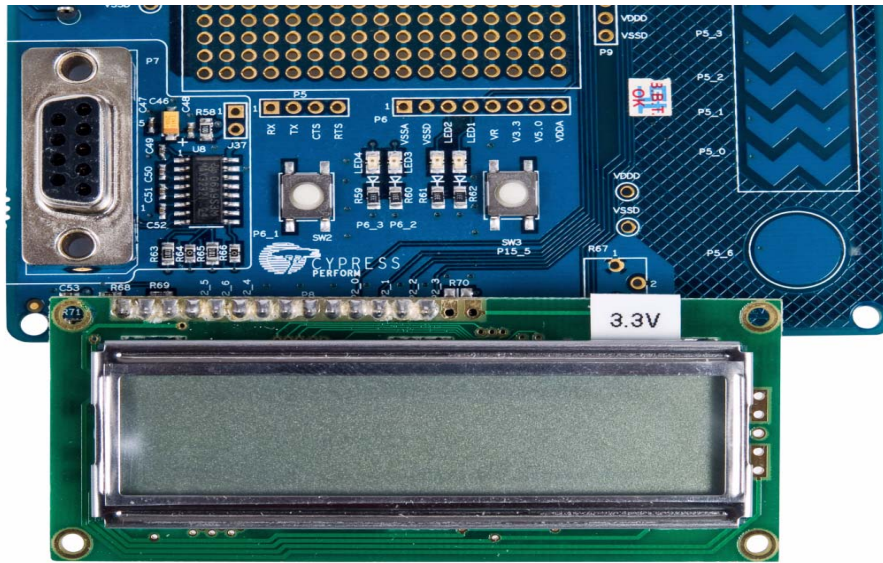




Figure 4-13. LCD Connected on P8 Connector



#### 4.2.10 CapSense Sensors

The board layout has considered the special requirements for CapSense. It has two CapSense buttons and a 5-element CapSense slider. The CapSense buttons are connected to pins P5[6] and P5[5]. The slider elements are connected to pins P5[0:4].

The Cmod (modulation capacitor) is connected to pin P6[4] and an optional Rb (bleeder resistor) is available on P15[4].

Figure 4-14. CapSense Sensors

