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CY8CKIT-050

# PSoC® 5LP Development Kit Guide

Doc. # 001-65816 Rev. *G

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# 1. Introduction

Thank you for your interest in the CY8CKIT-050 PSoC® 5LP Development Kit. This kit allows you to develop precision analog and low-power designs using PSoC 5LP. You can design your own projects with PSoC Creator™ or alter the sample projects provided with this kit.

The CY8CKIT-050 PSoC 5LP Development Kit is based on the PSoC 5LP family of devices. PSoC 5LP is a Programmable System-on-Chip™ platform for 8-bit, 16-bit, and 32-bit applications. It combines precision analog and digital logic with a high-performance CPU. With PSoC, you can create the exact combination of peripherals and integrated proprietary IP to meet your application requirements.

## 1.1 Kit Contents

The PSoC 5LP Development Kit contains:

- Development board
- Kit DVD
- Quick start guide
- USB A to mini-B cable
- 3.3-V LCD module

Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help.

## 1.2 PSoC Creator

Cypress's PSoC Creator software is a state-of-the-art, easy-to-use integrated development environment (IDE) that introduces a hardware and software design environment based on classic schematic entry and revolutionary embedded design methodology.

With PSoC Creator, you can:

- Create and share user-defined, custom peripherals using hierarchical schematic design.
- Automatically place and route select components and integrate simple glue logic, normally located in discrete muxes.
- Trade off hardware and software design considerations allowing you to focus on what matters and getting to market faster.

PSoC Creator also enables you to tap into an entire tools ecosystem with integrated compiler tool chains, RTOS solutions, and production programmers to support both PSoC 3 and PSoC 5LP.

## 1.3 Additional Learning Resources

Visit http://www.cypress.com/go/psoc5 for additional learning resources in the form of datasheets, application notes, and technical reference manual.

### 1.3.1 Beginner Resources

AN77759 - Getting Started with PSoC 5

PSoC Creator Training

### 1.3.2 Engineers Looking for More

AN54460 - PSoC 3, PSoC 4, and PSoC 5LP Interrupts

AN52705 - PSoC 3 and PSoC 5LP - Getting Started with DMA

AN52701 - PSoC 3 and PSoC 5LP - Getting Started with Controller Area Network (CAN)

AN54439 - PSoC 3 and PSoC 5LP External Crystal Oscillators

AN52927 - PSoC 3 and PSoC 5LP - Segment LCD Direct Drive

Cypress continually strives to provide the best support. Click here to view a growing list of application notes for PSoC 3, PSoC 4, and PSoC 5LP.

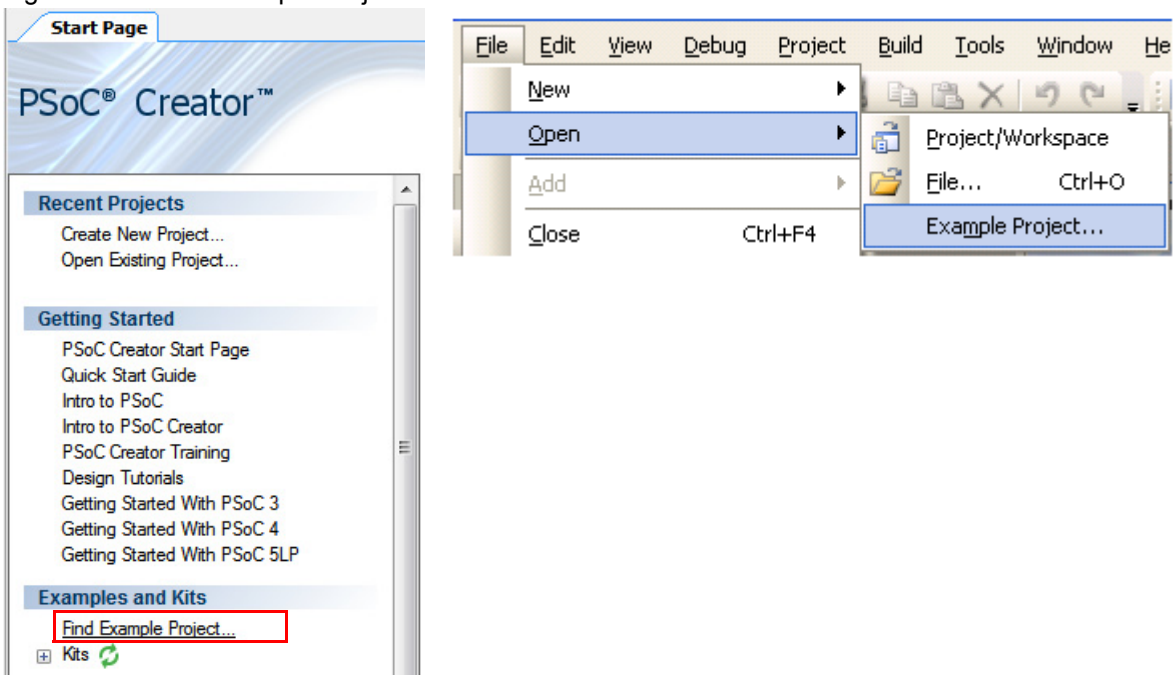
### 1.3.3 Learning from Peers

Cypress Developer Community Forums

### 1.3.4 More Code Examples

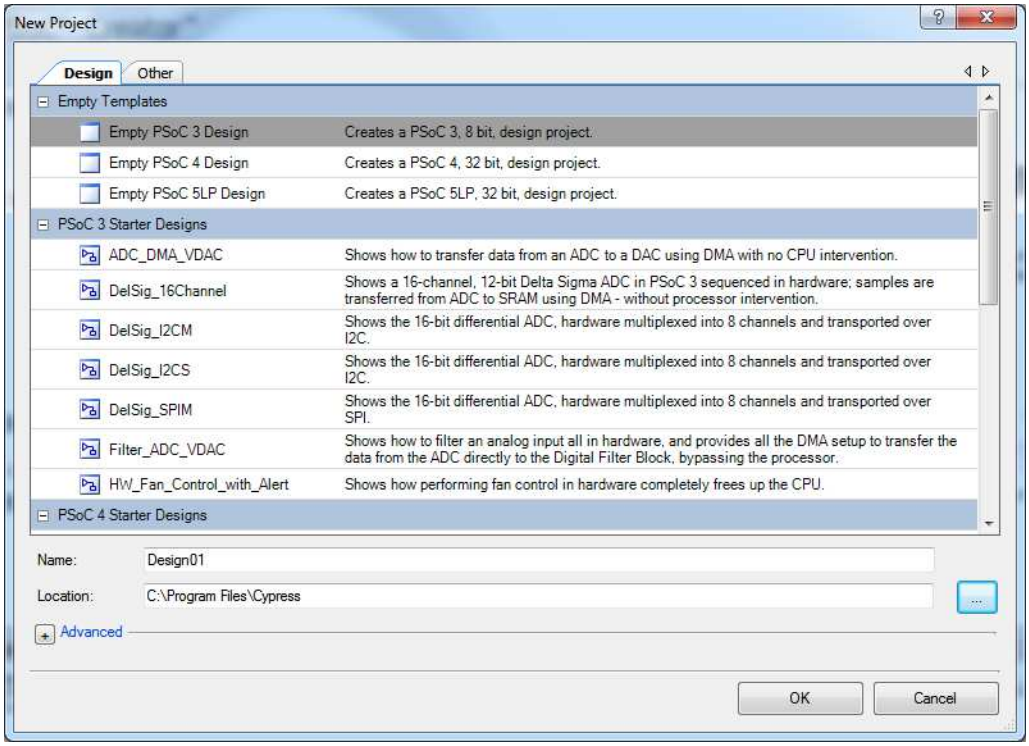
PSoC Creator provides several example projects that make code development fast and easy. To access these example projects, click on **Find Example Project…** under the **Example and Kits** section in the **Start Page** of PSoC Creator or navigate to **File > Open > Example Project…**

Figure 1-1. Find Example Project



The Find Example Project section has various filters that help you locate the most relevant project. PSoC Creator provides several starter designs. These designs highlight features that are unique to PSoC devices. They allow you to create a design with various components, instead of creating an empty design; the code is also provided. To use a starter design for your project, navigate to **File > New > Project** and select the design required.

Figure 1-2. New Project




The example projects and starter designs are designed for the CY8CKIT-001 PSoC Development Kit. However, these projects can be converted for use with the CY8CKIT-030 PSoC 3 Development Kit or CY8CKIT-050 PSoC 5LP Development Kit by following the procedure in the knowledge base article Migrating Project from CY8CKIT-001 to CY8CKIT-030 or CY8CKIT-050.

## 1.4 Document History

| Revision | PDF Creation Date | Origin of Change | Description of Change |
|---|---|---|---|
| ** | 03/01/2011 | PVKV | Initial version of kit guide |
| *A | 04/28/2011 | RKAD | Updated Schematic |
| *B | 12/15/2011 | RKAD | Added sections 4.2.1.4 and 4.2.1.5. Added Pin Assignment table in the Appendix. Updated bill of materials. Content updates throughout the document |
| *C | 05/15/2012 | SASH | Updated the Additional Resources section |
| *D | 06/18/2012 | SASH | Updated DVD Installation on page 9. |
| *E | 11/09/2012 | SASH | Updated images and content. |
| *F | 07/12/2013 | SASH | Added another item to the Warnings list in section 4.2.1.1. Updates for PSoC Creator 2.2. |
| *G | 08/22/2013 | SASH | Updated Figure 1-1, Figure 1-2, Figure 2-1, Figure 5-4, and Figure 5-5. Updated Install Software on page 10. Added note in Verify Output on page 35. Updated to PSoC Creator 3.0. |

## 1.5 Documentation Conventions

Table 1-1. Document Conventions for Guides

| Convention | Usage |
|---|---|
| `Courier New` | Displays file locations, user entered text, and source code:<br>`C:\ ...cd\icc\` |
| *Italics* | Displays file names and reference documentation:<br>Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*. |
| [**Bracketed, Bold**] | Displays keyboard commands in procedures:<br>[**Enter**] or [**Ctrl**] [**C**] |
| File > Open | Represents menu paths:<br>File > Open > New Project |
| **Bold** | Displays commands, menu paths, and icon names in procedures:<br>Click the **File** icon and then click **Open**. |
| Times New Roman | Displays an equation:<br>2 + 2 = 4 |
| Text in gray boxes | Describes cautions or unique functionality of the product. |

# 2. Getting Started

This chapter describes how to install and configure the PSoC 5LP Development Kit. Kit Operation chapter on page 11 describes the kit operation. It explains how to program a PSoC 5LP device with PSoC Programmer and use the kit with the help of a code example. To reprogram the PSoC device with PSoC Creator, see the installation instructions for PSoC Creator. Hardware chapter on page 14 details the hardware operation. Code Examples chapter on page 30 provides instructions to create a simple code example. The Appendix on page 40 provides the Schematic on page 40 and Bill of Materials (BOM) on page 50 associated with the PSoC 5LP Development Kit.

## 2.1 DVD Installation

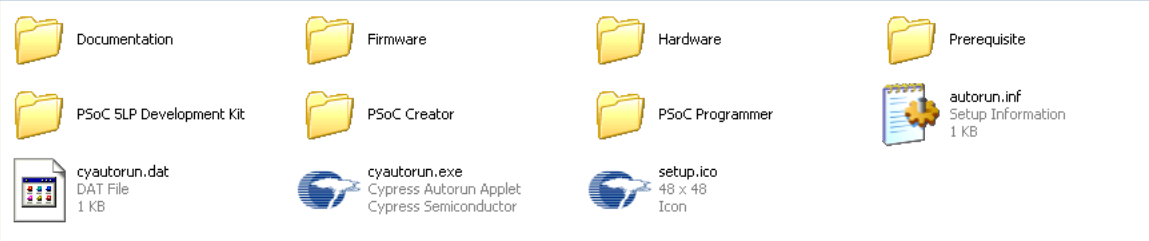
Follow these steps to install the PSoC 5LP Development Kit software:

1. Insert the kit DVD into the DVD drive of your PC. The DVD is designed to auto-run and the kit menu appears.

Figure 2-1. Kit Menu


**Note** If auto-run does not execute, double-click *cyautorun.exe* on the root directory of the DVD.

Figure 2-2. DVD Root Directory




After the installation is complete, the kit contents are available at the following location:
`<Install_Directory>\Cypress\PSoC 5LP Development Kit\<version>`

## 2.2 Install Hardware

No hardware installation is required for this kit.

## 2.3 Install Software

When installing the PSoC 5LP Development Kit, the installer checks if your system has the required software. These include PSoC Creator, PSoC Programmer, Windows Installer, .NET, and Keil Complier. If these applications are not installed, the installer installs them in your PC before installing the kit. If Acrobat Reader application is not installed in your PC, then the installer provides the link to install the same and this does not prevent kit installation. Note that Adobe reader is required to view the kit documents.

Install the following software from the kit DVD:

- PSoC Creator 3.0 or later
- PSoC Programmer 3.19.1 or later
  **Note** When installing PSoC Programmer, select **Typical** on the Installation Type page.
- Code examples (provided in the Firmware folder)

## 2.4 Uninstall Software

The software can be uninstalled using one of the following methods:

- Go to **Start** > **Control Panel** > **Add or Remove Programs**; select the **Remove** button.
- Go to **Start** > **All Programs** > **Cypress** > **Cypress Update Manager** > **Cypress Update Manager**; select the **Uninstall** button.
- Insert the installation DVD and click **Install PSoC 5LP Development Kit** button. In the **CyInstaller for PSoC 5LP Development Kit 2.1** window, select **Remove** from the Installation Type drop-down menu. Follow the instructions to uninstall.

## 2.5 Verify Kit Version

To know the kit revision, look for the white sticker on the bottom left, on the reverse of the kit box. If the revision reads CY8CKIT-050B, then, you own the latest version.

To upgrade CY8CKIT-050/CY8CKIT-050A to CY8CKIT-050B, you can purchase our latest kits at http://www.cypress.com/go/CY8CKIT-050.

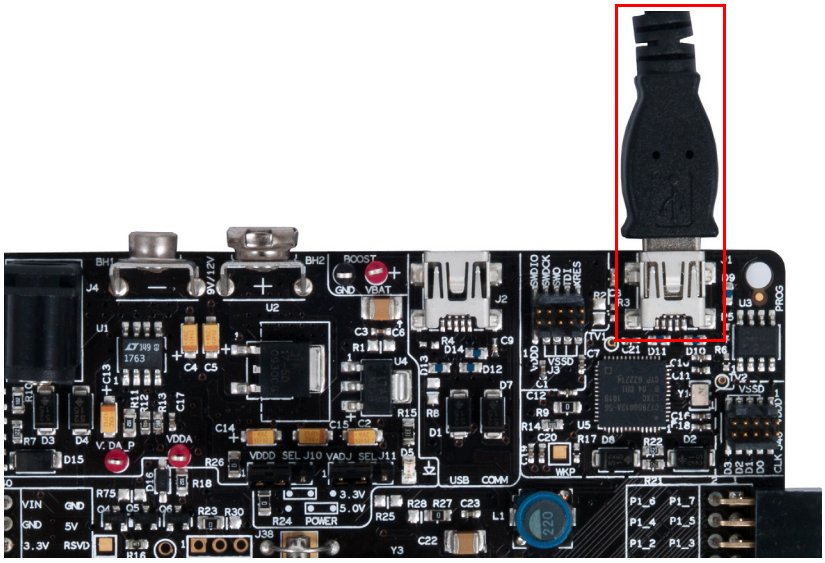
# 3. Kit Operation

The code examples in the PSoC 5LP Development Kit help you develop precision analog applications using the PSoC 5LP family of devices. The board also has hooks to enable low-power measurements for low-power application development and evaluation.

## 3.1 Programming PSoC 5LP Device

The default programming interface for the board is a USB-based onboard programming interface. To program the device, plug the USB cable to the programming USB connector J1, as shown in Figure 3-1.

Figure 3-1. Connect USB Cable to J1



When plugged in, the board enumerates as DVKProg5. After enumeration, initiate, build, and then program using PSoC Creator.

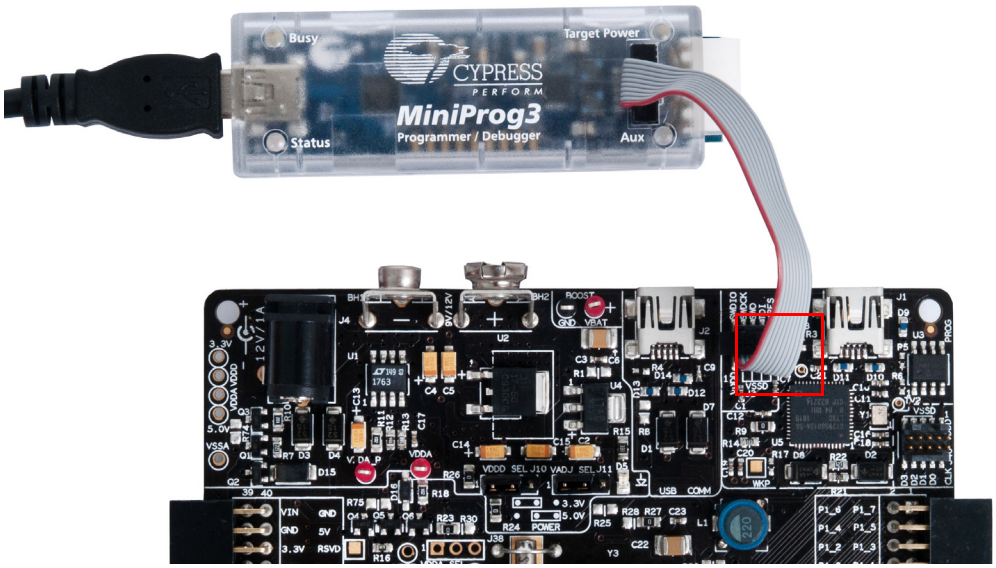
When using onboard programming, it is not necessary to power the board from the 12-V or 9-V DC supply or a battery. You can use the USB power to the programming section.

If the board is already powered from another source, plugging in the programming USB does not damage the board.

The PSoC 5LP device on the board can also be programmed using a MiniProg3 (CY8CKIT-002). To use MiniProg3 for programming, use the connector J3 on the board, as shown in Figure 3-2.

**Note** The MiniProg3 (CY8CKIT-002) is not part of the PSoC 5LP Development Kit contents. It can be purchased from the Cypress Online Store.

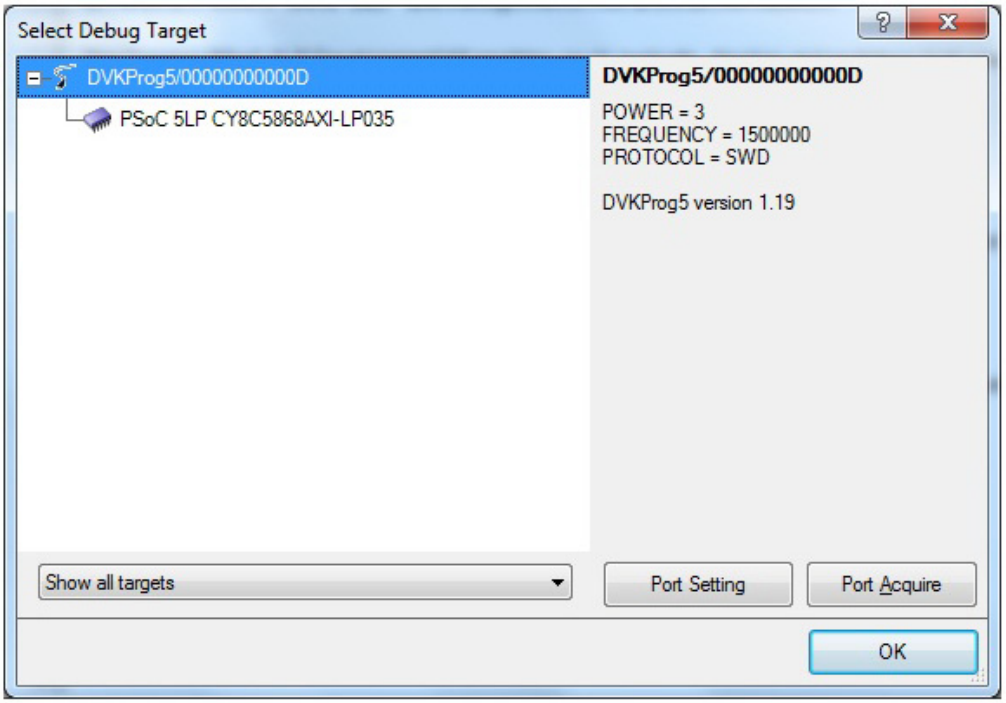
Figure 3-2. Connect MiniProg3




With the MiniProg3, programming is similar to the onboard programmer; however, the setup enumerates as a MiniProg3.

The Select Debug Target window may be displayed, as shown in the following figure.

Figure 3-3. Select Debug Target




Click **Port Acquire**. The window appears as follows. Click **Connect** to start programming.

Figure 3-4. Click Connect

# 4. Hardware

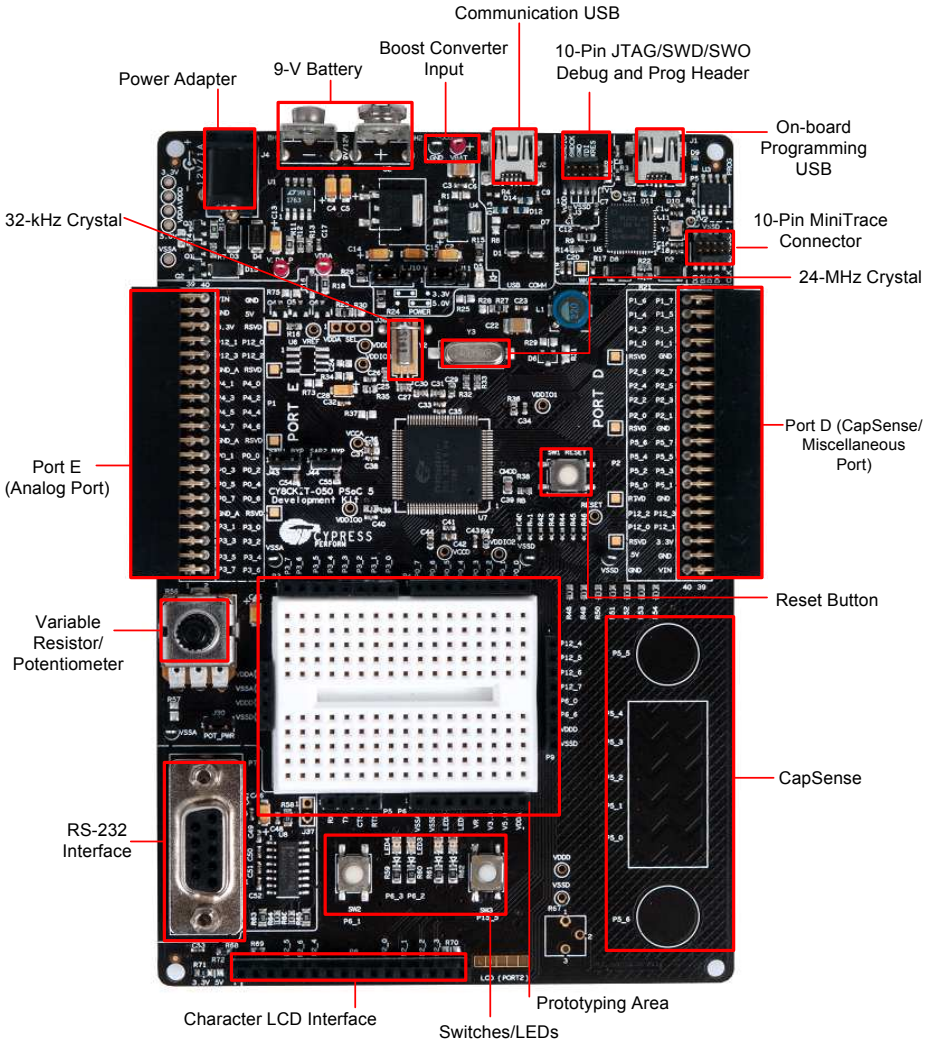
## 4.1 System Block Diagram

The PSoC 5LP Development Kit has the following sections:

- Power supply system
- Programming interface
- USB communications
- Boost convertor
- PSoC 5LP and related circuitry
- 32-kHz crystal
- 24-MHz crystal
- Port E (analog performance port) and port D (CapSense® or generic port)
- RS-232 communications interface
- Prototyping area
- Character LCD interface
- CapSense buttons and sliders

**Note** P0[2] is connected to the SAR bypass capacitor C40, which can be selected by shorting jumper J43. P0[4] is connected to the SAR bypass capacitor C55, which can be selected by shorting jumper J44.

Figure 4-1. PSoC 5LP Development Kit Details




## 4.2 Functional Description

### 4.2.1 Power Supply

The power supply system on this board is versatile; input supply can be from the following sources:

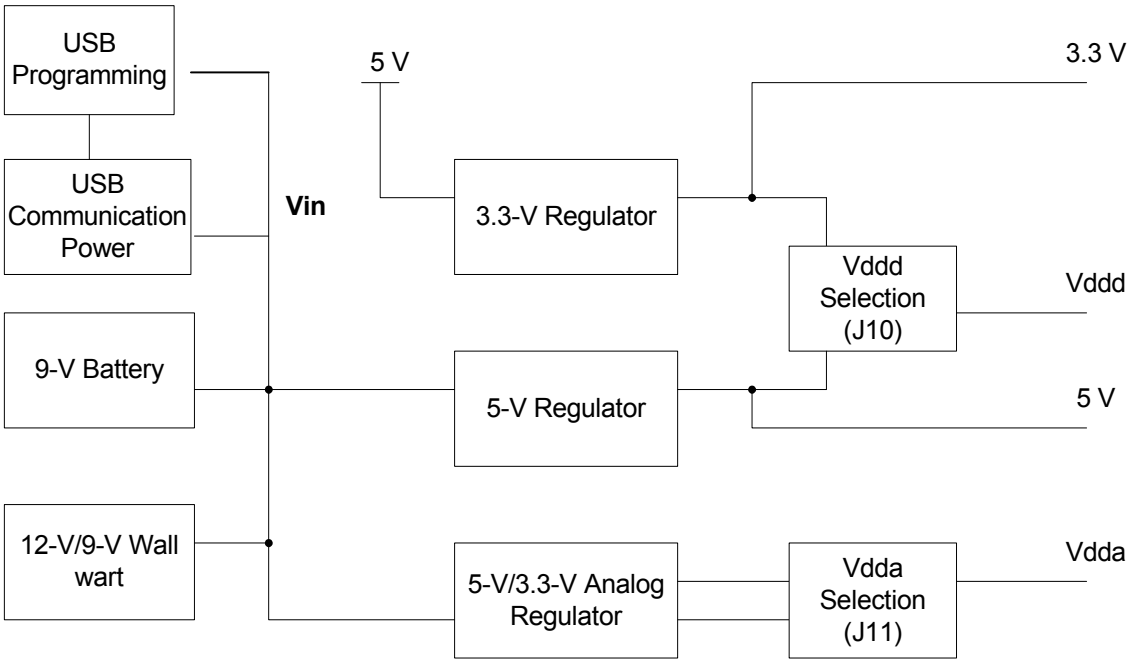
- 9-V or 12-V wall wart supply using connector J4
- 9-V battery connector using connectors BH1 and BH2
- USB power from communications section using connector J2
- USB power from the onboard programming section using connector J1
- Power from JTAG/SWD programming interface using connector J3
- Power through boost convertor that uses the input test points VBAT and GND

The board power domain has five rails:

- **Vin rail**: This is where the input of the onboard regulators are connected. This domain is powered through protection diodes.
- **5-V rail**: This is the output of the 5-V regulator U2. The rail has a fixed 5-V output regardless of jumper settings. The voltage in this rail can be less than 5 V only when the board is powered by the USB. This 5-V rail powers the circuits that require fixed 5-V supply.
- **3.3-V rail**: This is the output of the 3.3-V regulator U4. This rail remains 3.3 V regardless of jumper settings or power source changes. It powers the circuits requiring fixed 3.3-V supply such as the onboard programming section.
- **Vddd rail**: This rail provides power to the digital supply for the PSoC device. It can be derived from either the 5-V or 3.3-V rail. The selection is made using J10 (3-pin jumper).
- **Vdda rail**: This rail provides power to the analog supply of the PSoC device. It is the output of a low-noise regulator U1. The regulator is a variable output voltage and can be either 3.3 V or 5 V. This is done by changing the position on J11 (3-pin jumper).

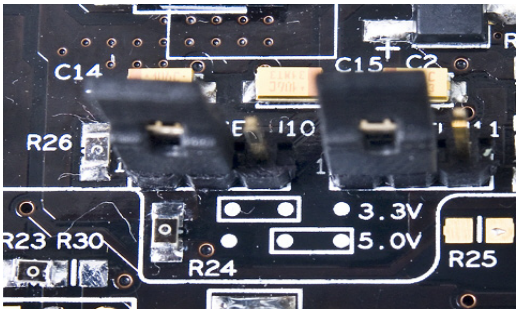
The following block diagram shows the structure of the power system on the board.

Figure 4-2. Power System Structure




### 4.2.1.1 *Power Supply Jumper Settings*

Figure 4-3. Jumper Settings



Two jumpers govern the power rails on the board. J10 is responsible for the selection of Vddd (digital power) and J11 selects the VADJ of Vdda (analog power).

The jumper settings for each power scheme are as follows.

| Powering Scheme | Jumper Settings |
|---|---|
| Vdda = 5 V, Vddd = 5 V | J10 in 5-V setting and J11 in 5-V setting. |
| Vdda = 3.3 V, Vddd = 3.3 V | J10 in 3.3-V setting and J11 in 3.3-V setting. |
| Vdda = 5 V, Vddd = 3.3 V | J10 in 3.3-V setting and J11 in 5-V setting. |
| Vdda = 3.3 V, Vddd = 5 V | Can be achieved, but is an invalid condition because the PSoC 5LP silicon performance cannot be guaranteed. |

**Warning**:

- The PSoC device performance is guaranteed when Vdda is greater than or equal to Vddd. Failure to meet this condition can have implications on the silicon performance.
- When USB power is used, ensure a 3.3-V setting on both analog and digital supplies. This is because the 5-V rail of the USB power is not accurate and is not recommended.
- If separate analog and digital power supplies are used, the analog supply ramp rate may be slower than that of the digital supply. This may cause I/Os to be in an indeterminate state until the power supplies stabilize.

#### *4.2.1.2 Grounding Scheme*

The board design considers analog designs as major target applications. Therefore, the grounding scheme in the board is unique to ensure precision analog performance.

The board has three types of ground:

- GND - This is the universal ground where all the regulators are referred. Both Vssd and Vssa connect to this ground through a star connection.
- Vssd - This is the digital ground and covers the digital circuitry on the board, such as RS-232 and LCD.
- Vssa - This is the analog ground and covers the grounding for analog circuitry present on the board, such as the reference block.

When creating custom circuitry in the prototyping area provided on the board, remember to use the Vssa for the sensitive analog circuits and Vssd for the digital ones.

Port E on the board is the designated analog expansion connector. This connector brings out ports 0, 3, and 4, which are the best performing analog ports on PSoC 3 and PSoC 5 devices. Port E has two types of grounds. One is the analog ground (GND_A in the silkscreen, Vssa in the schematic), which connects directly to the analog ground on the board. The other ground, known as GND, is used for the digital and high-current circuitry on the expansion board. This differentiation on the connector grounds helps the expansion board designer to separate the analog and digital ground on any high-precision analog boards being designed for port E.

#### *4.2.1.3 Low-Power Functionality*

The kit also facilitates application development, which requires low power consumption. Low-power functions require a power measurement capability, also available in this kit.

The analog supply is connected to the device through the 0-Ω resistor (R23). By removing this resistor and connecting an ammeter in series using the test points, Vdda_p and Vdda, you can measure the analog power used by the system.

The digital supply can be monitored by removing the connection on jumper J10 and connecting an ammeter in place of the short. This allows to measure the digital power used by the system.

The board provides the ability to measure analog and digital power separately. To measure power at a single point, rather than at analog and digital separately, remove resistor R23 to disconnect the analog regulator from powering the Vdda and short Vdda and Vddd through R30. The net power can now be measured at jumper J10 similar to the digital power measurement. To switch repeatedly between R23 and R30, moving around the 0-Ω resistors can be discomforting. Hence, a J38 (unpopulated) is provided to populate a male 3-pin header and have a shorting jumper in the place of R23/R30.

While measuring device power, make the following changes in the board to avoid leakage through other components that are connected to the device power rails.

- Disconnect the RS-232 power by disconnecting R58. An additional jumper capability is available as J37 if you populate it with a 2-pin male header.
- Disconnect the potentiometer by disconnecting J30.
- Ground the boost pins if boost operation is not used by populating R1, R28, and R29. Also make sure R25 and R31 are not populated.

#### *4.2.1.4 AC/DC Adaptor Specifications*

Use adaptors with the following specifications:

- Input voltage: 100 to 240 VAC, 50 Hz to 60 Hz, 1A
- Output voltage: 12 VDC, 1A
- Power output: 12 W
- Polarization: Positive center
- Certification: CE certified

Some recommended part numbers include EPSA120100U-P5P-EJ (CUI Inc.) and LTE12W-S2 (Li Tone Electronics Co. Ltd).

#### *4.2.1.5 Battery Specifications*

Use batteries with the following specifications:

- Battery size: 6LR61 (9 V)
- Output voltage: 9 VDC
- Type: Non-rechargeable alkaline consumer batteries
- RoHS status: RoHS compliant
- Lead free status: Pb-free

Some recommended part numbers include 6LR61XWA/1SB (Panasonic), MN1604 (Duracell), and 6LR61 (Energizer).

### 4.2.2 Programming Interface

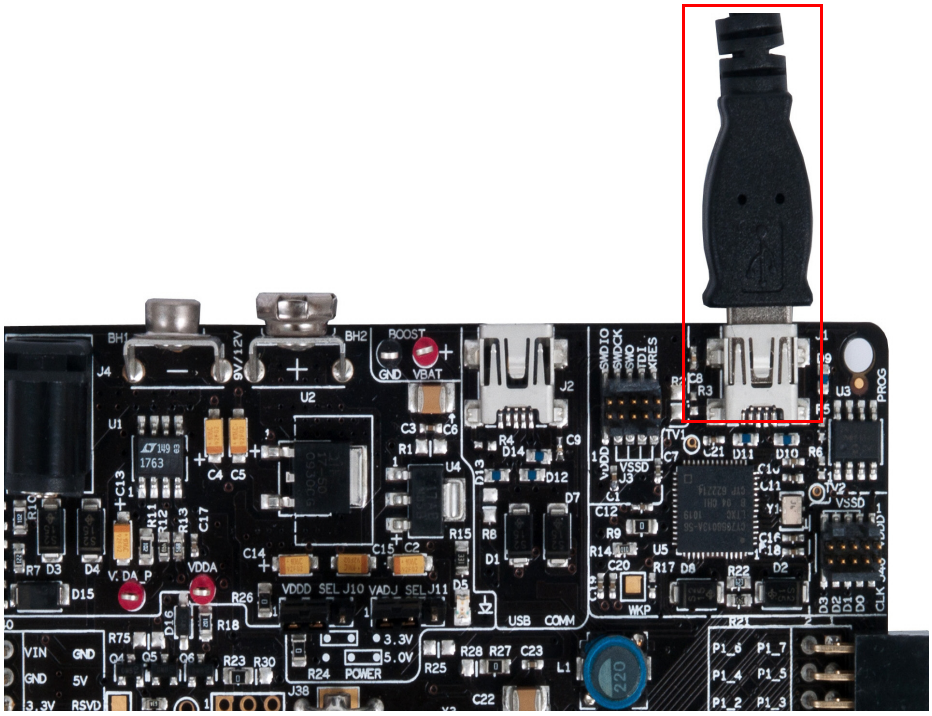
This kit allows programming in two modes:

- Using the onboard programming interface
- Using the JTAG/SWD programming interface with a MiniProg3

### 4.2.2.1 Onboard Programming Interface

The onboard programmer interfaces with your PC through a USB connector, as shown in Figure 4-4.

Figure 4-4. Onboard Programming Interface



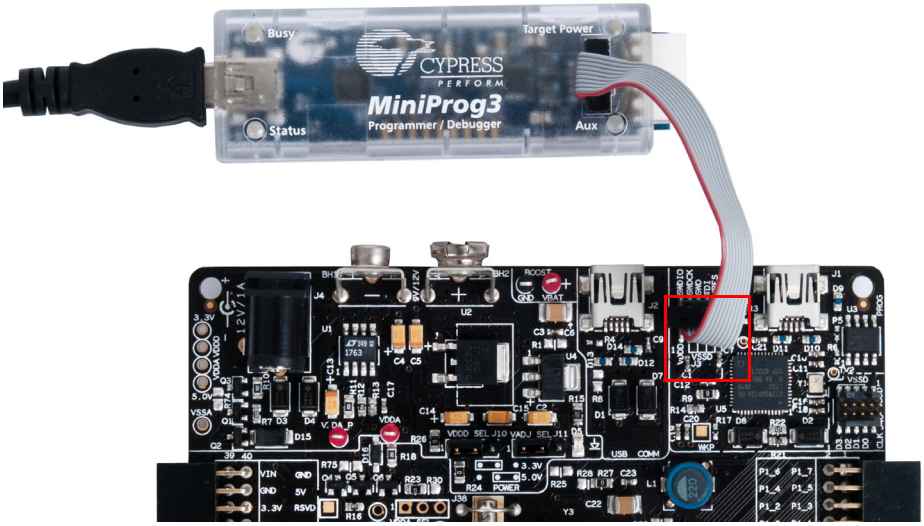

When the USB programming is plugged into the PC, it enumerates as DVKProg5 and you can use the normal programming interface from PSoC Creator to program this board through the onboard programmer.

A 0-Ω resistor R9 is provided on the board to disconnect power to the onboard programmer.

### 4.2.2.2 JTAG/SWD Programming

Apart from the onboard programming interface, the board also provides the option of using the MiniProg3. This interface is much faster than the onboard program interface. The JTAG/SWD programming is done through the 10-pin connector, J3.

Figure 4-5. JTAG/SWD Programming



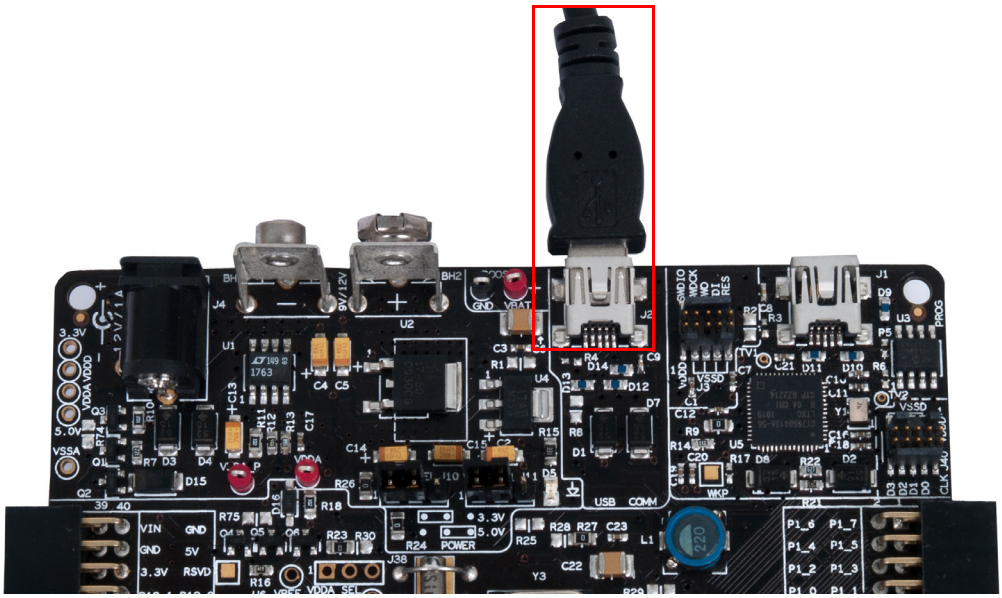

The JTAG/SWD programming using J3 requires the MiniProg3 programmer, which can be purchased from http://www.cypress.com/go/CY8CKIT-002.

**Note** While using MiniProg3, only the Reset mode is supported with this kit.

### 4.2.3 USB Communication

The board has a USB communications interface that uses the connector, as shown in Figure 4-6. The USB connector connects to the D+ and D– lines on the PSoC to enable development of USB applications using the board. This USB interface can also supply power to the board, as discussed in Power Supply on page 15.

Figure 4-6. USB Interface



### 4.2.4 Boost Convertor

The PSoC 5LP device has the unique capability of working from a voltage supply as low as 0.5 V. This is possible using the boost convertor. The boost convertor uses an external inductor and a diode. These components are prepopulated on the board. Figure 4-7 shows the boost convertor.

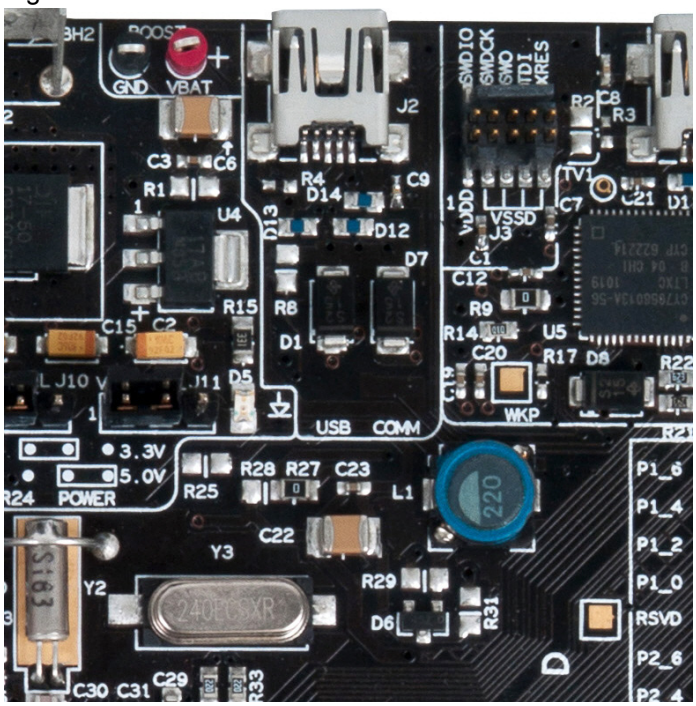
To enable the boost convertor functionality, make the following hardware changes on the board.

- Populate resistors R25, R27 (populated by default), R29, and R31 with 0-Ω resistors.

  **Note** See the Bill of Materials (BOM) on page 50 for the manufacturer part number.
- Ensure that R1 and R28 are not populated

After making these changes, you can configure the project to create a boost convertor-based design. The input power supply to the boost convertor must be provided through the test points marked Vbat and GND.

Figure 4-7. Boost Converter




### 4.2.5 32-kHz and 24-MHz Crystal

PSoC 5LP has an on-chip real time clock (RTC), which can function in sleep. This requires an external 32-kHz crystal, which is provided on the board to facilitate RTC-based designs. The PSoC 5LP also has an external MHz crystal option in applications where the IMO tolerance is not satisfactory. In these applications, the board has a 24-MHz crystal to provide an accurate main oscillator.

### 4.2.6 Protection Circuit

A reverse-voltage and over-voltage protection circuit is added to the expansion port on the 5-V and 3.3-V lines.

The protection circuit consists of two P-channel MOSFET on the power line, allowing the current to flow from input to output depending on the voltages applied at the external board connector. Figure 4-8 and Figure 4-9 are protection circuits placed between EBK and the onboard components on the 5-V and 3.3-V lines.

Figure 4-8. Schematic for Protection Circuit on 5-V Power Line

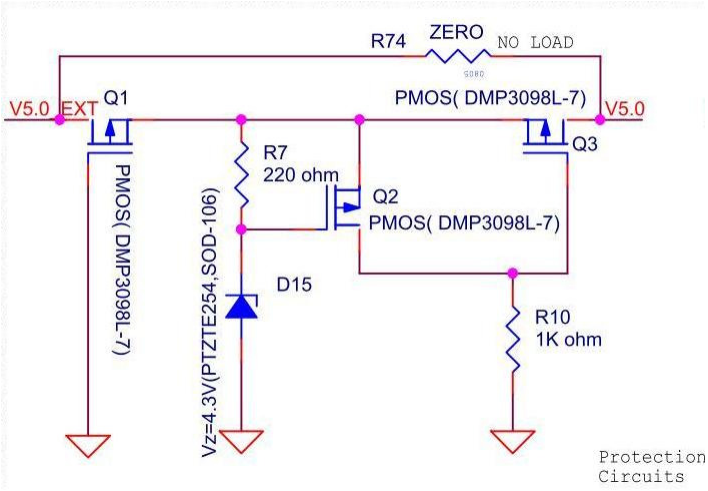
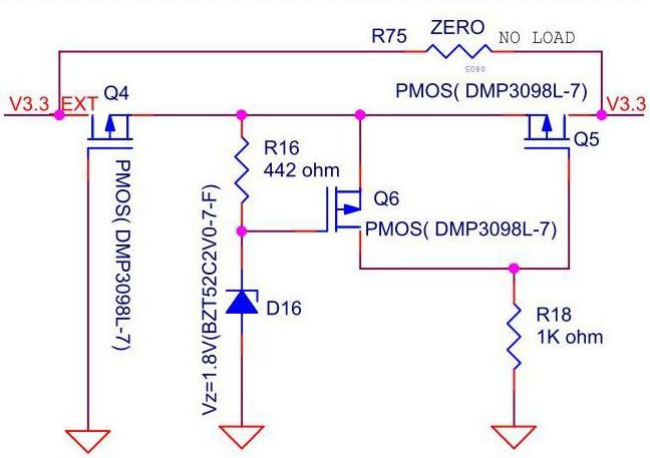



Figure 4-9. Schematic for Protection Circuit on 3.3-V Power Line




### 4.2.6.1 *Functional Description*

The protection circuit will protect from a maximum over-voltage or reverse-voltage of 12 V. The cut-off voltage on the 5-V line is 5.7 V and on the 3.3-V line is 3.6 V. This means, if you apply more than this voltage level from the external board connector side, the p-MOS Q5 will turn off, thus protecting PSoC and other onboard components. The current consumption of these protection circuits is less than 6 mA.

When voltage from the external connector is between 1.8 V and 3.3 V, the p-MOS Q4 conducts. Because the voltage across R16 is less than the threshold voltage (Vth) of p-MOS Q6, it will turn off and the p-MOS Q5 conducts, allowing voltage supply to the DVK.

When the external power supply exceeds 3.3 V, the p-MOS Q5 starts conducting. This eventually turns off p-MOS Q6 at 3.6 V, protecting the DVK from over-voltage.

When a reverse voltage is applied across the protection circuit from the external connector side, Q4 P-MOS will turn off, thus protecting the components on the board from reverse voltage.

If you are using the regulator power supply from the board to power the external modules, both the P-MOS Q4 and Q5 will always be in the On state, allowing the flow of current with a maximum of 22 mV drop across the circuit when the current consumed by the external module is 150 mA.

**Note** The working of protection circuit on the 3.3-V and 5-V lines is as described. For the purpose of explanation, the annotation of 3.3-V protection circuitry (Figure 4-9) is used.

## 4.2.7 PSoC 5LP Development Kit Expansion Ports

The PSoC 5LP Development Kit has two expansion ports, port D and port E, each with their own unique features.

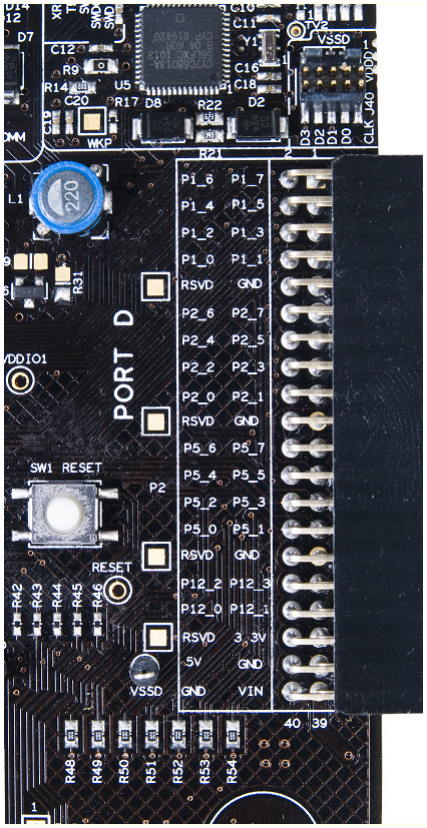
### *4.2.7.1 Port D*

This is the miscellaneous port designed to handle CapSense-based application boards and digital application boards. The signal routing to this port adheres to the stringent requirements needed to provide good performance CapSense. This port can also be used for other functions and expansion board kits (EBKs).

This port is not designed for precision analog performance. The pins on the port are functionally compatible to port B of the PSoC Development Kit. Any project made to function on port B of the PSoC Development Kit can be easily ported over to port D on this board. A caveat to this is that there is no opamp available on this port; therefore, opamp-based designs are not recommended for use on this port.

The following figure shows the pin mapping for the port.

Figure 4-10. Port D



### 4.2.7.2 Port E

This is the analog port on the kit and has special layout considerations. It also brings out all analog resources such as dedicated opamps to a single connect. Therefore, this port is ideal for precision analog design development. This port is functionally compatible to port A of the PSoC Development Kit and it is easy to port an application developed on port A.

This port has two types of grounds, CGND1 and CGND2. The two grounds are connected to the GND on the board, but are provided for expansion boards designed for analog performance. The expansion boards have an analog and digital ground. The two grounds on this port help to keep it distinct even on this board until it reaches the GND plane.

Figure 4-11. Port E