Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

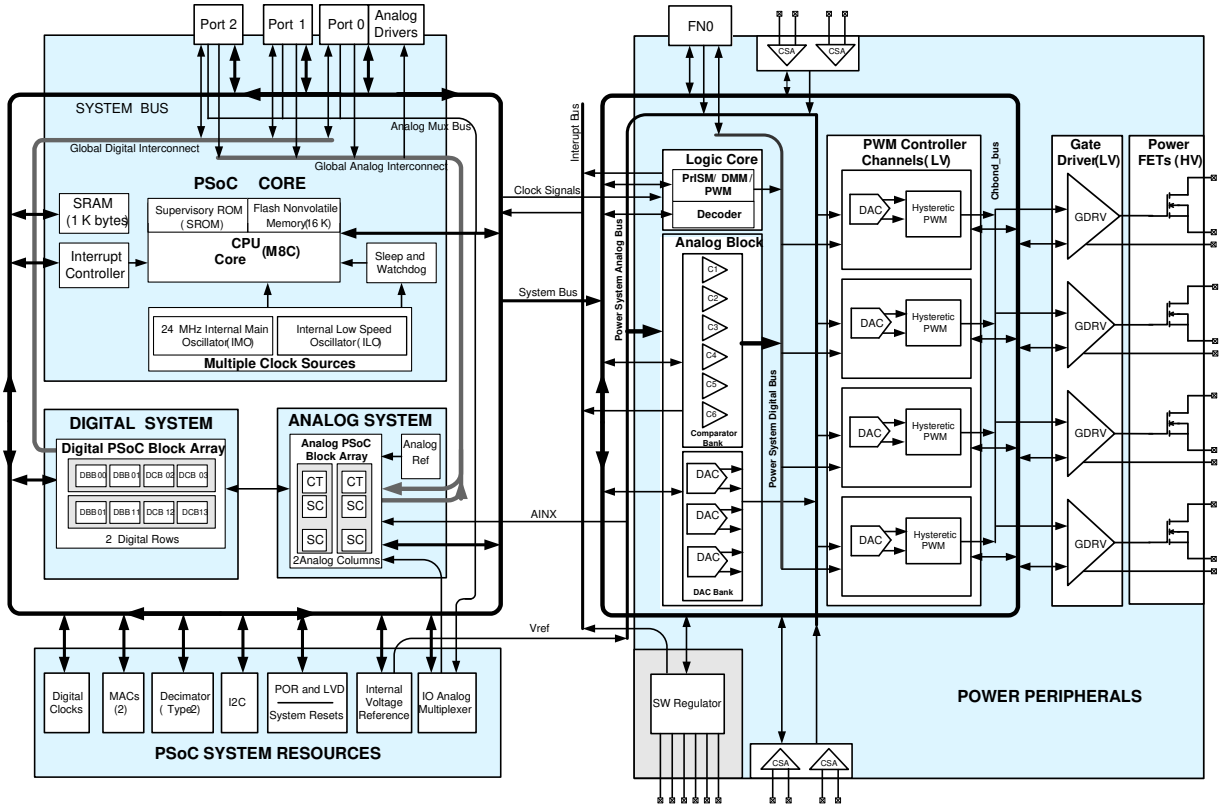
CY8CLED04D01/CY8CLED04D02/CY8CLED04G01
CY8CLED03D01/CY8CLED03D02/CY8CLED03G01
CY8CLED02D01/CY8CLED01D01

PowerPSoC® Intelligent LED Driver

1. Features

- **Integrated power peripherals**
  - Four internal 32 V low side N-Channel power FETs
    - $R_{DS(ON)}$ – 0.5 Ω for 1.0 A devices
    - Up to 2 MHz configurable switching frequency
  - Four hysteretic controllers
    - Independently programmable upper and lower thresholds
    - Programmable minimum ON/OFF timers
  - Four low side gate drivers with programmable drive strength
  - Four precision high side current sense amplifiers
  - Three 16-bit LED dimming modulators: PrISM, DMM, and PWM
  - Six fast response (100 ns) voltage comparators
  - Six 8-bit reference DACs
  - Built-in switching regulator eliminates external 5 V supply
  - Multiple topologies including floating load buck, floating load buck-boost, and boost
- **M8C CPU core**
  - Processor speeds up to 24 MHz
- **Advanced peripherals (PSoC® Blocks)**
  - Capacitive sensing application capability
  - DMX512 interface
  - I^2C master or slave
  - Full-duplex UARTs
  - Multiple SPI masters or slaves
  - Integrated temperature sensor
  - Up to 12-bit ADCs
  - 6 to 12-bit incremental ADCs
  - Up to 9-bit DACs
  - Programmable gain amplifiers
  - Programmable filters and comparators
  - 8 to 32-bit timers and counters
  - Complex peripherals by combining blocks
  - Configurable to all GPIO pins
- **Programmable pin configurations**
  - 25 mA sink, 10 mA source on all GPIO and function pins
  - Pull-up, pull-down, high Z, strong, or open drain drive modes on all GPIO and function pins
  - Up to 10 analog inputs on GPIO
  - Two 30 mA analog outputs on GPIO
  - Configurable interrupt on all GPIO
- **Flexible on-chip memory**
  - 16 K flash program storage 50,000 erase / write cycles
  - 1 K SRAM data storage
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- **Complete development tools**
  - Free development software (PSoC Designer™)
  - Full-featured, in-circuit emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- **Applications**
  - Stage LED lighting
  - Architectural LED lighting
  - General purpose LED lighting
  - Automotive and emergency vehicle LED lighting
  - Landscape LED lighting
  - Display LED lighting
  - Effects LED lighting
  - Signage LED lighting
- **Device options**
  - CY8CLED04D0x
    - Four internal FETs with 0.5 A and 1.0 A options
    - Four external gate drivers
  - CY8CLED04G01
    - Four external gate drivers
  - CY8CLED03D0x
    - Three internal FETs with 0.5 A and 1.0 A options
    - Three external gate drivers
  - CY8CLED03G01
    - Three external gate drivers
  - CY8CLED02D01
    - Two 1.0 A internal FETs
    - Two external gate drivers
  - CY8CLED01D01
    - One 1.0 A internal FET
    - One external gate driver
- **56-pin QFN package**

Figure 1-1. PowerPSoC Architectural Block Diagram



2. Contents

3. Logic Block Diagrams

Figure 3-1. CY8CLED04D0x Logic Block Diagram

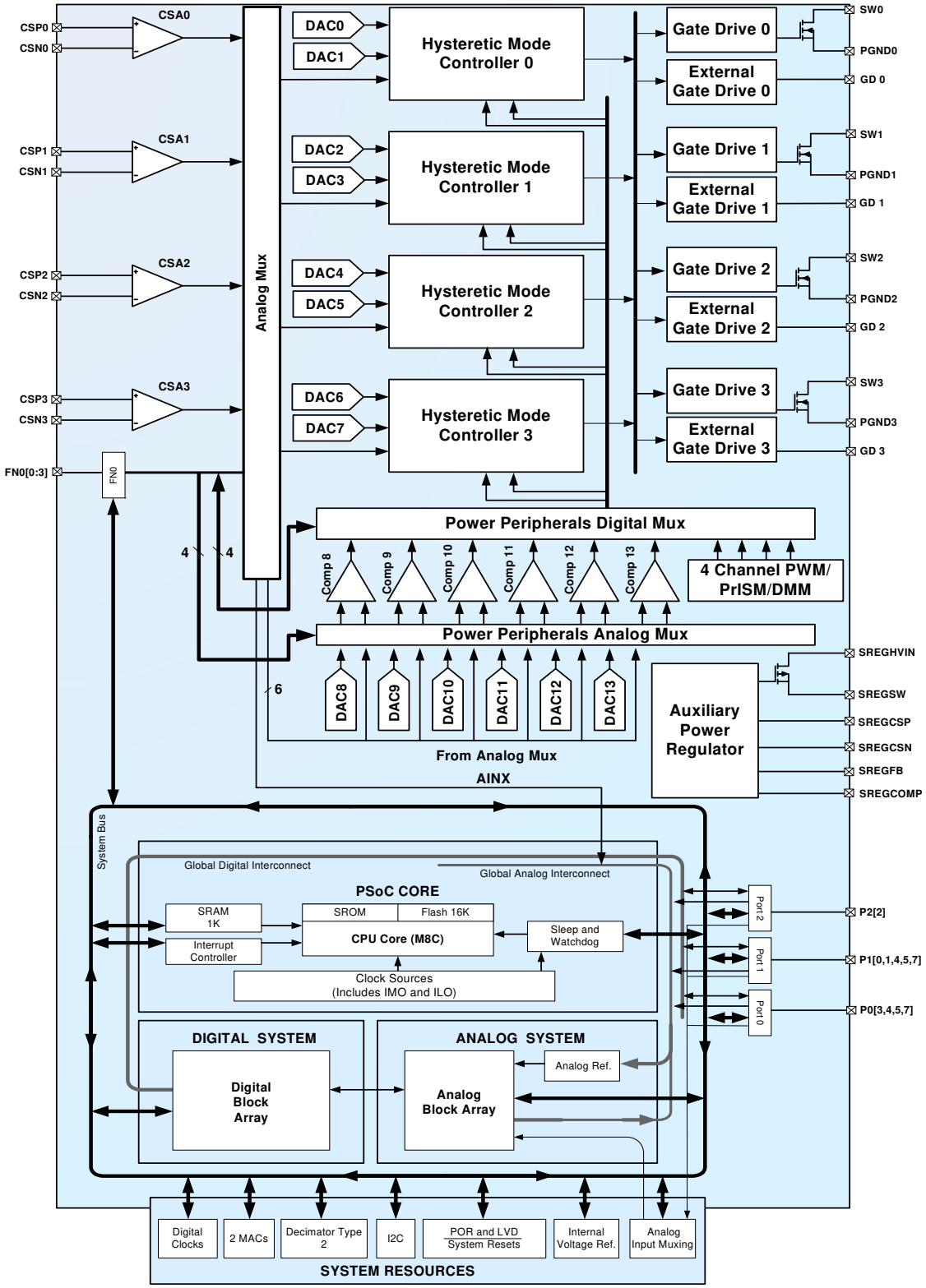


Figure 3-2. CY8CLED04G01 Logic Block Diagram

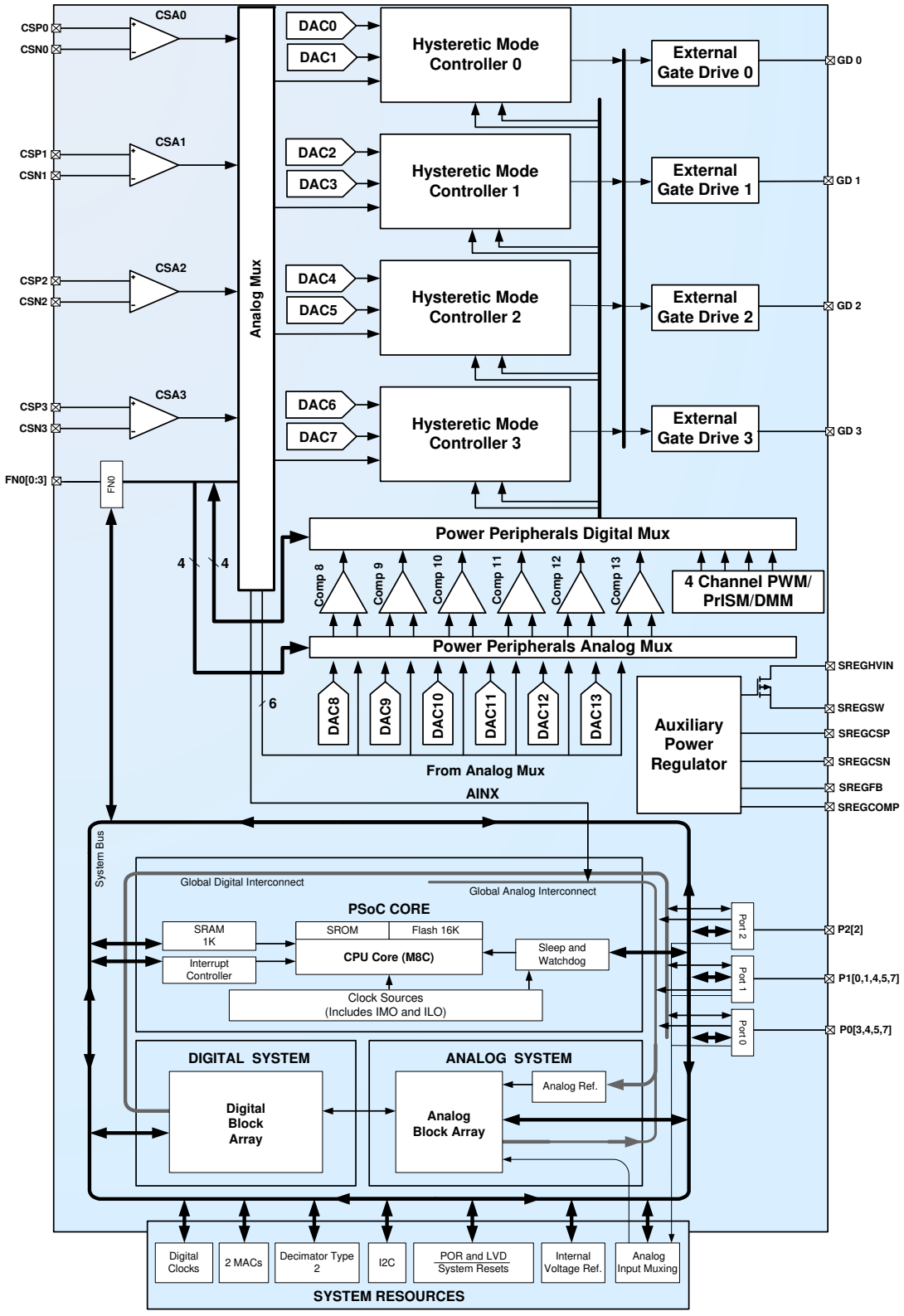


Figure 3-3. CY8CLED03D0x Logic Block Diagram

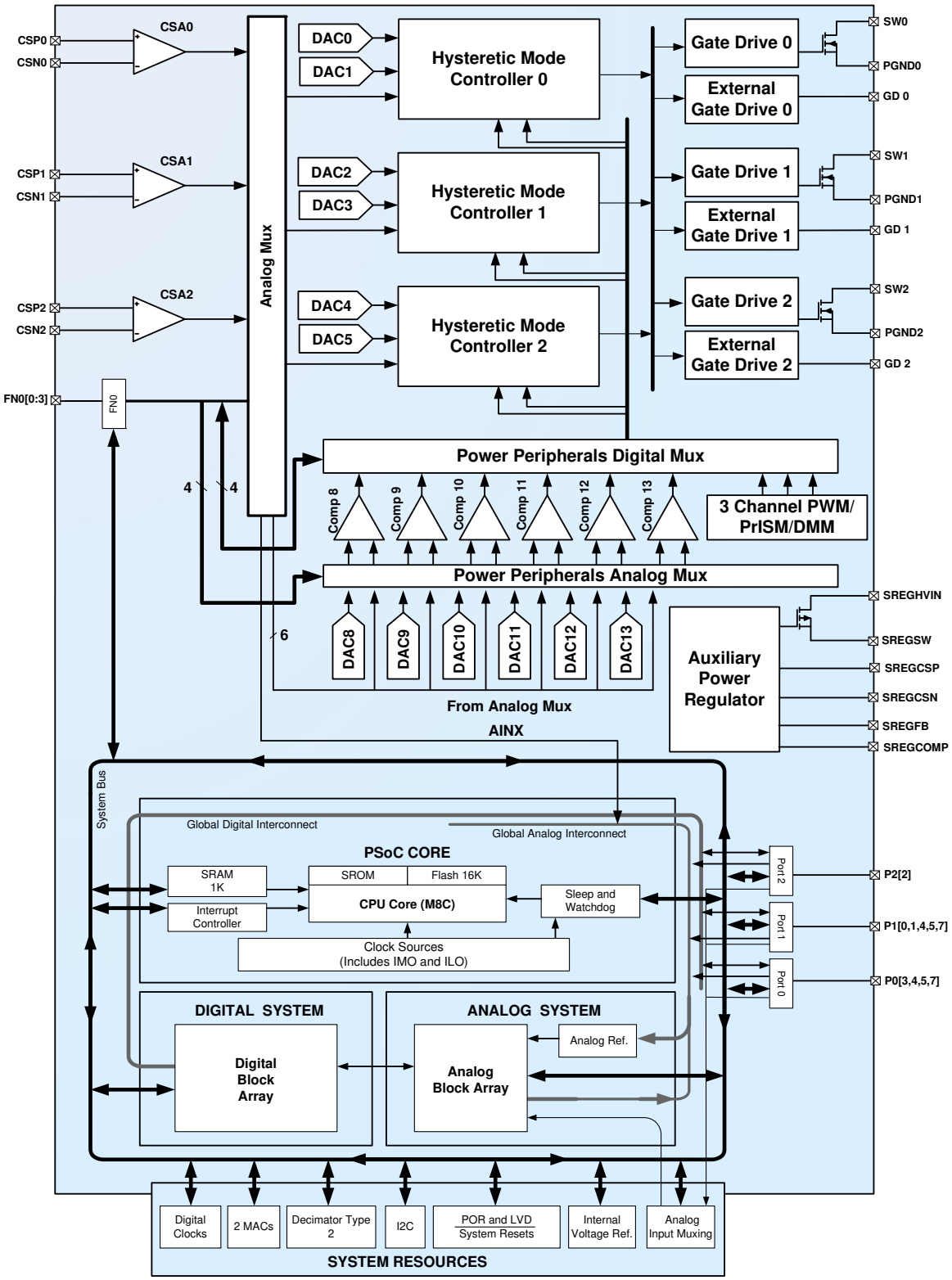


Figure 3-4. CY8CLED03G01 Logic Block Diagram

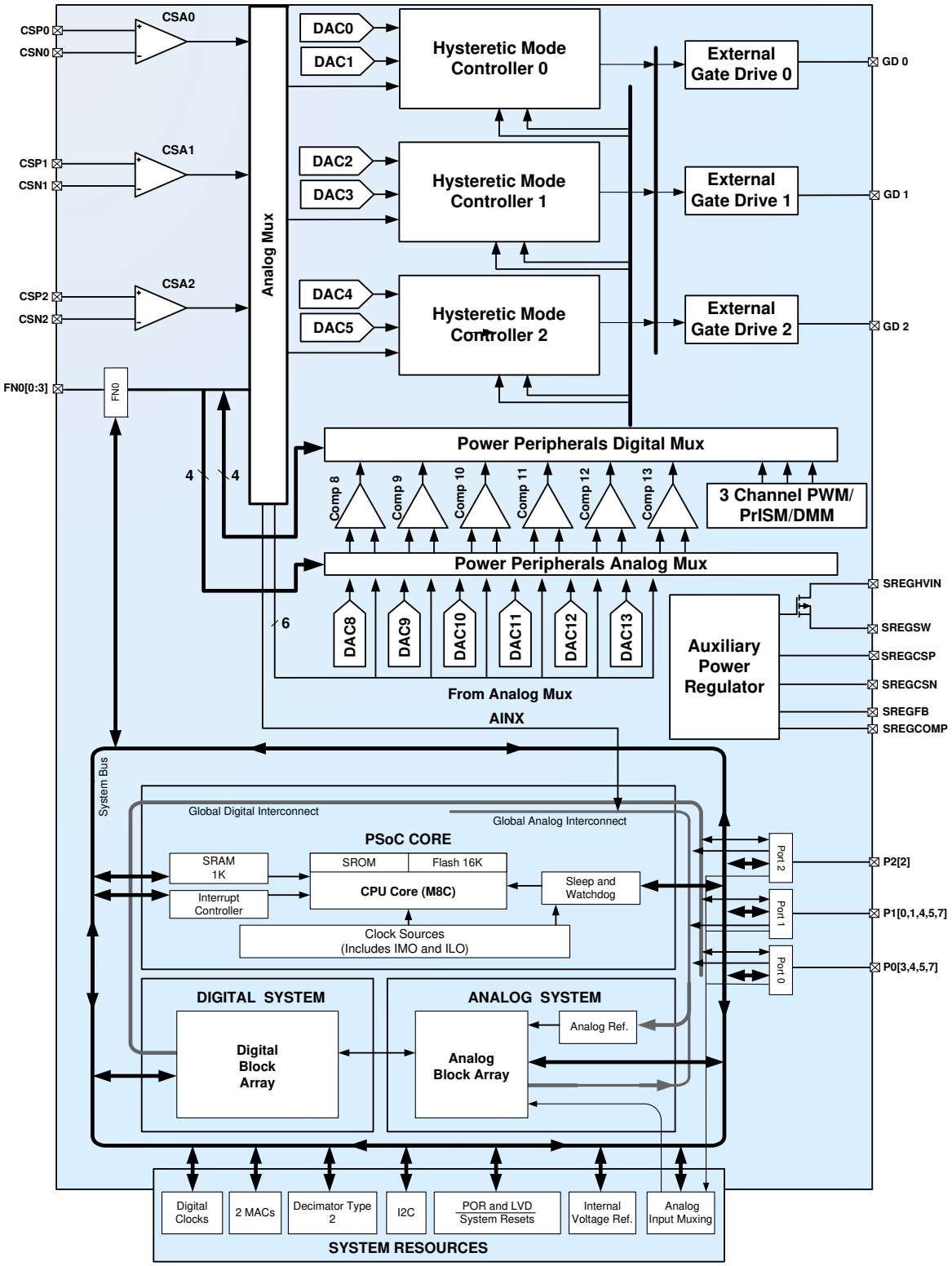


Figure 3-5. CY8CLED02D01 Logic Block Diagram

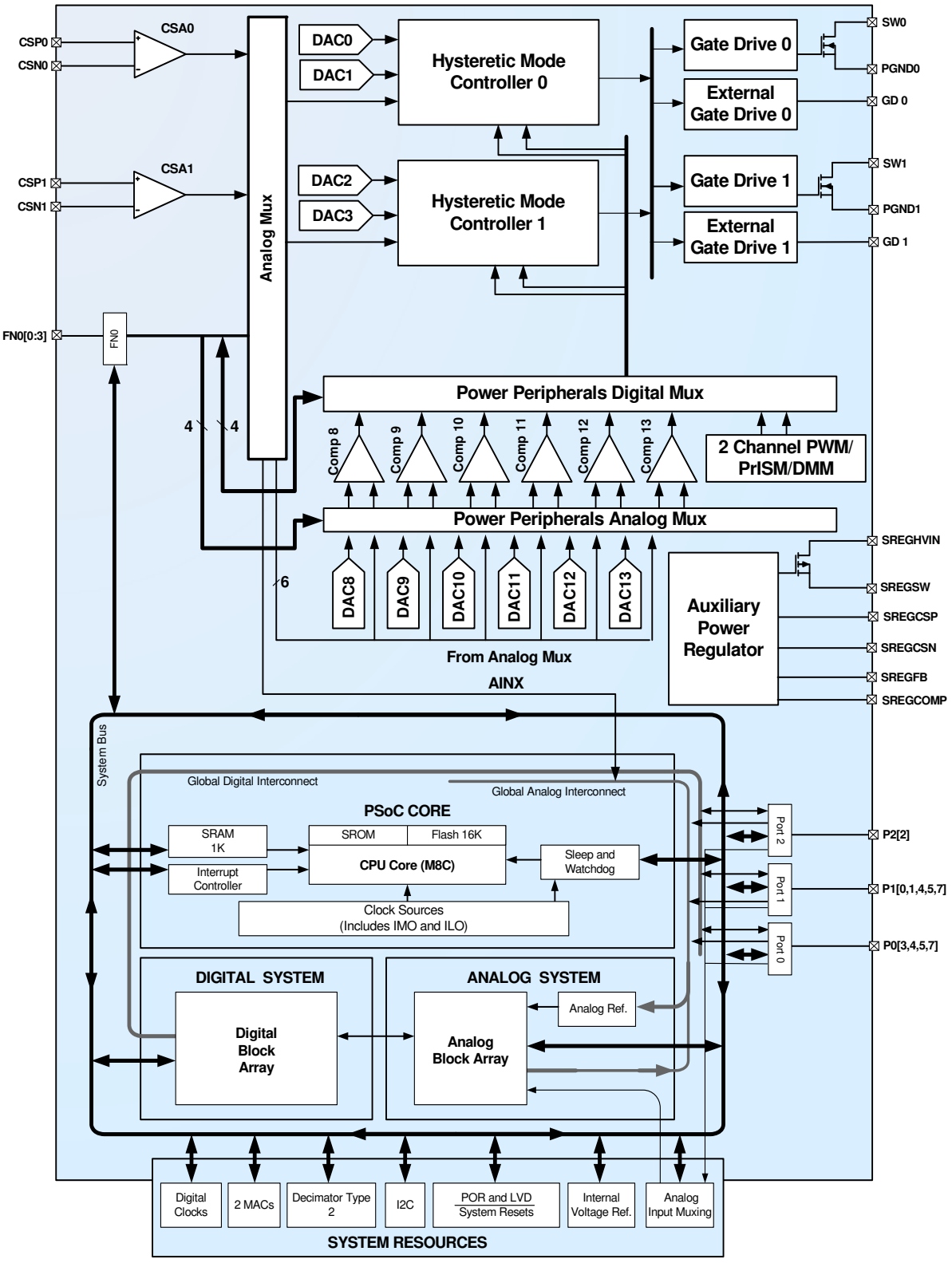
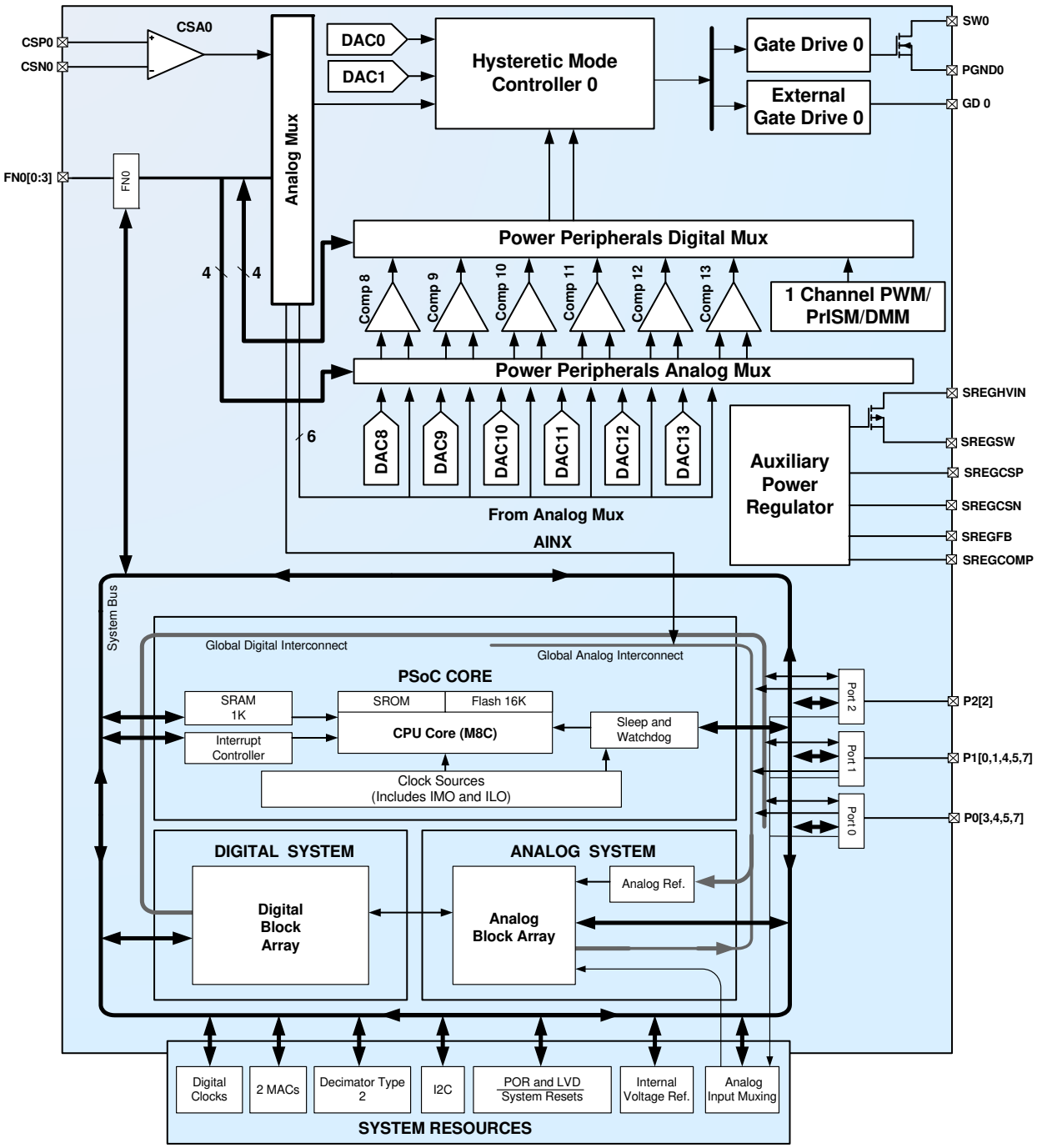


Figure 3-6. CY8CLED01D01 Logic Block Diagram



4. PowerPSoC® Functional Overview

The PowerPSoC family incorporates programmable system-on-chip technology with the best in class power electronics controllers and switching devices to create easy to use power-system-on-chip solutions for lighting applications.

All PowerPSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. PowerPSoC devices feature high performance power electronics including 1 ampere 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators to create a complete power electronics solution for LED power management. Configurable power, analog, digital, and interconnect circuitry enables a high level of integration in a host of industrial, commercial, and consumer LED lighting applications.

This architecture integrates programmable analog and digital blocks to enable you to create customized peripheral configurations that match the requirements of each individual application. Additionally, the device includes a 24 MHz CPU, Flash program memory, SRAM data memory, and configurable I/O in a range of convenient pinouts and packages.

The PowerPSoC architecture, as illustrated in the block diagrams, consists of five main areas: PSoC core, digital system, analog system, system resources, and power peripherals, which include power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. Configurable global busing combines all of the device resources into a complete custom system. The PowerPSoC family of devices have 10-port I/Os that connect to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

5. Power Peripherals

PowerPSoC is designed to operate at voltages from 7 V to 32 V, drive up to 1 ampere of current using internal MOSFET switches, and over 1 ampere with external MOSFETs.

This family of devices (CY8CLED0xD/G0y) combines up to four independent channels of constant current drivers. These drivers feature hysteretic controllers with the Programmable System-on-Chip (PSoC) that contains an 8-bit microcontroller, configurable digital and analog peripherals, and embedded flash memory.

The CY8CLED0xD/G0y is the first product in the PowerPSoC family to integrate power peripherals to add further integration for your power electronics applications.The PowerPSoC family of intelligent power controller ICs are used in lighting applications that need traditional MCUs and discrete power electronics support. The power peripherals of the CY8CLED0xD/G0y include up to four 32 volt power MOSFETs with current ratings up to 1 ampere each. It also integrates gate drivers that enable applications to drive external MOSFETs for higher current and voltage capabilities. The controller is a programmable threshold hysteretic controller, with user-selectable feedback paths that uses the IC in current mode floating load buck, floating load buck-boost, and boost configurations.

5.1 Hysteretic Controllers

The PowerPSoC contains four hysteretic controllers. There is one hysteretic controller for each channel of the device.

The hysteretic controllers provide cycle by cycle switch control with fast transient response, which simplifies system design by requiring no external compensation. The hysteretic controllers include the following key features:

- Four independent channels
- DAC configurable thresholds
- Wide switching frequency range from 20 kHz to 2 MHz
- Programmable minimum on and off time
- Floating load buck, floating load buck-boost and boost topology controller

The reference inputs (REF_A and REF_B in Figure 5-1.) of the hysteretic controller are provided by the reference DACs as illustrated in the top level block diagram (see Figure 3-1. on page 3).

The hysteretic control function output is generated by comparing the feedback value to two thresholds. Going below the lower threshold turns the switch ON and exceeding the upper threshold turns the switch OFF as shown in Figure 5-1. The output current waveforms are shown in Figure 5-2.

The hysteretic controller also controls the minimum on-time and off-time. This circuit prevents oscillation at very high frequencies; which can be very destructive to output switches.

The output to the gate drivers is gated by the Trip, DIM and Enable signals. The Enable signal is a direct result of the enable bit in the control register for the hysteretic controller.

The Trip signal can be any digital signal that follows TTL logic (logic high and logic low). It is an active high input.

The DIM Modulation signal is the output of the dedicated modulators that are present in the power peripherals, or any other digital modulation signal.

Figure 5-1. Generating Hysteretic Control Function Output

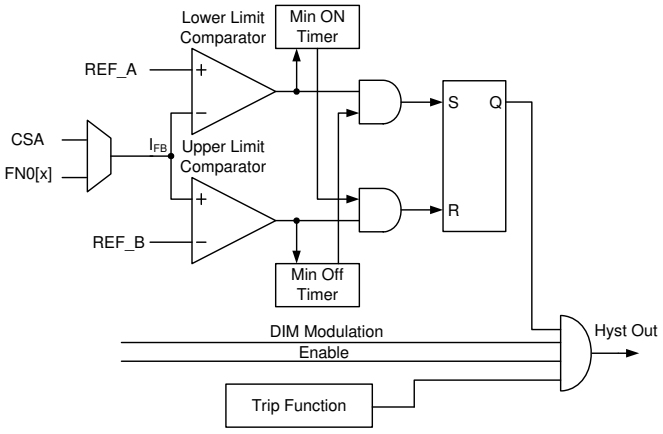
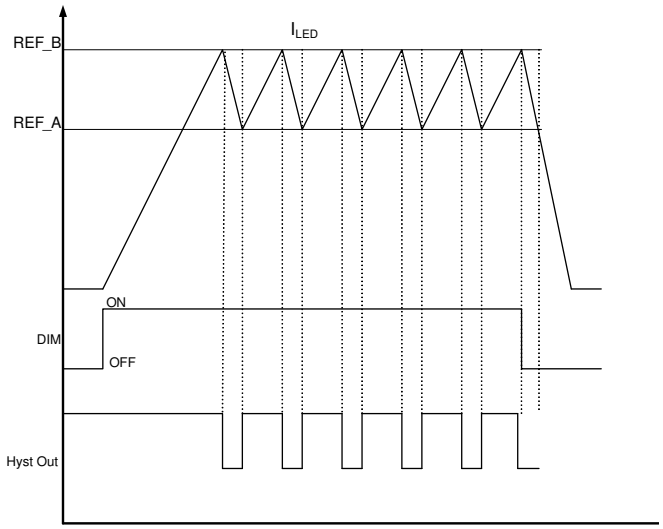


Figure 5-2. Current Waveforms



The minimum on-time and off-time circuits in the PowerPSoC prevent oscillations at very high frequencies, which can be very destructive to output switches.

5.2 Low Side N-Channel FETs

The internal low side N-Channel FETs are designed to enhance system integration. The low side N-Channel FETs include the following key features:

- Drive capability up to 1 A
- Switching times of 20 ns (rise and fall times) to ensure high efficiency (more than 90%)
- Drain source voltage rating 32 V
- Low $R_{DS(ON)}$ to ensure high efficiency
- Switching frequency up to 2 MHz

5.3 External Gate Drivers

These gate drivers enable the use of external FETs with higher current capabilities or lower $R_{DS(ON)}$. The external gate drivers directly drive MOSFETs that are used in switching applications. The gate driver provides multiple programmable drive strength steps to enable improved EMI management. The external gate drivers include the following key features:

- Programmable drive strength options (25%, 50%, 75%, 100%) for EMI management
- Rise and fall times at 55 ns with 4 nF load

5.4 Dimming Modulation Schemes

There are three dimming modulation schemes available with the PowerPSoC. The configurable modulation schemes are:

- Precise intensity signal modulation (PrISM)
- Delta Sigma modulation mode (DMM)
- Pulse-width modulation (PWM)

5.4.1 PrISM Mode Configuration

- High resolution operation up to 16 bits
- Dedicated PrISM module enables customers to use core PSoC digital blocks for other needs
- Clocking up to 48 MHz
- Selectable output signal density
- Reduced EMI

The PrISM mode compares the output of a pseudo-random counter with a signal density value. The comparator output asserts when the count value is less than or equal to the value in the signal density register.

5.4.2 DMM Mode Configuration

- High resolution operation up to 16 bits
- Configurable output frequency and delta sigma modulator width to trade off repeat rates versus resolution
- Dedicated DMM module enables customers to use PSoC digital blocks for other uses
- Clocking up to 48 MHz

The DMM modulator consists of a 12-bit PWM block and a 4-bit delta sigma modulator (DSM) block. The width of the PWM, the width of the DMM, and the clock defines the output frequency. The duty cycle of the PWM output is dithered by using the DSM block which has a user-selectable resolution up to 4 bits.

5.4.3 PWM Mode Configuration

- High resolution operation up to 16 bits
- User programmable period from 1 to 65535 clocks
- Dedicated PWM module enables customers to use core PSoC digital blocks for other use
- Interrupt on rising edge of the output or terminal count
- Precise PWM phase control to manage system current edges
- Phase synchronization among the four channels
- PWM output can be aligned to left, right, or center

The PWM features a down counter and a pulse width register. A comparator output is asserted when the count value is less than or equal to the value in the pulse width register.

5.5 Current Sense Amplifier

The high side current sense amplifiers provide a differential sense capability to sense the voltage across current sense resistors in lighting systems. The current sense amplifier includes the following key features:

- Operation with high common mode voltage to 32 V
- High common mode rejection ratio
- Programmable bandwidth to optimize system noise immunity

An off-chip resistor R_{sense} is used for high side current measurement as shown in Figure 5-3. on page 11. The output of the current sense amplifier goes to the power peripherals analog multiplexer where, you select the hysteretic controller to which

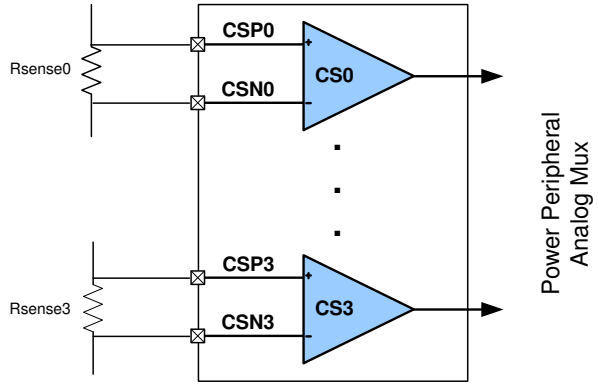
the routing is done. Table 5-1 illustrates example values of R_{sense} for different currents.

The method to calculate the R_{sense} value for a desired average current is explained in the application note CY8CLED0xx0x: Topology and Design Guide for Circuits using PowerPSoC - AN52699

Table 5-1. R_{sense} Values for Different Currents

Max Load Current (mA)	Typical R_{sense} (mΩ)
1000	100
750	130
500	200
350	300

Figure 5-3. High Side Current Measurement



5.6 Voltage Comparators

There are six comparators that provide high speed comparator operation for over voltage, over current, and various other system event detections. For example, the comparators may be used for zero crossing detection for an AC input line or monitoring total DC bus current. Programmable internal analog routing enables these comparators to monitor various analog signals. These comparators include the following key features:

- High speed comparator operation: 100 ns response time
- Programmable interrupt generation
- Low input offset voltage and input bias currents

Six precision voltage comparators are available. The differential positive and negative inputs of the comparators are routed from the analog multiplexer and the output goes to the digital multiplexer. A programmable inverter is used to select the output polarity. User-selectable hysteresis can be enabled or disabled to trade-off noise immunity versus comparator sensitivity.

5.7 Reference DACs

The reference DACs are used to generate set points for various analog modules such as Hysteretic controllers and comparators. The reference DACs include the following key features:

- 8-bit resolution
- Guaranteed monotonic operation
- Low gain errors
- 10 us settling time

These DACs are available to provide programmable references for the various analog and comparator functions and are controlled by memory mapped registers.

DAC[0:7] are embedded in the hysteretic controllers and are required to set the upper and lower thresholds for channel 0 to 3.

DAC [8:13] are connected to the Power Peripherals Analog Multiplexer and provide programmable references to the comparator bank. These are used to set trip points which enable over voltage, over current, and other system event detection.

5.8 Built-in Switching Regulator

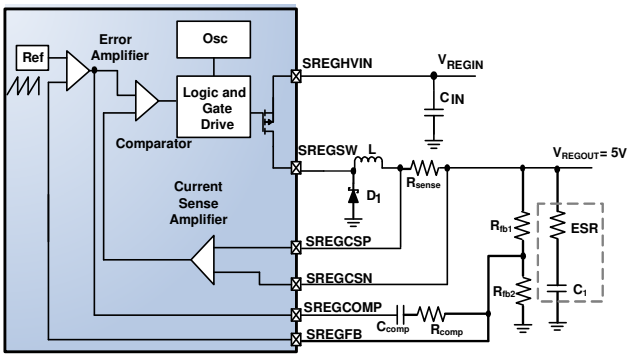
The switching regulator is used to power the low voltage (5 V portion of the PowerPSoC) from the input line. This regulator is based upon a peak current control loop which can support up to 250 mA of output current. The current not being consumed by PowerPSoC is used to power additional system peripherals. The key features of the built-in switching regulator include:

- Ability to self power device from input line
- Small filter component sizes
- Fast response to transients

Refer to Table 15-20 for component values.

The 'Ref' signal that forms the reference to the Error Amplifier is internally generated and there is no user control over it.

Figure 5-4. Built-in Switching Regulator



5.9 Analog Multiplexer

The PowerPSoC family's analog MUX is designed to route signals from the CSA output, function I/O pins and the DACs to comparator inputs and the current sense inputs of the hysteretic controllers. Additionally, CSA outputs can be routed to the AINX block using this MUX.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

The CPU configures the Power Peripherals Analog Multiplexer connections using memory mapped registers. The analog multiplexer includes the following key features:

- Signal integrity for minimum signal corruption

5.10 Digital Multiplexer

The PowerPSoC family's digital MUX is a configurable switching matrix that connects the power peripheral digital resources.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

This power peripheral digital multiplexer is independent of the main PSoC digital buses or global interconnect of the PSoC core. The digital multiplexer includes the following key features:

- Connect signals to ensure needed flexibility

5.11 Function Pins (FN0[0:3])

The function I/O pins are a set of dedicated control pins used to perform system level functions with the power peripheral blocks of the PowerPSoC. These pins are dynamically configurable, enabling them to perform a multitude of input and output functions. These I/Os have direct access to the input and output of the voltage comparators, input of the hysteretic controller, and output of the digital PWM blocks for the device. The function I/O pins are register mapped. The microcontroller can control and read the state of these pins and the interrupt function.

Some of the key system benefits of the function I/O are:

- Enabling an external higher voltage current-sense amplifier as shown in Figure 5-5.
- Synchronizing dimming of multiple PowerPSoC controllers as shown in Figure 5-6.
- Programmable fail-safe monitor and dedicated shutdown of hysteretic controller as shown in Figure 5-7.

Along with the these functions, these I/Os also provide interrupt functionality, enabling intelligent system responses to power control lighting system status.

Figure 5-5. External CSA and FET Application

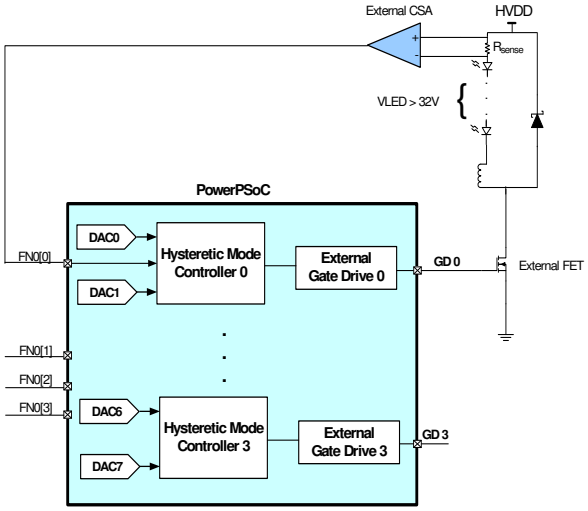


Figure 5-6. PowerPSoC in Master/Slave Configuration

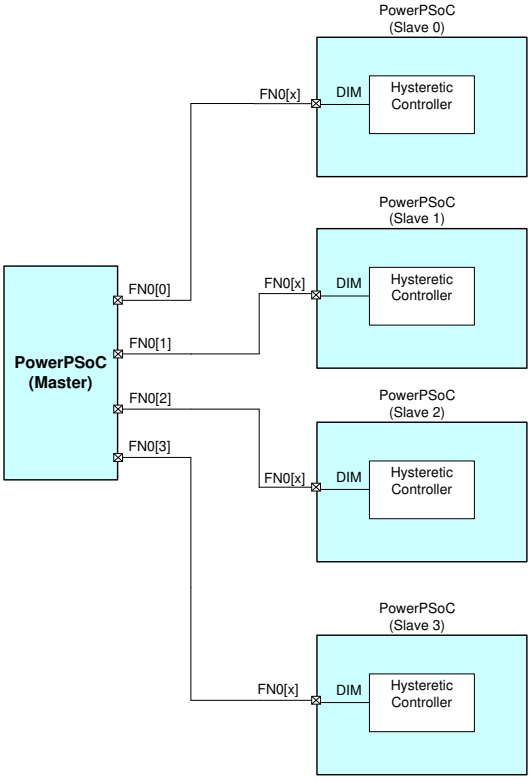
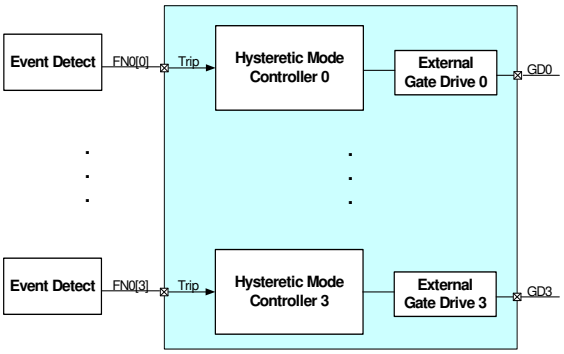


Figure 5-7. Event Detection



6. PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general purpose I/O(GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors to simplify programming of real time embedded events. The program execution is timed and protected using the included sleep and watchdog timers (WDT) time and protect program execution.

Memory encompasses 16 K of flash for program storage, 1 K of SRAM for data storage, and up to 2 K of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 4 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PowerPSoC device.

PowerPSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

6.1 Digital System

The digital system contains eight digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Digital peripheral configurations include:

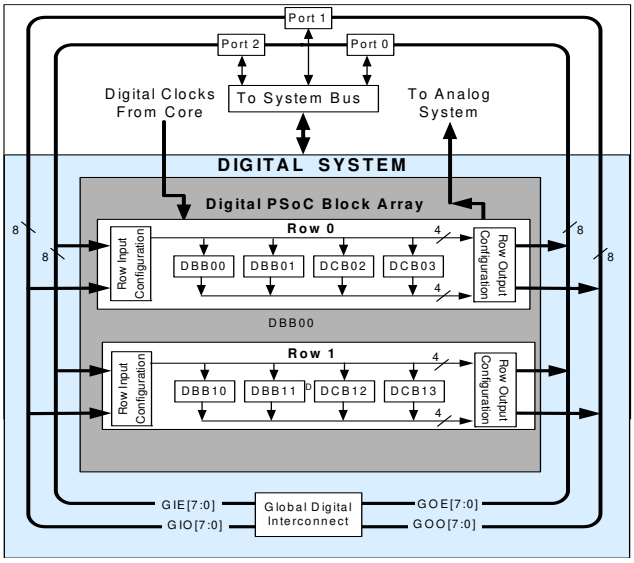
- DMX512
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C master, slave, and multi-master
- Cyclical redundancy checker/generator (8 to 32 bit)
- IrDA
- Pseudo random sequence generators (8 to 32 bit)

Note The DALI interface is supported through the use of a combination of the above mentioned user modules. For more details on the exact configuration and an example project, refer to the application note, PowerPSoC Firmware Design Guidelines, Lighting Control Interfaces - AN51012.

The digital blocks can be connected to any GPIO through a series of global buses that route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

There are four digital blocks in each row. This allows optimum choice of system resources for your application.

Figure 6-1. Digital System Block Diagram



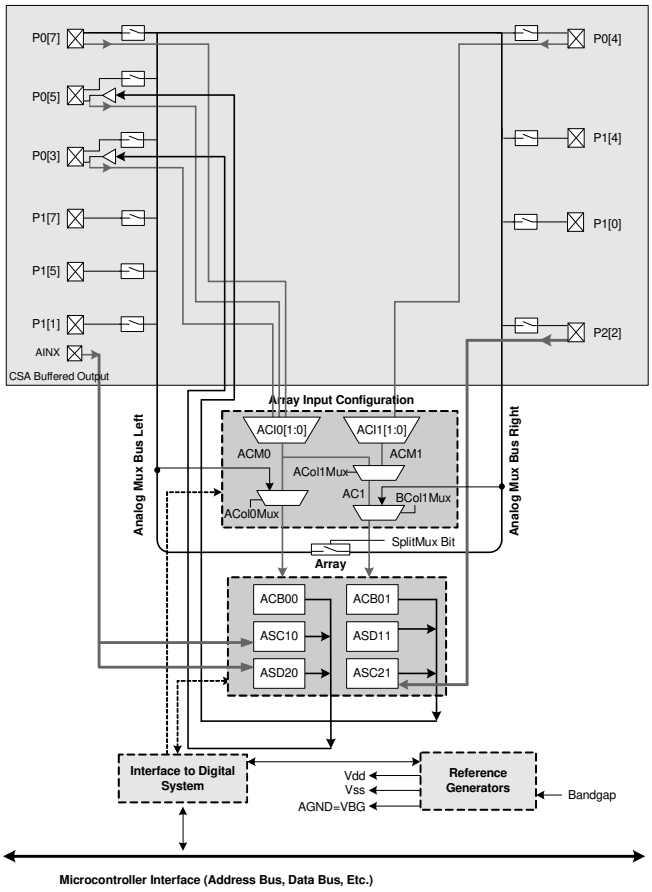
6.2 Analog System

The analog system contains six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PowerPSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to 2, with 6 to 12-bit resolution, selectable as incremental, Delta Sigma, and SAR)
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to 2, with 16 selectable thresholds)
- DACs (up to 2, with 6 to 9-bit resolution)
- Multiplying DACs (up to 2, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3 V reference (as a system resource)
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in two columns of three blocks each, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 6-2. on page 14.

Figure 6-2. Analog System Block Diagram



6.3 Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin in ports 0 to 2. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Crosspoint connection between any I/O pin combinations

Like other PSoC devices, PowerPSoC has specific pins allocated to the reference capacitor (Ref Cap) and modulation resistor (Mod resistor). These are indicated in the device pinouts (Section 13). For more details on capacitive sensing, see the design guide, Getting Started With CapSense. Apart from these, there are a number of application notes on Capacitive Sensing on the Cypress webbiest. The PowerPSoC Technical Reference Manual provides details on the analog system configuration that enables all I/Os in the device to be CapSense inputs.

6.4 Additional System Resources

System resources provide additional capability useful in complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- A decimator provides a custom hardware filter for digital signal processing applications including creation of delta sigma ADCs.
- Low-voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. The designer can generate additional clocks using digital PSoC blocks as clock dividers.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master applications are supported.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

7. Applications

The PowerPSoC family of devices can be used to add hysteretic current control capability to power applications. The devices can be used to control current in devices such as LEDs, heating elements, and solenoids. For LED applications, all high-brightness LEDs (HBLEDs) can be controlled using the PowerPSoC. The following figures show examples of applications in which the PowerPSoC family of devices adds intelligent power control for power applications.

Figure 7-1. LED Lighting with RGGB Color Mixing Configured as Floating Load Buck Converter

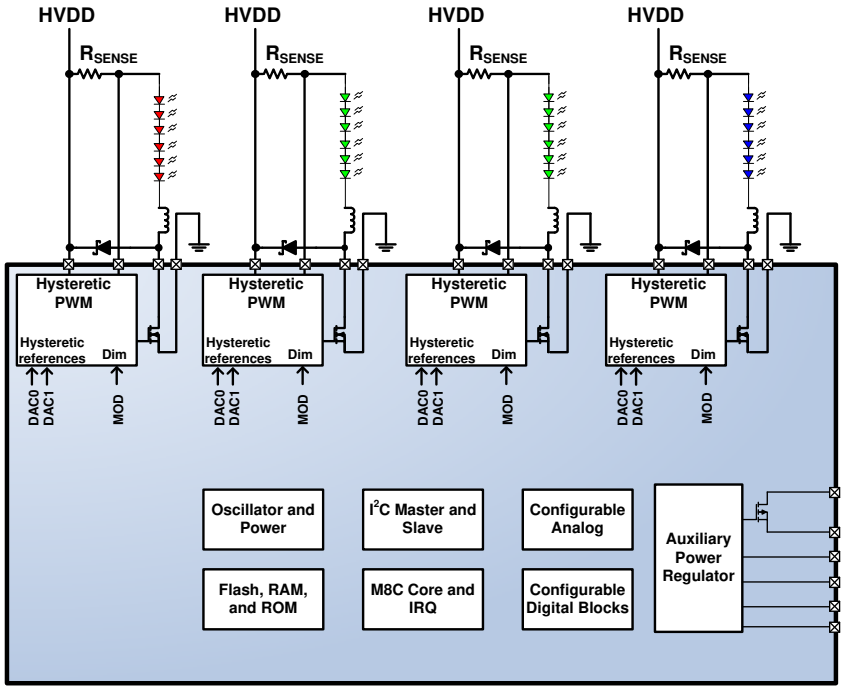


Figure 7-2. LED Lighting with RGBA Color Mixing Driving External MOSFETS as Floating Load Buck Converter

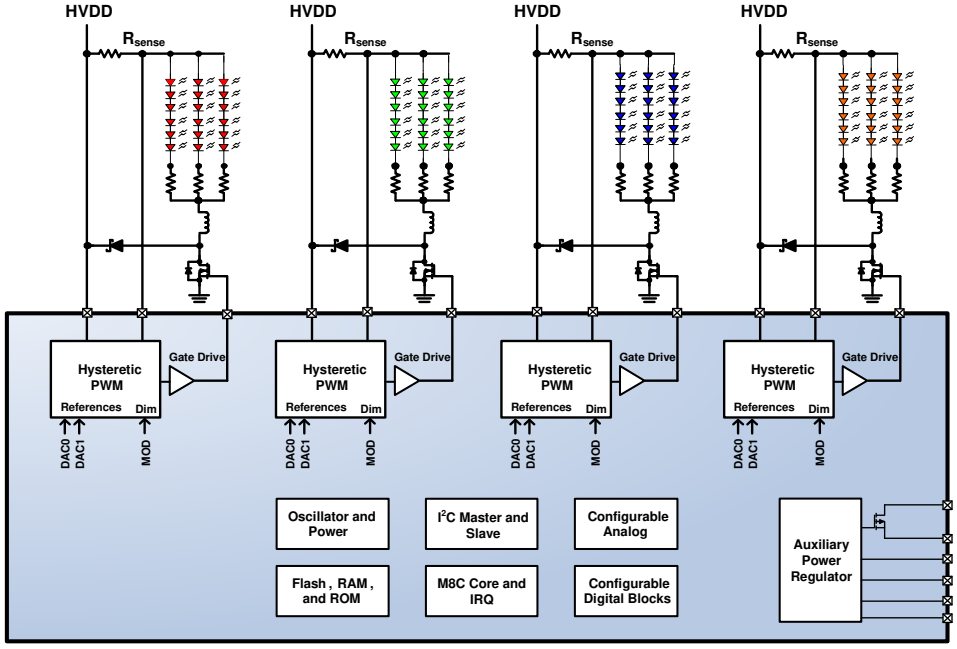
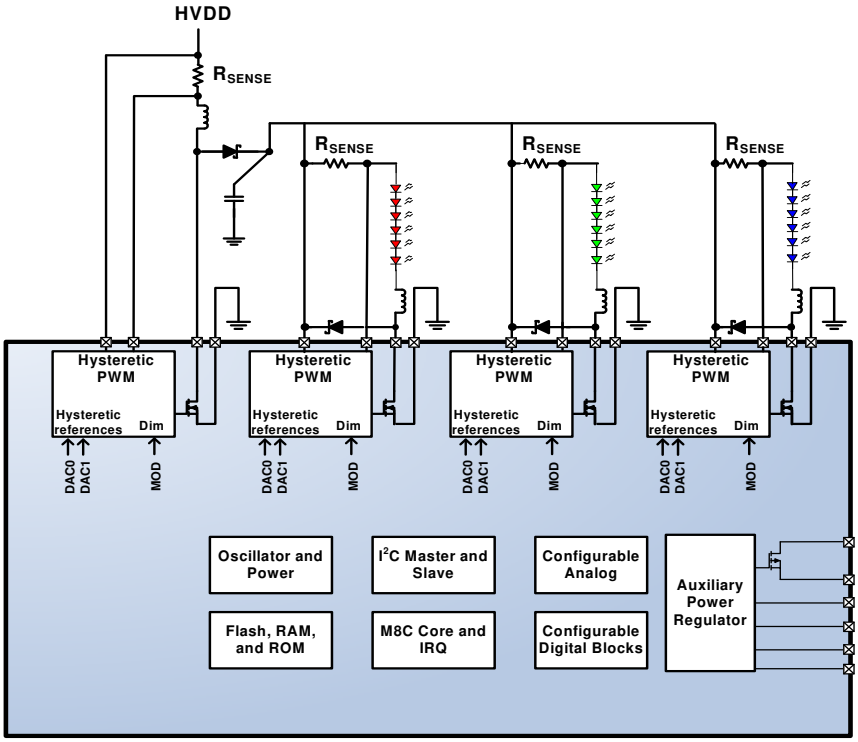


Figure 7-3. LED Lighting with a Single Channel Boost Driving Three Floating Load Buck Channels



8. PowerPSoC Device Characteristics

There are two major groups of devices in the PowerPSoC family. One group is a 4-channel 56-pin QFN and the other is a 3-channel 56-pin QFN. These are summarized in the following table.

Table 8-1. PowerPSoC Device Characteristics

Device Group	Internal Power FETs	External Gate Drivers	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8CLED04D01-56LTXI	4X1.0 A	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED04D02-56LTXI	4X0.5 A	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED04G01-56LTXI	0	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03D01-56LTXI	3X1.0 A	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03D02-56LTXI	3X0.5 A	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03G01-56LTXI	0	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED02D01-56LTXI	2X1.0 A	2	14	2	8	14	2	2	6	1 K	16 K
CY8CLED01D01-56LTXI	1X1.0 A	1	14	2	8	14	2	2	6	1 K	16 K
CY8CLED01D01-56LTXQ	1X1.0 A	1	14	2	8	14	2	2	6	1 K	16 K

9. Getting Started

The quickest way to understand the PowerPSoC device is to read this datasheet and then use the PSoC Designer integrated development environment (IDE). This datasheet is an overview of the PowerPSoC integrated circuit and presents specific pin, register, and electrical specifications. For in depth information, along with detailed programming information, refer to the *PowerPSoC Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PowerPSoC device datasheets on the web at www.cypress.com.

9.1 Application Notes

Application notes are an excellent introduction to a wide variety of possible PowerPSoC designs. Layout guidelines, thermal management and firmware design guidelines are some of the topics covered. To view the PowerPSoC application notes, go to htttp://www.cypress.com/powerpsoc and click on the Application Notes link.

9.2 Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PowerPSoC development. For more information on the kits or to purchase a kit from the Cypress web site, go to htttp://www.cypress.com/powerpsoc and click on the Development Kits link.

9.3 Training

Free PowerPSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

9.4 CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PowerPSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

9.5 Technical Support

PowerPSoC application engineers take pride in fast and accurate response. They can be reached with a 24-hour guaranteed response at http://www.cypress.com/support/. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

10. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP, Windows Vista, or Windows 7.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PowerPSoC family.

10.1 PSoC Designer Software Subsystems

10.1.1 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PowerPSoC blocks. Examples of user modules are current sense amplifiers, PrISM, PWM, DMM, Floating Load Buck, and Boost. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

10.1.2 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PowerPSoC family of devices. The products allow you to create complete C programs for the PowerPSoC family of devices.

The optimizing C compilers provide all the features of C tailored to the PowerPSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

10.1.3 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PowerPSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

10.1.4 Online Help System

The online help system displays online, context-sensitive help for you. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to faqs and an Online Support Forum to aid the designer in getting started.

10.2 In-Circuit Emulator

A low cost, high functionality in-circuit emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PowerPSoC devices.

11. Designing with User Modules

The development process for the PowerPSoC device differs from that of a traditional fixed function microprocessor. The configurable power, analog, and digital hardware blocks give the PowerPSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PowerPSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PowerPSOC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and connect
4. Generate, Verify and debug

Select Components. In the chip-level view the components are called “user modules”. User modules make selecting and implementing peripheral devices simple and come in power, analog, digital, and mixed signal varieties. The standard user module library contains over 50 common peripherals such as current sense amplifiers, PrISM, PWM, DMM, Floating Buck, Boost, ADCs, DACs, Timers, Counters, UARTs, and other not so common peripherals such as DTMF generators and Bi-Quad analog filter sections.

Configure Components. Each of the components selected establishes the basic register settings that implement the selected function. They also provide parameters allowing precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

The chip-level user modules are documented in datasheets that are viewed directly in PSoC Designer. These datasheets explain the internal operation of the component and provide performance specifications. Each datasheet describes the use of each user module parameter and other information needed to successfully implement your design.

Organize and Connect. Signal chains can be built at the chip level by interconnecting user modules to each other and the I/O pins. In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug. When ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high level user module API functions.

The chip-level designs generate software based on your design. The chip-level view provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows development and customization of your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

12. Pin Information

12.1 CY8CLED04D0x 56-Pin Part Pinout (without OCD)

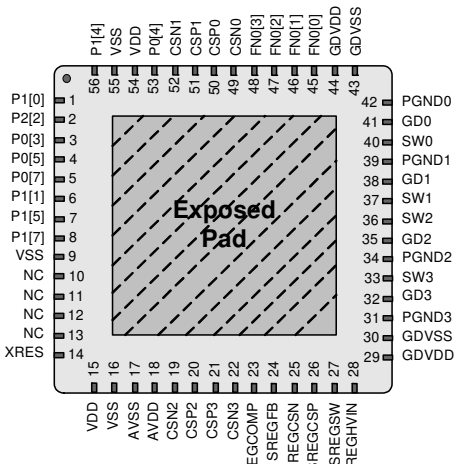
The CY8CLED04D01 and CY8CLED04D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-1. CY8CLED04D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[1]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				SW3	Power Switch 3
34				PGND2[1]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[1]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[1]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-1. CY8CLED04D0x 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Note
1. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.2 CY8CLED04G01 56-Pin Part Pinout (without OCD)

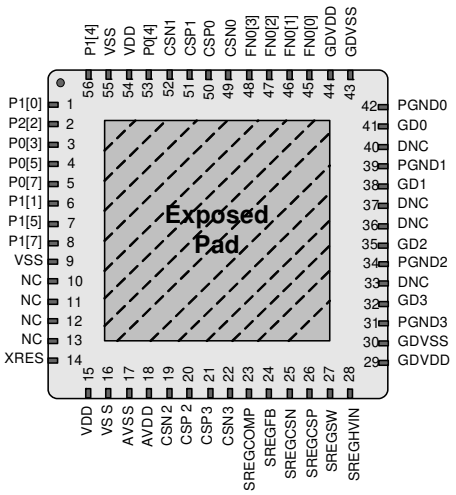
The CY8CLED04G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-2. CY8CLED04G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I²C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I²C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I²C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I²C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[3]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				DNC[2]	Do Not Connect
34				PGND2[3]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[2]	Do Not Connect
37				DNC[2]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[3]	Power FET Ground 1
40				DNC[2]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[3]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-2. CY8CLED04G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
2. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
3. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.3 CY8CLED04DOCD1 56-Pin Part Pinout (with OCD)

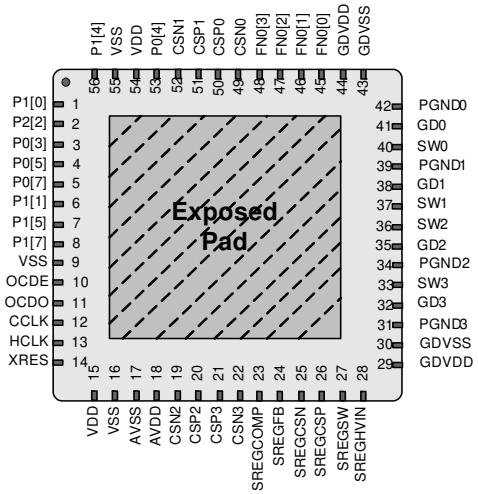
The CY8CLED04DOCD1 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-3. CY8CLED04DOCD1 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1) / Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10	I/O			OCDE	On Chip Debugger Port
11	I/O			OCDO	On Chip Debugger Port
12	I/O			CCLK	On Chip Debugger Port
13	I/O			HCLK	On Chip Debugger Port
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[4]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				SW3	Power Switch 3
34				PGND2[4]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[4]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[4]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-3. CY8CLED04DOCD1 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Note
4. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.4 CY8CLED03D0x 56-Pin Part Pinout (without OCD)

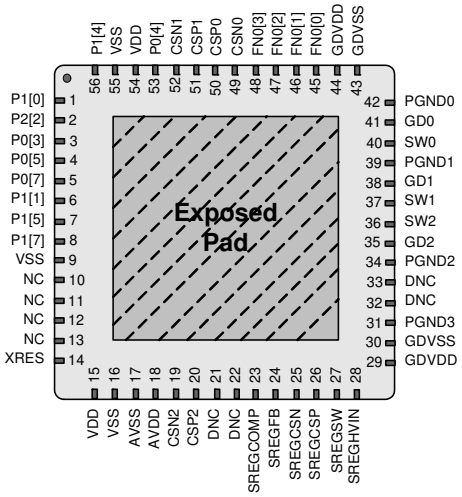
The CY8CLED03D01 and CY8CLED03D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-4. CY8CLED03D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[5]	Do Not Connect
22				DNC[5]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[6]	Power FET Ground 3
32				DNC[5]	Do Not Connect
33				DNC[5]	Do Not Connect
34				PGND2[6]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[6]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[6]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-4. CY8CLED03D0x 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Notes
5. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
6. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.5 CY8CLED03G01 56-Pin Part Pinout (without OCD)

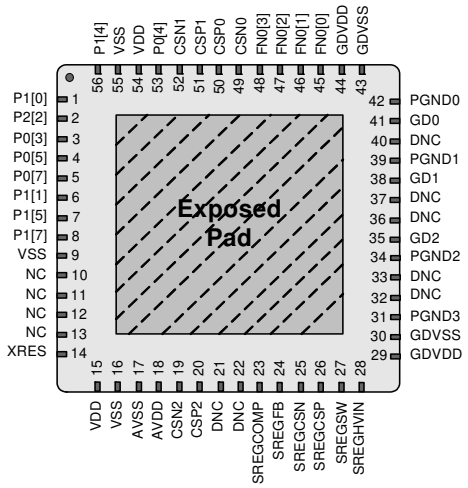
The CY8CLED03G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-5. CY8CLED03G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I²C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I²C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I²C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I²C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[7]	Do Not Connect
22				DNC[7]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[8]	Power FET Ground 3
32				DNC[7]	Do Not Connect
33				DNC[7]	Do Not Connect
34				PGND2[8]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[7]	Do Not Connect
37				DNC[7]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[8]	Power FET Ground 1
40				DNC[7]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[8]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-5. CY8CLED03G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
7. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
8. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

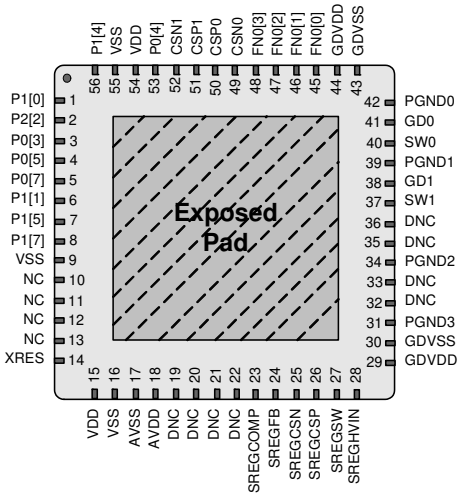
12.6 CY8CLED02D01 56-Pin Part Pinout (without OCD)

The CY8CLED02D01 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-6. CY8CLED02D01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19				DNC[9]	Do Not Connect
20				DNC[9]	Do Not Connect
21				DNC[9]	Do Not Connect
22				DNC[9]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[10]	Power FET Ground 3
32				DNC[9]	Do Not Connect
33				DNC[9]	Do Not Connect
34				PGND2[10]	Power FET Ground 2
35				DNC[9]	Do Not Connect
36				DNC[9]	Do Not Connect
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[10]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[10]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-6. CY8CLED02D01 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

Notes
9. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
10. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.