imall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832 Email & Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





CapSense[®] Express[™] Controllers with SmartSense[™] Auto-tuning - 16 Buttons, 2 Sliders, Proximity Sensors

General Description

The CY8CMBR3xxx CapSense[®] Express™ controllers enable advanced, yet easy-to-implement, capacitive touch sensing user interface solutions. This register-configurable family, which supports up to 16 capacitive sensing inputs, eliminates time-consuming firmware development. These controllers are ideal for implementing capacitive buttons, sliders, and proximity sensing solutions with minimal development-cvcle times.

The CY8CMBR3xxx family features an advanced analog sensing channel and the Capacitive Sigma Delta PLUS (CSD PLUS) sensing algorithm, which delivers a signal-to-noise ratio (SNR) of greater than 100:1 to ensure touch accuracy even in extremely noisy environments. These controllers are enabled with Cypress's SmartSense™ Auto-tuning algorithm, which compensates for manufacturing variations and dynamically monitors and maintains optimal sensor performance in all environmental conditions. In addition, SmartSense Auto-tuning enables a faster time-to-market by eliminating the time-consuming manual tuning efforts during development and production ramp-up.

Advanced features, such as LED brightness control, proximity sensing, and system diagnostics, save development time. These controllers enable robust liquid-tolerant designs by eliminating false touches due to mist, water droplets, or streaming water. The CY8CMBR3xxx controllers are offered in a variety of small form factor industry-standard packages.

The ecosystem for the CY8CMBR3xxx family includes development tools—software and hardware—to enable rapid user interface designs. For example, the EZ-Click Customizer tool is a simple graphical user interface software for configuring the device features through the I²C interface. This tool also supports CapSense data viewing to monitor system performance and support validation and debugging. Another tool, the Design Toolbox, simplifies circuit board layout by providing design guidelines and layout recommendations to optimize sensor size, trace lengths, and parasitic capacitance. To guickly evaluate the CY8CMBR3xxx family features, use the CY3280-MBR3 Evaluation Kit.

Features

- Register-configurable CapSense Express controller
 - No firmware development required
 - Patented CSD sensing algorithm
 - □ High sensitivity (0.1 pF)
 - Overlay thickness of up to 15 mm for glass and 5 mm for plastic
 - · Proximity solutions
 - · Sensitivity up to 2 fF per count
 - □ Best-in-class >100:1 SNR performance
 - · Superior noise-immunity performance against conducted and radiated noise
 - Ultra-low radiated emissions
 - SmartSense Auto-tuning
 - · Sets and maintains optimal sensor performance during run time
 - · Eliminates manual tuning during development and production
- Low-power CapSense
 - Average current consumption of 22 µA per sensor at 120-ms refresh interval
 - □ Wide parasitic capacitance (C_P) range: 5–45 pF
- Advanced user interface features
 - Liquid tolerance
 - User-configurable LED brightness for visual touch feedback Up to eight high-sink current GPOs to drive LEDs
 - Buzzer signal output for audible touch feedback

- □ Flanking Sensor Suppression (FSS) to eliminate false touches in closely spaced buttons
- Analog voltage output
- □ Attention line interrupt to the host to indicate any change in sensor status
- System diagnostics to detect
 - Improper value of the modulating capacitor (CMOD)
 - Out of range sensor parasitic capacitance (C_P)
- □ Sensor shorts
- EZ-Click[™] Customizer tool
 - Simple GUI for device configuration
 - Data viewing and monitoring for CapSense buttons, sliders, and proximity sensors
 - System diagnostics for rapid debug
- I²C slave
 - □ Supports up to 400 kHz
 - Wake-on-hardware address match
 - No bus-stalling or clock-stretching during transactions
- Low-power 1.71-V to 5.5-V operation
- Deep Sleep mode with wake-up on interrupt and I²C address detect
- Industrial temperature range: -40 °C to +85 °C
- Package options

8-pin SOIC (150 mil) □ 16-pin SOIC (150 mil) 16-pin QFN (3 × 3 × 0.6 mm) □ 24-pin QFN (4 × 4 × 0.6 mm)

Cypress Semiconductor Corporation Document Number: 001-85330 Rev. *N

198 Champion Court

San Jose, CA 95134-1709 •408-943-2600 Revised March 16, 2017



More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right CapSense device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: Refer to the "CapSense Selector Guide" chapter in the Getting Started with CapSense design guide.

CY8CMBR3xxx Ecosystem

Cypress provides a complete ecosystem to enable a quick development cycle with the CY8CMBR3xxx CapSense controller family. This ecosystem includes simple tools for device configuration, design validation, and diagnostics.

Documentation

Design Guides

eleo But Butt

Design guides are an excellent introduction to a variety of possible CapSense-based designs. They provide an introduction to the solution and complete system design guidelines. Refer to the following design guides for CY8CMBR3xxx:

- 1. Getting Started with CapSense an ideal starting point for all CapSense users
- 2. CY8CMBR3xxx CapSense Design Guide provides complete system design guidelines for CY8CMBR3xxx

You can download these design guides from our website: www.cypress.com/go/capsense.

Registers TRM

The CY8CMBR3xxx Registers TRM lists and details all the registers of the CY8CMBR3xxx family of controllers in order of their addresses. These registers may be accessed through an I^2C interface with the host.

Software Utility

EZ-Click Customizer Tool

The EZ-Click Customizer Tool is a simple, GUI-based software utility that can be used to customize the CY8CMBR3xxx device configurations.

Use this GUI-based tool to do the following:

- 1. Select the appropriate part number based on an end-application requirement using the Product Selector
- 2. Configure the device features
- 3. Observe CapSense data for button and proximity sensors
- 4. Use the System Diagnostics and built-in test self-test (BIST) features for debug and production-line testing

							Color mark hour	Start page	apSense sensor co	nfiguration G	lobal configuration	epSense output Syster	n diagnostics			
ce filters		Part number	Buttons Slider	s LEDs	Driven shields	Proximity sensors	Shield	Number of	liders:	0 -	I BR filter	I Automatic thresh	old Scan j	period (ms):	120	
2.84 	U +	🖶 CapSense Express						Number of	proximity sensors:	0 *	Median filter	Advanced low-pass	filter;	0		
ons:	0 .	CY8CM8R2oor	~									PET/35	20			500
	0	CV8CM8R2110 10	Ó	10 0	0	6	False	Buttons								
umity sensors:	0 *	CV8CM8R3xx		12 10	a la	07	Falce	Enable	Pin		Sensor	Sensitivity (IF)	Finger Threshold	FSS	Initial Response Time (ms)	Response Ti
		CVBCM6R3102 2	(1 1		6	True	10	CS0/P50 (1)	Buttonl		100 -	128		180	60
Univen shield		CV8CM6831065 11		0 1		en el composition de la compos	True	10	CSL/PSL (Z)	Button2		100 -	128	n	180	60
Buzzer drive		CV8CM683108_8	10	4			True		CS2/GUARD (7)	Button3		100 -	128	- D	140	63
Dimming effe		CV8CM8R3110 10	0	5 1			True	- 171	CSTIAL	Buttoni		1/00 *	128		160	60
naturning cirec		CV8CMBR3816 16	0	8 1	2	0.	True	101	C54.(20)	Buttons			178		180	60
Suard sensor		i contra contra						10	055.000	Rutton			24	-	180	65
LED intensity control				 	CS5 (18)	Button7			28	-	180	60				
					CS7.(17)	Buttonil			5.28		180	60				
				- 14	CS8/GP00/143	Battoni		100 -	128	m	180	60				
ne CanSen	se sensor confic	guration Global configurat	ion CapSense o	output System	m diagnostic	ne		- 201	C00/00/01/05	Eutton10		100 -	138		380	65
ie copoen.					1000			1.3	CSIN/GPO2 (LA)	Euthorit		100 -	128		180	60
Butt	on output	•	Displ	layed Samples	: 1000	-	Sample	11.7	C011/C000 (14)	Buttou 22		100	120	10	180	10
output									COLUCION (I)	Puttonia.		100	1.00		300	100
	BTN1	•	Button status:	Off		Sta	art 🕨	10	CETT/00004 (12)	Button15		100	116		180	60
threshold:	128		Cn (nE):	8	Graph	Signal +	o noise ratio	0 0 Errors	1 0 Warnings	0 Notes		A 517			2. AVC	
	L		-b. (b.),			orginal to		Description	the second s							
								- new second little								
								11/1/02/02/02/								
¹⁹								in her stand dates								
19 18	\frown							No target dev	ce selected							
19 18 17 16	\neg	\square (3				File Cor	No target dev	ce selected elp							
19 18 17 16 15	\neg	\square	3)				File Cor	No target dev ofiguration F	ce selected elp 🗗 📑 😭 🟈	Þ						
19 18 17 16 15 14	\square		3				File Cor	No target dev nfiguration H	ce selected elp P 🗟 🗎 🧼	tion Global	configuration CapS	ense output System	diagnostics			
19 18 17 16 15 14 13 12			3				File Cor	hin target dev nfiguration +	ce selected elp P 🕘 🛅 🛹 sensor configura	iion Global	configuration CapS	ense output System	diagnostics			
19 18 17 16 15 14 13 12 11			3				File Cor Start pag Test co	figuration I- Part CapSense onfiguration:	ce selected elp P 🗟 🖹 🗇	tion Global	configuration CapS	ense output System	diagnostics	1	Sto	p
19 18 17 16 15 14 13 12 11 10			3				File Cor Start pag Test co Test m	hin tamet dev nfiguration II CapSense ofiguration: ode:	elp Postorype	tion Global	configuration CapS alibrated Cp: 11	ense output System	diagnostics	1	Calculat	p
19 18 17 16 15 14 14 13 12 11 10 9 8			3				File Cor Start pag Test co Test m V Pov	hin tamet dev nfiguration H CapSense Infiguration: - ode: wer on self tes	elp P D D D D D D D D D D D D D D D D D D D	tion Global	configuration CapS alibrated Cp: 11 olerance: - 11	ense output System	diagnostics Calibrated SNR: Folerance: - 1	1	4 triangle Sto	p
19 18 17 16 15 14 13 12 11 10 9 8 7			3				File Cor Start pag Test co Test m V Por Cmo	nfiguration F CapSense infiguration: ode: wer on self test d test: No faul	es selected elp P D D P sensor configura Prototype ts detected	tion Global	configuration CapS alibrated Cp: 11 olerance: - 11 Shield not ens	ense output System	diagnostics Calibrated SNR: 'olerance: - 1	1	A total action of the second s	p
19 17 16 17 16 15 14 12 11 10 9 8 7 6			3				File Cor Start pag Test cc Test m Pov Cmo Sensor	nfiguration F CapSense infiguration: ode: wer on self test d test: No faul Status	ce selected elp P I I I I I I I I I I I I I I I I I I I	tion Global	configuration CapS alibrated Cp: 11 olerance: - 11 Shield not ens	ense output System	diagnostics Calibrated SNR: folerance: - 1 n diagnostics resu	1 + + [] t	4 🚖 Sto Calculat BTN2	p
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5			3				File Cor Start pag Test co Test m Pov Cmo Sensor BTN1	An tarnet dev figuration I CapSense Infiguration: ode: wer on self tes d test: No faul Status Off N	ce selected elp P I I I I I I I I I I I I I I I I I I I	v 🌮 tion Global V C T Pass	configuration CapS alibrated Cp: 11 Olerance: - 11 Shield not ens	ense output System	diagnostics Calibrated SNR: Folerance: - 1 n diagnostics resu	1 ** + 1	Sto Calculat # BTN2	p e SNR for:
19 18 17 16 17 16 17 16 17 18 19 8 7 6 5 4 3			3				File Cor Start pag Test co Test m Pov Cmo Sensor BTN1 BTN2	nfiguration F GapSense ode: wer on self tess ode: Status Off N On 11	cestivited lelp sensor configura Prototype is cs detected SNR Cp (A 8 0 12	C C C C C T P Pass Pass	configuration CapS alibrated Cp: 11 olerance: - 11 Shield not ent	ense output System	diagnostics Calibrated SNR: 'olerance: - 1 n diagnostics resu	1 ** + 1 It	Sto Calculat BTN2	p ie SNR for:
19 18 17 16 17 16 17 18 17 16 17 18 11 12 11 12 13 6 5 4 3 2			3				File Cor Start pag Test cc Test m Pov Cmo Sensor BTN1 BTN2 BTN3	In tanget dev figuration P Que CapSense infiguration: ode: wer on self tes: d test: No faul Status Off N On 11 Off N	ce selected elp Prototype is detected SNR C(/A 8 0 12 /A 10	C C C Pass Pass Pass Pass	configuration CapS alibrated Cp: 11 olerance: - 11 Shield not ent	ense output System	diagnostics Calibrated SNR: 'olerance: - 1 n diagnostics resu	1 • + 1 It	A transformed and transformed	p ie SNR for: v
19 18 17 16 15 14 13 13 13 13 14 15 16 17 18 19 8 7 6 5 4 3 2 1			3				File Con Start pass Test cc Test m Pov Cmo Sensor BTN1 BTN2 BTN3	Ho tannet dev hfiguration H je CapSenso: ode: wer on self tes d test: No faul Status Off N On 1 Off N Off N	cristicited elp sensor configura <u>Prototype</u> is detected <u>SNR C(</u> /A 8) 12 /A 10	b tion Global C T Pass Pass Pass Pass Pass	configuration CapS alibrated Cp: 11 olerance: - 11 Shield not end	ense output System	diagnostics Calibrated SNR: Tolerance: - 1 n diagnostics resu	1 * + 1	4 🚖 Sto	p
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			3	500 550			File Cor Start pag Test cc Test m V Pov Sensor BTN1 BTN2 BTN3 BTN4	Figuration Figuration Figuration Figuration Figuration Figuration: CapSense Infiguration: ode: wer on self test Wer on self test Wer on self test Vio fault Status Off N On 10 Off N Off N Off N Off N	residenced elp F I I I I I I I I I I I I I I I I I I I	De la construction Global Construction Global Construction Global Pass Pas Pas Pas Pas Pas Pas Pas	configuration CapS alibrated Cp: 11 olerance - 11 Shield not ena	ense output System	diagnostics Calibrated SNR: Folerance: - 1 n diagnostics resu	1 * + 1 k	Sto Calculat BTN2	p
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0 5 5	0 100 160	0 200 260 300 34	3	500 550	600 6	50 700	File Cor Start pag Test cc Test m Ø Poo Cmoo Sensor BTN1 BTN2 BTN3 BTN4	ring target devices and the second se	cr subseted elp P in	tion Global C Pass Pass Pass Pass	configuration CapS alibrated Cp: 11 olerance: - 11 Shield not ens	ense output System	diagnostics Calibrated SNR: folerance: - 1 n diagnostics resu	1 * + 1 It	Sto Calculat BTN2	p ie SNR for: v
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 5 5	0 100 150	0 200 250 300 34	3	500 550 550	600 6		File Cor Start pag- Test cc Test m I P Poo Croo Sensor BTN1 BTN2 BTN3 BTN4	Finite series of the series of	cs selected elp Point Point Point sessor configura sis detected SNR CI A 8 D 12 A 10 /A 14	Pass Pass Pass Pass Pass	configuration CapS alibrated Cp: 11 lolerance: - 11 Shield not ens	ense output System	diagnostics Calibrated SNR: Olerance: - 1 n diagnostics resu	1 * 1 t	Sto Calculat 4 2 8TN2	p



Tools

Design Toolbox

The Design Toolbox is an interactive spreadsheet tool that provides application-specific design guidelines for capacitive buttons. It is used to configure and validate the CapSense system.

The Design Toolbox:

- Provides general layout guidelines for a CapSense PCB
- Estimates button dimensions based on end-application requirements
- Calculates power consumption based on button dimensions
- Validates layout design

Evaluation Kits

The CY3280-MBR3 Evaluation Kit can be used to quickly evaluate the various features of the CY8CMBR3xxx solution. The kit also functions as an Arduino shield, making it compatible with the various Arduino-based controllers in the market. You can purchase this kit at the Cypress online store.

Online

In addition to print documentation, there are abundant web resources. The dedicated web page for the CY8CMBR3xxx family has all the current information.

Training

Free PSoC and CapSense technical training (on-demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and supports different skill levels to assist you in your designs.

Technical Support

For assistance with technical issues, search the Knowledge Base articles and forums at www.cypress.com/support. If you cannot find an answer to your question, create a technical support case or call technical support at 1-800-541-4736.



Contents

System Overview	5
Features Overview	6
CapSense Sensors	6
Sliders	6
Proximity Sensors	6
SmartSense Auto-tuning	6
Liquid Tolerance	6
Noise Immunity	6
Flanking Sensor Suppression (FSS)	6
Touch Feedback	6
General-Purpose Outputs (GPOs)	6
Buzzer Drive	6
Register Configurability	7
Communication to Host	7
System Diagnostics	7
Ultra-Low Power Consumption	7
MPN versus Features Summary	8
Pinouts	9
CY8CMBR3116 (16 Sensing Inputs)	9
CY8CMBR3106S (16 Sensing Inputs;	
Sliders Supported)	11
CY8CMBR3108 (8 Sensing Inputs)	12
CY8CMBR3110 (10 Sensing Inputs)	13
CY8CMBR3102 (2 Sensing Inputs)	14
CY8CMBR3002 (2 Sensing Inputs)	14
Unused SPO Pin Connection	15
Unused SPO Pin Connection for AXRES pins	15
Unused GPO Pin Connection	15
Device Feature Details	16
Automatic Threshold	16
Sensitivity Control	16
Sensor Auto Reset	16
Noise Immunity	17
Flanking Sensor Suppression	17
General-Purpose Outputs	17
LED ON Time	18
Toggle	18
Buzzer Signal Output	18
Host Interrupt	19
Latch Status Output	19

Analog Voltage Output	19
System Diagnostics	
Register Configurability	20
Example Application Schematics	
Power Supply Information	
Electrical Specifications	24
Absolute Maximum Ratings	24
Operating Temperature	24
DC Electrical Characteristics	24
AC Electrical Specifications	
I2C Specifications	
System Specifications	27
Power Consumption and Operational States	29
Response Time	31
CY8CMBR3xxx Resets	31
Host Communication Protocol	31
I2C Slave Address	31
I2C Communication Guidelines	
Write Operation	
Setting the Device Data Pointer	32
Read Operation	33
Layout Guidelines and Best Practices	34
Ordering Information	34
Ordering Code Definitions	
Packaging Dimensions	35
Thermal Impedances	
Solder Reflow Specifications	
Document Conventions	38
Units of Measure	
Glossary	39
Reference Documents	39
Document History Page	40
Sales, Solutions, and Legal Information	
Worldwide Sales and Design Support	42
Products	
PSoC® Solutions	
Cypress Developer Community	
Technical Support	



System Overview

A capacitive sensor detects changes in capacitance to determine the presence of a touch or proximity to conductive objects. The capacitive sensor can be a capacitive button that replaces the traditional mechanical buttons, a capacitive slider that replaces mechanical knobs, or a proximity sensor that replaces an infrared sensor in a user interface solution. A typical capacitive user interface system consists of the following:

- A capacitive sensor
- An audio-visual output, such as a buzzer or an LED
- A capacitive sensing controller connected to the sensor
- A host processor

The capacitive controller connects the sensor and the output to the host processor through a communication interface, such as an I^2C or a GPO.

The capacitive user interface system serves as a human-machine interface that takes the user's touch inputs and provides audio-visual feedback through a buzzer or an LED. CY8CMBR3xxx is a family of capacitive sensing controllers, which senses the change in capacitance based on touch or proximity, and controls the user interface system accordingly. The sensing algorithm, built in the controllers, determines the presence of touch and drives the outputs or sends signals to the host processor. This algorithm can distinguish between the signal (based on touch or proximity) and noise, which can be caused by environmental or electrical conditions.

Figure 2 shows a typical user interface system with capacitive buttons connected to a CY8CMBR3xxx CapSense Express controller, which controls the system and also communicates with the host processor through I^2C .

Traditionally, capacitive sensing controllers require firmware development to perform specific user interface functions and manual system tuning to achieve optimal performance. However, the CY8CMBR3xxx CapSense Express family of controllers does not require any firmware development, accelerating time-to-market. These devices feature SmartSense Auto-tuning, which eliminates the need for manual tuning, providing optimal performance even under extremely noisy conditions.



Figure 2. Typical CapSense System



Features Overview

CapSense Sensors

The CY8CMBR3xxx family of controllers supports up to 16 capacitive sensors. These can be configured as follows:

- Up to 16 CapSense buttons
- Up to two sliders: Configurable as linear or radial sliders
- Up to two proximity sensors that can detect up to 30-cm proximity distance

Sliders

- Supports up to two 5-segment sliders
- Configures each slider individually as linear or radial
- Combines both sliders to form one 10-segment slider
- Slider resolution is user-configurable

Proximity Sensors

- The CY8CMBR3xxx family supports up to two proximity sensors with a detection range of up to 30 cm. These proximity sensors are capable of detecting both proximity and touch events.
- The wake-on-approach feature wakes the devices from a low-power state to Active mode on a proximity event.
- The device also features driven shield, which enhances the proximity sensing range in the presence of metal objects.
- The device supports proximity sensors with C_P ranging from 8 pF to 45 pF.

SmartSense Auto-tuning

The CY8CMBR3xxx family features SmartSense Auto-tuning, Cypress's patented CapSense algorithm, which continuously compensates for system and environmental changes during run time. SmartSense Auto-tuning has the following advantages:

- Reduces design effort by eliminating manual tuning
- Adapts to variations in PCB, overlay, paint, and manufacturing that degrade touch-sensing performance
- Eliminates manual tuning in production
- Adapts to changes in the system environment due to noise
- Allows a platform design approach with different overlays, button shapes, and trace lengths

Liquid Tolerance

The CY8CMBR3xxx family delivers water-tolerant designs that eliminate false touches due to wet conditions, such as water droplets, moisture, mist, steam, or even wet hands. The CapSense controller locks up the user interface in firmware to prevent touch inputs in streaming water. The CY8CMBR3xxx family offers liquid-tolerance to liquids such as water, ketchup, oil, and blood.

Enable the shield electrode through the register map, using EZ-Click, to prevent false touches under wet conditions and enable both the shield electrode and guard sensor to prevent false touches in streaming water conditions. The shield electrode and guard sensor consume a port pin each in the CapSense controller. Refer to the CY8CMBR3xxx CapSense Design Guide for best practices and design guidelines for implementing liquid-tolerant designs.

Noise Immunity

The CY8CMBR3xxx family features the robust CSD PLUS capacitive sensing algorithm. Additionally, it implements the advanced noise immunity algorithm, EMC, for stable operation in extremely noisy conditions.

The EMC algorithm has higher average power consumption. For low-power applications, where noise conditions are not extreme, you can disable this feature through the I^2C interface.

Flanking Sensor Suppression (FSS)

This feature distinguishes between signals from closely spaced buttons, eliminating false touches. It ensures that the system recognizes only the first button touched.

Touch Feedback

The CY8CMBR3xxx family has pins that you can configure for audio-visual feedback through a buzzer or an LED.

General-Purpose Outputs (GPOs)

The GPOs are high-sink current outputs that can drive most LEDs. The GPO status can be controlled directly by the CapSense sensors so that a sensor 'ON' status automatically turns ON a corresponding LED. Alternatively, GPOs can be controlled by the host through the I^2C interface.

The GPOs also support advanced features, such as:

- CSx to GPOx Direct Drive: Directly control the GPOs upon button touch or proximity event.
- Pulse width modulation (PWM): Controls LED brightness.
- Toggle: The GPO status is toggled upon every touch event on the button sensors, and proximity event on proximity sensors, to mimic the functionality of the mechanical toggle switch.
- Voltage output: Analog voltage that represents the button status.

Buzzer Drive

The output pins of the CY8CMBR3xxx controllers can be configured for driving a single-input DC Piezo-electric buzzer through a PWM. The PWM frequency and buzzer activation duration are configurable. The buzzer output is activated for a finite amount of time when a finger touch is detected.



Register Configurability

The CY8CMBR3xxx registers may be configured through the l^2C interface. Device features may be enabled, disabled, or modified by writing appropriate values to the l^2C configurable register map. This register map also provides various status outputs to indicate the touch/release status and system performance and debug parameters.

You can access the register map of the device through the I^2C interface by a host controller, such as a microcontroller or the EZ-Click Customizer.

The CY8CMBR3xxx devices feature a safe register map update mechanism to overcome configuration data corruption, which can occur due to power failure during flash writes or any other spurious events. If the configuration data is corrupted during a register map update, the devices reconfigure themselves to the last known valid configuration.

Communication to Host

The CY8CMBR3xxx family communicates to a host processor through the following methods:

- The I²C interface allows the host to configure parameters and receive status information on touch events
- The host interrupt alerts the host when a new touch event occurs. This helps to build effective communication between the host and the CapSense controller. Alternatively, the CPU can poll the device status by reading through I²C.
- The GPO provides the ON or OFF sensor status to the host. The GPO ports can also be used to implement analog voltage and DC output (DCO) using an external resistor network.

System Diagnostics

The CY8CMBR3xxx devices are equipped with a system diagnostics feature to detect system-level fault conditions and to

avoid failure of the user interface design. The system diagnostic features also help to monitor system-level parameters to debug the design during development.

The built-in system diagnostics detects the following fault conditions at power-up and helps to monitor the following:

- Improper value of the modulating capacitor (C_{MOD})
- C_P value out of range
- Sensor shorts

Ultra-Low Power Consumption

For low-power applications, such as those operated by a battery, select a capacitive sensing controller that has ultra-low average power consumption.

The CY8CMBR3xxx controllers draw an average current of 22 μ A per sensor at 1.8 V.

The CY8CMBR3xxx family supports two operating modes:

- Active: The sensors are scanned periodically for power optimization.
- Deep Sleep: The sensors are not scanned until a command from the host is received to resume sensor scanning.

In the Active mode, CY8CMBR3xxx family implements additional techniques, such as optimizing the average power consumption and providing a smooth user interface experience without increasing the refresh interval.

In addition to these modes, the device has a wake-on approach feature, which uses proximity sensing to reduce the average power consumption, ensuring power saving when the system is inactive.

Details of all features are documented in Device Feature Details on page 16.



MPN versus Features Summary

The CY8CMBR3xxx family consists of six MPNs, each MPN supporting a different feature set. The following table lists all MPNs and a summary of the features supported by each.

#	Feature	CY8CMBR3116	CY8CMBR3106S	CY8CMBR3110	CY8CMBR3108	CY8CMBR3102	CY8CMBR3002
1	Maximum number of buttons	16	11	10	8	2	2
2	Maximum number of sliders	×	2	×	×	×	×
3	Maximum number of proximity sensors	2	2	2	2	2	×
4	Shield electrode	~	~	~	~	~	×
5	Guard Sensor	~	×	~	~	×	×
6	Wake-on-approach	~	~	~	~	~	×
7	Liquid tolerance	~	×	~	~	~	×
8	Automatic threshold	✓ Configurable	~				
9	Threshold Override	×	V	×	~	~	×
10	Sensitivity Control	v	V	~	~	V	×
11	Sensor auto-reset	~	~	~	~	V	✔ 20s
12	Median & IIR filter	~	v	~	~	~	~
13	Advanced-Low-Pass Filter	~	×	~	~	V	×
14	Electromagnetic Compatibility (EMC)	~	V	~	~	V	×
15	FSS	~	V	~	~	~	×
16	Maximum number of GPOs/LED drive outputs	8	0	5	4	1	2
17	GPO/LED Sink and Source Drive Support	✓ Configurable	×	✓ Configurable	✓ Configurable	✓ Configurable	Sink
18	LED brightness control	~	×	~	~	~	×
19	LED ON time	~	×	~	~	~	×
20	Toggle	~	×	~	~	~	×
21	Buzzer Signal Output	~	v	~	~	×	×
22	Host interrupt	~	~	~	~	×	×
23	Latch Status Output	~	~	~	>	~	×
24	Analog Voltage Output	~	×	~	~	~	~
25	System diagnostics	~	~	~	~	~	~
26	I ² C Interface	~	~	~	~	~	×



Pinouts

CY8CMBR3116 (16 Sensing Inputs)

Table 1. Pin Diagram and Definitions - CY8CMBR3116

			24-QFN			
Pin #	Pin Name	Туре	Description	If unused	Default Configuration	Pin Diagram
1	CS0/PS0	-	CapSense button / proximity sensor, controls GPO0	Ground/Ground	CS0	20
2	CS1/PS1	-	CapSense button / proximity sensor, controls GPO1	Ground/Ground	CS1	
3	CS2/GUARD	-	CapSense button / guard sensor, controls GPO2	Ground/Ground	CS2	
4	CS3	-	CapSense button, controls GPO3	Ground	CS3	
5	CMOD	-	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	CMOD	CS1/PS1 = 2 17 CS7 CS2/GUARD = 3 QFN 16 CS8/GP00 CS3 = 4 (Top View) 15 CS9/GP01
6	VCC	Power	Internal regulator output. Connect a $0.1-\mu$ F decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD.	NA	VCC	CMOD 5 VCC 6 VCC 6 CMOD 5 14 CS10/GPO2 CS11/GPO3 CS11/GPO3
7	VDD	Power	Power	NA	VDD	VDD VSS PO6 PO45
8	VSS	Power	Ground	NA	VSS	315/S 315/S 313/G 312/G
9	CS15/SH/HI	I/DO	CapSense button / shield electrode/ Host Interrupt (SPO1 in the register map)	Refer to Unused SPO Pin Connection on page 15	HI	8 8 8 8



Table 1. Pin Diagram and Definitions - CY8CMBR3116 (continued)

			24-QFN			
Pin #	Pin Name	Туре	Description	If unused	Default Configuration	Pin Diagram
10	CS14/GPO6	I/DO	CapSense button / general purpose output (GPO)	Ground/Refer to Unused GPO Pin Connection on page 15	GPO6	
11	CS13/GPO5	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO5	
12	CS12/GPO4	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO4	
13	CS11/GPO3	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO3	
14	CS10/GPO2	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO2	
15	CS9/GPO1	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO1	
16	CS8/GPO0	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO0	
17	CS7	-	CapSense button, controls GPO7	Ground	CS7	
18	CS6 ^[2]	-	CapSense button, controls GPO6	Connect to VDD	CS6	
19	CS5	-	CapSense button, controls GPO5	Ground	CS5	
20	CS4	-	CapSense button, controls GPO4	Ground	CS4	
21	I2C SDA	DIO	I2C data	Pull up	I2C SDA	
22	I2C SCL	DIO	I2C clock	Pull up	I2C SCL	
23	HI/BUZ/ GPO7	DO	Host Interrupt / buzzer output / GPO (SPO0 in the register map)	Refer to Unused SPO Pin Connection on page 15	GPO7	
24	XRES	XRES	Active Low external reset (an active low pulse on this pin resets the CapSense Controller)	Leave open	XRES	
25	Center Pad ^[1]	E-pad	Connect to VSS for best mechanical, thermal, and electrical performance	Floating, not connected to any other signal	E-pad	

Legend: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, DO = Digital Output, CS = CapSense Button, PS = Proximity Sensor SH = Shield Electrode, BUZ = Buzzer Output, GPO = General Purpose Output, GUARD = Guard Sensor, SPO = Special purpose output.

Notes

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If it is not connected to ground, it should be left floating without being connected to any other signal.
 This I/O functions as reset (AXRES) pin during boot-up. Make certain that this pin is not grounded during power-up for the device to boot up properly. After boot-up,

this I/O functions as indicated by the pin name.



CY8CMBR3106S (16 Sensing Inputs; Sliders Supported)

Table 2. Pin Diagram and Definitions - CY8CMBR3106S

		24-QFN				
Pin #	Pin Name	Туре	Description	If unused	Default Configuration	Pin Diagram
1	CS0/PS0	-	CapSense button / proximity sensor	Ground/Ground	CS0	
2	CS1/PS1	-	CapSense button / proximity sensor	Ground/Ground	CS1	RES RBUZ C SCL C SDA S5(SH/h S5(SH/h
3	CS2	-	CapSense button	Ground	CS2	
4	CS3	-	CapSense button	Ground	CS3	CS0/PS0 ■ 1 18■ CS15/SLD24
5	CMOD	Ι	External modulator capacitor. Connect 2.2 nF/ 5 V/X7R or NPO capacitor	NA	CMOD	CS1/PS1 = 2 17 CS14/SLD23 CS2 = 3 QFN 16 CS13/SLD22 CS3 = 4 (Top View) 15 CS12/SLD21 CMOD 5 14 CS11/SLD20
6	VCC	Power	Internal regulator output. Connect a 0.1 - μ F decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD.	NA	VCC	VCC = 6 [] 3 SLD14
7	VDD	Power	Power	NA	VDD	
8	VSS	Power	Ground	NA	VSS	
9	SLD10	-	Slider1, segment0	Ground	SLD10	
10	SLD11	-	Slider1, segment1	Ground	SLD11	
11	SLD12	-	Slider1, segment2	Ground	SLD12	
12	SLD13	-	Slider1, segment3	Ground	SLD13	
13	SLD14	-	Slider1, segment4	Ground	SLD14	
14	CS11/SLD20	-	CapSense button / Slider2, segment0	Ground/Ground	SLD20	
15	CS12/SLD21	-	CapSense button / Slider2, segment1	Ground/Ground	SLD21	
16	CS13/SLD22	-	CapSense button / Slider2, segment2	Ground/Ground	SLD22	
17	CS14/SLD23	_	CapSense button / Slider2, segment3	Ground/Ground	SLD23	
18	CS15/SLD24 ^[4]	-	CapSense button / Slider2, segment4	Connect to VDD/Connect to VDD	SLD24	
19	CS5/SH/HI	-	CapSense button / shield electrode/host interrupt. (SPO1 in the register map)	Refer to Unused SPO Pin Connection on page 15	CS5	
20	CS4	-	CapSense Button	Ground	CS4	
21	I2C SDA	DIO	I2C Data	Pull up	I2C SDA	
22	I2C SCL	DIO	I2C Clock	Pull up	I2C SCL	
23	HI/BUZ	0	Host interrupt / buzzer output. This pin acts as SPO0 for this device (SPO0 in register map).	Refer to Unused SPO Pin Connection on page 15	Ħ	
24	XRES	XRES	External reset	Leave open	XRES	
25	Center Pad ^[3]	E-pad	Connect to VSS for best mechanical, thermal and electrical performance	Floating, not connected to any other signal	E-pad	

Legend: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, CS = CapSense Button, PS = Proximity Sensor, SH = Shield Electrode, BUZ = Buzzer Output, SPO = Special Purpose Output.

Notes

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If it is not connected to ground, it should be left floating with<u>out being</u> connected to any other signal. This I/O functions as reset (AXRES) pin during boot-up. Make certain that this pin is not grounded during power-up for the device to boot up properly. After boot-up, this I/O functions as indicated by the pin name. 4.

^{3.}



CY8CMBR3108 (8 Sensing Inputs)

Table 3. Pin Diagram and Definitions - CY8CMBR3108

		16-QFN				
Pin #	Pin Name	Туре	Description	If unused	Default Configuration	Pin Diagram
1	CS0/PS0	-	CapSense button / proximity sensor, controls GPO0	Ground/Ground	CS0	
2	CS1/PS1	-	CapSense button / proximity sensor, controls GPO1	Ground/Ground	CS1	Hirbuz 12C Sol CS3
3	CMOD	-	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	CMOD	CS0/PS0 = 1
4	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD	NA	VCC	$\begin{array}{c} CMOD \\ VCC \\ \downarrow \\$
5	VDDIO	Power	Power for I2C and HI lines	Connect to VDD	VDDIO	CS4/C
6	VDD	Power	Power	NA	VDD	_
7	VSS	Power	Ground	NA	VSS	
8	CS4/GPO0	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO0	
9	CS5/GPO1	-	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO1	
10	CS6/GPO2	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO2	
11	CS7/GPO3/ SH	I/DO	CapSense button / GPO/ shield electrode. (SPO1 in the register map)	Refer to Unused SPO Pin Connection on page 15	GPO3	
12	CS2/GUARD ^[6]	-	CapSense button, controls GPO2 / guard sensor	Connect to VDD/Connect to VDD	CS2	
13	CS3	-	CapSense button, controls GPO3	Ground	CS3	
14	I2C SDA	DIO	I2C data	Pull up	I2C SDA	
15	I2C SCL	DIO	I2C clock	Pull up	I2C SCL	
16	HI/BUZ	DO	Host interrupt / buzzer output Supply voltage for <u>b</u> uzzer and pull-up resistor on HI should be equal to VDDIO (SPO0 in the register map).	Refer to Unused SPO Pin Connection on page 15	H	
17	Center Pad ^[5]	E-pad	Connect to VSS for best mechanical, thermal and electrical performance	Floating, not connected to any other signal	E-pad	

Legend: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, CS = CapSense Button, PS = Proximity Sensor SH = Shield Electrode, BUZ = Buzzer Output, GPO = General Purpose Output, GUARD = Guard Sensor, SPO = Special Purpose Output.

Notes

6.

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If it is not connected to ground, it should be left floating without being connected to any other signal. This I/O functions as reset (AXRES) pin during boot-up. Make certain that this pin is not grounded during power-up for the device to boot up properly. After boot-up, this I/O functions as indicated by the pin name. 5.



CY8CMBR3110 (10 Sensing Inputs)

Table 4. Pin Diagram and Definitions - CY8CMBR3110

				16-SOIC		
Pin #	Pin Name	Туре	Description	If unused	Default Configuration	Pin Diagram
1	I2C SDA	DIO	I2C data	Pull up	I2C SDA	
2	I2C SCL	DIO	I2C clock	Pull up	I2C SCL	
3	CS0/PS0	Ι	CapSense button / proximity sensor, controls GPO0	Ground/Ground	CS0	I2C SCL ■ 2 15 ■ CS3 CS0/PS0 ■ 3 14 ■ CS9/GP04/Hi/BUZ
4	CS1/PS1	-	CapSense button / proximity sensor, controls GPO1	Ground/Ground	CS1	CS1/PS1 4 SOIC 13 CS2/GUARD CMOD 5 12 CS8/GP03
5	CMOD	-	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	CMOD	VCC = 6 11 = CS7/GP02 VDD = 7 10 = CS6/GP01 VSS = 8 9 = CS5/GP00
6	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD	NA	VCC	
7	VDD	Power	Power	NA	VDD	
8	VSS	Power	Ground	NA	VSS	
9	CS5/GPO0	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO0	
10	CS6/GPO1	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO1	
11	CS7/GPO2	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO2	
12	CS8/GPO3	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO3	
13	CS2/GUARD	_	CapSense button, controls GPO2 / guard sensor	Ground/Ground	CS2	
14	CS9/GPO4/HI/ BUZ ^[7]	I/DO	CapSense button / GPO / host interrupt / buzzer output. (SPO1 in the register map)	Refer Unused SPO Pin Connection for AXRES pins on page 15	GPO4	
15	CS3	_	CapSense button, controls GPO3	Ground	CS3	
16	CS4/SH	I/O	CapSense button, controls GPO4 / shield electrode (SPO0 in the register map).	Refer to Unused SPO Pin Connection on page 15	CS4	

Legend: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, CS = CapSense Button, PS = Proximity Sensor SH = Shield Electrode, BUZ = Buzzer Output, GPO = General Purpose Output, GUARD = Guard Sensor, SPO = Special Purpose Output.

Note

This I/O functions as reset (AXRES) pin during boot-up. Make certain that this pin is not grounded during power-up for the device to boot up properly. After boot-up, this I/O functions as indicated by the pin name.



CY8CMBR3102 (2 Sensing Inputs)

Table 5. Pin Diagram and Definitions - CY8CMBR3102

				8-SOIC		
Pin #	Pin Name	Туре	Description	If unused	Default Configuration	Pin Diagram
1	I2C SCL	DIO	I2C clock	Pull up	I2C SCL	
2	CMOD	-	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	CMOD	
3	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD.	NA	VCC	$\begin{array}{c c} CMOD & \square & 2 \\ VCC & \square & 3 \end{array} \xrightarrow{7} & CS0/PS0 \\ \hline & & 6 & \square & CS1/PS1/GP00/SH \\ VDD & \square & 4 \end{array} \xrightarrow{7} & VSS \end{array}$
4	VDD	Power	Power	NA	VDD	
5	VSS	Power	Ground	NA	VSS	
6	CS1/PS1/ GPO0/SH	I/DO/O	CapSense button / proximity sensor/ GPO/ shield electrode (SPO0 in the register map).	Refer to Unused SPO Pin Connection on page 15	GPO0	
7	CS0/PS0 ^[8]	-	CapSense button / proximity sensor, controls GPO0	Connect to VDD/ Connect to VDD	CS0	
8	I2C SDA	DIO	I2C data	Pull up	I2C SDA	

Legend: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, CS = CapSense Button, PS = Proximity Sensor, SH = Shield Electrode, GPO = General Purpose Output, SPO = Special Purpose Output.

CY8CMBR3002 (2 Sensing Inputs)

Table 6. Pin Diagram and Definitions - CY8CMBR3002

			8-S	OIC	
Pin #	Pin Name	Туре	Description	If unused	Pin Diagram
1	GPO1	DO	Active-low GPO with open-drain-low drive mode	Ground	
2	CMOD	I/O	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	
3	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD.	NA	$\begin{array}{c} \text{CMOD} \ \Box 2 \\ \text{VCC} \ \Box 3 \\ \text{VDD} \ \Box 4 \\ \text{VDD} \ \Box 4 \\ \text{VSS} \end{array}$
4	VDD	Power	Power	NA	
5	VSS	Power	Ground	NA	
6	CS1	-	CapSense button, controls GPO1	Ground	
7	CS0 ^[8]	-	CapSense button, controls GPO0	Connect to VDD	
8	GPO0	DO	Active-low GPO with open-drain-low drive mode	Ground	

Legend: I = Analog Input, DO = Digital Output, CS = CapSense Button, GPO = General Purpose Output

Note

8. This I/O functions as reset (AXRES) pin during boot-up. Make certain that this pin is not grounded during power-up for the device to boot up properly. After boot-up, this I/O functions as indicated by the pin name.



Unused SPO Pin Connection

The following table lists the recommended pin connections for different configurations of SPO pins if an SPO pin is unused. Note that this table is not applicable to SPO pins which act as AXRES during boot up.

Table 7. Unused SPO Pin Connection

SPO Pin Configuration	Recommended pin connection if unused
CS	Connect to Ground
HI	Leave Open
SH	Leave Open
GPO	Refer to "Unused GPO Pin Connection" Table
BUZ	Leave Open
Disabled	Leave Open

Unused SPO Pin Connection for AXRES pins

Unused SPO pins which act as AXRES during boot up should be left open and should be disabled through the I2C configurable register map (using Ez-Click or any other configuration tool mentioned in section "Configuring CY8CMBR3xxx" of CY8CMBR3xxx CapSense Design Guide).

Unused GPO Pin Connection

The following table lists the recommended pin connections for different drive modes of GPO pins if a GPO pin is unused. Note that this table is not applicable to GPO pins which act as AXRES during boot up.

Table 8. Unused GPO Pin Connection

GPO drive mode	Recommended pin connection if unused
Open Drain Low	Connect to Ground
Strong	Leave Open



Device Feature Details

Table 9. Device Feature Benefits

Feature	Benefits
Automatic Threshold	Automatically tunes all the threshold parameters of the sensors for different noise settings
Sensitivity Control	Maintains optimal button performance for different overlay and noise conditions
Sensor Auto Reset	Recalibrates the sensor when a stuck-sensor (fault) condition occurs, and avoids invalid sensor output status to host
Noise Immunity	Provides immunity against external noise and the ability to detect touches without false trigger in noisy environments
Flanking Sensor Suppression (FSS)	Avoids multiple button triggers in a design with closely spaced buttons
Host Controlled GPOs	GPO pins, which can be controlled by the host processor through I ² C
LED On time	GPO output status stays ON for a set duration after the touch is released to provide better visual feedback to the user
Toggle	Sensor output status toggles on every sensor activation to mimic the mechanical toggle button functionality
Buzzer Signal Output	Provides audio feedback on button touch
Host Interrupt	Provides interrupt to host when there is a change in sensor status
Latch Status Output	Latches the sensor status changes in the register until the host reads the activated sensor status; this ensures that the sensor status is always read by the host even if the host is late to service the host interrupt signal from CY8CMBR3xxx
Analog Voltage Output	Indicates the button status through voltage levels
System Diagnostics	Supports production testing and debugging
Low-Power Sleep Mode and Deep Sleep Mode	Reduces power consumption

Automatic Threshold

- Dynamically sets all threshold parameters for button sensors, depending on the noise in the environment.
- Can be enabled or disabled through the register map.
- Applicable only to button sensors.
- Mutually exclusive from the EMC feature. If EMC is enabled, automatic threshold is automatically disabled.
- Allows overriding of calculated thresholds with particular values specified through the register map. Refer to the CY8CMBR3xxx CapSense Design Guide for more details.

Sensitivity Control

This feature allows specification of the minimum change in sensor capacitance that can trigger a sensor state change (OFF to ON or vice-versa).

- Sensitivity can be specified individually for each CapSense button and slider.
- Sensitivity can be specified as one of the four available values: 0.1 pF, 0.2 pF, 0.3 pF, and 0.4 pF.
- Higher sensitivity values can be used for thick overlays or small button diameters.
- Lower sensitivity values should be used for large buttons or thin overlays to minimize power consumption.

Sensor Auto Reset

This feature resets the CapSense sensors to the OFF state after a specific time period, even though they continue to be activated.

- Resets the sensor baseline to the current raw count after a specific time period, even though the sensors continue to be activated.
- Prevents a stuck sensor when a metal object is placed close to that sensor.
- The Auto Reset period can be set to 5 or 20 seconds and can be configured through two global settings provided in the register map:
 - Global setting for all proximity sensors
 - □ Global setting for all CapSense buttons and slider segments
- The guard sensor does not undergo Auto Reset.

Figure 3. Example of Button Auto Reset on GPO0 (DC Active Low Output)





Noise Immunity

- The CY8CMBR3xxx family features the robust CSD PLUS capacitive sensing algorithm.
- Uses pseudo-random sequence (PRS) clock source to minimize electromagnetic interference.
- Provides advanced noise immunity algorithm, that is, electromagnetic compatibility (EMC), for superior noise immunity against external radiated and conducted noise
 - EMC algorithm has higher average power consumption. For low-power applications, where noise conditions are not extreme, this feature can be disabled using the EZ-Click tool.
- Provides median and IIR filters for button and slider sensors.
- Provides an Advanced-Low-Pass (ALP) filter for proximity sensors.

Flanking Sensor Suppression

- Distinguishes between signals from closely spaced buttons, eliminating false touches.
- Can be enabled or disabled individually on each CapSense button.
- On touch detection by two or more sensors on which FSS is enabled, only the first touched sensor reports active status.
- Allows only one button at a time to be in the Touch state.
- Supported only on CapSense buttons.

Figure 4. Reported Sensor Status with FSS Enabled



CS1 is touched, CS1 reported ON

CS2 also touched along with CS1, CS1 is reported ON

Only CS2 is touched; reported ON

General-Purpose Outputs

- Supports up to eight GPOs, multiplexed with sensor inputs or other functionality, depending on the part number.
- Provides GPO status control. GPOs can be configured to be controlled by the sensor input or the host through the I^2C interface.
- Allows for configurable Active LOW or Active HIGH logic output. The Active LOW logic output can be configured to directly drive LEDs in the current sink mode. The Active HIGH logic output can be configured to interface the GPOs with the host and other circuits.
- The GPOx status will not be retained in the Deep Sleep mode. The GPOx output state will be reset to default during deep sleep and upon wake-up from deep sleep.

Figure 5. CSx Controls GPOx (Active HIGH Logic)



- Supports two drive modes:
 - Open-drain drive mode (HIGH-Z and GND) for analog voltage outputs and LED direct drive
 - Strong drive mode (V_{DD} and GND) to interface with the host Π and other circuits
- Supports PWM on GPOs for LED brightness control. Two different duty cycles can be configured for Sensor Touch and No Touch states (Active and Inactive state duty cycles). When the GPO is host-controlled, and if the PWM control is enabled for the GPO, the same Touch and No Touch duty cycles will be used for the On and Off states of the host-controlled GPO.
- When the proximity sensor is enabled, the proximity event controls the respective GPOs. A touch event on a proximity sensor is indicated only through the I²C register map.
- Sensor fault conditions are indicated with the pulse signal on the respective GPOs at power-up by system diagnostics.



LED ON Time

Keeps the GPO status ON for a particular period of time after the falling edge of a sensor, for better visual indication through LEDs

Figure 6. CSx Controls GPOx with LED ON Time Enabled



- Can be enabled only when the GPO is directly controlled by a CapSense sensor
- Can be enabled or disabled on each sensor and the ON Time duration can be configured from 0 to 2 seconds in 20-ms increments
- Can be enabled in all configurations of GPOs except the Toggle mode
- Not applicable when the sensor status is turned off by Sensor Auto Reset

Toggle

The controller can toggle the GPO state at every rising edge of a sensor activation event to mimic the functionality of a mechanical toggle switch (a touch event for a button sensor and a proximity event for proximity sensors activates a sensor).

Figure 7. CSx Controls GPOx with the Toggle Enabled



- Can be enabled only when the GPO is directly controlled by a capacitive sensor.
- Can be enabled or disabled individually on each capacitive sensor.
- Can be enabled in all configurations of GPOs—that is, Active LOW and Active HIGH DC output, PWM output, open-drain, and strong drive modes.

Buzzer Signal Output

- Produces a PWM signal to drive a Piezo-Buzzer that generates audio feedback when a touch is detected on a CapSense button or a guard sensor.
- Supports buzzer connection, as shown in the following figure.

Figure 8. Buzzer Connection^[9]



- PWM frequency is configurable: The buzzer frequency is configurable to meet different Piezo-Buzzer drive requirements and to provide different tones. The buzzer frequency may be configured either by using the EZ-Click tool or by writing to the corresponding control register. Refer to System Specifications on page 27 for the supported buzzer frequencies.
- Generates PWM output for a fixed duration (ON time) when a touch is detected. The ON time is configurable through EZ-Click, from 100 ms to 12.7 s, in steps of 100 ms,
- Buzzer signal output and EMC (refer to the CY8CMBR3xxx Registers TRM) are mutually exclusive features. These must not be enabled simultaneously.

Figure 9. Buzzer Activation on a Touch Event



The buzzer output does not restart if multiple trigger events occur before the Buzzer ON Time elapses.

Note

9. Buzzer must be connected between V_{DDIO} and the BUZ pin. If V_{DDIO} is not available on the device, connect the buzzer to V_{DDI} instead of V_{DDIO}.



Figure 10. Buzzer Operation with Consecutive Touches



If the buzzer is not currently active, the buzzer output starts on each trigger event.

- When the buzzer is enabled, the buzzer output toggles between a Logic HIGH state and a Logic LOW state, to drive the buzzer when active. When the buzzer is inactive, the buzzer output maintains a Logic HIGH state.
- The buzzer ON Time has a range of (1 to 127) × 100 ms.

Host Interrupt

This feature generates a pulse signal on any change in the CapSense sensors' status.

- The host interrupt is an active LOW pulse signal generated on the HI pin during any change in the sensor status or slider position.
- The duration of the active LOW host interrupt pulse is T_{HI} (refer to System Specifications on page 27).
- The minimum time between two HI pulses is equal to one refresh interval.

Figure 11. Host Interrupt Line with CSx Buttons Touched Separately



- The host interrupt pin has the open-drain low-drive mode.
- This pin is powered by V_{DDIO} in CY8CMBR3108. This allows communication with a host processor at voltage levels lower than the chip V_{DD}.
- Only one pin can be configured as the host interrupt on devices that have a host interrupt functionality on multiple pins.

- Allows to read both current status (CS) and latch status (LS) to avoid missing button touches.
- CS and LS can be read through registers, BUTTON_STAT, and LATCHED_BUTTON_STAT respectively.
- Table 10 explains the various combinations of CS and LS.

Table 10. Latch Status Read

CS	LS	Description
0	0	CSx is not touched during the current I ² C read Host has already acknowledged any previous CSx touch in the previous I ² C read
0	1	CSx was touched before the current I ² C read This CSx touch was missed by the host

Analog Voltage Output

Some of the applications use analog voltage as an effective method to indicate the sensor status to the host controller. A simple external resistor network can be used with GPOs of CY8CMBR3xxx to generate analog voltage output upon touch detection for such applications.

The CY8CMBR3xxx GPOs support the open-drain low-drive mode. In this mode, the sensor "touch" state is indicated by a logic LOW signal on the GPO and a "no touch" state is indicated by the HIGH-Z signal. With the external resistor shown in Figure 12, when a sensor is touched, the respective GPO is driven to a logic LOW signal. This forms a simple voltage divider and produces a voltage output. All the other GPOs are in HIGH-Z states because their respective sensors are in the "no touch" state.

Figure 12. Voltage Output Using GPO and Resistor Network



The output analog voltage can be calculated based on the following equation:

$$Vout = \frac{VDD \times Rn}{R + Rn}$$

Here, Rn represents the series resistor value of any given GPO.

Note If more than one button is activated at the same time, the Rn becomes equivalent (parallel) to all Rn resistors.



- For the circuit represented in Figure 12 to work, GPOs should be configured in the Active LOW logic, open-drain drive mode. PWM must be disabled and the CSx-to-GPOx direct drive must be enabled (that is, GPOs must be configured as sensor-controlled).
- The FSS feature can be enabled so only one button is reported ON at a time.

System Diagnostics

System Diagnostics is a BIST feature that tests for faulty sensor, shield, or CMOD conditions at device resets.

- If any sensor fails these tests, a 50-ms pulse is sent out on the corresponding GPO (that is, the pulse is observed on GPOx if CSx fails the test), and the sensor is disabled.
- If the shield fails the tests, a 50-ms pulse is sent out on all GPOs and all the sensors are disabled.
- If CMOD fails the tests, a 50-ms pulse is sent out on all GPOs and all the sensors are disabled.
- System Diagnostics failure pulses are sent within device boot-up time.
- The System Diagnostics status is also updated in the register map. Therefore, the host can also read test results through the I²C interface.

Sensor C_P > 45 pF

If the parasitic capacitance of a sensor is more than 45 pF, the sensor is disabled.

Improper value of CMOD

If the value of CMOD is less than 1 nF or greater than 4 nF, all sensors are disabled (the recommended value of CMOD is 2.2 nF).

Sensor shorts

System Diagnostics also checks for the following errors:

- Sensor shorted to V_{ss}^[10]
- Sensor shorted to V_{DD}
- Sensor shorted to another sensor
- Sensor shorted to shield

Register Configurability

The CY8CMBR3xxx family features an I²C configurable register map. The CY8CMBR3xxx registers are divided into three categories, as Table 11 shows.

Table 11. CY8CMBR3xxx Registers

Register Category	Register Map Address range	Description
Configu- ration Registers	0x00-0x7E	These registers contain the config- uration data for the CY8CMBR3xxx controllers. A host can write into these registers and save the data to non-volatile memory by writing to CTRL_CMD command register. Note that the new configuration takes effect only after the configu- ration is saved to non-volatile memory and the device is reset (see CY8CMBR3xxx Resets on page 31).
Command Registers	0x80-0x87	These registers accept commands from host. Any command written to these register is executed within $T_{12C_LATENCY_MAX}$ from the I^2C acknowledgement of the command.
Status Registers	0x88-0xFB	These are read only registers and indicate the status of command execution, system diagnostics and sensor data.

The CY8CMBR3xxx devices feature a safe register map update mechanism to overcome configuration data corruption, which can occur due to power failure during execution of "Save" command or any other spurious events.

If the configuration data is corrupted when the device is saving data, on the next reset, the devices reconfigure themselves to the last known valid configuration. If there is no valid configuration saved by user, the devices load the factory default configuration as specified in Register TRM.



Example Application Schematics



Figure 13. Example Schematics Demonstrating Four Buttons and Four GPOs

In Figure 13^[11, 12], the CY8CMBR3108 device is configured in the following manner:

- CS0–CS3: CapSense buttons
 - All CapSense pins must have a 560-ohm series resistance (placed close to the chip) for improved noise immunity.
- GPO0–GPO3: To external LEDs
 - LEDs are connected in sinking mode because the CY8MBR3xxx devices have high sink current capability.
 - \square Series resistances are connected to limit the GPO current to be with ${\rm I_{IL}}$ limits.
- CMOD pin: 2.2 nF to ground
- VCC pin: 0.1 µF to ground

- VDD pin: To external supply voltage
 □ 1-µF and 0.1-µF decoupling capacitors connected to VDD
- VDDIO pin: To supply voltage, which is ≤ VDD
 □ VDDIO powers I²C and HI lines.
 □ 1-µF and 0.1-µF decoupling capacitors connected to VDDIO.
- I2C_SCL and I2C_SDA pins: 330 ohms to the I²C header
 For I²C communication: It is assumed that the I²C line pull-up resistors are present on the host side outside the I²C header.
- HI pin: To host
- To prompt the host to initiate an I²C transaction for reading the changed sensor status.

Notes

12. Proper ground layout is important for better SNR performance. Refer to the CY8CMBR3xxx CapSense Design Guide and Getting started with CapSense guide for all layout guidelines.

^{11.} VCC should be connected to VDD for 1.71 V \leq VDD \leq 1.89 V.





Figure 14. Example Schematics Demonstrating Multiple Sensor Types

In Figure $14^{[13, 15]}$, the CY8CMBR3106S device is configured in the following manner:

- PS0: CapSense proximity sensor
- CS1–CS4: CapSense buttons^[14]
- CMOD pin: 2.2 nF to ground
- VCC pin: 0.1 uF to ground
- VDD pin: To external supply voltage
 □ 1-µF and 0.1-µF decoupling capacitors connected to VDD
- SLD10-SLD14: CapSense linear slider segments
- SLD20-SLD24: CapSense radial slider segments
- BUZ: To buzzer

□ AC buzzer (1-pin).

Buzzer second pin to ground.

- I2C_SCL and I2C_SDA pins: 330 ohm to the I²C header. It is assumed that the I²C line pull-up resistors are present on the host side outside the I²C header.
 For I2C communication.
- HI pin: To host
 - To prompt the host to initiate an I²C transaction for reading the changed sensor status.
- XRES pin: Floating □ For external reset.

Notes

- 13. VCC should be shorted to VDD for 1.71 V \leq VDD \leq 1.89 V.
- 14. All CapSense pins have 560-ohm series resistance (placed close to the chip) for improved noise immunity.

15. Proper ground layout is important for better SNR performance. Refer to the CY8CMBR3xxx CapSense Design Guide and Getting started with CapSense guide for all layout guidelines.



Power Supply Information

The CY8CMBR3xxx family of controllers contains three supply domains: $V_{DD},\,V_{CC},\,\text{and}\,\,V_{DDIO}.$

- V_{DD} : This is the primary supply to the chip and can be powered from 1.8 V ± 5% (Externally regulated mode) or 1.8 to 5.5 V (Internally regulated mode). The CapSense controller is powered by the V_{DD} supply, and all the I/O signal levels (except I²C lines, HI, and XRES) are referenced with respect to the V_{DD} supply. For packages and <u>MPNs</u> that do not have V_{DDIO}, the I²C SDA, I²C SCL, HI, and XRES signal levels are also referenced with respect to the V_{DD} supply.
- V_{DDIO} : This is the supply input for I²C SDA, I²C SCL, \overline{HI} , and XRES lines. The signal levels of these I/Os are referenced with respect to V_{DDIO} . The V_{DDIO} supply can be as low as 1.71 V and as high as the voltage of the V_{DD} supply. The V_{DDIO} should not be powered at a voltage higher than that of the V_{DD} supply. The V_{DDIO} is available only on select packages. For a package that does not have V_{DDIO} , the I²C SDA, I²C SCL, \overline{HI} , and XRES signal levels are referenced with respect to the V_{DD} supply.
- V_{CC}: This is the internal regulator output, which powers the core and capacitive sensing circuits. A 0.1-µF, 5-V ceramic capacitor should be connected close to the V_{CC} pin for better performance.
- Power sequencing: The CY8CMBR3xxx device does not require any power supply sequencing for the VDD and VDDIO supplies. Either of these supplies can ramp earlier or later than the other. The only requirement is that VDDIO should not be greater than VDD.

■ 1.8-V externally regulated operation: When V_{DD} is powered with a 1.8 V ±5% supply, the V_{CC} and V_{DD} pins should be shorted externally and the SUPPLY_LOW_POWER bit in the DEVICE_CFG3 register should be set to 1 through the I²C interface (refer to the CY8CMBR3xxx Registers TRM for details on the register). When the VCC and VDD pins are shorted, this bypasses the internal voltage regulator. Under this condition, make certain that VDD does not exceed 1.89 V.

Note: If EZ-Click is used to configure the device, it automatically takes care of the required register settings based on the voltage settings selected in EZ-Click.

The CY8CMBR3xxx family of controllers is factory-configured for 1.8-V to 5.5-V operation. To configure a factory-configured device for 1.8-V externally regulated operation, you can use the following procedure:

- Short V_{DD} and V_{CC}.
- Power the device at 1.8 V (note that regardless of the value of the SUPPLY_LOW_POWER bit, the device can be powered at 1.8 V for configuring the device; only CapSense operation is not guaranteed if the SUPPLY_LOW_POWER bit is not properly configured)
- Use EZ-Click to configure the device for 1.8-V operation.
- Save and reset the device.
- Ground consideration: Both the V_{SS} pin and the metal pad (E-pad) of the device should be connected to board ground.



Figure 15. Power Supply Connections for CY8CMBR3xxx CapSense Controllers^[16]

Power supply connections* when $1.71 \le V_{DD} \le 1.89 \text{ V}$

*SUPPLY_LOW_POWER bit in DEVICE_CFG3 register should be set to 1 to operate device at 1.8V (\pm 5%)

Note

16. Proper ground layout is important for best performance. Refer to the layout guidelines mentioned in the CY8CMBR3xxx CapSense Design Guide and Getting started with CapSense guide.

Power supply connections when $1.8 \le V_{\text{DD}} \le 5.5 \text{ V}$ Power



Electrical Specifications

Absolute Maximum Ratings

Table 12. Absolute Maximum Ratings^[17]

Parameter	Description	Conditions	Min	Тур	Max	Units
V _{DD_MAX}	Max voltage on the V_{DD} pin relative to V_{SS}	–40 °C to +85 °C T _A , absolute maximum	-0.5	_	6	V
V _{DDIO_MAX}	Max voltage on the V_{DDIO} pin relative to V_{SS}	–40 °C to +85 °C T _A , absolute maximum	0.5	-	6	V
V _{CC_MAX}	Max voltage on the VCC pin relative to V_{SS}	Absolute maximum	-0.5	-	1.89	V
V _{IO}	DC input voltage relative to V_{SS} on I/O	–40 °C to +85 °C T _A , absolute maximum	-0.5	-	V _{DD} +0.5	V
ESD_HBM	Electrostatic discharge, human body model	Human body model ESD.	2200	-	-	V
ESD_CDM	Electrostatic discharge, charged device model	Charged device model ESD	500	_	_	V
I _{LU}	Latch-up current limits	Maximum/minimum current to any input or output, pin-to-pin or pin-to-supply	-140	Ι	140	mA
I _{IO}	Current per GPIO		_	_	25	mA

Operating Temperature

Table 13. Operating Temperature

Parameter	Description	Conditions	Min	Тур	Max	Units
т _о	Operation temperature	Ambient temperature inside system enclosure	-40	25	85	°C
Τ _J	Junction temperature		-40	Ι	100	°C

DC Electrical Characteristics

DC Chip-Level Specifications

The specifications in Table 14 are valid under these conditions: –40 °C \leq T_A \leq 85 °C. Typical values are specified at T_A = 25 °C, V_{DD} = 3.3 V, and are for design guidance only.

Table 14. DC Chip-Level Specifications

Parameter	Description	Conditions/Details	Min	Тур	Max	Units
		V _{CC} shorted to V _{DD}	1.71	1.8	1.89	V
V _{DD}	Chip supply voltage	V_{CC} not shorted to $V_{DD}.$ V_{CC} connected to 0.1 μF decoupling capacitor	1.8	-	5.5	V
Vedia	Supply voltage I/O	1.71 V < V _{DD} < 1.89 V	1.71	Ι	V_{DD}	V
VOIDO		1.8 V < V _{DD} < 5.5 V	1.71	-	V_{DD}	V
V	Maximum allowed ripple on power	+25 °C T _A , V _{DD} > 2 V, sensitivity \ge 0.1 pF	_	-	±50	mV
* DD_RIPPLE	supply, DC to 10 MHz	+25 °C T _{A,} V _{DD >} 1.75 V, C _P < 20 pF, sensitivity = 0.4 pF	_	-	±25	mV
C _{EFC}	External regulator voltage bypass (capacitor to be connected to the V _{CC} pin)	X5R ceramic ±10% or better	_	0.1	-	μF
C _{EXC}	Power supply decoupling capacitor on V_{DD}	X5R ceramic or better	_	1	_	μF

Note

^{17.} Usage above the absolute maximum conditions listed in Table 12 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions, but above normal operating conditions, the device may not operate to specification.



XRES DC Specifications

Table 15. XRES DC Specifications

Parameter	Description	Conditions/Details	Min	Тур	Max	Units
V _{IH_XRES}	Input voltage high threshold on XRES pin	CMOS input	0.7*V _{DD}	_	Ι	V
V _{IL_XRES}	Input voltage low threshold on XRES pin	CMOS input	-	_	0.3*V _{DD}	V
C _{IN_XRES}	Input capacitance on XRES pin		_	-	7	pF
V _{HYSXRES}	Input voltage hysteresis on XRES pin	V _{DD} ≤ 4.5 V	-	0.05*V _{DD}	-	mV
		V _{DD} > 4.5 V	200	-	-	mV
R _{PULLUP}	Pull-up resistor		3.5	5.6	8.5	kΩ

DC I/O Port Specifications

The specifications in Table 16 are valid at –40 °C \leq T_A \leq +85 °C. Typical parameters are specified at T_A = 25 °C and are for design guidance only.

Table 16. DC I/O Port Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
Vou		I _{OH} = –4 mA at 3 V V _{DD}	V _{DD} -0.6	Ι	_	V
VОН		I _{OH} = –1 mA at 1.8 V V _{DD}	V _{DD} -0.5	Ι	_	V
N		I _{OL} = 4 mA at 1.8 V V _{DD}	_	-	0.6	V
VOL		I _{OL} = 10 mA at 3 V V _{DD}	-	_	0.6	V
C _{PIN}	Pin capacitance	All V _{DD} , all packages, all I/Os	-	3	7	pF
I _{TOT_GPIO}	Maximum total sink chip current		_	-	85	mA

AC Electrical Specifications

Table 17. AC Chip-Level Specifications

Parameter	Description	Conditions	Min	Тур	Мах	Units
T _{SR_POWER_UP}	Power supply slew rate during power-up	–40 °C ≤ TA ≤ 85 °C, all V _{DD}	1	Ι	67	V/ms

XRES AC Specifications

Table 18. XRES AC Specifications

Parameter	Description	Conditions/Details	Min	Тур	Max	Units
T _{XRES}	External reset pulse width	–40 °C ≤ T_A ≤ 85 °C, all V_{DD}	5	-	-	μs