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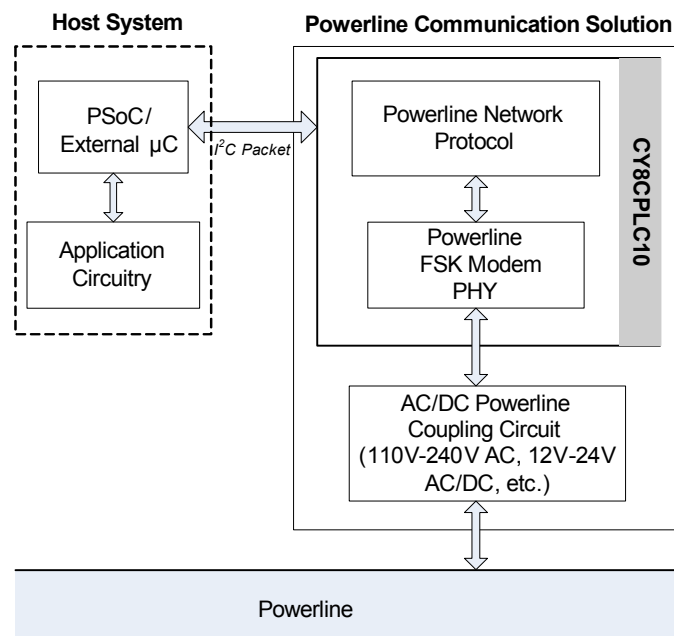
Features

- Integrated Powerline Modem PHY
- 2400 bps Frequency Shift Keying Modulation
- Powerline Optimized Network Protocol
- Integrates Data Link, Transport, and Network Layers
- Supports Bidirectional Half-Duplex Communication
- 8-bit CRC Error Detection to Minimize Data Loss
- I²C enabled Powerline Application Layer
- Supports I²C Frequencies of 50, 100, and 400 kHz
- Reference Designs for 110V to 240V AC, 12V to 24V AC/DC Powerlines
- Reference Designs Comply with CENELEC EN50065-1:2001 and FCC Part 15

Applications

- Residential and Commercial Lighting Control
- Home Automation
- Automatic Meter Reading
- Industrial Control and Signage
- Smart Energy Management

Logic Block Diagram



Functional Description

The CY8CPLC10 is an integrated Powerline Communication chip with the Powerline Modem PHY and Powerline Network Protocol Stack. This chip provides robust communication between different nodes on a Powerline.

Powerline Transmitter

The application residing on a host microcontroller generates messages to be transmitted on the Powerline. These messages are delivered to the CY8CPLC10 over an I²C serial link.

The Powerline Network Layer residing on the CY8CPLC10 receives these I²C messages and generates a Powerline Transceiver (PLT) packet. These packets are modulated by the FSK Modem and coupled with Powerline by the external coupling circuit.

Powerline Receiver

Powerline signals are received by the coupling circuit and demodulated by the FSK Modem PHY to reconstruct PLT packets. These PLT packets are decoded by the Powerline Network Protocol and then transferred to the external host microcontroller in an I²C format.

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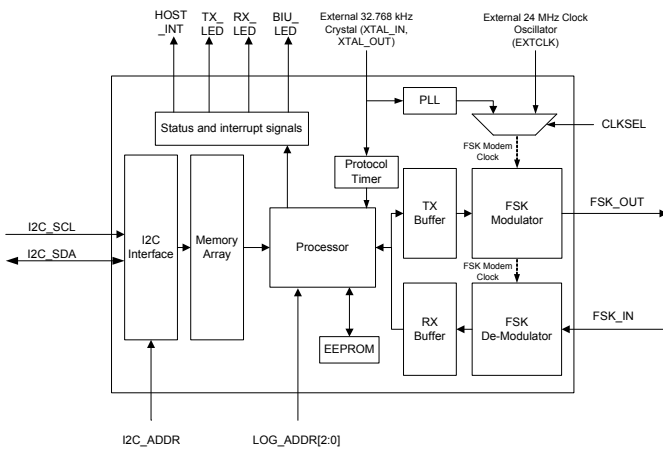
Robust Communication using Cypress's PLC Solution

Powerlines are one of the most widely available communication mediums for PLC technology. The pervasiveness of Powerlines also makes it difficult to predict the characteristics and operation of PLC products. Because of the variable quality of Powerline around the world, implementing robust communication over Powerline is an engineering challenge. Keeping this in mind, Cypress's PLC solution has been designed to enable secure and reliable communication over Powerlines. Cypress PLC features that enable robust communication over Powerline include:

- Integrated Powerline PHY modem with optimized filters and amplifiers to work with lossy high voltage and low voltage Powerlines.
- Powerline optimized Network Protocol that supports bidirectional communication with acknowledgement based signaling. In case of data packet loss due to bursty noise on the Powerline, the transmitter can retransmit data.
- The Powerline Network Protocol also supports 8-bit CRC for error detection and data packet retransmission.
- A Carrier Sense Multiple Access (CSMA) scheme, built into the Network Protocol, minimizes collisions between packet transmissions on the Powerline. This provides support for multiple masters and reliable communication on a bigger network.

Detailed Description

Figure 1. CY8CPLC10 Internal Block Diagram



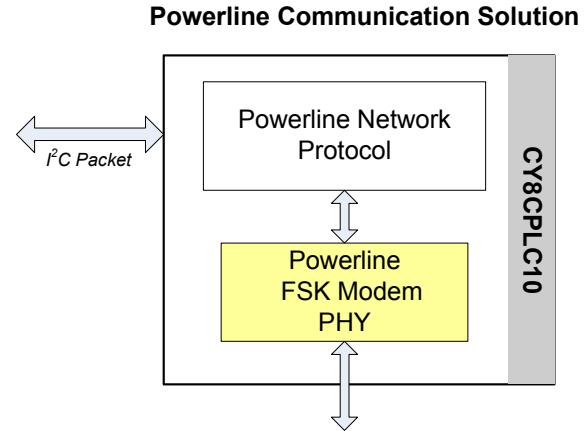
The CY8CPLC10 consists of two main functional components:

- Powerline Modem PHY
- Powerline Network Protocol

The user application resides on a host system such as PSoC®, EZ-Color™, or any other microcontroller. The messages generated by the application are communicated to the CY8CPLC10 over I²C and processed by these functional components. The following sections present a brief description of each of these components.

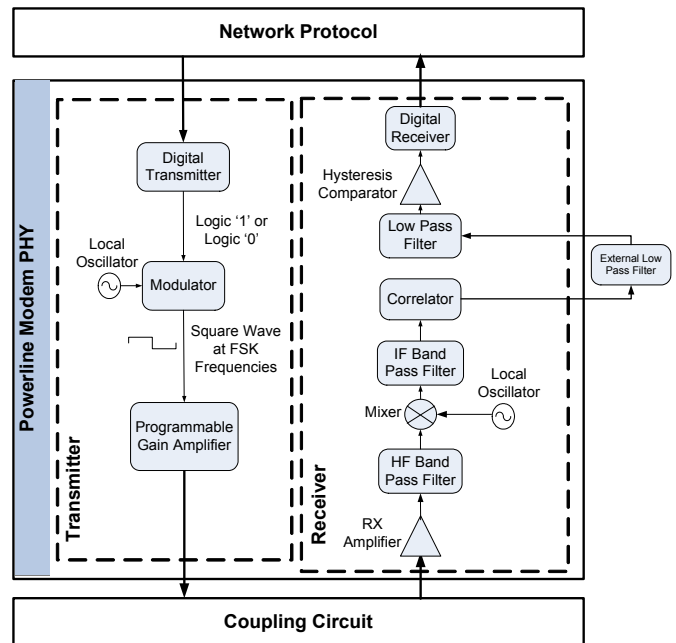
Powerline Modem PHY

Figure 2. CY8CPLC10: FSK Modem PHY



The physical layer of Cypress's PLC solution is implemented using an FSK modem that enables half duplex communication on a Powerline. This modem supports data rates up to 2400 bps.

Figure 3. CY8CPLC10: FSK Modem PHY Block Diagram



Transmitter Section

Digital data from the network layer is serialized by the digital transmitter and fed as input to the modulator. The modulator divides the local oscillator frequency by a definite factor depending on whether the input data is high level logic '1' or low level logic '0'. It then generates a sine wave at 133.3 kHz (Logic '0') or 131.8 kHz (Logic '1'), which is fed to the Programmable Gain Amplifier to generate FSK modulated signals. The logic '1' frequency can also be configured as 130.4 kHz for wider FSK bandwidth.

Receiver Section

The incoming FSK signal from the Powerline is input to a High Frequency (HF) Band Pass Filter that filters out-of-band frequency components and outputs filtered signal within the desired spectrum of 125 kHz to 140 kHz for further demodulation. The Mixer block multiplies the filtered FSK signals with a locally generated signal to produce heterodyned frequencies.

The Intermediate Frequency (IF) Band Pass Filters further remove out-of-band noise as required for further demodulation. This signal is fed to the correlator which produces a DC component (consisting of Logic '1' and '0') and a higher frequency component.

The output of the correlator is fed to an external Low Pass filter with a cut-off frequency of 7.5 KHz. The signal is then fed to the internal Low Pass Filter (LPF) that outputs only the demodulated digital data at 2400 baud and suppresses all other higher frequency components generated in the correlation process. The output of the LPF is digitized by the hysteresis comparator. This eliminates the effects of correlator delay and false logic triggers due to noise. The Digital Receiver deserializes this data and outputs to the Network Layer for interpretation.

Coupling Circuit Reference Design

The coupling circuit couples low voltage signals from CY8CPLC10 to the Powerline. The topology of this circuit is determined by the voltage on the Powerline and design constraints mandated by Powerline usage regulations.

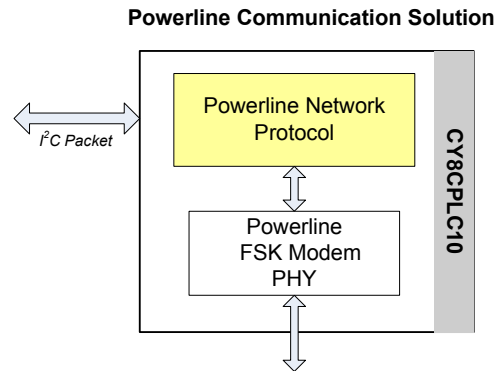
Cypress provides reference designs for a range of Powerline voltages such as 110V AC, 240V AC, 12V DC, 12V AC, 24V DC, and 24V AC. The CY8CPLC10 is capable of data communication over other AC/DC Powerlines as well with the appropriate external coupling circuit. The 110V AC and 240V AC designs are compliant to the following Powerline usage regulations:

- FCC part 15 for North America
- EN50065-1:2001

Powerline Network Protocol

Cypress's Powerline optimized Network Protocol performs the functions of the data link, network, and transport layers in an ISO/OSI Equivalent Model.

Figure 4. CY8CPLC10: Powerline Network Protocol



The Network Protocol implemented on the CY8CPLC10 chip supports the following features:

- Bidirectional half-duplex communication
- Master and slave as well as peer-to-peer network of Powerline nodes
- Multiple masters on Powerline network
- 8-bit logical addressing supports up to 256 Powerline nodes
- 16-bit extended logical addressing supports up to 65536 Powerline nodes
- 64-bit physical addressing supports up to 2^{64} Powerline nodes
- Individual broadcast or group mode addressing
- Carrier Sense Multiple Access (CSMA)
 - Full control over transmission parameters
 - Acknowledged
 - Unacknowledged
 - Repeated transmit
 - Sequence numbering

CSMA and Timing Parameters

- CSMA: The protocol provides the random selection of a period between 85 and 115 ms (out of seven possible values in this range) in which the band in use detector must indicate that the line is not in use, before attempting a transmission. After completing a transmission when band-in-use is enabled for the system, the application should wait 125 ms before the next transmission.

- **Band-In-Use (BIU):** A Band-In-Use detector, as defined under CENELEC EN 50065-1, is active whenever a signal that exceeds 86 dBuVrms in the range 131.5 KHz to 133.5 KHz is present for at least 4 ms. This threshold can be configured for different end-system applications not requiring CENELEC compliance. The modem tries to retransmit after every 85 to 115 ms when the Band is in use. The Transmitter times out after 1.1 seconds to 3 seconds (depending on the noise on the Powerline) and generates an interrupt to indicate that the transmitter was unable to acquire the Powerline.

Powerline Transceiver Packet

The Powerline Network Protocol defines a Powerline Transceiver (PLT) packet structure, which is used for data transfer between nodes across the Powerline. Packet formation and data transmission across the Powerline network is implemented internally in CY8CPLC10.

A PLT Packet is apportioned into a variable length header (minimum 6 bytes to maximum 20 bytes, depending on address type), a variable length payload (minimum 0 bytes to maximum 31 bytes), and a packet CRC byte.

This packet (preceded by a one byte preamble "0xAB") is then transmitted by the Powerline Modem PHY and the external coupling circuit across the Powerline.

The format of the PLT packet is shown in [Table 1](#).

Table 1. Powerline Transceiver (PLT) Packet Structure

Byte Offset	Bit Offset							
	7	6	5	4	3	2	1	0
0x00	SA Type	DA Type	Service Type	RSVD	Response	RSVD		
0x01	Destination Address (8-bit Logical, 16-bit Extended Logical or 64-bit Physical)							
0x02	Source Address (8-bit Logical, 16-bit Extended Logical or 64-bit Physical)							
0x03	Command							
0x04	RSVD		Payload Length					
0x05	Seq Num			Powerline Packet Header CRC				
0x06	Payload (0 to 31 Bytes)							
	Powerline Transceiver Packet CRC							

Packet Header

The Packet Header comprises the first six bytes of the packet when 1-byte logical addressing is used. When 8-byte physical addressing is used, the source and destination addresses each contain eight bytes. In this case, the header can consist of a maximum of 20 bytes. Unused fields marked RSVD are for future expansion and are transmitted as bit 0. [Table 2](#) describes the PLT Packet Header fields in detail.

Table 2. Powerline Transceiver (PLT) Packet Header

Field Name	No. of Bits	Tag	Description
SA Type	1	Source Address Type	0 - Logical Addressing 1 - Physical Addressing
DA Type	2	Destination Address Type	00 - Logical Addressing 01 - Group Addressing 10 - Physical Addressing 11 - Invalid
Service Type	1		0 - Unacknowledged Messaging 1 - Acknowledged Messaging
Response	1	Response	0 - Not an acknowledgement or response packet 1 - Acknowledgement or response packet
Seq Num	4	Sequence Number	Four bit Unique Identifier for each packet between source and destination
Header CRC	4		Four bit CRC Value. This enables the receiver to suspend receiving the rest of the packet if its header is corrupted

Payload

The packet payload has a length of 0 to 31 bytes. Payload content is user defined and can be read or written through I²C.

Packet CRC

The last byte of the packet is an 8-Bit CRC value used to check packet data integrity. This CRC calculation includes the header and payload portions of the packet and is in addition to the Powerline Packet Header CRC.

Sequence Numbering

The sequence number is increased for every new unique packet transmitted. If in acknowledged mode and an acknowledgment is not received for a given packet, that packet is re-transmitted (if TX_Retry > 0) with the same sequence number. If in unacknowledged mode, the packet is transmitted (TX_Retry + 1) times with the same sequence number.

If the receiver receives consecutive packets from the same source address with the same sequence number and packet CRC, it does not notify the host of the duplicate packet reception. If in acknowledged mode, it still sends an acknowledgment so that the transmitter knows that the packet was received.

Addressing

The logical address of the PLC node is set through software by the external host controller or by a remote node on the Powerline. The logical address can also be set through hardware with the 3-bit LOG_ADDR (Logical Address) Port (for example, an on-board 3-bit DIP switch). However, it is overwritten when set in software. Every CY8CPLC10 chip also has a unique 64-bit physical address which can be used for assigning the logical addresses.

All the address pins are logically inverted, that is, applying a high voltage on these pins corresponds to writing a logic '0' and vice versa.

Group Membership

Group Membership enables the user to multicast messages to select groups. The CY8CPLC10 supports two types of group addressing.

- **Single Group Membership:** The Network protocol supports up to 256 different groups on the network in this mode. In this mode, each PLC node can only be part of a single group. For example, multiple PLC nodes can be part of Group 131.
- **Multiple Group Membership:** The Network protocol supports eight different groups in this mode and each PLC node can be a part of multiple groups. For example, a single PLC node can be a part of Group 3, Group 4, and Group 7 at the same time.

Both these modes can also be used together for Group membership. For example, a single PLC node can be a part of Group 131 and also multiple groups such as Group 3, Group 4, and Group 7.

The Group membership ID for broadcasting messages to all nodes in the network is 0x00.

The Service Type is always set to Unacknowledgment Mode in Group Addressing Mode. This is to avoid Acknowledgment flooding on the Powerline during multicast.

CY8CPLC10 Memory Map

Table 3 gives the detailed CY8CPLC10 memory location information. This information can be used for application development on an external host controller. Several PLC Commands are instantiated from the Powerline Network Protocol based on which memory location is written.

Table 3. CY8CPLC10 Memory Map

Offset	Register Name	Access	7	6	5	4	3	2	1	0	
0x00	INT_Enable	RW	INT_Clear	INT_Polarity	INT_UnableTo TX	INT_TX_NO_ACK	INT_TX_NO_RESP	INT_RX_Packet_Dropped	INT_RX_Data_Available	INT_TX_Data_Sent	
0x01	Local_LA_LSB	RW	8 - bit Logical Address/LSB for extended 16-bit address								
0x02	Local_LA_MSB	RW	MSB for extended 16-bit address								
0x03	Local_Group	RW	8-bit Group Address								
0x04	Local_Group_Hot	RW	One Hot Encoded (e.g. if byte = 0b00010001, then member of groups #5 and #1)								
0x05	PLC_Mode	RW	TX_Enable	RX_Enable	Lock Configuration	Disable_BIU	Rx_Overwrite	Set_Ext_Address	Promiscuous_MASK	Promiscuous_CRC_MASK	
0x06	TX_Message_Length	RW	Send_Message	Reserved		Payload_Length_MASK					
0x07	TX_Config	RW	TX_SA_Type	TX_DA_Type		TX_Service_Type	TX_Retry				
0x08	TX_DA	RW	Remote Node Destination Address (8 bytes)								
0x10	TX_CommandID	RW	TX Command ID								
0x11	TX_Data	RW	TX Data (31 bytes)								
0x30	Threshold_Noise	RW	Reserved	Auto_BIU_Threshold	Reserved			BIU_Threshold_Constant			
0x31	Modem_Config	RW	Reserved	TX_Delay		Reserved	Modem_FSKBW_MASK	Reserved	Modem_BPS_MASK		
0x32	TX_Gain	RW	Reserved				TX_Gain				
0x33	RX_Gain	RW	Reserved					RX_Gain			
0x34-0x3F	Reserved	RW	Reserved								
0x40	RX_Message_INFO	R	New_RX_Msg	RX_DA_Type	RX_SA_Type	RX_Msg_Length					
0x41	RX_SA	R	Remote Node Source Address (8 Bytes)								
0x49	RX_CommandID	R	RX Command ID								
0x4a	RX_Data	R	RX Data (31 bytes)								
0x69	INT_Status	R	Status_Value_Change	Reserved	Status_BUSY	Status_TX_NO_ACK	Status_TX_NO_RESP	Status_RX_Packet_Dropped	Status_RX_Data_Available	Status_TX_Data_Sent	
0x6A	Local_PA	R	Physical Address (8 bytes), "0x6A -> MSB"								
0x72	Local_FW	R	Version Number								

Table 4 gives the description of the various fields outlined in Table 3 on page 6 [1].

Table 4. Memory Field Description

Field Name	No. of Bits	Description
INT_Enable Register (0x00) for the HOST_INT pin		
INT_Clear	1	0 - INT Cleared (W) 1 - INT Triggered (Set Internally) Note: The user should set this bit to Logic 0 after reading the INT_Status register. This clears the INT_Status register, except for Status_RX_Packet_Dropped and Status_RX_Data_Available.
INT_Polarity	1	0 - Active High 1 - Active Low
INT_UnableToTX	1	Enable Interrupt for BIU Timeout and the Modem is unable to Transmit if Disable BIU = 0
INT_TX_NO_ACK	1	Enable Interrupt for no acknowledgment received if Service Type = 1 (Ack Mode)
INT_TX_NO_RESP	1	Enable Interrupt for No Response Received
INT_RX_Packet_Dropped	1	Enable Interrupt when RX Packet is dropped because RX Buffer is full. Note: If there is a prior status change that hasn't been cleared (Status_Value_Change = '1') when an RX Packet is dropped, the HOST_INT pin will be asserted regardless of the value of this bit.
INT_RX_Data_Available	1	Enable Interrupt when RX buffer has new data. Note: If there is a prior status change that hasn't been cleared (Status_Value_Change = '1') when a new message is received, the HOST_INT pin will be asserted regardless of the value of this bit.
INT_TX_Data_Sent	1	Enable Interrupt when TX data is sent successfully
PLC_Mode Register (0x05)		
TX_Enable	1	0 - TX Disabled (Can send ACKs only) 1 - TX Enabled
RX_Enable	1	0 - RX Disabled (Can Receive ACKs only) 1 - RX Enabled
Lock_Configuration	1	0 - Allow Remote Access to change config (TX Enable, Ext Address, Disable BIU, Threshold Value, Logical Address, Group Membership) 1 - Lock Remote Access to change config
Disable_BIU	1	0 - Enables Band-In-Use 1 - Disables Band-In-Use
RX_Overwrite	1	0 - If RX Buffer is full, new RX Message is dropped 1 - If RX Buffer is full, new RX Message overwrites RX Buffer
Set_Ext_Address	1	0 - 8-bit Addressing Mode 1 - Extended 16-bit Addressing Mode Note: This mode should be the same in all the devices in the network
Promiscuous_MASK	1	0 - Drops the RX Message if Destination Address does not match the Local Address 1 - Ignores Destination Address match and accepts all CRC-verified RX Messages
Promiscuous_CRC_MASK	1	0 - Drops the RX Message if the 8-bit packet CRC fails 1 - Ignores the 8-bit packet CRC and accepts all RX Messages if Destination Address matches Local Address
TX_Message_Length Register (0x06)		
Send_Message	1	0 - Transmitter is idle. Automatically cleared after each Transmit 1 - Triggers the Transmit to send message in TX Data across Powerline Note: The registers TX Config, TX Destination Address, TX Command ID and TX Data need to be set before the user sets this bit to Logic 1
Payload_Length_MASK	5	5-bit value for variable payload length. The payload length can vary from 0 to 31.

Note

- To ensure that the receiver has sufficient time to start up and read the first byte, the transmit delay parameter (Modem_TXDelay) should be set to ≥ 18 ms for 600 bps and ≥ 12 ms for 1200 bps. For 1800 bps and 2400 bps, the delay can be set to any value.

Table 4. Memory Field Description (continued)

Field Name	No. of Bits	Description
TX_Config Register(0x07.)		
TX_SA_Type	1	0 - Logical Address 1 - Physical Address
TX_DA_Type	2	00 - Logical Address 01 - Group Address 10 - Physical Address 11 - Invalid
TX_Service_Type	1	0 - Unacknowledgement mode 1 - Acknowledgement Mode
TX_Retry	4	4-bit value for variable TX Retry Count
TX_DA Register (0x08 - 0x0F)		
8-bit Logical Address		0x08
16-bit Logical Address		0x08 - LSB 0x09 - MSB
64-bit Physical Address		0x08 - MSB 0x0F - LSB
Threshold_Noise Register (0x30)		
Auto_BIU_Threshold	1	0 - Auto Set Threshold is disabled 1 - Auto Set Threshold is enabled. This state overrides the Threshold Values in Register 0x30.
BIU_Threshold_Constant	3	000 - 70 dBuVrms 001 - 75 dBuVrms 010 - 80 dBuVrms 011 - 87 dBuVrms (default) 100 - 90 dBuVrms 101 - 93 dBuVrms 110 - 96 dBuVrms 111 - 99 dBuVrms
Modem_Config Register (0x31)		
TX_Delay	2	00 - 7 ms 01 - 13 ms 10 - 19 ms 11 - 25 ms
Modem_FSK_BW_MASK	1	0 - Logic '0' - 133.3 kHz Logic '1' - 131.8 kHz 1 - Logic '0' - 133.3 kHz Logic '1' - 130.4 kHz
Modem_BPS_MASK	2	00 - 600 bps ^[1] 01 - 1200 bp ^[1] 10 - 1800 bps 11 - 2400 bps (default)

Table 4. Memory Field Description (continued)

Field Name	No. of Bits	Description
TX_Gain Register (0x32)		
TX_Gain	4	The following values are the output AC voltage swing for the given settings: 0000 - 55 mVp-p 0001 - 75 mVp-p 0010 - 100 mVp-p 0011 - 125 mVp-p 0100 - 180 mVp-p 0101 - 250 mVp-p 0110 - 360 mVp-p 0111 - 480 mVp-p 1000 - 660 mVp-p 1001 - 900 mVp-p 1010 - 1.25 Vp-p 1011 - 1.55 Vp-p (default) 1100 - 2.25 Vp-p 1101 - 3.00 Vp-p 1110 - 3.50 Vp-p 1111 - Reserved
RX_Gain Register (0x33)		
RX_Gain	3	The following values are the minimum RX input sensitivity for the given settings: 000 - 5 mVrms (default) 001 - 5 mVrms 010 - 2.5 mVrms 011 - 1.25 mVrms 100 - 600 μ Vrms 101 - 350 μ Vrms 110 - 250 μ Vrms 111 - 125 μ Vrms
RX_Message_INFO Register (0x40)		
New_RX_Msg	1	0 - No Packet received 1 - New Packet received Note: User sets this bit to Logic 0 after reading the RX Message. This allows the device to receive a new RX message. This also clears the Status_Value_Change, Status_RX_Packet_Dropped, and Status_RX_Data_Available bits in the INT_Status register.
RX_DA_Type	1	0 - Logical / Physical Addressing 1 - Group Addressing
RX_SA_Type	1	0 - Logical Address 1 - Physical Address
RX_Msg_Length	5	5-bit value for variable payload length. The payload length can vary from 0 to 31.
RX_SA Register (0x41 - 0x48)		
8-bit Logical Address		0x41
16-bit Logical Address		0x41 - LSB 0x42 - MSB
64-bit Physical Address		0x41 - MSB 0x48 - LSB
INT_Status Register (0x69)		
Note: When the user sets INT_Clear to Logic 0, every bit in this register (except Status_RX_Packet_Dropped and Status_RX_Data_Available) will be cleared to Logic 0. When the user sets New_RX_MSG, the Status_Value_Change, Status_RX_Packet_Dropped and Status_RX_Data_Available bits will be cleared to Logic 0.		
Status_Value_Change	1	0 - No Change 1 - Change

Table 4. Memory Field Description (continued)

Field Name	No. of Bits	Description
Status_BUSY	1	0 - No BIU Timeout 1 - BIU Timeout or transmission is attempted when TX_Enable = 0
Status_TX_NO_ACK	1	If Service Type = 1 (ACK Mode) 0 - ACK Received (when TX Data sent = 1) 1 - No ACK received (when TX Data sent = 0) Note: The timeout window for receiving the ACK is 500ms
Status_TX_NO_RESP	1	0 - Response Received (when TX Data sent = 1) 1 - No Response Received (when TX Data sent = 0) Note: The timeout window for receiving Responses is 1.5s
Status_RX_Packet_Dropped	1	If RX Overwrite = 0 0 - No RX Packet is dropped 1 - RX Packet is dropped because RX Buffer is full
Status_RX_Data_Available	1	0 - No new data available in RX buffer 1 - RX buffer has new data available
Status_TX_Data_Sent	1	0 - No TX data sent 1 - TX data sent successfully

Baud rate

Sets the baud rate for the Powerline Communication PHY. You can configure the baud rate to 600, 1200, 1800, or 2400 bits per second. To ensure that the receiver has sufficient time to start up and read the first byte, the transmit delay parameter (Modem_TXDelay) should be set to ≥ 19 ms for 600 bps and ≥ 13 ms for 1200 bps. For 1800 bps and 2400 bps, the delay can be set to any value.

TX Gain

Sets the gain of the transmitter's programmable gain amplifier.

RX Gain

Sets the gain of the receiver's programmable gain amplifier. This in turn determines the minimum input sensitivity for the receiver.

Noise Level Threshold

Sets the Noise Level Threshold for Brand In Use (BIU) detection.

FSK Bandwidth

Sets the separation of the FSK signals representing logic '1' and logic '0'. Can either be set to a deviation of ~ 1.5 kHz or ~ 3 kHz. The logic '0' frequency is always 133.3 kHz. The logic '1' frequency can be configured to either 131.8 kHz or 130.4 kHz.

This parameter is sometimes referred to as FSK Deviation.

Modem_TXDelay

Sets the amount of delay from when the transmission is initiated to when the data starts being output from the Transmit Programmable Gain Amplifier. This gives the external circuitry time to set up. The TX_Shutdown signal (Port2[7]) is set before the delay.

BIU Timeout

Sets the condition for timing out the BIU detector. It can be either on the first BIU detection of a signal or if the BIU detector can't acquire the line after 1.1 seconds. (This value can be up to 3.5s depending on the amount of noise on the line).

ACK Timeout

Sets the amount of time that the device will wait for an acknowledgment after it completes the transmission of a packet. This only applies when the Service Type is acknowledgment mode. The time can be a fixed 500ms, or can be based on the expected time to receive the acknowledgment packet plus a buffer. For example, the "Auto + 20ms" property will set the timeout to be 20 ms longer than the time it would normally take to receive the acknowledgement. This gives the receiver extra time to perform other functions in between checking for a received message. The calculation is based on the length of the acknowledgment packet, the baud rate, and the Modem_TXDelay.

Addressing Mode

Sets the logical addressing length to 8-bit or 16-bit.

Logical Address of Node

Set the logical address for the Powerline node. The available addresses vary depending on whether 8-bit or 16-bit addressing is used.

Transmit Enable

Enables Transmit Mode operation. When transmit mode is disabled, no new messages are transmitted. Acknowledgments are transmitted, regardless of Transmit Enable.

Transmit Source Address Type

Sets the Transmit SA Type. Choose Logical Address or Physical Address. You cannot change this parameter if Transmit Enable is set to Disable.

Transmit Destination Address Type

Sets the Transmit DA Type. Choose from Logical Address, Group Address, and Physical Address. This parameter is not editable if the Transmit Enable option is set to Disable.

Transmit Service Type

Sets the Transmit Acknowledgment Mode. Transmissions are acknowledged in acknowledgement mode. This parameter is not editable if the Transmit Enable option is set to Disable.

Transmit Retry Count

Sets the transmitter retry count. In Acknowledgment mode, sets the maximum transmit retries if no acknowledgment is received. In Unacknowledgment mode, sets how many times the transmitter retransmits the same packet. This parameter is not editable if the Transmit Enable option is set to Disable.

Transmit Payload Length

Sets the Payload Length from 0 to 31 bytes. This parameter is not editable if the Transmit Enable option is set to Disable.

Receive Enable

Enables Receive Mode. When receive mode is disabled, no new messages are accepted.

Lock Configuration

Allows remote access to change the configuration.

Rx Overwrite

Enables receive buffer overwrite mode. When enabled, newly received messages overwrite the Rx Buffer when it contains an unread packet. When disabled and the Rx Buffer contains an unread packet, the newly received message is dropped. To clear the RX buffer, the New_RX_Msg must be set to '0'.

Destination Address Verification

Allows the receiver to ignore destination address verification. When the setting is Do Not Ignore the received packet is dropped if it does not match the local address. When set to Ignore, the received packet is accepted regardless of the local address.

CRC Messages Verification

Allows the receiver to ignore cyclic redundancy check message verification. When the setting is Do Not Ignore the packet is dropped if the 8-bit packet CRC fails.

Single Group Membership ID

Sets the group number when the network is placed in 'single group membership' mode.

Multiple Group Membership ID

Sets the group number when network is placed in 'multiple group membership' mode. This parameter is an 8-bit value and is expressed in binary. Each instance of 1 in the number indicates that the group is member of the group corresponding to the binary position of the number. For example, if the value is 01000001, then the particular node is part of the 1st and 7th group.

I2C Slave Address

Can be any value from 0x01 to 0x7F.

External Host Application

The application residing on the external host microcontroller has direct access to the local PLC memory over I²C. The I²C communication enables the host controller to instantiate several PLC functions by reading or writing to the appropriate memory locations in the PLC chip. Thus the host application can configure the CY8CPLC10, read status and configuration information, and transmit data to remote Powerline nodes. Refer to the CY8CPLC10 application note (AN52478 at <http://www.cypress.com>) on how to build a PLC command set using the CY8CPLC10 memory map. The device has a dedicated pin (I2C_ADDR) for selecting the I²C slave address while communicating with the external controller. The two I²C slave addresses available are 0x01 and 0x7A.

Remote Commands

In addition to sending normal data over the Powerline, the CY8CPLC10 can also send (and request) control information to (and from) another node on the network. The type of remote command to transmit is set by the TX_CommandID register and when received, is stored in the RX_CommandID register.

When a control command (Command ID = 0x01 - 0x08 and 0x0C - 0x0F) is received, the protocol automatically processes the packet (if Lock_Configuration is '0'), responds to the initiator, and notifies the host of the successful transmission and reception.

When the send data command (ID 0x09) or request for data command (ID 0x0A) is received, the protocol replies with an acknowledgment packet (if TX_Service_Type = '1'), and notifies the host of the new received data. If the initiator does not receive

the acknowledgment packet within 500 ms, it notifies the host of the 'no acknowledgment received' condition.

When a response command (ID 0x0B) is received by the initiator within 1.5s of sending the request for data command, the protocol notifies the host of the successful transmission and reception. If the response command is not received by the initiator within 1.5s, it notifies the host of the no response received condition.

The host is notified by updating the appropriate values in the INT_Status register (including Status_Value_Change) and asserting the HOST_INT pin (if the corresponding bit is set in the INT_Enable register).

The command IDs 0x30-0xff can be used for custom commands that will be processed by the external host (for example, set an LED color, get a temperature/voltage reading).

The available remote commands are described in Table 5 with the respective Command IDs.

EEPROM Back Up for Remote Reset

The device also has an EEPROM to back up Memory Registers 0x00-0x05 and 0x30-0x33. When the device is reset remotely by the SetRemote_Reset command (described in Table 5), it clears its memory map and loads from the EEPROM and returns to idle mode.

Table 5. Remote Commands

Cmd ID	Command Name	Description	Payload (TX Data)	Response (RX Data)
0x01	SetRemote_TXEnable	Sets the TX Enable bit in the PLC Mode Register. Rest of the PLC Mode register is unaffected	0 - Disable Remote TX 1 - Enable Remote TX	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x02	SetRemote_Reset	Reset the Remote Node Configuration	None	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x03	SetRemote_ExtendedAddr	Set the Addressing to Extended Addressing Mode	0 - Disable Extended Addressing 1 - Enable Extended Addressing	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x04	SetRemote_LogicalAddr	Assigns the specified logical address to the remote PLC node	If Ext Address = 0, Payload = 8-bit Logical Address If Ext Address = 1, Payload = 16-bit Logical Address	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x05	GetRemote_LogicalAddr	Get the Logical Address of the remote PLC node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, {If Ext Address = 0, Response = 8-bit Logical Address If Ext Address = 1, Response = 16-bit Logical Address}

Table 5. Remote Commands (continued)

Cmd ID	Command Name	Description	Payload (TX Data)	Response (RX Data)
0x06	GetRemote_PhysicalAddr	Get the Physical Address of the remote PLC node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = 64-bit Physical Address
0x07	GetRemote_State	Request PLC_Mode Register content from a Remote PLC node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = Remote PLC Mode register
0x08	GetRemote_Version	Get the Version Number of the Remote Node	None	If TX Enable = 0, Response = None If TX Enable = 1, Response = Remote Version register
0x09	SendRemote_Data	Transmit data to a Remote Node.	Payload = Local TX Data	If Local Service Type = 0, Response = None If Local Service Type = 1, Response = Ack
0x0A	RequestRemote_Data	Request data from a Remote Node	Payload = Local TX Data	If Local Service Type = 1, Response = Ack Then, the remote node host must send a ResponseRemote_Data command. The response must be completely transmitted within 1.5s of receiving the request. Otherwise, the requesting node will time out.
0x0B	ResponseRemote_Data	Transmit response data to a Remote Node.	Payload = Local TX Data	None
0x0C	SetRemote_BIU	Enables/Disables BIU functionality at the remote node	0 - Enable Remote BIU 1 - Disable Remote BIU	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0D	SetRemote_ThresholdValue	Sets the Threshold Value at the Remote node	3-bit Remote Threshold Value	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0E	SetRemote_GroupMembership	Sets the Group Membership of the Remote node	Byte0 - Remote Single Group Membership Address Byte1 - Remote Multiple Group Membership Address	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0F	GetRemote_GroupMembership	Gets the Group Membership of the Remote node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = Byte0 - Remote Single Group Membership Address Byte1 - Remote Multiple Group Membership Address
0x10 - 0x2F	Reserved			
0x30 - 0xFF	User Defined Command Set			

Target Applications

Lighting Control

CY8CPLC10 enables control of incandescent, sodium vapor, fluorescent, and LED lighting fixtures over existing Powerlines. Cypress's Powerline communication solution easily integrates with wall-switch dimmers and lamp and appliance modules, enabling on and off, dimming, color mixing, and tunable white light control. The CY8CPLC10 can control individual or a group of lighting fixtures in a home or a commercial building. Elaborate lighting scenes can be created using application software. Household lighting fixtures can also be programmed to turn on and off at user defined intervals using a PC based Graphical User Interface.

Figure 5. Powerline Communication for Home Lighting

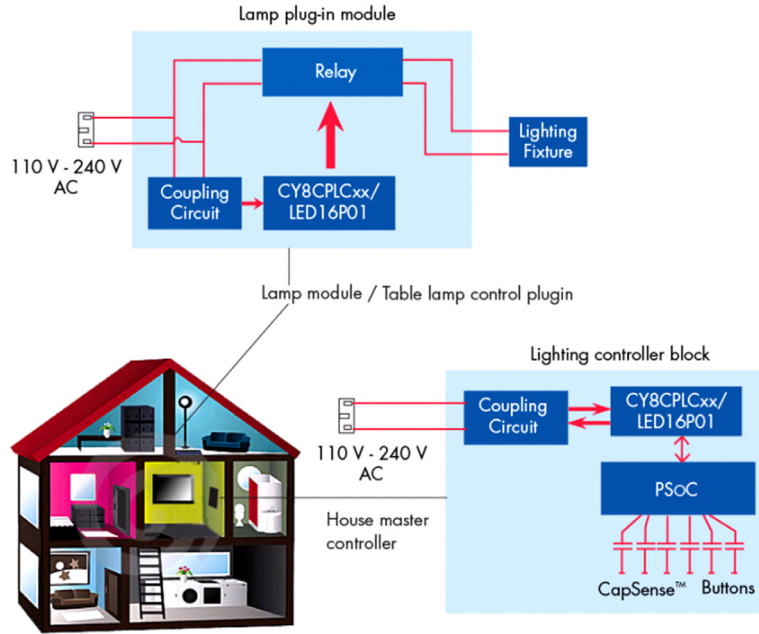
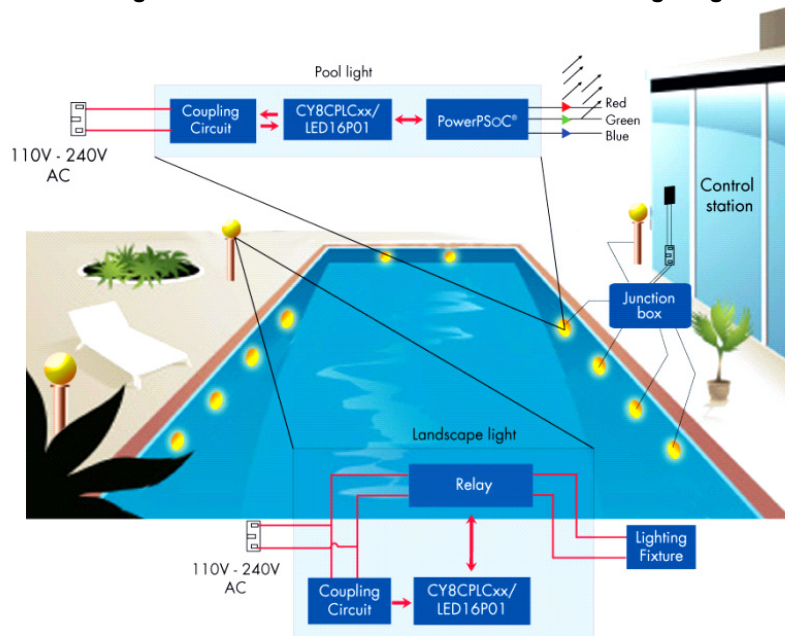


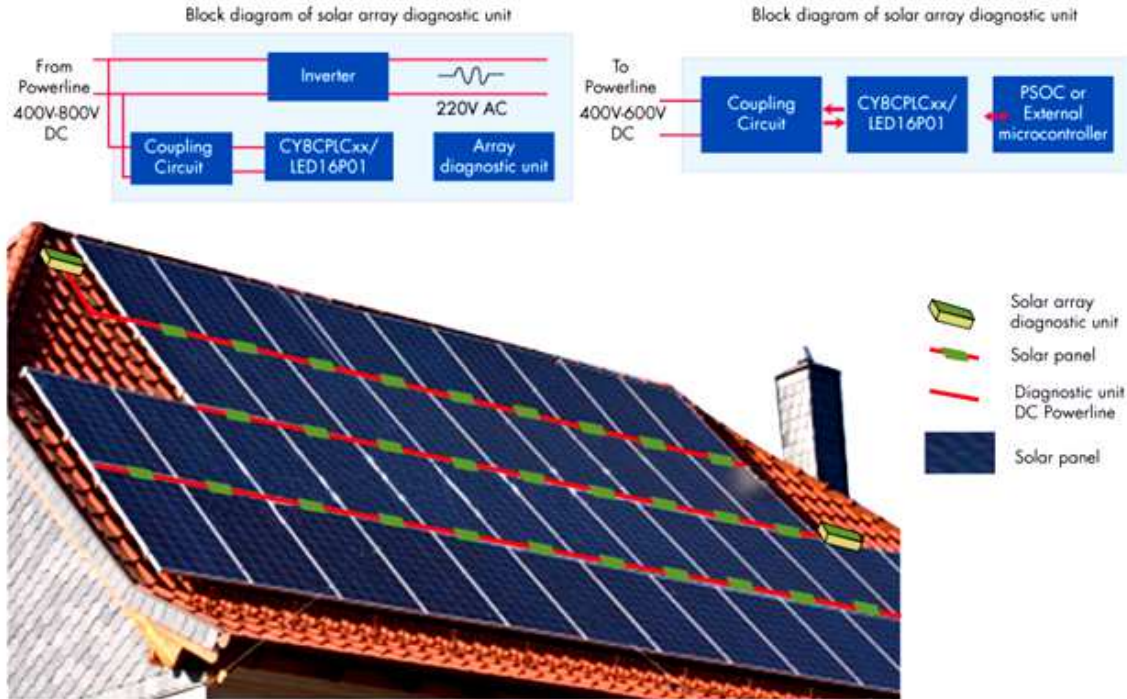
Figure 6. Powerline Communication for Pool Lighting



Smart Energy Management

Using the CY8CPLC10, individual panels in a solar array can transmit diagnostic data over the existing DC powerlines. An Array Diagnostic Unit Controller can communicate with individual solar panels to probe specific diagnostic information. When the diagnostic data is collected by the controller, it is transmitted across the Powerline to a data monitoring console. This makes it possible to acquire and transmit real time data regarding energy output of individual panels to the array controller and subsequently even to a solar farm control station over the Powerline.

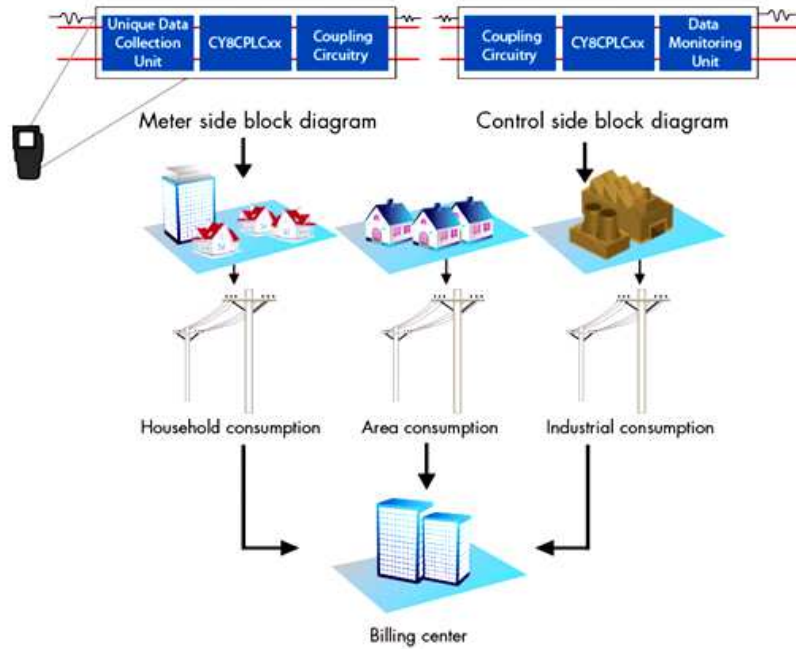
Figure 7. Powerline Communication for Smart Energy Management (Solar Diagnostics)



Automatic Meter Reading

The CY8CPLC10 can be designed in electric meters in household and industrial environments to transmit power usage information to a centralized billing system. The Cypress Powerline communication solution is ideally suited to handle multiple data sources because of the in-built Network Protocol Stack that enables individual addressing of multiple nodes on the same Powerline. In physical addressing mode, up to 2^{64} power meters can transmit usage statistics to the local billing center. Application Layer software can be used to provide real time usage statistics to a customer. Energy utilities can improve customer service and control meter reading costs, especially in areas where accessing meters is difficult or unsafe, while making the invoicing process more efficient.

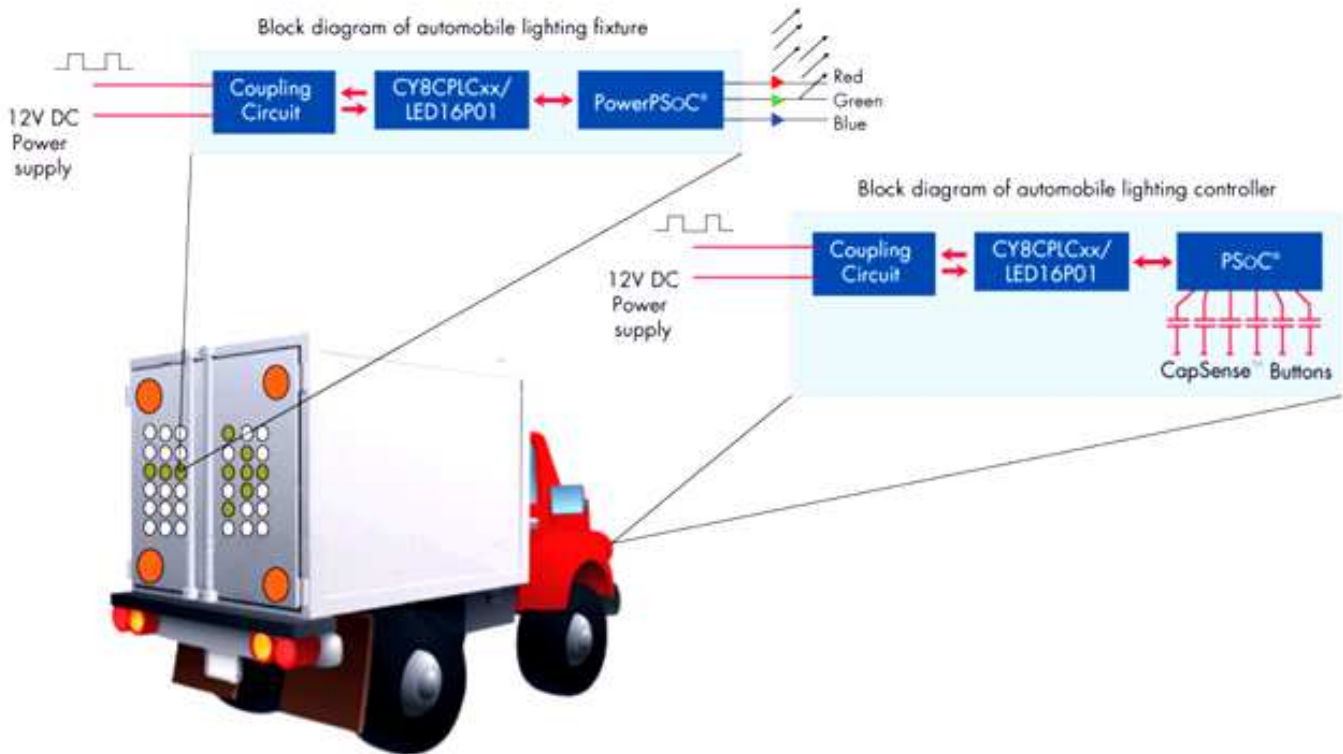
Figure 8. Powerline Communication for Automatic Meter Reading



Industrial Signage

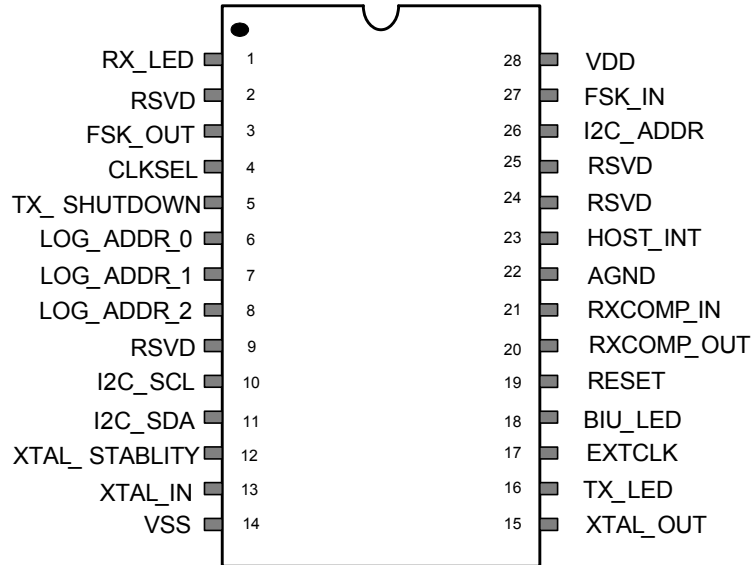
An entire array of new convenience and advanced control features are available in automobiles today. It is projected that a high feature content car cannot have enough space to contain multiple wiring segments and connectors without compromising power loss and safety. One solution is to reduce the number of cables by using existing Powerline as the transmission medium of digital control signals. The CY8CPLC10 enables control of Automotive LED strobe, beacon, tail lights, and indicators over the existing direct current (DC) 12V to 42V battery Powerline. Combined with Cypress's EZ-Color lighting solution, dimming and color mixing of LED based automotive lighting fixtures in applications such as mobile LED displays is possible.

Figure 9. Powerline Communication for Industrial Signage



Pinouts

Figure 10. CY8CPLC10 28-pin SSOP



Pin Definitions

Pin Number	Pin Name	I/O	Description
1	RX_LED	Output	RX Indicator LED
2	RSVD	Reserved	Reserved Pin ^[2]
3	FSK_OUT	Analog Output	Analog FSK Output. This signal is coupled to the powerline through an external coupling circuit
4	CLKSEL	Input (Internal Pull up)	FSK Modem Clock Source Select Logic '0' – External Clock Oscillator (EXTCLK) selected Logic '1' – External Crystal (XTAL_IN, XTAL_OUT) selected Note: The external crystal (XTAL_IN, XTAL_OUT) is always required for the protocol timing.
5	TX_SHUTDOWN	Output	Output to Disable external transmit circuitry during Receive Mode. Logic '0' - When the Modem is transmitting Logic '1' - When the Modem is not transmitting
6	LOG_ADDR_0	Input (Internal Pull up)	Connected to the Least Significant Bit of the 3-bit Logical Address. This is an inverted pin; applying a high voltage on this pin corresponds to writing a logic '0' and vice versa.
7	LOG_ADDR_1	Input (Internal Pull up)	Connected to the 2nd Most Significant Bit of the 3-bit Logical Address. This is an inverted pin; applying a high voltage on this pin corresponds to writing a logic '0' and vice versa.
8	LOG_ADDR_2	Input (Internal Pull up)	Connected to the Most Significant Bit of the 3-bit logical address. This is an inverted pin; applying a high voltage on this pin corresponds to writing a logic '0' and vice versa.
9	RSVD	Reserved	Reserved pin ^[2]
10	I2C_SCL	Input	I ² C Serial Clock
11	I2C_SDA	Input/Output	I ² C Serial Data

Note

2. Reserved pins must be left unconnected.

Pin Definitions (continued)

Pin Number	Pin Name	I/O	Description
12	XTAL_STABILITY	Input/Output	External Crystal Stability. Connect a 0.1 μ F capacitor between the pin and VSS.
13	XTAL_IN	Input	External Crystal Input. This is the input clock from an external crystal oscillator. This crystal is always required for protocol timing.
14	Vss	Ground	Ground
15	XTAL_OUT	Output	External Crystal Output. This pin is used along with XTAL_IN to connect to the external oscillator. This crystal is always required for protocol timing.
16	TX_LED	Output	TX Indicator LED
17	EXTCLK	Input	Optional external 24 MHz clock oscillator input for PLC modem.
18	BIU_LED	Output	BIU Indicator LED
19	RESET	Reset	Reset Pin
20	RXCOMP_OUT	Analog Output	Analog Output to the external Low Pass Filter circuitry.
21	RXCOMP_IN	Analog Input	Analog Input from the external Low Pass Filter circuitry
22	AGND	Ground	Analog Ground. Connect a 1.0 μ F capacitor between the pin and VSS.
23	HOST_INT	Output	Interrupt Output to Host Controller. Polarity and enable are configured by the INT_Enable register.
24	RSVD	Reserved	Reserved Pin ^[3]
25	RSVD	Reserved	Reserved Pin ^[3]
26	I2C_ADDR	Input (Internal Pull up)	Set I2C Slave Address. When high - Slave Address '0x01' When low - Slave Address '0x7A'
27	FSK_IN	Input	Analog FSK Input. This is the input signal from the Powerline.
28	VDD	Power	Supply Voltage. 5V \pm 5%

Note

- Reserved pins must be left unconnected.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CPLC10 PLC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at <http://www.cypress.com>.

Absolute Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Table 6. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T _{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrades reliability.
T _{BAKETEMP}	Bake Temperature	–	125	See package label	°C	
T _{BAKETIME}	Bake Time	See package label	–	72	Hours	
T _A	Ambient Temperature with Power Applied	-40	–	+85	°C	
V _{dd}	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V _{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V _{IOZ}	DC Voltage Applied to Tristate	Vss - 0.5	–	Vdd + 0.5	V	
I _{MIO}	Maximum Current into any Input/Output Pin	-25	–	+50	mA	
I _{MAIO}	Maximum Current into any Input/Output Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up Current	–	–	200	mA	

Operating Temperature

Table 7. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T _A	Ambient Temperature	-40	–	+85	°C	
T _J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 24. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics
DC Power Supply

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 8. DC Power Supply

Symbol	Description	Min	Typ	Max	Units	Notes
V _{DD}	Supply Voltage	4.75	–	5.25	V	
I _{DD} (TX Mode)	Supply current (TX Mode)		30		mA	Conditions are 5.0V, T _A = 25°C
I _{DD} (RX Mode)	Supply current (RX Mode)		41		mA	Conditions are 5.0V, T _A = 25°C

DC I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9. DC I/O Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R _{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R _{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V _{OH}	High Output Level	V _{DD} - 1.0	–	–	V	I _{OH} = 10 mA
V _{OL}	Low Output Level	–	–	0.75	V	I _{OL} = 25 mA
I _{OH}	High Level Source Current	10	–	–	mA	V _{OH} = V _{DD} - 1.0V. See the limitations of the total current in the Note for V _{OH} .
I _{OL}	Low Level Sink Current	25	–	–	mA	V _{OL} = 0.75V. See the limitations of the total current in the Note for V _{OL} .
V _{IL}	Input Low Level	–	–	0.8	V	
V _{IH}	Input High Level	2.1	–		V	
V _H	Input Hysteresis	–	60	–	mV	
I _{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C _{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Pin dependent. Temp = 25°C.
C _{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Pin dependent. Temp = 25°C.

DC Modem Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10. DC Modem Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{FSK_OUTDC}	FSK_OUT DC Voltage		V _{DD} /2		V	
V _{FSK_INDC}	FSK_IN DC Voltage		V _{DD} /2		V	

DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 11. DC I²C Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
V _{IL} I2C ^[4]	Input low level	–	–	0.25 × V _{DD}	V	4.75 V ≤ V _{DD} ≤ 5.25 V
V _{IH} I2C ^[4]	Input high level	0.7 × V _{DD}	–	–	V	4.75V ≤ V _{DD} ≤ 5.25 V

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 12. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
T _{XRST}	External Reset Pulse Width	10	–	–	μs	
SR _{POWER UP}	Power Supply Slew Rate	–	–	250	V/ms	V _{dd} slew rate during power up.
T _{POWERUP}	Time from End of POR to Readiness for PLC and I2C Communication	–	1.25	–	s	Power up from 0V.

AC Modem Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 13. AC Modem Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{FSK_OUTH2} _{125mV}	FSK_OUT Second Harmonic (Fundamental = 125 mVp-p)	–	–32	–	dB _C	
V _{FSK_OUTH3} _{125mV}	FSK_OUT Third Harmonic (Fundamental = 125 mVp-p)	–	–9	–	dB _C	
V _{FSK_OUTH2} _{1.55V}	FSK_OUT Second Harmonic (Fundamental = 1.55Vp-p)	–	–34	–	dB _C	
V _{FSK_OUTH3} _{1.55V}	FSK_OUT Third Harmonic (Fundamental = 1.55Vp-p)	–	–15	–	dB _C	
V _{FSK_INMAX}	Maximum FSK_IN Signal	–	V _{DD}	–	Vp-p	

AC I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. Typical parameters apply to 5V at 25°C and are for design guidance only.

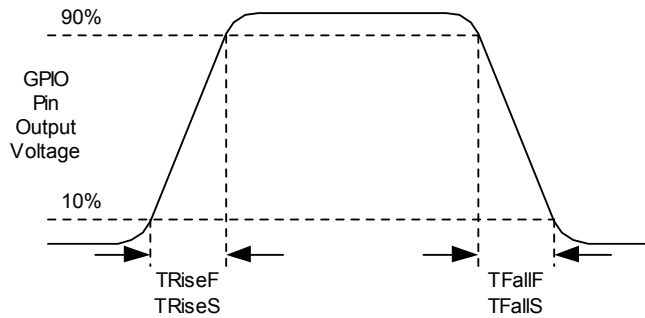
Table 14. AC I/O Specifications

Symbol	Description	Min	Typ	Max	Units ^[5]	Notes
T _{RiseS}	Rise Time, Cload = 50 pF	10	27	–	ns	10% - 90%
T _{FallS}	Fall Time, Cload = 50 pF	10	22	–	ns	10% - 90%

Note

- All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO specifications sections. The I²C GPIO pins also meet the mentioned specs.

Figure 11. I/O Timing Diagram



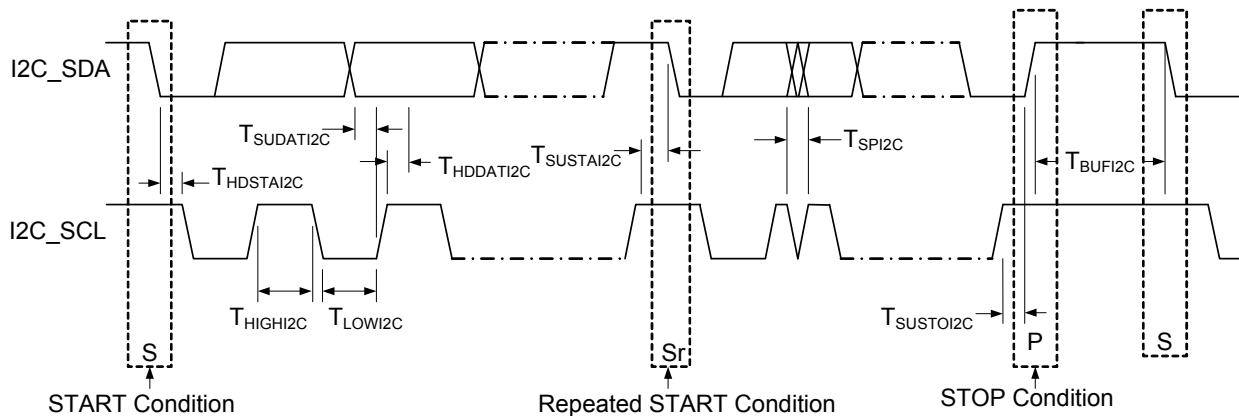
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 15. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Fast-Mode		Units	Notes
		Min	Max		
F _{SCL I2C}	SCL Clock Frequency	0	400	kHz	
T _{HDSTA I2C}	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	0.6	–	μs	
T _{LOW I2C}	LOW Period of the SCL Clock	1.3	–	μs	
T _{HIGH I2C}	HIGH Period of the SCL Clock	0.6	–	μs	
T _{SUSTA I2C}	Setup Time for a Repeated START Condition	0.6	–	μs	
T _{HDDAT I2C}	Data Hold Time	0	–	μs	
T _{SUDAT I2C}	Data Setup Time	100 ^[6]	–	ns	
T _{SUSTOI2C}	Setup Time for STOP Condition	0.6	–	μs	
T _{BUFI2C}	Bus Free Time Between a STOP and START Condition	500	–	μs	
T _{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	0	50	ns	

Figure 12. Definition for Timing on the I²C Bus Packaging Dimensions



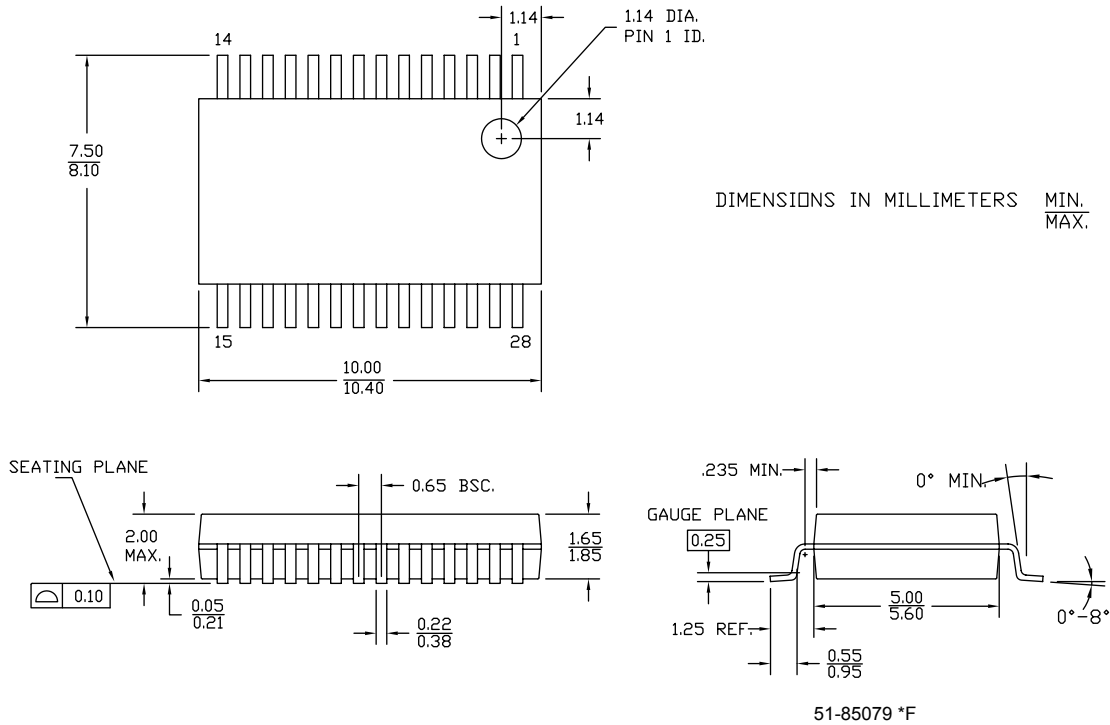
Notes

- 5. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period)
- 6. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement t_{SU, DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU, DAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the CY8CPLC10 PLC device, along with the thermal impedances for the package and the typical package capacitance on crystal pins.

Figure 13. 28-pin SSOP (210 Mils) O28.21 Package Outline, 51-85079



Thermal Impedances

Table 16. Thermal Impedances per Package^[8]

Package	Typical θ_{JA} ^[7]	Typical θ_{JC}
28-pin SSOP	94 °C/W	29 °C/W

Capacitance on Crystal Pins

Table 17. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28-pin SSOP	2.8 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 18. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
28-pin SSOP	260 °C	20 s

Notes

7. $T_J = T_A + \text{POWER} \times \theta_{JA}$

8. To achieve the thermal impedance specified for the QFN package, refer to "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at <http://www.amkor.com>.

Development Tool Selection

Development Kits

The development kits do not have on-board Powerline capability, but can be used with a PLC kit for development purposes. All development tools and development kits are sold at the Cypress Online Store.

CY3215A-DK Basic Development Kit

The [CY3215A-DK](#) is for prototyping and development with PSoC Designer. This kit can be used in conjunction with the PLC kits to support in-circuit emulation. The software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer also supports the advanced emulation features. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Kits

CY3217-MiniProg1

The [CY3217-MiniProg1](#) kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The [CY3210-PSoCEval1](#) kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread

boarding space to meet all your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The [CY3214-PSoCEvalUSB](#) evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator, and plenty of bread boarding space to meet all your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MiniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3217-MiniProg1

The [CY3217-MiniProg1](#) kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable