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PSoC CY8CTMG20x, CY8CTMG20xA, CY8CTST200, CY8CTST200A TRM

PSoC® CY8CTMG20x, CY8CTMG20xA, CY8CTST200, CY8CTST200A

Technical Reference Manual (TRM)

Document No. 001-53603 Rev. *C

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Section A: Overview

The PSoC® family consists of many Programmable System-on-Chip with On-Chip Controller devices. The CY8CTMG20x and CY8CTST200 PSoC devices have fixed analog and digital resources in addition to a fast CPU, Flash program memory, and SRAM data memory to support various TrueTouch™ algorithms.

For the most up-to-date ordering, pinout, packaging, or electrical specification information, refer to the PSoC device's data sheet. For the most current technical reference manual information and newest product documentation, go to the Cypress web site at http://www.cypress.com >> Documentation.

This section contains:

- Pin Information on page 19.

Document Organization

This manual is organized into sections and chapters, according to PSoC functionality. Each section contains a top-level architectural diagram and a register summary (if applicable). Most chapters within the sections have an introduction, an architectural/application description, register definitions, and timing diagrams. The sections are as follows:

- **Overview** – Presents the top-level architecture, helpful information to get started, and document history and conventions. The PSoC device ***pinouts*** are detailed in the chapter Pin Information, on page 19.
- **PSoC Core** – Describes the heart of the PSoC device in various chapters, beginning with an architectural overview and a summary list of registers pertaining to the PSoC core.
- **TrueTouch System** – Describes the configurable PSoC TrueTouch system in various chapters, beginning with an architectural overview and a summary list of registers pertaining to the TrueTouch system.
- **System Resources** – Presents additional PSoC system resources, beginning with an overview and a summary list of registers pertaining to system resources.
- **Registers** – Lists all PSoC device registers in register mapping tables, and presents bit-level detail of each register in its own Register Reference chapter. Where applicable, detailed register descriptions are also located in each chapter.
- **Glossary** – Defines the specialized terminology used in this manual. Glossary terms are presented in ***bold, italic font*** throughout this manual.
- **Index** – Lists the location of key topics and elements that constitute and empower the PSoC devices.

Top Level Architecture

The PSoC block diagram on the next page illustrates the top-level architecture of the CY8CTMG20x and CY8CTST200 devices. Each major grouping in the diagram is covered in this manual in its own section: PSoC Core, TrueTouch System, and the System Resources. Banding these three main areas together is the communication network of the system ***bus***.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses the ***SRAM*** for data storage, an ***interrupt*** controller for easy program execution to new addresses, sleep and watchdog timers, a regulated 3.0V output option is provided for Port 1 I/Os, and multiple ***clock*** sources that include the IMO (internal main oscillator) and ILO (internal low speed oscillator) for precision, programmable clocking.

The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four MIPS 8-***bit*** Harvard architecture microprocessor. Within the CPU core are the ***SROM*** and ***Flash*** memory components that provide flexible programming.

PSoC GPIOs provide connection to the CPU and the TrueTouch resources of the device. Each pin's drive mode is selectable from four options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on low level and change from last read.

TrueTouch™ System

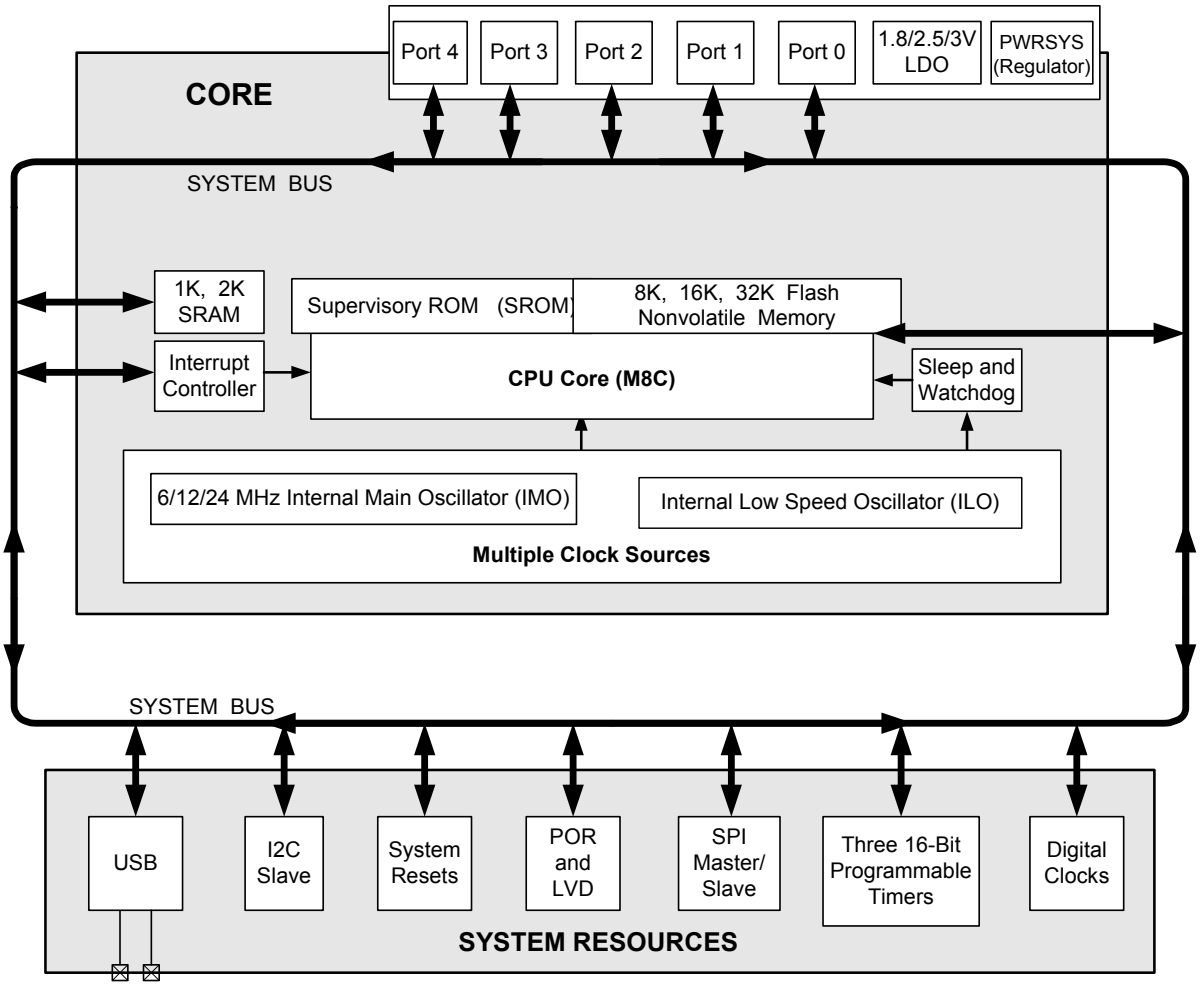
The TrueTouch System is composed of comparators, reference drivers, I/O multiplexers, and digital logic to support various capacitive sensing algorithms. Various reference selections are provided. Digital logic is mainly comprised of counters and timers.

System Resources

The System Resources provide additional PSoCcapability. These system resources include:

- Digital clocks to increase the flexibility of the PSoC programmable system-on-chip.
- I2C functionality with "no bus stalling."
- Various system resets supported by the M8C.
- Power-On-Reset (POR) circuit protection.
- SPI master and slave functionality.
- A programmable timer to provide periodic interrupts.
- Clock boost network providing a stronger signal to switches.
- Full-speed USB interface for USB 2.0 communication with 512 bytes of dedicated buffer memory and an internal 3V regulator.

PSoC Core Top-Level Block Diagram



Getting Started

The quickest path to understanding PSoC is by reading the PSoC device's data sheet and using *PSoC Designer™ Integrated Development Environment (IDE)*. This manual is useful for understanding the details of the PSoC integrated circuit.

Important Note For the most up-to-date Ordering, Packaging, or Electrical Specification information, refer to the individual PSoC device's data sheet or go to http://www.cypress.com.

Support

Free support for PSoC products is available online at http://www.cypress.com. Resources include Training Seminars, Discussion Forums, Application Notes, TightLink Technical Support Email/Knowledge Base, and Application Support Technicians.

Technical Support can be reached at http://www.cypress.com/support.

Product Upgrades

Cypress provides scheduled upgrades and version enhancements for PSoC Designer free of charge. You can order the upgrades from your distributor on CD-ROM or download them directly from http://www.cypress.com under Software. Also provided are critical updates to system documentation under http://www.cypress.com >> Documentation.

Development Kits

The Cypress Online Store contains development kits, ***C*** compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com under Order >> PSoC Kits.

Document History

This section serves as a chronicle of the *PSoC® CY8CTMG20x, CY8CTMG20xA, CY8CTST200, CY8CTST200A Technical Reference Manual*.

Technical Reference Manual History

Version/ Release Date	Originator	Description of Change
** May 2009	DSG	First release of the CY8CTMG20x, CY8CTST200 Technical Reference Manual.
*A August 2009	DSG	Second release of the CY8CTMG20x, CY8CTST200 Technical Reference Manual.
*B November 2009	FSU	Multiple fixes, primarily to the sleep and I2C chapters.
*C December 2009	FSU	Multiple fixes, primarily to the External Crystal Oscillator chapter.

Documentation Conventions

There are only four distinguishing font types used in this manual, besides those found in the headings.

- The first is the use of *italics* when referencing a document title or file name.
- The second is the use of ***bold italics*** when referencing a term described in the Glossary of this manual.
- The third is the use of Times New Roman font, distinguishing equation examples.
- The fourth is the use of `Courier New` font, distinguishing code examples.

Register Conventions

The following table lists the register conventions that are specific to this manual. A more detailed set of register conventions is located in the Register Reference chapter on page 187.

Register Conventions

Convention	Example	Description
'x' in a register name	PRTxIE	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
O	RO : 00	Only a read/write register or bit(s).
L	RL : 00	Logical register or bit(s)
C	RC : 00	Clearable register or bit(s)
00	RW : 00	Reset value is 0x00 or 00h
XX	RW : XX	Register is not reset
0,	0,04h	Register is in bank 0
1,	1,23h	Register is in bank 1
x,	x,F7h	Register exists in register bank 0 and register bank 1
Empty, grayed-out table cell		Reserved bit or group of bits, unless otherwise stated

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah') and ***hexadecimal*** numbers may also be represented by a '0x' prefix, the ***C*** coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are ***decimal***.

Units of Measure

This table lists the units of measure used in this manual.

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femtofarad
Hz	hertz
k	kilo, 1000
K	2^{10}, 1024
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz (32.000)
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µVrms	microvolts root-mean-square
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoamphere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
pp	peak-to-peak
ppm	parts per million
sps	samples per second
σ	sigma: one standard deviation
V	volt

Acronyms

This table lists the acronyms that are used in this manual.

Acronyms

Acronym	Description
ABUS	analog output bus
AC	alternating current
ADC	analog-to-digital converter
API	Application Programming Interface
BC	broadcast clock
BR	bit rate
BRA	bus request acknowledge
BRQ	bus request
CBUS	comparator bus
CI	carry in
CMP	compare
CO	carry out
CPU	central processing unit
CRC	cyclic redundancy check
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
DI	digital or data input
DMA	direct memory access
DO	digital or data output
ECO	external crystal oscillator
FB	feedback
GIE	global interrupt enable
GPIO	general purpose I/O
ICE	in-circuit emulator
IDE	integrated development environment
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
IOR	I/O read
IOW	I/O write
IPOR	imprecise power on reset
IRQ	interrupt request
ISR	interrupt service routine
ISSP	in system serial programming
IVR	interrupt vector read
LFSR	linear feedback shift register
LRb	last received bit
LRB	last received byte
LSb	least significant bit
LSB	least significant byte
LUT	look-up table
MISO	master-in-slave-out
MOSI	master-out-slave-in
MSb	most significant bit
MSB	most significant byte
PC	program counter

Acronyms *(continued)*

Acronym	Description
PCH	program counter high
PCL	program counter low
PD	power down
PMA	PSoC® memory arbiter
POR	power on reset
PPOR	precision power on reset
PRS	pseudo random sequence
PSoC®	Programmable System-on-Chip
PSSDC	power system sleep duty cycle
PWM	pulse width modulator
RAM	random access memory
RETI	return from interrupt
RO	relaxation oscillator
ROM	read only memory
RW	read/write
SAR	successive approximation register
SC	switched capacitor
SIE	serial interface engine
SE0	single-ended zero
SOF	start of frame
SP	stack pointer
SPI	serial peripheral interconnect
SPIM	serial peripheral interconnect master
SPIS	serial peripheral interconnect slave
SRAM	static random access memory
SROM	supervisory read only memory
SSADC	single slope ADC
SSC	supervisory system call
TC	terminal count
USB	universal serial bus
WDT	watchdog timer
WDR	watchdog reset
XRES	external reset

1. Pin Information

This chapter lists, describes, and illustrates all pins and pinout configurations for the CY8CTMG20x, CY8CTMG20xA, CY8CTST200, and CY8CTST200A PSoC devices. For up-to-date ordering, pinout, and packaging information, refer to the individual PSoC device's data sheet or go to http://www.cypress.com.

1.1 Pinouts

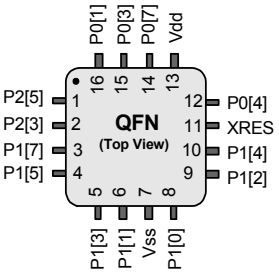
The CY8CTMG20x, CY8CTMG20xA, CY8CTST200, and CY8CTST200A PSoC devices are available in a variety of packages. Every ***port*** pin (labeled with a "P"), except for ***Vss***, ***Vdd***, and XRES in the following tables and illustrations, is capable of Digital I/O.

1.1.1 CY8CTMG200-16LGXI, CY8CTMG200A-16LGXI, CY8CTST200-16LGXI, CY8CTST200A-16LGXI PSoC 16-Pin Part Pinout

Table 1-1. 16-Pin QFN/COL Part Pinout

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I	P2[5]	XTAL Out
2	IO	I	P2[3]	XTAL In
3	IOHR	I	P1[7]	I2C SCL, SPI SS
4	IOHR	I	P1[5]	I2C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	TC CLK*, I2C SCL, SPI MOSI
7	Power		Vss	Ground pin
8	IOHR	I	P1[0]	TC DATA*, I2C SDA, SPI CLK
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	EXTCLK
11	Input		XRES	Active high external reset with internal pull down
12	IOH	I	P0[4]	
13	Power		Vdd	Power pin
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

CY8CTMG200-16LGXI, CY8CTMG200A-16LGXI, CY8CTST200-16LGXI CY8CTST200A-16LGXI PSoC Devices



LEGEND A = Analog, I = Input, O = Output, H = 5 mA High Output Drive, R = Regulated Output Option.

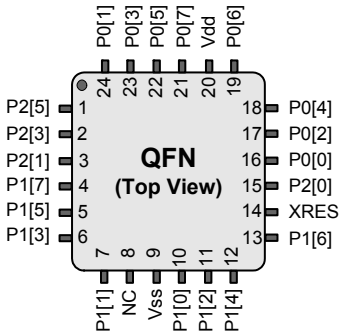
* These are the ISSP pins, which are not High Z at POR (Power On Reset).

1.1.2 CY8CTMG200-24LQXI, CY8CTMG200A-24LQXI, CY8CTST200-24LQXI, CY8CTST200A-24LQXI PSoC 24-Pin Part Pinout

Table 1-2. 24-Pin QFN Part Pinout **

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I	P2[5]	XTAL Out
2	IO	I	P2[3]	XTAL In
3	IO	I	P2[1]	
4	IOHR	I	P1[7]	I2C SCL, SPI SS
5	IOHR	I	P1[5]	I2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	TC CLK*, I2C SCL, SPI MOSI
8			NC	No connection
9	Power		Vss	Ground pin
10	IOHR	I	P1[0]	TC DATA*, I2C SDA, SPI CLK
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	EXTCLK
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull down
15	IO	I	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Power		Vdd	Power pin
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input

CY8CTMG200-24LQXI, CY8CTMG200A-24LQXI, CY8CTST200-24LQXI, CY8CTST200-24LQXI PSoC Device



LEGEND A = Analog, I = Input, O = Output, H = 5 mA High Output Drive, R = Regulated Output Option.

* These are the ISSP pins, which are not High Z at POR (Power On Reset).

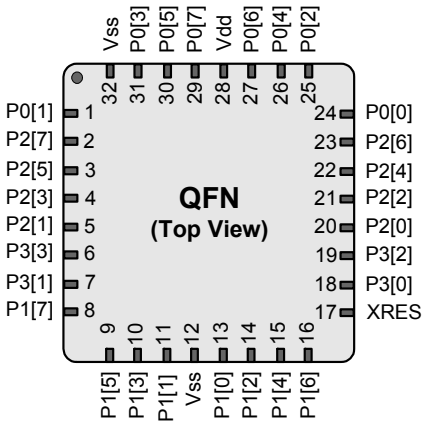
** The center pad on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.

1.1.3 CY8CTMG200-32LQXI, CY8CTMG200A-32LQXI, CY8CTST200-32LQXI, CY8CTST200A-32LQXI, CY8CTMG201-32LQXI, CY8CTMG201A-32LQXI PSoC 32-Pin Part Pinout

Table 1-3. 32-Pin QFN Part Pinout **

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[1]	Integrating input
2	IO	I	P2[7]	
3	IO	I	P2[5]	XTAL Out
4	IO	I	P2[3]	XTAL In
5	IO	I	P2[1]	
6	IO	I	P3[3]	
7	IO	I	P3[1]	
8	IOHR	I	P1[7]	I2C SCL, SPI SS
9	IOHR	I	P1[5]	I2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK
11	IOHR	I	P1[1]	TC CLK*, I2C SCL, SPI MOSI
12	Power		Vss	Ground pin
13	IOHR	I	P1[0]	TC DATA*, I2C SDA, SPI CLK
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	EXTCLK
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down
18	IO	I	P3[0]	
19	IO	I	P3[2]	
20	IO	I	P2[0]	
21	IO	I	P2[2]	
22	IO	I	P2[4]	
23	IO	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		Vdd	Power pin
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	
32	Power		Vss	Ground pin

CY8CTMG200-32LQXI, CY8CTMG200A-32LQXI, CY8CTST200-32LQXI, CY8CTST200A-32LQXI, CY8CTMG201-32LQXI, CY8CTMG201A-32LQXI PSoC Devices



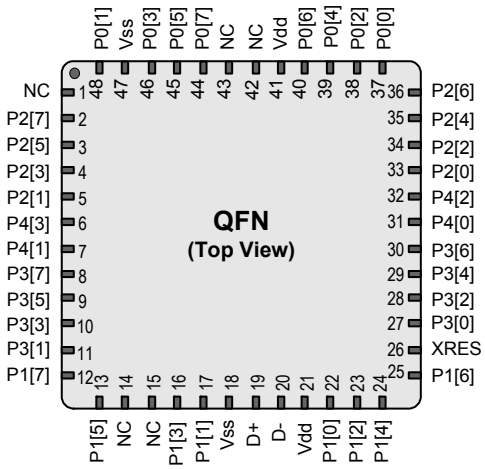
LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.
* ISSP pin which is not High Z at POR (Power On Reset).
** The center pad on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.

1.1.4 CY8CTMG200-48LTXI, CY8CTMG200A-48LTXI, CY8CTST200-48LTXI, CY8CTST200A-48LTXI, CY8CTMG201-48LTXI, CY8CTMG201A-48LTXI PSoC 48-Pin Part Pinout

Table 1-4. 48-Pin Part Pinout **

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	IO	I	P2[7]	
3	IO	I	P2[5]	XTAL Out
4	IO	I	P2[3]	XTAL In
5	IO	I	P2[1]	
6	IO	I	P4[3]	
7	IO	I	P4[1]	
8	IO	I	P3[7]	
9	IO	I	P3[5]	
10	IO	I	P3[3]	
11	IO	I	P3[1]	
12	IOHR	I	P1[7]	I2C SCL, SPI SS
13	IOHR	I	P1[5]	I2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	TC CLK*, I2C SCL, SPI MOSI
18	Power		Vss	Ground pin
19	IO		D +	USB PHY
20	IO		D -	USB PHY
21	Power		Vdd	Power pin
22	IOHR	I	P1[0]	TC DATA*, I2C SDA, SPI CLK
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	EXTCLK
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	IO	I	P3[0]	
28	IO	I	P3[2]	
29	IO	I	P3[4]	
30	IO	I	P3[6]	
31	IO	I	P4[0]	
32	IO	I	P4[2]	
33	IO	I	P2[0]	
34	IO	I	P2[2]	
35	IO	I	P2[4]	
36	IO	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	

CY8CTMG200-48LTXI, CY8CTMG200A-48LTXI, CY8CTST200-48LTXI, CY8CTST200A-48LTXI, CY8CTMG201-48LTXI, CY8CTMG201A-48LTXI PSoC Devices



Pin No.	Digital	Analog	Name	Description
41	Power		Vdd	Power pin
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		Vss	Ground pin
48	IOH	I	P0[1]	Integrating input

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.
* ISSP pin which is not High Z at POR (Power On Reset).
** The center pad on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.

Section B: PSoC Core

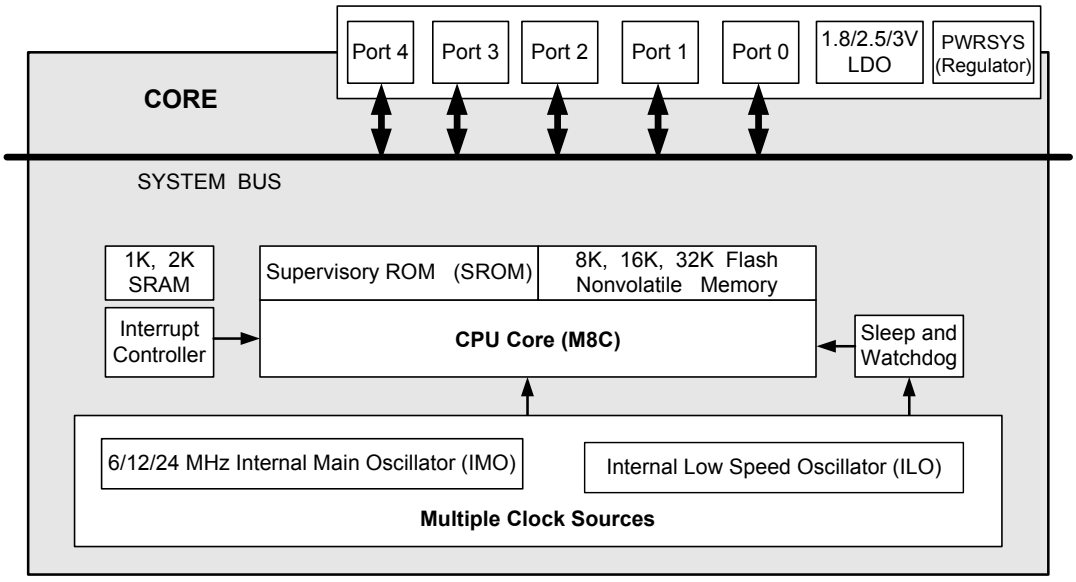
The PSoC Core section discusses the core components of a PSoC device with a base part number of CY8CTMG20x or CY8CTST200 and the registers associated with those components. The core section covers the heart of the PSoC device, which includes the M8C ***microcontroller***; SROM, interrupt controller, GPIO, and ***SRAM*** paging; multiple clock sources such as IMO and ILO; and sleep and watchdog functionality. This section includes these chapters:

- CPU Core (M8C) on page 27.
- Supervisory ROM (SROM) on page 33.
- RAM Paging on page 39.
- Interrupt Controller on page 45.
- General Purpose I/O (GPIO) on page 55.
- Internal Main Oscillator (IMO) on page 63.
- Internal Low Speed Oscillator (ILO) on page 67.
- External Crystal Oscillator (ECO), on page 69
- Sleep and Watchdog on page 73.

Top-Level Core Architecture

This figure displays the top level architecture of the PSoC core. Each component of the figure is discussed at length in this section.

PSoC Core Block Diagram



Core Register Summary

This table lists all the PSoC registers for the CPU core in ***address*** order within their system resource configuration. The grayed out bits are reserved bits. If you write these bits always write them with a value of '0'. For the core registers, the first 'x' in some ***register*** addresses represents either bank 0 or bank 1. These registers are listed throughout this manual in bank 0, even though they are also available in bank 1.

Summary Table of the Core Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
M8C REGISTER (page 27)										
x,F7h	CPU_F	PgMode[1:0]		XIO_1	XIO		Carry	Zero	GIE	RL : 02
RAM PAGING (SRAM) REGISTERS (page 39)										
x,6Ch	TMP_DR0	Data[7:0]								RW : 00
x,6Dh	TMP_DR1	Data[7:0]								RW : 00
x,6Eh	TMP_DR2	Data[7:0]								RW : 00
x,6Fh	TMP_DR3	Data[7:0]								RW : 00
0,D0h	CUR_PP						Page Bits[2:0]			RW : 0
0,D1h	STK_PP						Page Bits[2:0]			RW : 0
0,D3h	IDX_PP						Page Bits[2:0]			RW : 0
0,D4h	MVR_PP						Page Bits[2:0]			RW : 0
0,D5h	MVW_PP						Page Bits[2:0]			RW : 0
INTERRUPT CONTROLLER REGISTERS (page 45)										
0,DAh	INT_CLR0	I2C	Sleep	SPI	GPIO	Timer0	TrueTouch	Analog	V Monitor	RW : 00
0,DBh	INT_CLR1	Endpoint3	Endpoint2	Endpoint1	Endpoint0	USB SOF	USB Bus Rst	Timer2	Timer1	RW : 00
0,DCh	INT_CLR2			USB_WAKE	Endpoint8	Endpoint7	Endpoint6	Endpoint5	Endpoint4	RW : 00
0,DEh	INT_MSK2			USB Wakeup	Endpoint8	Endpoint7	Endpoint6	Endpoint5	Endpoint4	RW : 00
0,DFh	INT_MSK1	Endpoint3	Endpoint2	Endpoint1	Endpoint0	USB SOF	USB Bus Reset	Timer2	Timer1	RW : 00
0,E0h	INT_MSK0	I2C	Sleep	SPI	GPIO	Timer0	TrueTouch	Analog	V Monitor	RW : 00
0,E1h	INT_SW_EN								ENSWINT	RW : 0
0,E2h	INT_VC	Pending Interrupt[7:0]								RC : 00
GENERAL PURPOSE I/O (GPIO) REGISTERS (page 59)										
0,00h	PRT0DR	Data[7:0]								RW : 00
0,01h	PRT0IE	Interrupt Enables[7:0]								RW : 00
0,04h	PRT1DR	Data[7:0]								RW : 00
0,05h	PRT1IE	Interrupt Enables[7:0]								RW : 00
0,08h	PRT2DR	Data[7:0]								RW : 00
0,09h	PRT2IE	Interrupt Enables[7:0]								RW : 00
0,0Ch	PRT3DR	Data[7:0]								RW : 00
0,0Dh	PRT3IE	Interrupt Enables[7:0]								RW : 00
1,00h	PRT0DM0	Drive Mode 0[7:0]								RW : 00
1,01h	PRT0DM1	Drive Mode 1[7:0]								RW : FF
1,04h	PRT1DM0	Drive Mode 0[7:0]								RW : 00
1,05h	PRT1DM1	Drive Mode 1[7:0]								RW : FF
1,08h	PRT2DM0	Drive Mode 0[7:0]								RW : 00
1,09h	PRT2DM1	Drive Mode 1[7:0]								RW : FF
1,0Ch	PRT3DM0	Drive Mode 0[7:0]								RW : 00
1,0Dh	PRT3DM1	Drive Mode 1[7:0]								RW : FF
0,10h	PRTxDR	Data[7:0]								RW : 00
0,11h	PRTxIE	Interrupt Enables[7:0]								RW : 00
1,10h	PRTxDM0	Drive Mode 0[7:0]								RW : 00
1,11h	PRTxDM1	Drive Mode 0[7:0]								RW : 00

Summary Table of the Core Registers *(continued)*

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
1,DCh	IO_CFG1	StrongP		Range[1:0]		P1_LOW_THRS	SPICLK_ON_P10	REG_EN	IOINT	RW : 00
INTERNAL MAIN OSCILLATOR (IMO) REGISTER (page 64)										
1,E8h	IMO_TR	Trim[7:0]								W: 00
1,FAh	IMO_TR1						Fine Trim[2:0]			RW : 00
x,FEh	CPU_SCR1	IRESS			SLIM[1:O]				IRAMDIS	# : 00
1,E2h	OSC_CR2				CLK48MEN		EXTCLKEN	IMODIS		RW : 00
INTERNAL LOW SPEED OSCILLATOR (ILO) REGISTER (page 68)										
1,E9h	ILO_TR		PD_MODE	ILOFREQ	SATBIASB	Freq Trim[3:0]				RW : 18
EXTERNAL CRYSTAL OSCILLATOR (ECO) REGISTERS (page 69)										
1,D2h	ECO_ENBUS						ECO_ENBUS[2:0]			RW : 07
1,D3h	ECO_TRIM				ECO_XGM[2:0]			ECO_PL[1:0]		RW : 00
1,E1h	ECO_CFG						ECO_LPM	ECO_EXW	ECO_EX	RW : 00
SLEEP AND WATCHDOG REGISTERS (page 77)										
0,E3h	RES_WDT	WDSL_Clear[7:0]								W : 00
1,EBh	SLP_CFG	PSSDC[1:0]								RW : 0
1,ECh	SLP_CFG2					ALT_Buzz [1:0]		I2C_ON	LSO_OFF	RW : 00
1,EDh	SLP_CFG3		DBL_TAPS	T2TAP [1:0]		T1TAP [1:0]		T0TAP [1:0]		RW : 0x7F

LEGEND
L The and f, expr; or f, expr; and xor f, expr instructions can be used to modify this register.
x An “x” before the comma in the address field indicates that this register can be accessed or written to no matter what bank is used.
C Clearable register or bit(s).
R Read register or bit(s).
W Write register or bit(s).