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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PRoC™ BLE: CYBL1XX7X Family Datasheet

Programmable Radio-on-Chip With Bluetooth Low Energy

General Description

PRoC™ BLE is a 32-bit, 48-MHz ARM® Cortex®-M0 BLE solution with CapSense®, 12-bit ADC, four timer, counter, pulse-width modulators (TCPWM), Direct memory access (DMA), thirty-six GPIOs, two serial communication blocks (SCBs), LCD, and I²S. PRoC BLE includes a royalty-free BLE stack compatible with Bluetooth® 4.2 and provides a complete, programmable, and flexible solution for HID, remote controls, toys, beacons, and wireless chargers. In addition to these applications, PRoC BLE provides a simple, low-cost way to add BLE connectivity to any system.

Features

Bluetooth® Smart Connectivity

- Bluetooth 4.2 single-mode device
- 2.4-GHz BLE radio and baseband with integrated balun
- TX output power: –18 dBm to +3 dBm
- Received signal strength indicator (RSSI) with 1-dB resolution
- RX sensitivity: –92 dBm
- TX current: 15.6 mA at 0 dBm
- RX current: 16.4 mA

ARM Cortex-M0 CPU Core

- 32-bit processor (0.9 DMIPS/MHz) with single-cycle 32-bit multiply, operating at up to 48 MHz
- 256-KB flash memory
- 32-KB SRAM memory
- Emulated EEPROM using flash memory
- Watchdog timer with dedicated internal low-speed oscillator (ILO)
- Eight-channel direct memory access (DMA) controller

Ultra-Low-Power

- 1.5-µA Deep-Sleep mode with watch crystal oscillator (WCO) on
- 150-nA Hibernate mode current with SRAM retention
- 60-nA Stop mode current with GPIO wakeup

CapSense® Touch Sensing with Two-Finger Gestures

- Up to 36 capacitive sensors for buttons, sliders, and touchpads
- One-finger gestures: finger tracking, scroll, inertial scroll, edge-swipe, click, double-click
- Two-finger gestures: scroll, inertial scroll, zoom-in, zoom-out
- Cypress Capacitive Sigma-Delta (CSD) provides best-in-class SNR (> 5:1) and liquid tolerance
- Automatic hardware-tuning algorithm (SmartSense™)

Peripherals

- 12-bit, 1-Msps SAR ADC with internal reference, sample-and-hold (S/H), and channel sequencer
- Ultra-low-power LCD segment drive for 128 segments with operation in Deep-Sleep mode
- Two serial communication blocks (SCBs) supporting I²C (Master/Slave), SPI (Master/Slave), or UART
- Four dedicated 16-bit TCPWMs
  - Additional four 8-bit or two 16-bit PWMs
- Programmable LVD from 1.8 V to 4.5 V
- I²S Master interface

Clock, Reset, and Supply

- Wide supply-voltage range: 1.9 V to 5.5 V
- 3-MHz to 48-MHz internal main oscillator (IMO) with 2% accuracy
- 24-MHz external clock oscillator (ECO) without load capacitance
- 32-kHz WCO

Programmable GPIOs

- 36 GPIOs configurable as open drain high/low, pull-up/pull-down, HI-Z, or strong output
- Any GPIO pin can be CapSense, LCD, or analog, with flexible pin routing

Programming and Debug

- 2-pin SWD
- In-system flash programming support

Temperature and Packaging

- Operating temperature range: –40 °C to +105 °C
- Available in 56-pin QFN (7 mm × 7 mm) and 76-ball WLCSP (3.52 mm × 3.91 mm) packages

PSoC® Creator™ Design Environment

- Easy-to-use IDE to configure, develop, program, and test a BLE application
- Option to export the design to Keil, IAR, or Eclipse

Bluetooth Low Energy Protocol Stack

- Bluetooth Low Energy protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
  - Switches between Central and Peripheral roles on-the-go
- Standard Bluetooth Low Energy profiles and services for interoperability
  - Custom profile and service for specific use cases

More Information

Cypress provides a wealth of data at http://www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for Bluetooth® Low Energy (BLE) Products. Following is an abbreviated list for PRoC BLE:

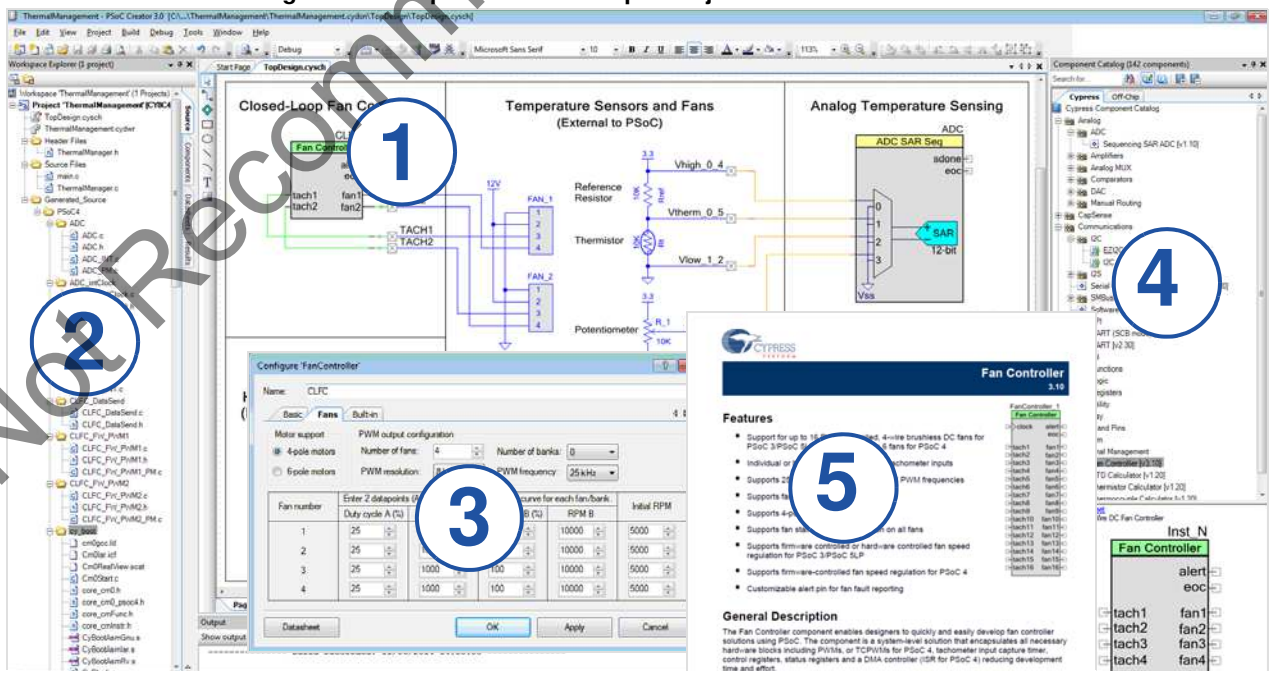
- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PRoC BLE, PSoC 4 BLE, PSoC 5LP In addition, PSoC Creator includes a device selection tool.
- Application Notes: Cypress offers a large number of PSoC application notes converting a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PRoC BLE are:
  - AN94020: Getting Started with PRoC BLE
  - AN97060: PSoC 4 BLE and PRoC BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91184: PSoC 4 BLE - Designing BLE Applications
  - AN91162: Creating a BLE Custom Profile
  - AN91445: Antenna Design and RF Layout Guidelines
  - AN96841: Getting Started With EZ-BLE Module
  - AN85951: PSoC 4 CapSense Design Guide
  - AN95089: PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques
  - AN92584: Designing for Low Power and Estimating Battery Life for BLE Applications
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PRoC BLE functional block
  - Registers TRM describes each of the PRoC BLE registers
- Development Kits:
  - CY8CKIT-042-BLE Pioneer Kit, is a flexible, Arduino-compatible, Bluetooth LE development kit for PSoC 4 BLE and PRoC BLE.
  - CY5676, PRoC BLE 256KB Module, features a PRoC BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-142, PSoC 4 BLE Module, features a PSoC 4 BLE device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-143, PSoC 4 BLE 256KB Module, features a PSoC 4 BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents

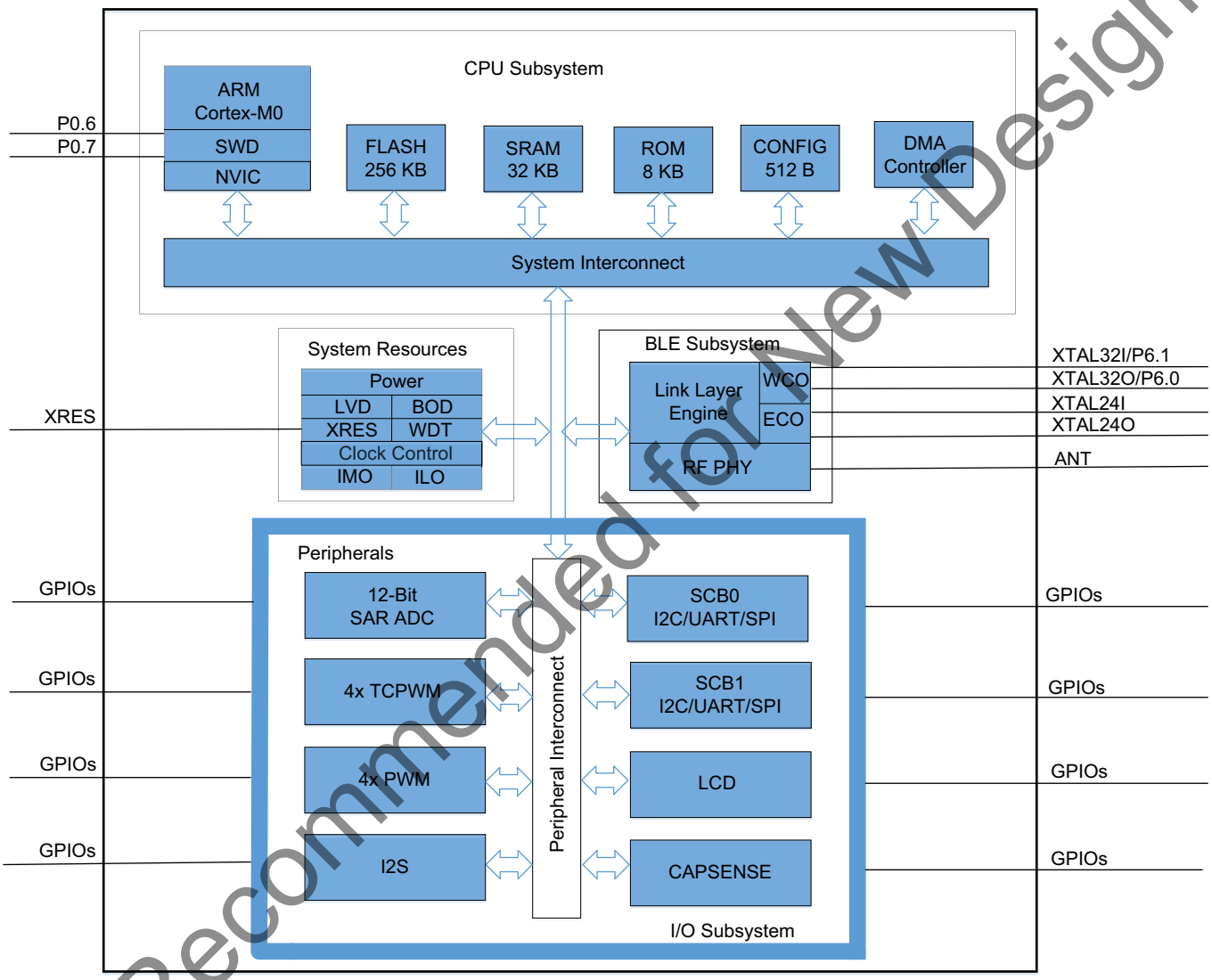


Contents

Blocks and Functionality

The CYBL1XX7X block diagram is shown in Figure 2. There are five major subsystems: CPU subsystem, BLE subsystem, system resources, peripheral blocks, and I/O subsystem.

Figure 2. Block Diagram



The PRoC BLE family includes extensive support for programming, testing, debugging, and tracing both hardware and firmware. The complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for PRoC BLE devices. The SWD interface is fully compatible with industry-standard third-party tools. PRoC BLE also supports disabling the SWD interface and has a robust flash-protection feature.

CPU Subsystem

CPU

The CYBL1XX7X device is based on an energy-efficient ARM Cortex-M0 32-bit processor, offering low power consumption, high performance, and reduced code size using 16-bit thumb instructions. The Cortex-M0's ability to perform single-cycle 32-bit arithmetic and logic operations, including single-cycle 32-bit multiplication, helps in better performance. The inclusion of the tightly-integrated Nested Vectored Interrupt Controller (NVIC) with 32 interrupt lines enables the Cortex-M0 to achieve a low latency and a deterministic interrupt response.

The CPU also includes a 2-pin interface, the serial wire debug (SWD), which is a 2-wire form of JTAG. The debug circuits are enabled by default and can only be disabled in firmware. If disabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with the new firmware that enables debugging. In addition, it is possible to use the debug pins as GPIO too. The device has four break-points and two watchpoints for effective debugging.

Flash

The device has a 256-KB flash memory with a flash accelerator, tightly coupled to the CPU to improve average access times from flash. The flash is designed to deliver 1-wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash can be used to emulate EEPROM operation, if required.

During flash erase and programming operations (the maximum erase and program time is 20 ms per row), the IMO will be set to 48 MHz for the duration of the operation. This also applies to the emulated EEPROM. System design must take this into account because peripherals operating from different IMO frequencies will be affected. If it is critical that peripherals continue to operate with no change during flash programming, always set the IMO to 48 MHz and derive the peripheral clocks by dividing down from this frequency.

SRAM

The low-power 32-KB SRAM memory retains its contents even in Hibernate mode.

ROM

The 8-KB supervisory ROM contains a library of executable functions for flash programming. These functions are accessed through supervisory calls (SVC) and enable in-system programming of the flash memory.

DMA

DMA controller provides DataWrite (DW) and Direct Memory Access (DMA). The DMA controller has following features

- Supports up to 8 DMA channels with two independent descriptors per channel
- Four levels of priority for each channel
- Byte, half-word (2 bytes), and word (4 bytes) transfers
- Three modes of operation supported for each channel
- Configurable interrupt generation
- Output trigger on completion of transfer (transfer sizes up to 65536 data elements)

BLE Subsystem

The BLE subsystem consists of the link layer engine and physical layer. The link layer engine supports both master and slave roles. The link layer engine implements time-critical functions such as encryption in the hardware to reduce the power consumption, and provides minimal processor intervention and a high performance. The key protocol elements, such as host control interface (HCI) and link control, are implemented in firmware. The direct test mode (DTM) is included to test the radio performance using a standard Bluetooth tester.

The physical layer consists of a modem and an RF transceiver that transmits and receives BLE packets at the rate of 1 Mbps over the 2.4-GHz ISM band. In the transmit direction, this block performs GFSK modulation and then converts the digital baseband signal of these BLE packets into radio frequency before transmitting them to air through an antenna. In the receive direction, this block converts an RF signal from the antenna to a digital bit stream after performing GFSK demodulation.

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna terminal through a pi-matching network. The output power is programmable from –18 dBm to +3 dBm to optimize the current consumption for different applications.

The Bluetooth Low Energy protocol stack uses the BLE subsystem and provides the following features:

- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Encryption
  - Low-duty-cycle advertising
  - LE Ping
  - LE Data Packet Length Extension (Bluetooth 4.2 feature)
  - Link Layer Privacy (with extended scanning filter policy) (Bluetooth 4.2 feature)
- Bluetooth Low Energy 4.2 single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- Master and slave roles
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, 3, and 4
  - Security mode 2: Level 1 and 2
  - User-defined advertising data
  - Multiple-bond support
- GATT features
  - GATT client and server
  - Supports GATT subprocedures
  - 32-bit universally unique identifiers (UUID)
- Security Manager (SM)
  - LE Secure Connections (Bluetooth 4.2 feature)
  - Pairing methods: Just Works, Passkey Entry, Out of Band, and Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
- Supports all SIG-adopted BLE profiles

System Resources Subsystem

Power

The power block includes internal LDOs that supply required voltage levels for different blocks. The power system also includes POR, BOD, and LVD circuits. The POR circuit holds the device in the reset state until the power supplies have stabilized at appropriate levels and the clock is ready. The BOD circuit resets the device when the supply voltage is too low for proper device operation. The LVD circuit generates an interrupt if the supply voltage drops below a user-selectable level.

An external active-LOW reset pin (XRES) can be used to reset the device. The XRES pin has an internal pull-up resistor and, in most applications, does not require any additional pull-up resistors. The power system is described in detail in the "Power" section on page 14.

Clock Control

The PRoC BLE clock control is responsible for providing clocks to all subsystems and also for switching between different clock sources without glitching. The clock control for PRoC BLE consists of the IMO and the internal low-speed oscillator (ILO). It uses the 24-MHz external crystal oscillator (ECO) and the 32-kHz WCO. In addition, an external clock may be supplied from a pin.

The device has 12 dividers with 16 divider outputs. Two dividers have additional fractional division capability. The HFCLK signal is divided down, as shown in Figure 3, to generate the system clock (SYSCLK) and peripheral clock (PERx_CLK) for different peripherals. The system clock (SYSCLK) driving buses, registers, and the processor must be higher than all the other clocks in the system that are divided off HFCLK. The ECO and WCO are present in the BLE subsystem and the clock outputs are routed to the system resources.

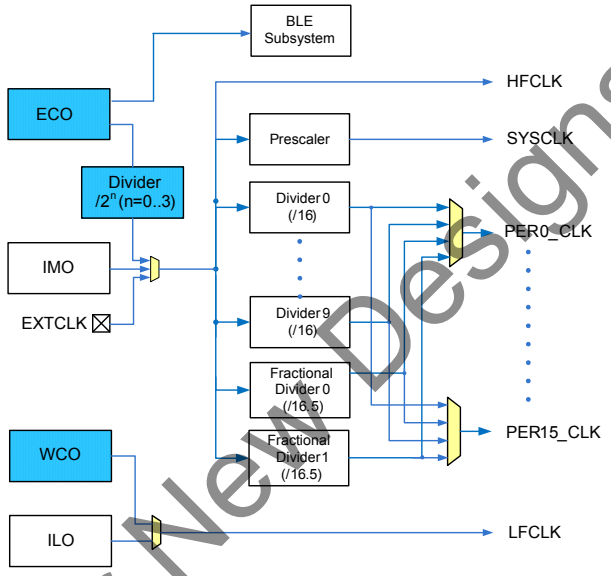
Internal Main Oscillator (IMO)

The IMO is the primary system clock source, which can be adjusted in the range of 3 MHz to 48 MHz in steps of 1 MHz. The IMO accuracy is ±2%.

Internal Low-Speed Oscillator (ILO)

The ILO is a very-low-power 32-kHz oscillator, which is primarily used to generate clocks for peripheral operations in Deep-Sleep mode. The ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Figure 3. Clock Control



External Crystal Oscillator (ECO)

The ECO is used as the active clock for the BLE subsystem to meet the ±50-ppm clock accuracy requirement of the Bluetooth Low Energy Specification. The internal tunable load capacitor is provided to tune the crystal clock frequency. The high-accuracy ECO clock can also be used as a system clock.

Watch Crystal Oscillator (WCO)

The WCO is used as the sleep clock for the BLE subsystem to meet the ±500-ppm clock accuracy requirement of the Bluetooth Low Energy Specification. The sleep clock provides accurate sleep timing and enables wakeup at specified advertisement and connection intervals. With the WCO and firmware, an accurate real-time clock (within the bounds of the 32.768-kHz crystal accuracy) can be realized.

Voltage Reference

The internal bandgap reference circuit with 1% accuracy provides the voltage reference for the 12-bit SAR ADC. To enable better SNRs and absolute accuracy, it will be possible to bypass the internal bandgap reference using a REF pin and to use an external reference for the SAR.

Watchdog Timer (WDT)

A watchdog timer is implemented in the system resources subsystem running from the ILO; this allows watchdog operations during Deep-Sleep mode and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the 'Reset Cause' register.

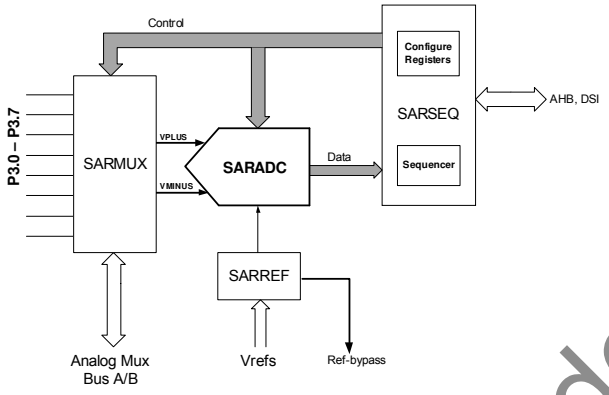
Peripheral Blocks

12-Bit SAR ADC

The ADC is a 12-bit, 1-Msps SAR ADC with a built-in sample-and-hold (S/H) circuit. The ADC can operate with either an internal voltage reference or an external voltage reference.

Preceding the SAR ADC is the SARMUX, which can route external pins and internal signals (analog mux bus and temperature sensor output) to the eight internal channels of the SAR ADC. The sequencer controller (SARSEQ) is used to control the SARMUX and SAR ADC to do an automatic scan on all enabled channels without CPU intervention and for preprocessing tasks such as averaging the output data. A Cypress-supplied software driver (Component) is used to control the ADC peripheral.

Figure 4. SAR ADC System Diagram



A diode based, on-chip temperature sensor is used to measure the die temperature. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using the Cypress-supplied software that includes calibration and linearization.

4x Timer Counter PWM (TCPWM)

The 16-bit TCPWM module can be used to generate the PWM output or to capture the timing of edges of input signals or to provide a timer functionality. TCPWM can also be used as a 16-bit counter that supports up, down, and up/down counting modes.

Rising edge, falling edge, combined rising/falling edge detection, or pass-through on all hardware input signals can be used to derive counter events. Three routed output signals are available to indicate underflow, overflow, and counter/compare match events. A maximum of four TCPWMs are available.

4x PWM

These PWMs are in addition to the TCPWMs. The PWM peripheral can be configured as 8-bit or 16-bit resolution. The PWM provides compare outputs to generate single or continuous timing and control signals in hardware. It also provides an easy method of generating complex real-time events accurately with minimal CPU intervention. A maximum of four 8-bit PWMs or two 16-bit PWMs are available.

Serial Communication Block (SCB0/SCB1)

The SCB can be configured as an I^2C, UART, or SPI interface. It supports an 8-byte FIFO for receive and transmit buffers to reduce CPU intervention. A maximum of two SCBs (SCB0, SCB1) are available.

I^2C mode: The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-Mode-Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIOs in open-drain modes.

The hardware I^2C block implements a full multimaster and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast-Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. The I^2C function is implemented using the Cypress-provided software Component (EzI2C) that creates a mailbox address range in the memory of PRoC BLE and effectively reduces the I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-byte FIFO for receive and transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time.

When SCB0 is used, Serial Data (SDA) and Serial Clock (SCL) of I^2C can be connected to P0.4 and P0.5, or P1.4 and P1.5, or P3.0 and P3.1.

When SCB1 is used, SDA and SCL can be connected to P0.0 and P0.1, or P3.4 and P3.5, or P5.0 and P5.1.

Configurations for I^2C are as follows:

- SCB1 is fully compliant with the Standard-mode (100 kHz), Fast-mode (400 kHz), and Fast-Mode-Plus (1 MHz) I^2C signaling specifications when routed to GPIO pins P5.0 and P5.1, except for hot-swap capability during I^2C active communication.
- SCB1 is compliant only with Standard mode (100 kHz) when not used with P5.0 and P5.1.
- SCB0 is compliant with Standard mode (100 kHz) only.

UART mode: This is a full-feature UART operating up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols. In addition, it supports the 9-bit multiprocessor mode, which allows addressing of peripherals connected over common RX and TX lines. The UART hardware flow control is supported to allow slow and fast devices to communicate with each other over UART without the risk of losing data. Refer to Table 4 on page 13 for possible UART connections to the GPIOs.

SPI Mode: The SPI mode supports full Motorola® SPI, Texas Instruments® Secure Simple Pairing (SSP) (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The block supports an 8-byte FIFO for receive and transmit. Refer to Table 4 on page 13 for the possible SPI connections to the GPIOs.

Inter-IC Sound Bus (I^2S)

Inter-IC Sound Bus (I^2S) is a serial bus interface standard used for connecting digital audio devices. The specification is from Philips® Semiconductor (I^2S bus specification; February 1986, revised June 5, 1996).

I^2S operates only in the Master mode, supporting the transmitter (TX) and the receiver (RX), which have independent data byte streams. These byte streams are packed with the most significant byte first. The number of bytes used for each sample (a sample for the left or right channel) is the minimum number of bytes to hold a sample.

LCD

The LCD controller can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments providing ultra-low power consumption. The two methods used are referred to as digital correlation and PWM.

The digital correlation method modulates the frequency and signal levels of the commons and segments to generate the highest RMS voltage across a segment to light it up or to maintain the RMS signal as zero. This method is good for STN displays but may result in reduced contrast in TN (cheaper) displays.

The PWM method drives the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but provides better results in driving TN displays.

LCD operation is supported during Deep-Sleep mode by refreshing a small display buffer (four bits; one 32-bit register per port).

CapSense

CapSense is supported on all GPIOs through a Capacitive Sigma-Delta (CSD) block, which can be connected to any GPIO through an analog mux bus. Any GPIO pin can be connected to the analog mux bus via an analog switch. The CapSense function can thus be provided on any pin or group of pins in a system under software control. A software Component in PSoC Creator is provided for the CapSense block to make it easy for the user. The shield voltage can be driven on another mux bus to provide liquid-tolerance capability. Driving the shield electrode in phase with the sense electrode keeps the shield capacitance from attenuating the sensed input.

The CapSense trackpad/touchpad with gestures has the following features:

- Supports 1-finger and 2-finger touch applications
- Supports up to 36 X/Y sensor inputs
- Includes a gesture-detection library:
  - 1-finger touch: Finger tracking, scroll, inertial scroll, click, double-click, edge swipe
  - 2-finger touch: Scroll, inertial scroll, zoom-in, zoom-out

I/O Subsystem

The I/O subsystem, which comprises the GPIO block, implements the following:

- Eight drive-strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Weak pull-up with weak pull-down
  - Strong pull-up with weak pull-down
  - Strong pull-up with strong pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
- Port pins: 36
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffers (enabling/disabling) in addition to drive-strength modes
- Hold mode for latching the previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt to improve EMI
- The GPIO pins P5.0 and P5.1 are overvoltage-tolerant
- The GPIO cells, including P5.0 and P5.1, cannot be hot-swapped or powered up independent of the rest of the system.

Pinouts

Table 1 shows the pin list for the CYBL1XX7X device.

Table 1. CYBL1XX7X Pin List (QFN Package)

Pin	Name	Type	Description
1	VDDD	POWER	1.71-V to 5.5-V digital supply
2	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
3	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
4	XRES	RESET	Reset, active LOW
5	P4.0	GPIO	Port 4 Pin 0, analog/digital/lcd/csd
6	P4.1	GPIO	Port 4 Pin 1, analog/digital/lcd/csd
7	P5.0	GPIO	Port 5 Pin 0, analog/digital/lcd/csd
8	P5.1	GPIO	Port 5 Pin 1, analog/digital/lcd/csd
9	VSSD	GROUND	Digital ground
10	VDDR	POWER	1.9-V to 5.5-V radio supply
11	GANT1	GROUND	Antenna shielding ground
12	ANT	ANTENNA	Antenna pin
13	GANT2	GROUND	Antenna shielding ground
14	VDDR	POWER	1.9-V to 5.5-V radio supply
15	VDDR	POWER	1.9-V to 5.5-V radio supply
16	XTAL24I	CLOCK	24-MHz crystal or external clock input
17	XTAL24O	CLOCK	24-MHz crystal
18	VDDR	POWER	1.9-V to 5.5-V radio supply
19	P0.0	GPIO	Port 0 Pin 0, analog/digital/lcd/csd
20	P0.1	GPIO	Port 0 Pin 1, analog/digital/lcd/csd
21	P0.2	GPIO	Port 0 Pin 2, analog/digital/lcd/csd
22	P0.3	GPIO	Port 0 Pin 3, analog/digital/lcd/csd
23	VDDD	POWER	1.71-V to 5.5-V digital supply
24	P0.4	GPIO	Port 0 Pin 4, analog/digital/lcd/csd
25	P0.5	GPIO	Port 0 Pin 5, analog/digital/lcd/csd
26	P0.6	GPIO	Port 0 Pin 6, analog/digital/lcd/csd
27	P0.7	GPIO	Port 0 Pin 7, analog/digital/lcd/csd
28	P1.0	GPIO	Port 1 Pin 0, analog/digital/lcd/csd
29	P1.1	GPIO	Port 1 Pin 1, analog/digital/lcd/csd
30	P1.2	GPIO	Port 1 Pin 2, analog/digital/lcd/csd
31	P1.3	GPIO	Port 1 Pin 3, analog/digital/lcd/csd
32	P1.4	GPIO	Port 1 Pin 4, analog/digital/lcd/csd
33	P1.5	GPIO	Port 1 Pin 5, analog/digital/lcd/csd
34	P1.6	GPIO	Port 1 Pin 6, analog/digital/lcd/csd
35	P1.7	GPIO	Port 1 Pin 7, analog/digital/lcd/csd
36	VDDA	POWER	1.71-V to 5.5-V analog supply
37	P2.0	GPIO	Port 2 Pin 0, analog/digital/lcd/csd
38	P2.1	GPIO	Port 2 Pin 1, analog/digital/lcd/csd
39	P2.2	GPIO	Port 2 Pin 2, analog/digital/lcd/csd/WAKEUP
40	P2.3	GPIO	Port 2 Pin 3, analog/digital/lcd/csd

Table 1. CYBL1XX7X Pin List (QFN Package) *(continued)*

Pin	Name	Type	Description
41	P2.4	GPIO	Port 2 Pin 4, analog/digital/lcd/csd
42	P2.5	GPIO	Port 2 Pin 5, analog/digital/lcd/csd
43	P2.6	GPIO	Port 2 Pin 6, analog/digital/lcd/csd
44	P2.7	GPIO	Port 2 Pin 7, analog/digital/lcd/csd
45	VREF	REF	1.024-V reference
46	VDDA	POWER	1.71-V to 5.5-V analog supply
47	P3.0	GPIO	Port 3 Pin 0, analog/digital/lcd/csd
48	P3.1	GPIO	Port 3 Pin 1, analog/digital/lcd/csd
49	P3.2	GPIO	Port 3 Pin 2, analog/digital/lcd/csd
50	P3.3	GPIO	Port 3 Pin 3, analog/digital/lcd/csd
51	P3.4	GPIO	Port 3 Pin 4, analog/digital/lcd/csd
52	P3.5	GPIO	Port 3 Pin 5, analog/digital/lcd/csd
53	P3.6	GPIO	Port 3 Pin 6, analog/digital/lcd/csd
54	P3.7	GPIO	Port 3 Pin 7, analog/digital/lcd/csd
55	VSSA	GROUND	Analog ground
56	VCCD	POWER	Regulated 1.8-V supply; connect to 1.3-µF capacitor
57	EPAD	GROUND	Ground paddle for the QFN package

Table 2 shows the pin list for the CYBL1XX7X device (WLCSP package).

Table 2. CYBL1XX7X Pin List (WLCSP Package)

Pin	Name	Type	Description
A1	NC	NC	Do not connect
A2	VREF	REF	1.024-V reference
A3	VSSA	GROUND	Analog ground
A4	P3.3	GPIO	Port 3 Pin 3, analog/digital/lcd/csd
A5	P3.7	GPIO	Port 3 Pin 7, analog/digital/lcd/csd
A6	VSSD	GROUND	Digital ground
A7	VSSA	GROUND	Analog ground
A8	VCCD	POWER	Regulated 1.8-V supply, connect to 1-µF capacitor
A9	VDDD	POWER	1.71-V to 5.5-V digital supply
B1	NB	NO BALL	No Ball
B2	P2.3	GPIO	Port 2 Pin 3, analog/digital/lcd/csd
B3	VSSA	GROUND	Analog ground
B4	P2.7	GPIO	Port 2 Pin 7, analog/digital/lcd/csd
B5	P3.4	GPIO	Port 3 Pin 4, analog/digital/lcd/csd
B6	P3.5	GPIO	Port 3 Pin 5, analog/digital/lcd/csd
B7	P3.6	GPIO	Port 3 Pin 6, analog/digital/lcd/csd
B8	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
B9	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
C1	NC	NC	Do not connect
C2	VSSA	GROUND	Analog ground

Table 2. CYBL1XX7X Pin List (WLCSP Package) *(continued)*

Pin	Name	Type	Description
C3	P2.2	GPIO	Port 2 Pin 2, analog/digital/lcd/csd
C4	P2.6	GPIO	Port 2 Pin 6, analog/digital/lcd/csd
C5	P3.0	GPIO	Port 3 Pin 0, analog/digital/lcd/csd
C6	P3.1	GPIO	Port 3 Pin 1, analog/digital/lcd/csd
C7	P3.2	GPIO	Port 3 Pin 2, analog/digital/lcd/csd
C8	XRES	RESET	Reset, active LOW
C9	P4.0	GPIO	Port 4 Pin 0, analog/digital/lcd/csd
D1	NC	NC	Do not connect
D2	P1.7	GPIO	Port 1 Pin 7, analog/digital/lcd/csd
D3	VDDA	POWER	1.71-V to 5.5-V analog supply
D4	P2.0	GPIO	Port 2 Pin 0, analog/digital/lcd/csd
D5	P2.1	GPIO	Port 2 Pin 1, analog/digital/lcd/csd
D6	P2.5	GPIO	Port 2 Pin 5, analog/digital/lcd/csd
D7	VSSD	GROUND	Digital ground
D8	P4.1	GPIO	Port 4 Pin 1, analog/digital/lcd/csd
D9	P5.0	GPIO	Port 5 Pin 0, analog/digital/lcd/csd
E1	NC	NC	Do not connect
E2	P1.2	GPIO	Port 1 Pin 2, analog/digital/lcd/csd
E3	P1.3	GPIO	Port 1 Pin 3, analog/digital/lcd/csd
E4	P1.4	GPIO	Port 1 Pin 4, analog/digital/lcd/csd
E5	P1.5	GPIO	Port 1 Pin 5, analog/digital/lcd/csd
E6	P1.6	GPIO	Port 1 Pin 6, analog/digital/lcd/csd
E7	P2.4	GPIO	Port 2 Pin 4, analog/digital/lcd/csd
E8	P5.1	GPIO	Port 5 Pin 1, analog/digital/lcd/csd
E9	VSSD	GROUND	Digital ground
F1	NC	NC	Do not connect
F2	VSSD	GROUND	Digital ground
F3	P0.7	GPIO	Port 0 Pin 7, analog/digital/lcd/csd
F4	P0.3	GPIO	Port 0 Pin 3, analog/digital/lcd/csd
F5	P1.0	GPIO	Port 1 Pin 0, analog/digital/lcd/csd
F6	P1.1	GPIO	Port 1 Pin 1, analog/digital/lcd/csd
F7	VSSR	GROUND	Radio ground
F8	VSSR	GROUND	Radio ground
F9	VDDR	POWER	1.9-V to 5.5-V radio supply
G1	NC	NC	Do not connect
G2	P0.6	GPIO	Port 0 Pin 6, analog/digital/lcd/csd
G3	VDDD	POWER	1.71-V to 5.5-V digital supply
G4	P0.2	GPIO	Port 0 Pin 2, analog/digital/lcd/csd
G5	VSSD	GROUND	Digital ground
G6	VSSR	GROUND	Radio ground

Table 2. CYBL1XX7X Pin List (WLCSP Package) *(continued)*

Pin	Name	Type	Description
G7	VSSR	GROUND	Radio ground
G8	GANT	GROUND	Antenna shielding ground
G9	VSSR	GROUND	Radio ground
H1	NC	NC	Do not connect
H2	P0.5	GPIO	Port 0 Pin 5, analog/digital/lcd/csd
H3	P0.1	GPIO	Port 0 Pin 1, analog/digital/lcd/csd
H4	XTAL24O	CLOCK	24-MHz crystal
H5	XTAL24I	CLOCK	24-MHz crystal or external clock input
H6	VSSR	GROUND	Radio ground
H7	VSSR	GROUND	Radio ground
H8	ANT	ANTENNA	Antenna pin
J1	NC	NC	Do not connect
J2	P0.4	GPIO	Port 0 Pin 4, analog/digital/lcd/csd
J3	P0.0	GPIO	Port 0 Pin 0, analog/digital/lcd/csd
J4	VDDR	POWER	1.9-V to 5.5-V radio supply
J7	VDDR	POWER	1.9-V to 5.5-V radio supply
J8	NO CONNECT	–	–

The I/O subsystem consists of a high-speed I/O matrix (HSIOM), which is a group of high-speed switches that routes GPIOs to the resources inside the device. These resources include CapSense, TCPWMs, I^2C, SPI, UART, and LCD. HSIOM_PORT_SELx are 32-bit-wide registers that control the routing of GPIOs. Each register controls one port; four dedicated bits are assigned to each GPIO in the port. This provides up to 16 different options for GPIO routing as shown in Table 3.

Table 3. HSIOM Port Settings

Value	Description
0	Firmware-controlled GPIO
1	Reserved
2	Reserved
3	Reserved
4	Pin is a CSD sense pin
5	Pin is a CSD shield pin
6	Pin is connected to AMUXA
7	Pin is connected to AMUXB
8	Pin-specific Active function #0
9	Pin-specific Active function #1
10	Pin-specific Active function #2
11	Reserved
12	Pin is an LCD common pin
13	Pin is an LCD segment pin
14	Pin-specific Deep-Sleep function #0
15	Pin-specific Deep-Sleep function #1

The selection of peripheral functions for different GPIO pins is given in Table 4.

Table 4. Port Pin Connections[1]

Name	Analog	Digital					
		GPIO	Active #0	Active #1	Active #2	Deep Sleep #0	Deep Sleep #1
P0.0	–	GPIO	TCPWM0_P[3]	SCB1_UART_RX[1]	–	SCB1_I2C_SDA[1]	SCB1_SPI_MOSI[1]
P0.1	–	GPIO	TCPWM0_N[3]	SCB1_UART_TX[1]	–	SCB1_I2C_SCL[1]	SCB1_SPI_MISO[1]
P0.2	–	GPIO	TCPWM1_P[3]	SCB1_UART_RTS[1]	–	–	SCB1_SPI_SS0[1]
P0.3	–	GPIO	TCPWM1_N[3]	SCB1_UART_CTS[1]	–		SCB1_SPI_SCLK[1]
P0.4	–	GPIO	TCPWM1_P[0]	SCB0_UART_RX[1]	EXT_CLK[0]/ ECO_OUT[0]	SCB0_I2C_SDA[1]	SCB0_SPI_MOSI[1]
P0.5	–	GPIO	TCPWM1_N[0]	SCB0_UART_TX[1]	–	SCB0_I2C_SCL[1]	SCB0_SPI_MISO[1]
P0.6	–	GPIO	TCPWM2_P[0]	SCB0_UART_RTS[1]	–	SWDIO[0]	SCB0_SPI_SS0[1]
P0.7	–	GPIO	TCPWM2_N[0]	SCB0_UART_CTS[1]	–	SWDCLK[0]	SCB0_SPI_SCLK[1]
P1.0	–	GPIO	TCPWM0_P[1]	–	–	–	WCO_OUT[2]
P1.1	–	GPIO	TCPWM0_N[1]	–	–	–	SCB1_SPI_SS1
P1.2	–	GPIO	TCPWM1_P[1]	–	–	–	SCB1_SPI_SS2
P1.3	–	GPIO	TCPWM1_N[1]	–	–	–	SCB1_SPI_SS3
P1.4	–	GPIO	TCPWM2_P[1]	SCB0_UART_RX[0]	–	SCB0_I2C_SDA[0]	SCB0_SPI_MOSI[1]
P1.5	–	GPIO	TCPWM2_N[1]	SCB0_UART_TX[0]	–	SCB0_I2C_SCL[0]	SCB0_SPI_MISO[1]
P1.6	–	GPIO	TCPWM3_P[1]	SCB0_UART_RTS[0]	–	–	SCB0_SPI_SS0[1]
P1.7	–	GPIO	TCPWM3_N[1]	SCB0_UART_CTS[0]	–	–	SCB0_SPI_SCLK[1]
P2.0	–	GPIO	–	–	–	–	SCB0_SPI_SS1
P2.1	–	GPIO	–	–	–	–	SCB0_SPI_SS2
P2.2	–	GPIO	–	–	–	WAKEUP	SCB0_SPI_SS3
P2.3	–	GPIO	–	–	–	–	WCO_OUT[1]
P2.4	–	GPIO	–	–	–	–	–
P2.5	–	GPIO	–	–	–	–	–
P2.6	–	GPIO	–	–	–	–	–
P2.7	–	GPIO	–	–	EXT_CLK[1]/ ECO_OUT[1]	–	–
P3.0	SARMUX_0	GPIO	TCPWM0_P[2]	SCB0_UART_RX[2]	–	SCB0_I2C_SDA[2]	–
P3.1	SARMUX_1	GPIO	TCPWM0_N[2]	SCB0_UART_TX[2]	–	SCB0_I2C_SCL[2]	–
P3.2	SARMUX_2	GPIO	TCPWM1_P[2]	SCB0_UART_RTS[2]	–	–	–
P3.3	SARMUX_3	GPIO	TCPWM1_N[2]	SCB0_UART_CTS[2]	–	–	–
P3.4	SARMUX_4	GPIO	TCPWM2_P[2]	SCB1_UART_RX[2]	–	SCB1_I2C_SDA[2]	–
P3.5	SARMUX_5	GPIO	TCPWM2_N[2]	SCB1_UART_TX[2]	–	SCB1_I2C_SCL[2]	–
P3.6	SARMUX_6	GPIO	TCPWM3_P[2]	SCB1_UART_RTS[2]	–	–	–
P3.7	SARMUX_7	GPIO	TCPWM3_N[2]	SCB1_UART_CTS[2]	–	–	WCO_OUT[0]
P4.0	CMOD	GPIO	TCPWM0_P[0]	SCB1_UART_RTS[0]	–	–	SCB1_SPI_MOSI[0]

Note
1. For devices with only 1 SCB, use pins corresponding to SCB1.

Table 4. Port Pin Connections[1] *(continued)*

Name	Analog	Digital					
		GPIO	Active #0	Active #1	Active #2	Deep Sleep #0	Deep Sleep #1
P4.1	CTANK	GPIO	TCPWM0_N[0]	SCB1_UART_CTS[0]	–	–	SCB1_SPI_MISO[0]
P5.0	–	GPIO	TCPWM3_P[0]	SCB1_UART_RX[0]	EXTPA_EN	SCB1_I2C_SDA[0]	SCB1_SPI_SS0[0]
P5.1	–	GPIO	TCPWM3_N[0]	SCB1_UART_TX[0]	EXT_CLK[2]/ ECO_OUT[2]	SCB1_I2C_SCL[0]	SCB1_SPI_SCLK[0]
P6.0_XTAL32O	–	GPIO	–	–	–	–	–
P6.1_XTAL32I	–	GPIO	–	–	–	–	–

Power

PRoC BLE can be supplied from batteries with a voltage range of 1.9 V to 5.5 V by directly connecting to the digital supply (V_{DDD}), analog supply (V_{DDA}), and radio supply (V_{DDR}) pins. The internal LDOs in the device regulate the supply voltage to required levels for different blocks. The device has one regulator for the digital circuitry and separate regulators for radio circuitry for noise isolation. The analog circuits run directly from the analog supply (V_{DDA}) input. The device uses separate regulators for Deep Sleep and Hibernate modes to minimize the power consumption. The radio stops working below 1.9 V, but the rest of the system continues to function down to 1.71 V without RF.

Bypass capacitors must be used from VDDx (x = A, D, or R) to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (for example, 0.1 µF). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design to obtain optimal bypassing.

Power Supply	Bypass Capacitors
V_{DDD}	0.1-µF ceramic at each pin plus bulk capacitor 1-µF to 10-µF
V_{DDA}	0.1-µF ceramic at each pin plus bulk capacitor 1-µF to 10-µF
V_{DDR}	0.1-µF ceramic at each pin plus bulk capacitor 1-µF to 10-µF
V_{CCD}	1.3-µF ceramic capacitor at the VCCD pin
V_{REF} (optional)	The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor

Low-Power Modes

PRoC BLE supports five power modes. Refer to Table 5 for more details on the system status. The PRoC BLE device consumes the lowest current in Stop mode; the device wakeup from stop mode is with a system reset through the XRES or WAKEUP pin. It can retain the SRAM data in Hibernate mode and is capable of retaining the complete system status in Deep-Sleep mode. Table 5 shows the different power modes and the peripherals that are active.

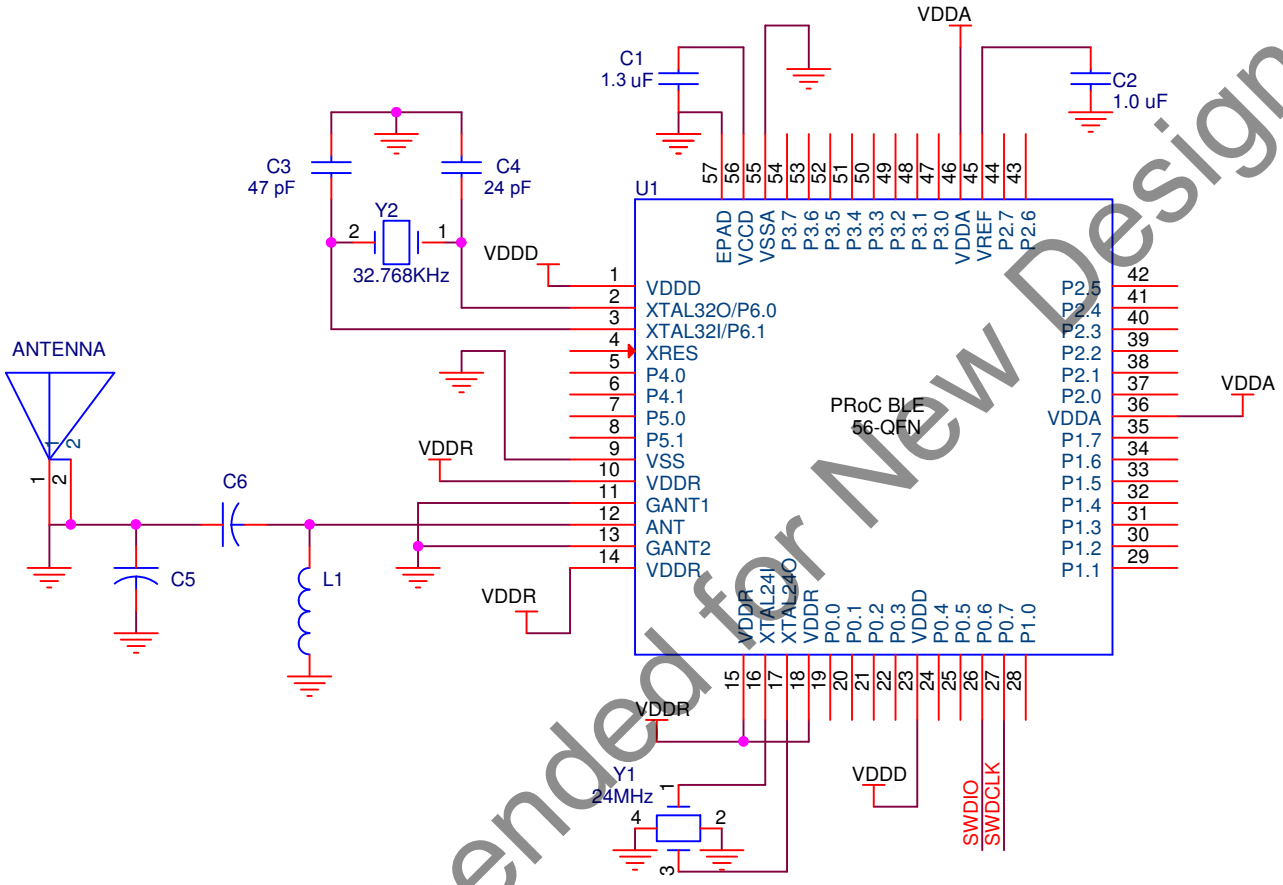
Table 5. Power Modes System Status

Power Mode	Current Consumption	Code Execution	Digital Peripherals Available	Analog Peripherals Available	Clock Sources Available	Wake Up Sources	Wake-Up Time
Active	850 µA + 260 µA per MHz[2]	Yes	All	All	All	–	–
Sleep	1.1 mA at 3 MHz	No	All	All	All	Any interrupt source	0
Deep Sleep	1.5 µA	No	WDT, LCD, I²C/SPI, Link-Layer	POR, BOD	WCO, ILO	GPIO, WDT, I²C/SPI Link Layer	25 µs
Hibernate	150 nA	No	No	POR, BOD	No	GPIO	0.7 ms
Stop	60 nA	No	No	No	No	Wake-Up pin, XRES	2.2 ms

Note
2. For CPU subsystem.

A typical system application connection diagram for the 56-QFN package is shown in Figure 5.

Figure 5. PRoC BLE Applications Diagram



Development Support

The CYBL1XX7X family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/procble to find out more.

Documentation

A suite of documentation supports the CYBL1XX7X family to ensure that you find answers to your questions quickly. This section contains a list of some of the key documents.

Component Datasheets: PSoC Creator Components provide hardware abstraction using APIs to configure and control peripheral activity. The Component datasheet covers Component features, its usage and operation details, API description, and electrical specifications. This is the primary documentation used during development. These Components can represent peripherals on the device (such as a timer, I^2C, or UART) or high-level system functions (such as the BLE Component).

Application Notes: Application notes help you to understand how to use various device features. They also provide guidance on how to solve a variety of system design challenges.

Technical Reference Manual (TRM): The TRM describes all peripheral functionality in detail, with register-level descriptions. This document is divided into two parts: the Architecture TRM and the Register TRM.

Online

In addition to the print documentation, Cypress forums connect you with fellow users and experts from around the world, 24 hours a day, 7 days a week.

Tools

With industry-standard cores, programming, and debugging interfaces, the CYBL1XX7X family is part of a development tool ecosystem.

Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy-to-use PSoC Creator IDE, supported third-party compilers, programmers, and debuggers.

Kits

Cypress provides a portfolio of kits to accelerate time-to-market. Visit us at www.cypress.com/procble.

Electrical Specifications

This section provides detailed electrical characteristics. Absolute maximum rating for the CYBL1XX7X devices is listed in Table 6 through Table 50. Usage above the absolute maximum conditions may cause permanent damage to the device.

Exposure to absolute maximum conditions for extended periods of time may affect device reliability.

The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions, but above normal operating conditions, the device may not operate to the specification.

Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Analog, digital, or radio supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	6	V	Absolute max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute max
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} +0.5	V	Absolute max
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
BID57	ESD_HBM	Electrostatic discharge human body model	2200[3]	–	–	V	–
BID58	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
BID61	LU	Pin current for latch up	–200	–	200	mA	–

BLE Subsystem

Table 7. BLE Subsystem

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
RF Receiver Specifications							
SID340	RXS, IDLE	RX sensitivity with idle transmitter	–	–89	–	dBm	–
SID340A		RX sensitivity with idle transmitter excluding Balun loss	–	–91	–	dBm	Guaranteed by design simulation
SID341	RXS, DIRTY	RX sensitivity with dirty transmitter	–	–87	–70	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
SID342	RXS, HIGHGAIN	RX sensitivity in high-gain mode with idle transmitter	–	–91	–	dBm	–
SID343	PRXMAX	Maximum input power	–10	–1	–	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
SID344	CI1	Co-channel interference, Wanted signal at –67 dBm and Interferer at F_{RX}	–	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)

Note
3. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500-V HBM.

Table 7. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID345	CI2	Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±1 MHz	–	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID346	CI3	Adjacent channel interference Wanted signal at –67 dBm and Interferer at F_{RX} ±2 MHz	–	–29	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID347	CI4	Adjacent channel interference Wanted signal at –67 dBm and Interferer at ≥F_{RX} ±3 MHz	–	–39	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID348	CI5	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (F_{IMAGE})	–	–20	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID349	CI6	Adjacent channel interference Wanted signal at –67 dBm and Interferer at Image frequency (F_{IMAGE} ± 1 MHz)	–	–30	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID350	OBB1	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 30–2000 MHz	–30	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID351	OBB2	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2,003–2,399 MHz	–35	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID352	OBB3	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2,484–2,997 MHz	–35	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID353	OBB4	Out-of-band blocking, Wanted signal a –67 dBm and Interferer at F = 3,000–12,750 MHz	–30	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID354	IMD	Intermodulation performance Wanted signal at –64 dBm and 1-Mbps BLE, third, fourth, and fifth offset channel	–50	–	–	dBm	RF-PHY Specification (RCV-LE/CA/05/C)
SID355	RXSE1	Receiver spurious emission 30 MHz to 1.0 GHz	–	–	–57	dBm	100-kHz measurement bandwidth ETSI EN300 328 V1.8.1
SID356	RXSE2	Receiver spurious emission 1.0 GHz to 12.75 GHz	–	–	–47	dBm	1-MHz measurement bandwidth ETSI EN300 328 V1.8.1
RF Transmitter Specifications							
SID357	TXP, ACC	RF power accuracy	–	±1	–	dB	–
SID358	TXP, RANGE	RF power control range	–	20	–	dB	–
SID359	TXP, 0 dBm	Output power, 0-dB gain setting (PA7)	–	0	–	dBm	–

Table 7. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID360	TXP, MAX	Output power, maximum power setting (PA10)	–	3	–	dBm	–
SID361	TXP, MIN	Output power, minimum power setting (PA1)	–	–18	–	dBm	–
SID362	F2AVG	Average frequency deviation for 10101010 pattern	185	–	–	kHz	RF-PHY Specification (TRM-LE/CA/05/C)
SID363	F1AVG	Average frequency deviation for 11110000 pattern	225	250	275	kHz	RF-PHY Specification (TRM-LE/CA/05/C)
SID364	EO	Eye opening = ΔF2AVG/ΔF1AVG	0.8	–	–		RF-PHY Specification (TRM-LE/CA/05/C)
SID365	FTX, ACC	Frequency accuracy	–150	–	150	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID366	FTX, MAXDR	Maximum frequency drift	–50	–	50	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID367	FTX, INITDR	Initial frequency drift	–20	–	20	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID368	FTX,DR	Maximum drift rate	–20	–	20	kHz/ 50 µs	RF-PHY Specification (TRM-LE/CA/06/C)
SID369	IBSE1	In-band spurious emission at 2-MHz offset	–	–	–20	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
SID370	IBSE2	In-band spurious emission at ≥3-MHz offset	–	–	–30	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
SID371	TXSE1	Transmitter spurious emissions (average), <1.0 GHz	–	–	–55.5	dBm	FCC-15.247
SID372	TXSE2	Transmitter spurious emissions (average), >1.0 GHz	–	–	–41.5	dBm	FCC-15.247
RF Current Specification							
SID373	IRX	Receive current in normal mode	–	18.7	–	mA	–
SID373A	IRX_RF	Receive current in normal mode	–	16.4	–	mA	Measured at V_{DDR}
SID374	IRX, HIGHGAIN	Receive current in high-gain mode	–	21.5	–	mA	–
SID375	ITX, 3 dBm	TX current at 3-dBm setting (PA10)	–	20	–	mA	–
SID376	ITX, 0 dBm	TX current at 0-dBm setting (PA7)	–	16.5	–	mA	–
SID376A	ITX_RF, 0 dBm	TX current at 0-dBm setting (PA7)	–	15.6	–	mA	Measured at V_{DDR}
SID376B	ITX_RF, 0 dBm	TX current at 0 dBm excluding Balun loss	–	14.2	–	mA	Guaranteed by design simulation
SID377	ITX, -3 dBm	TX current at –3-dBm setting (PA4)	–	15.5	–	mA	–
SID378	ITX, -6 dBm	TX current at –6-dBm setting (PA3)	–	14.5	–	mA	–
SID379	ITX, -12 dBm	TX current at –12-dBm setting (PA2)	–	13.2	–	mA	–
SID380	ITX, -18 dBm	TX current at –18-dBm setting (PA1)	–	12.5	–	mA	–
SID380A	Iavg_1sec, 0 dBm	Average current at 1-second BLE connection interval	–	17.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy

Table 7. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID380B	Iavg_4sec, 0 dBm	Average current at 4-second BLE connection interval	–	6.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy
General RF Specification							
SID381	FREQ	RF operating frequency	2400	–	2482	MHz	–
SID382	CHBW	Channel spacing	–	2	–	MHz	–
SID383	DR	On-air data rate	–	1000	–	kbps	–
SID384	IDLE2TX	BLE Radio Idle to BLE Radio TX transition time	–	120	140	µs	–
SID385	IDLE2RX	BLE Radio Idle to BLE Radio RX transition time	–	75	120	µs	–
RSSI Specification							
SID386	RSSI, ACC	RSSI accuracy	–	±5	–	dB	–
SID387	RSSI, RES	RSSI resolution	–	1	–	dB	–
SID388	RSSI, PER	RSSI sample period	–	6	–	µs	–

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71-V to 5.5-V, except where noted.

Table 8. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID6	V_{DD}	Power supply input voltage (V_{DDA} = V_{DDD} = V_{DD})	1.8	–	5.5	V	With regulator enabled
SID7	V_{DD}	Power supply input voltage unregulated (V_{DDA} = V_{DDD} = V_{DD})	1.71	1.8	1.89	V	Internally unregulated supply
SID8	V_{DDR}	Radio supply voltage (Radio on)	1.9	–	5.5	V	–
SID8A	V_{DDR}	Radio supply voltage (Radio off)	1.71	–	5.5	V	–
SID9	V_{CCD}	Digital regulator output voltage (for core logic)	–	1.8	–	V	–
SID10	C_{VCCD}	Digital regulator output bypass capacitor	1	1.3	1.6	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V							
SID13	I_{DD3}	Execute from flash; CPU at 3 MHz	–	2.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID14	I_{DD4}	Execute from flash; CPU at 3 MHz	–	–	–	mA	T = –40 °C to 85 °C
SID15	I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID16	I_{DD6}	Execute from flash; CPU at 6 MHz	–	–	–	mA	T = –40 °C to 85 °C
SID17	I_{DD7}	Execute from flash; CPU at 12 MHz	–	4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID18	I_{DD8}	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 85 °C
SID19	I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V

Table 8. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID20	I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
SID21	I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID22	I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
Sleep Mode, V_{DD} = 1.8 to 5.5 V							
SID23	I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, V_{DD} = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 to 5.5 V							
SID24	I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, V_{DD} = 3.3 V, SYSCLK = 3 MHz
Deep-Sleep Mode, V_{DD} = 1.8 to 3.6 V							
SID25	I_{DD15}	WDT with WCO on	–	1.5	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID26	I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep-Sleep Mode, V_{DD} = 3.6 to 5.5 V							
SID27	I_{DD17}	WDT with WCO on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID28	I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep-Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID29	I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
SID30	I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.8 to 3.6 V							
SID37	I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID38	I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 3.6 to 5.5 V							
SID39	I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID40	I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID41	I_{DD31}	GPIO and reset active	–	–	–	nA	T = 25 °C
SID42	I_{DD32}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.8 to 3.6 V							
SID43	I_{DD33}	Stop-mode current (V_{DD})	–	20	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID44	I_{DD34}	Stop-mode current (V_{DDR})	–	40	–-	nA	T = 25 °C, V_{DDR} = 3.3 V
SID45	I_{DD35}	Stop-mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID46	I_{DD36}	Stop-mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C, V_{DDR} = 1.9 V to 3.6 V
Stop Mode, V_{DD} = 3.6 to 5.5 V							
SID47	I_{DD37}	Stop-mode current (V_{DD})	–	–	–	nA	T = 25 °C, V_{DD} = 5 V

Table 8. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	I_{DD38}	Stop-mode current (V_{DDR})	–	–	–	nA	T = 25 °C, V_{DDR} = 5 V
SID49	I_{DD39}	Stop-mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID50	I_{DD40}	Stop-mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID51	I_{DD41}	Stop-mode current (V_{DD})	–	–	–	nA	T = 25 °C
SID52	I_{DD42}	Stop-mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C

Table 9. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
SID54	T_{SLEEP}	Wakeup from Sleep mode	–	0		µs	Guaranteed by characterization
SID55	$T_{DEEPSLEEP}$	Wakeup from Deep-Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization
SID56	$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID57	T_{STOP}	Wakeup from Stop mode	–	–	2.2	ms	Guaranteed by characterization

GPIO

Table 10. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID58	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS input
SID59	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS input
SID60	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}	–	-	V	–
SID61	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3× V_{DD}	V	–
SID62	V_{IH}	LVTTL input, V_{DD} >= 2.7 V	2.0	–	-	V	–
SID63	V_{IL}	LVTTL input, V_{DD} >= 2.7 V	–	–	0.8	V	–
SID64	V_{OH}	Output voltage HIGH level	V_{DD} –0.6	–	–	V	I_{OH} = 4-mA at 3.3-V V_{DD}
SID65	V_{OH}	Output voltage HIGH level	V_{DD} –0.5	–	–	V	I_{OH} = 1-mA at 1.8-V V_{DD}
SID66	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8-mA at 3.3-V V_{DD}
SID67	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4-mA at 1.8-V V_{DD}
SID68	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 3-mA at 3.3-V V_{DD}
SID69	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID70	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–

Note
4. V_{IH} must not exceed V_{DD} + 0.2 V.

Table 10. GPIO DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID71	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.3 V
SID72	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
SID73	C_{IN}	Input capacitance	–	–	7	pF	–
SID74	V_{HYSTTL}	Input hysteresis LVTTL	25	40		mV	V_{DD} ≥ 2.7 V
SID75	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DD}	–	–	mV	–
SID76	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID77	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 11. GPIO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID78	T_{RISEF}	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID79	T_{FALLF}	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID80	T_{RISES}	Rise time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID81	T_{FALLS}	Fall time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID82	$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Fast-Strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID83	$F_{GPIOUT2}$	GPIO Fout; 1.7 V ≤ V_{DD} ≤ 3.3 V. Fast-Strong mode	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID84	$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Slow-Strong mode	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID85	$F_{GPIOUT4}$	GPIO Fout; 1.7 V ≤ V_{DD} ≤ 3.3 V. Slow-Strong mode	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID86	F_{GPIOIN}	GPIO input operating frequency. 1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

Table 12. OVT GPIO DC Specifications (P5_0 and P5_1 Only)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID71A	I_{IL}	Input leakage (absolute value). $V_{IH} > V_{DD}$	–	–	10	µA	25°C, V_{DD} = 0 V, V_{IH} = 3.0 V
SID66A	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 20-mA, V_{DD} > 2.9 V
SID78A	T_{RISE_OVFS}	Output rise time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD} = 3.3-V
SID79A	T_{FALL_OVFS}	Output fall time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD} = 3.3-V
SID80A	T_{RISESS}	Output rise time in Slow-Strong mode	10	–	60	ns	25-pF load, 10%-90%, V_{DD} = 3.3-V
SID81A	T_{FALLSS}	Output fall time in Slow-Strong mode	10	–	60	ns	25-pF load, 10%-90%, V_{DD} = 3.3-V
SID82A	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID83A	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25-pF load, 60/40 duty cycle

XRES

Table 13. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID87	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID88	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID89	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID90	C_{IN}	Input capacitance	–	3	–	pF	–
SID91	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
SID92	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

Table 14. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID93	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–

Analog Peripherals

Temperature Sensor

Table 15. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID155	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

SAR ADC

Table 16. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID156	A_RES	Resolution	–	–	12	bits	–
SID157	A_CHNIS_S	Number of channels – single-ended	–	–	16	–	8 full-speed
SID158	A-CHNKS_D	Number of channels – differential	–	–	8	–	Differential inputs use neighboring I/O
SID159	A-MONO	Monotonicity	–	–	–	–	Yes
SID160	A_GAINERR	Gain error	–	–	±0.1	%	With external reference
SID161	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}
SID162	A_ISAR	Current consumption	–	–	1	mA	–
SID163	A_VINS	Input voltage range – single-ended	V_{SS}	–	V_{DDA}	V	–
SID164	A_VIND	Input voltage range – differential	V_{SS}	–	V_{DDA}	V	–
SID165	A_INRES	Input resistance	–	–	2.2	kΩ	–
SID166	A_INCAP	Input capacitance	–	–	10	pF	–
SID312	VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of Vbg (1.024 V)

Table 17. SAR ADC AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID167	A_PSRR	Power supply rejection ratio	70	–	–	dB	Measured at 1-V reference
SID168	A_CMRR	Common-mode rejection ratio	66	–	–	dB	–
SID169	A_SAMP	Sample rate	–	–	1	Msps	–
SID313	Fsarintref	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution
SID170	A_SNR	Signal-to-noise ratio (SNR)	65	–	–	dB	F_{IN} = 10 kHz
SID171	A_BW	Input bandwidth without aliasing	–	–	A_SAMP/2	kHz	–
SID172	A_INL	Integral nonlinearity (INL). V_{DD} = 1.71 to 5.5 V, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 V to V_{DD}
SID173	A_INL	Integral nonlinearity. V_{DDD} = 1.71 to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 V to V_{DD}
SID174	A_INL	Integral nonlinearity. V_{DD} = 1.71 to 5.5 V, 500 ksps	–1.5	–	1.7	LSB	V_{REF} = 1 V to V_{DD}