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## General Description

The CYBLE-01201X-X0 is a Bluetooth® Low Energy (BLE) wireless module solution. The CYBLE-01201X-X0 is a turnkey solution and includes onboard crystal oscillators, trace antenna, passive components, and the Cypress PProC™ BLE. Refer to the CYBL10X6X [datasheet](#) for additional details on the capabilities of the PProC BLE device used on this module.

The CYBLE-01201X-X0 supports a number of peripheral functions (ADC, timers, counters, PWM) and serial communication protocols (I<sup>2</sup>C, UART, SPI) through its programmable architecture. The CYBLE-01201X-X0 includes a royalty-free BLE stack compatible with Bluetooth 4.1 and provides up to 23 GPIOs in a 14.52 × 19.20 × 2.00 mm package.

The CYBLE-01201X-X0 is available in a fully certified and qualified version (CYBLE-012011-00), and an uncertified version (CYBLE-012012-10). The CYBLE-012012-10 does not include an RF shield and is not certified by Bluetooth SIG or regulatory agencies.

The CYBLE-01201X-X0 is a complete solution targeted at applications requiring cost optimized BLE wireless connectivity.

## Module Description

- Module size: 14.52 mm × 19.20 mm × 2.00 mm (with shield)
- Castelated solder pad connections for ease-of-use
- 128-KB flash memory, 16-KB SRAM memory
- Up to 23 GPIOs configurable as open drain high/low, pull-up/pull-down, HI-Z analog, HI-Z digital, or strong output
- Bluetooth 4.1 qualified single-mode module
  - QDID: [79919](#) (CYBLE-012011-00 only)
  - Declaration ID: [D029885](#) (CYBLE-012011-00 only)
- Certified to FCC, IC, MIC, KC, and CE regulations
- Industrial temperature range: -40 °C to +85 °C
- 32-bit processor (0.9 DMIPS/MHz) with single-cycle 32-bit multiply, operating at up to 48 MHz
- Watchdog timer with dedicated internal low-speed oscillator (ILO)
- Two-pin SWD for programming

## Power Consumption

- TX output power: -18 dbm to +3 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution
- TX current consumption of 15.6 mA (radio only, 0 dbm)
- RX current consumption of 16.4 mA (radio only)

- Low power mode support
  - Deep Sleep: 1.3 µA with watch crystal oscillator (WCO) on
  - Hibernate: 150 nA with SRAM retention
  - Stop: 60 nA with GPIO (P2.2) or XRES wakeup

## Functional Capabilities

- Up to 22 capacitive sensors for buttons or sliders with best-in-class signal-to-noise ratio (SNR) and liquid tolerance
- 12-bit, 1-Msps SAR ADC with internal reference, sample-and-hold (S/H), and channel sequencer
- Two serial communication blocks (SCBs) supporting I<sup>2</sup>C (master/slave), SPI (master/slave), or UART
- Four dedicated 16-bit timer, counter, or PWM blocks (TCPWMs)
- LCD drive supported on all GPIOs (common or segment)
- Programmable low voltage detect (LVD) from 1.8 V to 4.5 V
- I<sup>2</sup>S master interface
- Bluetooth Low Energy protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
- Switches between Central and Peripheral roles on-the-go
- Standard Bluetooth Low Energy profiles and services for interoperability
- Custom profile and service for specific use cases

## Benefits

The CYBLE-01201X-X0 module is provided as a turnkey solution, including all necessary hardware required to use BLE communication standards.

- Proven hardware design ready to use
- Cost optimized for applications without space constraint, Footprint
  - 14.52 × 19.20 mm × 2.00 mm - CYBLE-012011-00
  - 14.52 × 19.20 mm × 1.55 mm - CYBLE-012012-10
- Reprogrammable architecture
- Fully certified module (CYBLE-012011-00) eliminates the time needed for design, development and certification processes
- Bluetooth SIG qualified with QDID and Declaration ID (CYBLE-012011-00 Only)
- Flexible communication protocol support
- PSoC Creator™ provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test a BLE application



## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

- Overview: [EZ-BLE Module Portfolio](#), [Module Roadmap](#)
- [EZ-BLE PSoC Product Overview](#)
- [PSoC BLE Silicon Datasheet](#)
- Application notes: Cypress offers a number of BLE application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with EZ-BLE modules are:
  - [AN96841](#) - Getting Started with EZ-BLE Module
  - [AN94020](#) - Getting Started with PSoC BLE
  - [AN97060](#) - PSoC<sup>®</sup> 4 BLE and PSoC<sup>™</sup> BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - [AN91162](#) - Creating a BLE Custom Profile
  - [AN91184](#) - PSoC 4 BLE - Designing BLE Applications
  - [AN92584](#) - Designing for Low Power and Estimating Battery Life for BLE Applications
  - [AN85951](#) - PSoC<sup>®</sup> 4 CapSense<sup>®</sup> Design Guide
  - [AN95089](#) - PSoC<sup>®</sup> 4/PSoC<sup>™</sup> BLE Crystal Oscillator Selection and Tuning Techniques
  - [AN91445](#) - Antenna Design and RF Layout Guidelines
- Technical Reference Manual (TRM):
  - PSoC<sup>®</sup> BLE [Technical Reference Manual](#)
- Knowledge Base Articles
  - [KBA09921](#) - Pin Mapping Differences Between the EZ-BLE<sup>™</sup> PSoC<sup>™</sup> Evaluation Board (CYBLE-012011-EVAL) and the BLE Pioneer Kit (CY8CKIT-042-BLE)
  - [KBA97095](#) - EZ-BLE<sup>™</sup> Module Placement
  - [KBA210638](#) - RF Regulatory Certifications for CYBLE-012011-00 and CYBLE-212019-00 EZ-BLE<sup>™</sup> PSoC<sup>®</sup> Modules - KBA210638
  - [KBA213976](#) - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - [KBA210802](#) - Queries on BLE Qualification and Declaration Processes
- Development Kits:
  - [CYBLE-012011-EVAL](#) - CYBLE-012011-00 and CYBLE-012012-10 Evaluation Board
  - [CY8CKIT-042-BLE](#) - Bluetooth<sup>®</sup> Low Energy (BLE) Pioneer Kit
  - [CY8CKIT-002](#) - PSoC<sup>®</sup> MiniProg3 Program and Debug Kit
- Test and Debug Tools:
  - [CYSmart](#) - Bluetooth<sup>®</sup> LE Test and Debug Tool (Windows)
  - [CYSmart Mobile](#) - Bluetooth<sup>®</sup> LE Test and Debug Tool (Android/iOS Mobile App)

## Two Design Environments to Get You Started Quickly

### PSoC<sup>®</sup> Creator<sup>™</sup> Integrated Design Environment (IDE)

[PSoC Creator](#) is an Integrated Design Environment (IDE) that enables concurrent hardware and firmware editing, compiling and debugging of PSoC 3, PSoC 4, PSoC 5LP, PSoC 4 BLE, PSoC BLE and EZ-BLE module systems with no code size limitations. PSoC peripherals are designed using schematic capture and simple graphical user interface (GUI) with over 120 pre-verified, production-ready PSoC Components<sup>™</sup>.

PSoC Components are analog and digital “virtual chips,” represented by an icon that users can drag-and-drop into a design and configure to suit a broad array of application requirements.

#### *Bluetooth Low Energy Component*

The [Bluetooth Low Energy Component](#) inside PSoC Creator provides a comprehensive GUI-based configuration window that lets you quickly design BLE applications. The Component incorporates a Bluetooth Core Specification v4.1 compliant BLE protocol stack and provides API functions to enable user applications to interface with the underlying Bluetooth Low Energy Sub-System (BLESS) hardware via the stack.

### EZ-Serial<sup>™</sup> BLE Firmware Platform

The [EZ-Serial Firmware Platform](#) provides a simple way to access the most common hardware and communication features needed in BLE applications. EZ-Serial implements an intuitive API protocol over the UART interface and exposes various status and control signals through the module’s GPIOs, making it easy to add BLE functionality quickly to existing designs.

Use a simple serial terminal and evaluation kit to begin development without requiring an IDE. Refer to the EZ-Serial webpage for User Manuals and instructions for getting started as well as detailed reference materials.

EZ-BLE modules are pre-flashed with the EZ-Serial Firmware Platform. If you do not have EZ-Serial pre-loaded on your module, you can download each EZ-BLE module’s firmware images on the [EZ-Serial webpage](#).

## Technical Support

- [Frequently Asked Questions \(FAQs\)](#): Learn more about our BLE ECO System.
- [Forum](#): See if your question is already answered by fellow developers on the PSoC 4 BLE and PSoC BLE forums.
- Visit our [support](#) page and create a [technical support case](#) or contact a [local sales representative](#). If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

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## Overview

### Module Description

The CYBLE-01201X-X0 module is a complete module designed to be soldered to the applications main board.

#### *Module Dimensions and Drawing*

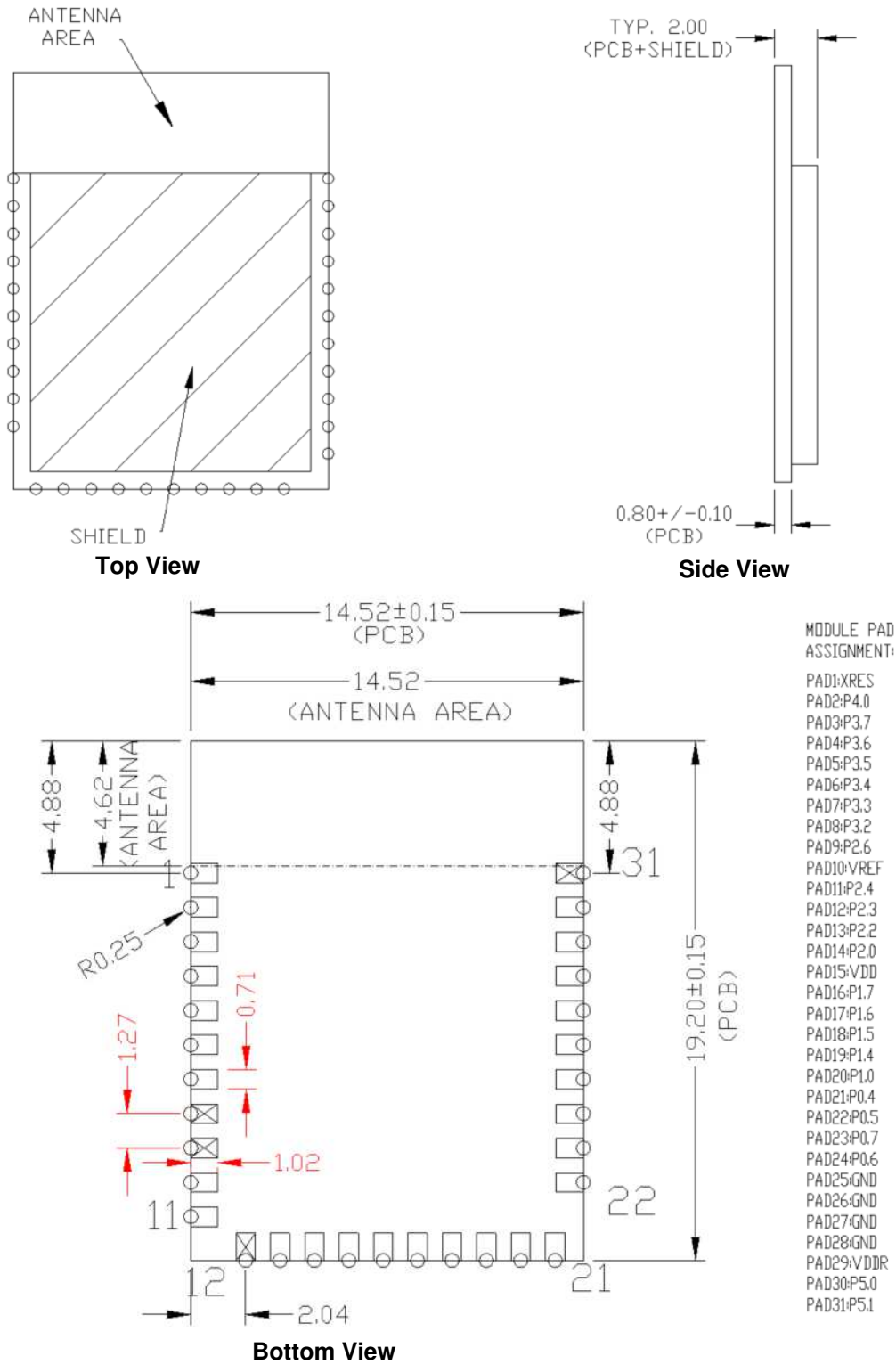
Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will still guarantee that all height restrictions of the component area are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in [Figure 1](#). All dimensions are in millimeters (mm).

**Table 1. Module Design Dimensions**

Dimension Item		Specification
Module dimensions	Length (X)	14.52 ± 0.15 mm
	Width (Y)	19.20 ± 0.15 mm
Antenna location dimensions	Length (X)	11.00 ± 0.15 mm
	Width (Y)	5.00 ± 0.15 mm
PCB thickness	Height (H)	0.80 ± 0.10 mm
Shield height	Height (H)	1.20 ± 0.10 mm
Maximum component height	Height (H)	1.20 mm typical (shield) - CYBLE-012011-00 0.75 mm typical (crystal) - CYBLE-012012-10
Total module thickness (bottom of module to highest component)	Height (H)	2.00 mm typical - CYBLE-012011-00 1.55 mm typical - CYBLE-012012-10

See [Figure 1](#) on page 5 for the mechanical reference drawing for CYBLE-01201X-X0.

Figure 1. Module Mechanical Drawing



**Note**

1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see [Figure 3](#), [Figure 4](#), [Figure 5](#), and [Figure 6](#) and [Table 3](#).

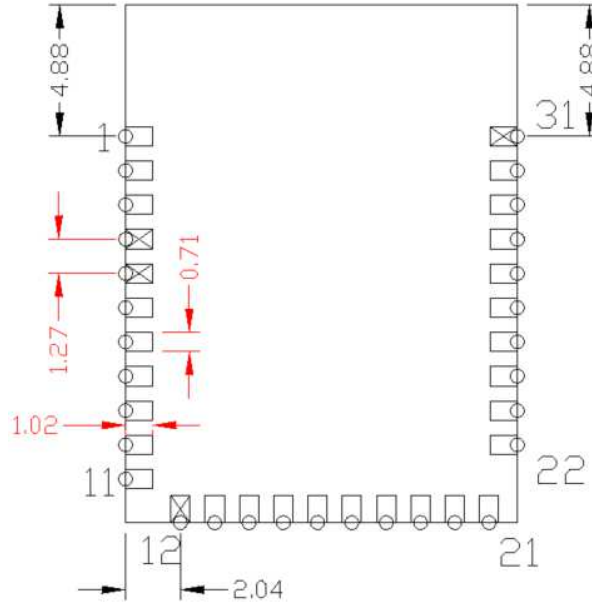
## Pad Connection Interface

As shown in the bottom view of [Figure 1](#) on page 5, the CYBLE-01201X-X0 connects to the host board via solder pads on the backside of the module. [Table 2](#) and [Figure 2](#) detail the solder pad length, width, and pitch dimensions of the CYBLE-01201X-X0 module.

**Table 2. Solder Pad Connection Description**

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	31	Solder Pads	1.02 mm	0.71 mm	1.27 mm

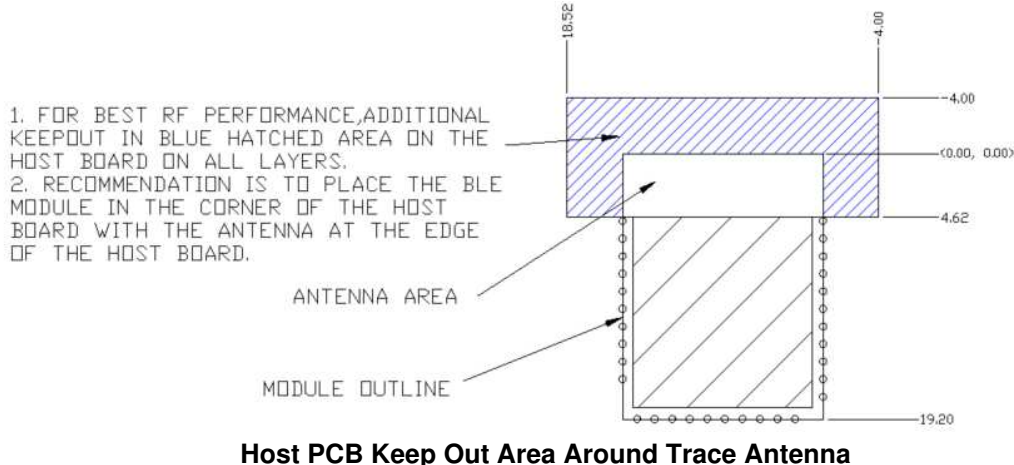
**Figure 2. Solder Pad Dimensions (Seen from Bottom)**



To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE module is in a corner of the host board with the trace antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2. Refer to [AN96841](#) for module placement best practices.
2. To maximize RF performance, the area immediately around the Cypress BLE module trace antenna should contain an additional keep out area, where no grounding or signal trace are contained. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in [Figure 3](#) (dimensions are in mm).

**Figure 3. Recommended Host PCB Keep Out Area Around the CYBLE-01201X-X0 Antenna**

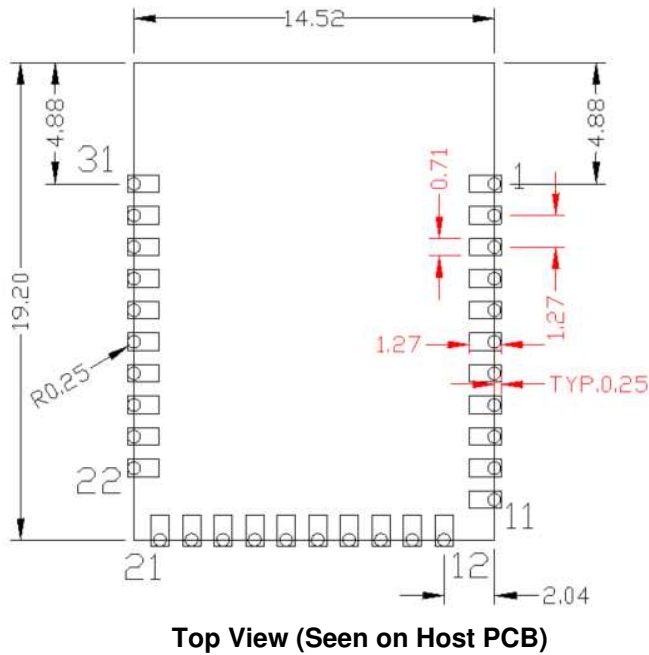


**Host PCB Keep Out Area Around Trace Antenna**

## Recommended Host PCB Layout

Figure 4, Figure 5, Figure 6, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-01201X-X0. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.635 mm from center of the pad on either side) shown in Figure 6 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 4, Figure 5, or Figure 6. It is not necessary to use all figures to complete the host PCB layout pattern.

**Figure 4. Host Layout Pattern for CYBLE-01201X-X0**



**Figure 5. Module Pad Location from Origin**

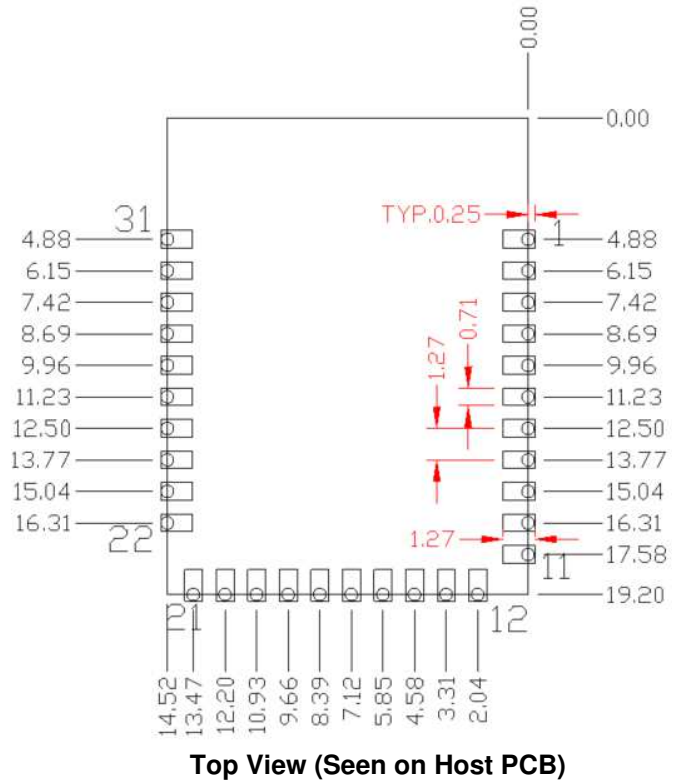


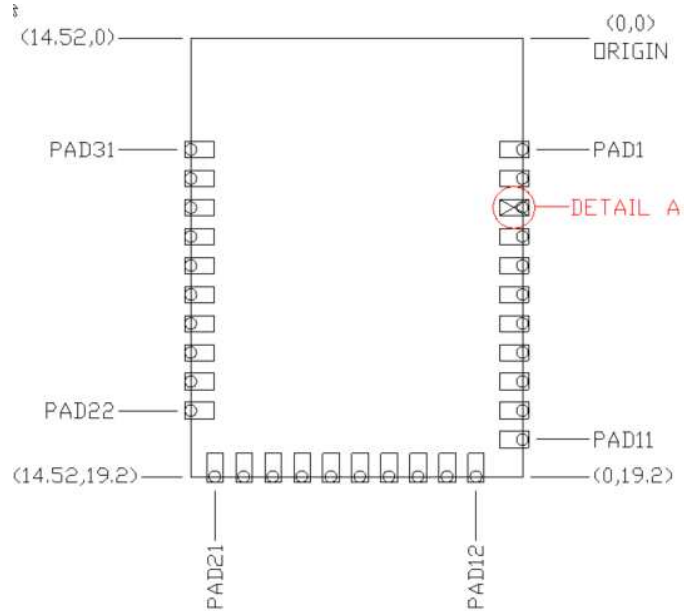


Table 3 provides the center location for each solder pad on the CYBLE-01201X-X0. All dimensions are referenced to the center of the solder pad. Refer to Figure 6 for the location of each module solder pad.

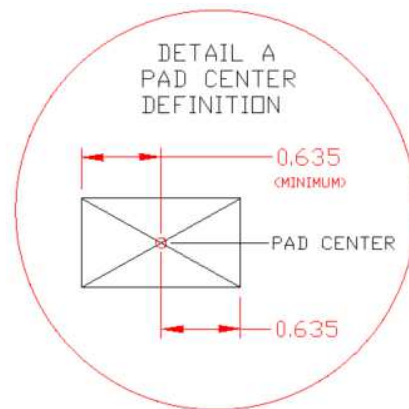
**Table 3. Module Solder Pad Location**

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Dimension from Origin (mils)
1	(0.39, 4.88)	(15.35, 192.13)
2	(0.39, 6.15)	(15.35, 242.13)
3	(0.39, 7.42)	(15.35, 292.13)
4	(0.39, 8.69)	(15.35, 342.13)
5	(0.39, 9.96)	(15.35, 392.13)
6	(0.39, 11.23)	(15.35, 442.13)
7	(0.39, 12.50)	(15.35, 492.13)
8	(0.39, 13.77)	(15.35, 542.13)
9	(0.39, 15.04)	(15.35, 592.13)
10	(0.39, 16.31)	(15.35, 642.13)
11	(0.39, 17.58)	(15.35, 692.13)
12	(2.04, 18.82)	(80.31, 740.94)
13	(3.31, 18.82)	(130.31, 740.94)
14	(4.58, 18.82)	(180.31, 740.94)
15	(5.85, 18.82)	(230.31, 740.94)
16	(7.12, 18.82)	(280.31, 740.94)
17	(8.39, 18.82)	(330.31, 740.94)
18	(9.66, 18.82)	(380.31, 740.94)
19	(10.93, 18.82)	(430.31, 740.94)
20	(12.20, 18.82)	(480.31, 740.94)
21	(13.47, 18.82)	(530.31, 740.94)
22	(14.14, 16.31)	(556.69, 642.12)
23	(14.14, 15.04)	(556.69, 592.12)
24	(14.14, 13.77)	(556.69, 542.12)
25	(14.14, 12.50)	(556.69, 492.12)
26	(14.14, 11.23)	(556.69, 442.12)
27	(14.14, 9.96)	(556.69, 392.12)
28	(14.14, 8.69)	(556.69, 342.12)
29	(14.14, 7.42)	(556.69, 292.12)
30	(14.14, 6.15)	(556.69, 242.12)
31	(14.14, 4.88)	(556.69, 192.12)

**Figure 6. Solder Pad Reference Location**



**Top View (Seen on Host PCB)**



## Digital and Analog Capabilities and Connections

Table 4 details the solder pad connection definitions and available functions for each connection pad. Table 4 lists the solder pads on CYBLE-01201X-X0, the BLE device port-pin, and denotes whether the function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

**Table 4. Solder Pad Connection Definitions**

Solder Pad Number	Device Port Pin	UART	SPI	I <sup>2</sup> C	TCPWM <sup>[2,3]</sup>	CapSense	WCO Out	ECO Out	LCD	SWD	GPIO
1	XRES	External Reset Hardware Connection Input									
2	P4.0 <sup>[4]</sup>	✓(SCB1_RTS)	✓(SCB1_MOSI)		✓(TCPWM0_P)	✓(C <sub>MOD</sub> )			✓		✓
3	P3.7	✓(SCB1_CTS)			✓(TCPWM)	✓(Sensor)	✓		✓		✓
4	P3.6	✓(SCB1_RTS)			✓(TCPWM)	✓(Sensor)			✓		✓
5	P3.5	✓(SCB1_TX)		✓(SCB1_SCL)	✓(TCPWM)	✓(Sensor)			✓		✓
6	P3.4	✓(SCB1_RX)		✓(SCB1_SDA)	✓(TCPWM)	✓(Sensor)			✓		✓
7	P3.3	✓(SCB0_CTS)			✓(TCPWM)	✓(Sensor)			✓		✓
8	P3.2	✓(SCB0_RTS)			✓(TCPWM)	✓(Sensor)			✓		✓
9	P2.6				✓(TCPWM)	✓(Sensor)			✓		✓
10	VREF	Reference Voltage Input (Optional)									
11	P2.4				✓(TCPWM)	✓(Sensor)			✓		✓
12	P2.3				✓(TCPWM)	✓(Sensor)	✓		✓		✓
13	P2.2		✓(SCB0_SS3)		✓(TCPWM)	✓(Sensor)			✓		✓
14	P2.0		✓(SCB0_SS1)		✓(TCPWM)	✓(Sensor)			✓		✓
15	V <sub>DD</sub>	Digital Power Supply Input (1.8 to 5.5V)									
16	P1.7	✓(SCB0_CTS)	✓(SCB0_SCLK)		✓(TCPWM)	✓(Sensor)			✓		✓
17	P1.6	✓(SCB0_RTS)	✓(SCB0_SS0)		✓(TCPWM)	✓(Sensor)			✓		✓
18	P1.5	✓(SCB0_TX)	✓(SCB0_MISO)	✓(SCB0_SCL)	✓(TCPWM)	✓(Sensor)			✓		✓
19	P1.4	✓(SCB0_RX)	✓(SCB0_MOSI)	✓(SCB0_SDA)	✓(TCPWM)	✓(Sensor)			✓		✓
20	P1.0				✓(TCPWM)	✓(Sensor)			✓		✓
21	P0.4	✓(SCB0_RX)	✓(SCB0_MOSI)	✓(SCB0_SDA)	✓(TCPWM)	✓(Sensor)		✓	✓		✓
22	P0.5	✓(SCB0_TX)	✓(SCB0_MISO)	✓(SCB0_SCL)	✓(TCPWM)	✓(Sensor)			✓		✓
23	P0.7	✓(SCB0_CTS)	✓(SCB0_SCLK)		✓(TCPWM)	✓(Sensor)			✓	✓(SWDCLK)	✓
24	P0.6	✓(SCB0_RTS)	✓(SCB0_SS0)		✓(TCPWM)	✓(Sensor)			✓	✓(SWDIO)	✓
25	GND <sup>[5]</sup>	Ground Connection									
26	GND <sup>[5]</sup>	Ground Connection									
27	GND <sup>[5]</sup>	Ground Connection									
28	GND <sup>[5]</sup>	Ground Connection									
29	V <sub>DDR</sub>	Radio Power Supply (1.9V to 5.5V)									
30	P5.0	✓(SCB1_RX)	✓(SCB1_SS0)	✓(SCB1_SDA)	✓(TCPWM3_P)	✓(Sensor)			✓		✓
31	P5.1	✓(SCB1_TX)	✓(SCB1_SCLK)	✓(SCB1_SCL)	✓(TCPWM3_N)	✓(Sensor)		✓	✓		✓

### Notes

2. TCPWM: Timer, Counter, and Pulse Width Modulator. If supported, the pad can be configured to any of these peripheral functions.
3. TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.
4. When using the capacitive sensing functionality, Pad 2 (P4.0) must be connected to a C<sub>MOD</sub> capacitor (located off of Cypress BLE Module). The value of this capacitor is 2.2 nF and should be placed as close to the module as possible.
5. The main board needs to connect all GND connections (Pad 25/26/27/28) on the module to the common ground of the system.
6. If the I<sup>2</sup>S feature is used in the design, the I<sup>2</sup>S pins shall be dynamically routed to the appropriate available GPIO by PSoC Creator

## Power Supply Connections and Recommended External Components

### Power Connections

The CYBLE-01201X-X0 contains two power supply connections, VDD and VDDR. The VDD connection supplies power for both digital and analog device operation. The VDDR connection supplies power for the device radio.

VDD accepts a supply range of 1.71 V to 5.5 V. VDDR accepts a supply range of 1.9 V to 5.5 V. These specifications can be found in Table 9. The maximum power supply ripple for both power connections on the module is 100 mV, as shown in Table 7.

The power supply ramp rate of VDD must be equal to or greater than that of VDDR.

### Connection Options

Two connection options are available for any application:

1. Single supply: Connect VDD and VDDR to the same supply.
2. Independent supply: Power VDD and VDDR separately.

### External Component Recommendation

In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

Figure 7 details the recommended host schematic options for a single supply scenario. The use of one or two ferrite beads will depend on the specific application and configuration of the CYBLE-01201X-X0.

Figure 8 details the recommended host schematic for an independent supply scenario.

The recommended ferrite bead value is 330 Ω, 100 MHz. (Murata BLM21PG331SN1D).

**Figure 7. Recommended Host Schematic Options for a Single Supply Option**

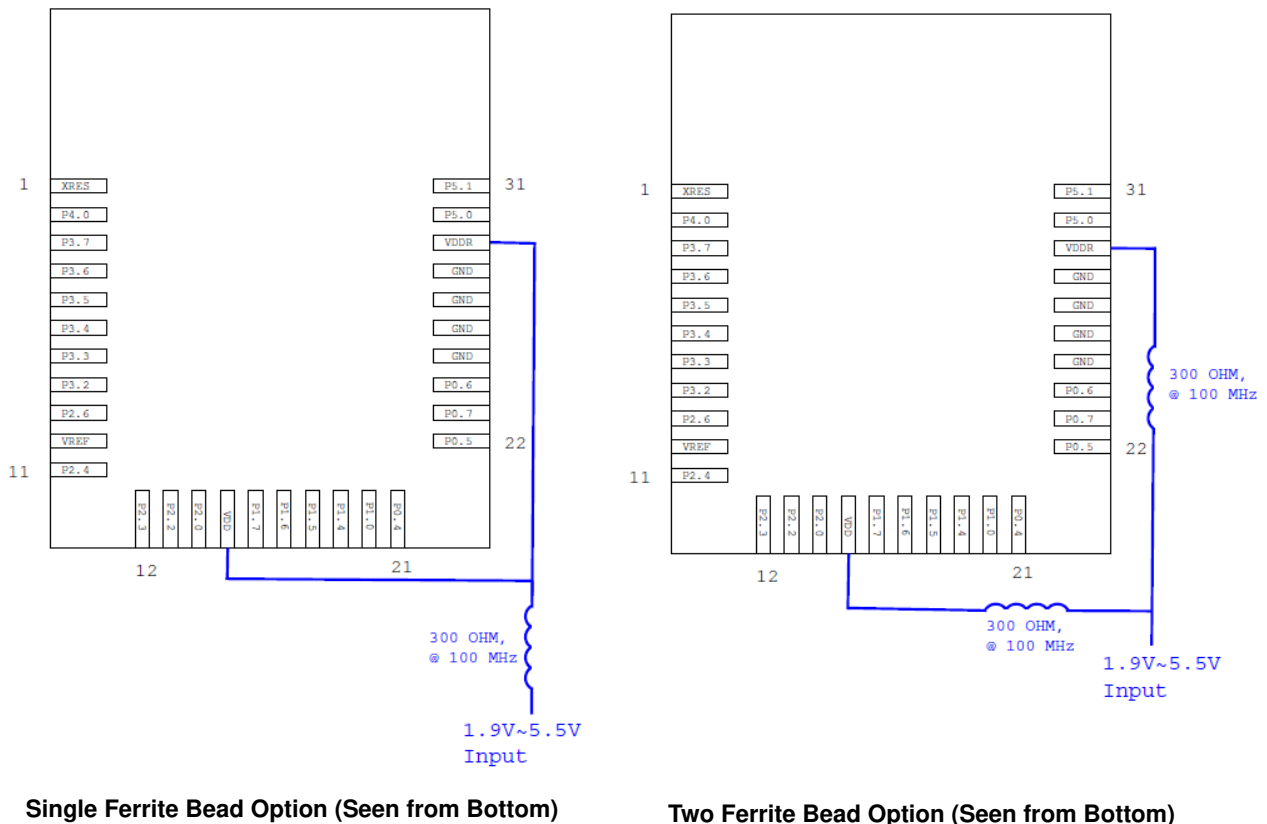
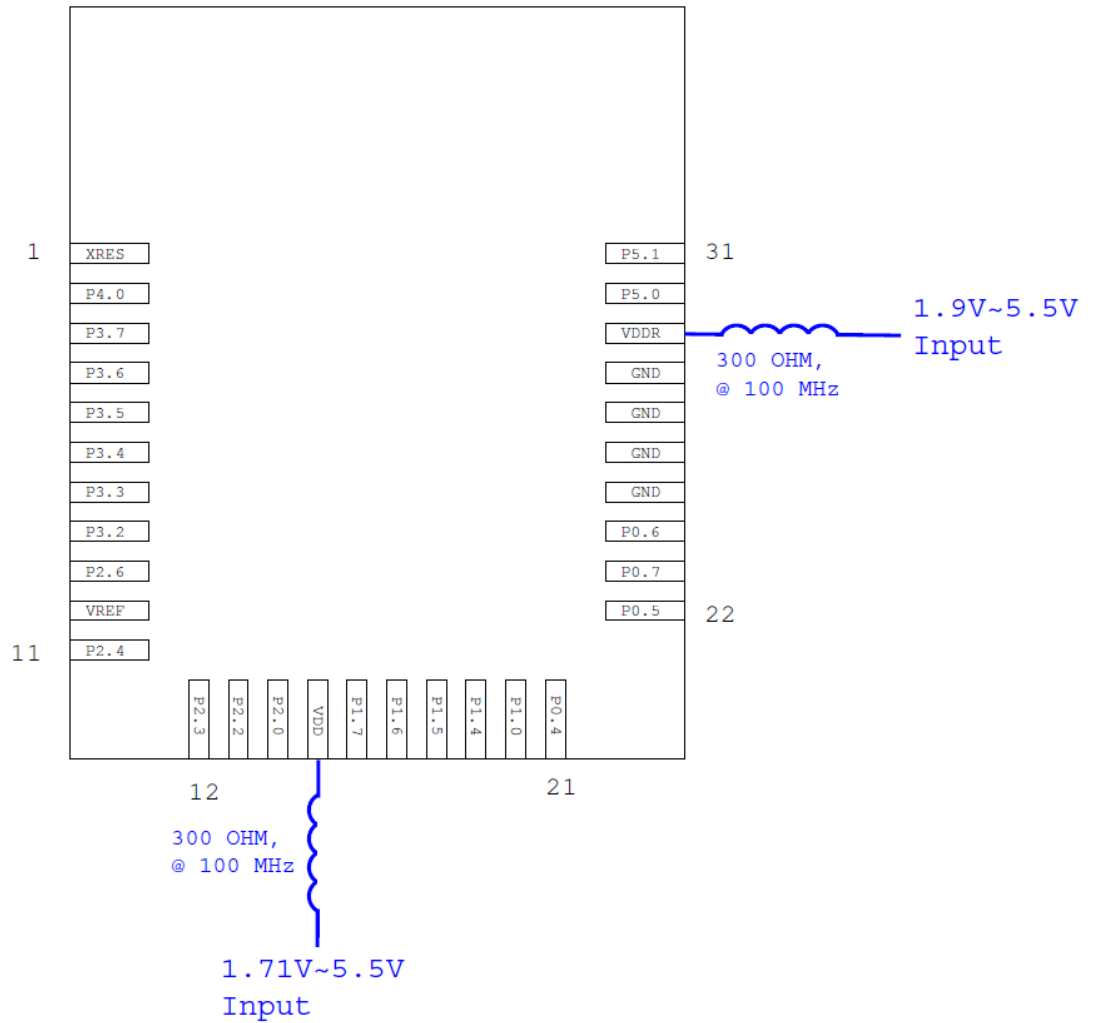


Figure 8. Recommended Host Schematic for an Independent Supply Option



Independent Power Supply Option (Seen from Bottom)





## Critical Components List

Table 5 details the critical components used in the CYBLE-01201X-X0 module.

**Table 5. Critical Component List**

Component	Reference Designator	Description
Silicon	U1	56-pin QFN Programmable Radio-on-Chip (PProC) with BLE
Crystal	Y1	24.000 MHz, 12PF
Crystal	Y2	32.768 kHz, 12.5PF

## Antenna Design

Table 6 details trace antenna used in the CYBLE-01201X-X0 module. For more information, see Table 8.

**Table 6. Trace Antenna Specifications**

Item	Description
Frequency Range	2400–2500 MHz
Peak Gain	0.5-dBi typical
Average Gain	–0.5-dBi typical
Return Loss	10-dB minimum

## Electrical Specification

Table 7 details the absolute maximum electrical characteristics for the Cypress BLE module.

**Table 7. CYBLE-01201X-X0 Absolute Maximum Ratings**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>DDD_ABS</sub>	Analog, digital, or radio supply relative to V <sub>SS</sub> (V <sub>SSD</sub> = V <sub>SSA</sub> )	-0.5	-	6	V	Absolute maximum
V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to V <sub>SSD</sub>	-0.5	-	1.95	V	Absolute maximum
V <sub>DD_RIPPLE</sub>	Maximum power supply ripple for V <sub>DD</sub> and V <sub>DDR</sub> input voltage	-	-	100	mV	3.0V supply Ripple frequency of 100 kHz to 750 kHz
V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5	-	V <sub>DD</sub> + 0.5	V	Absolute maximum
I <sub>GPIO_ABS</sub>	Maximum current per GPIO	-25	-	25	mA	Absolute maximum
I <sub>GPIO_injection</sub>	GPIO injection current: Maximum for V <sub>IH</sub> > V <sub>DD</sub> and minimum for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	-	0.5	mA	Absolute maximum current injected per pin
LU	Pin current for latch up	-200	-	200	mA	-

Table 8 details the RF characteristics for the Cypress BLE module.

**Table 8. CYBLE-01201X-X0 RF Performance Characteristics**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
RF <sub>O</sub>	RF output power on ANT	-18	0	3	dBm	Configurable via register settings
RX <sub>S</sub>	RF receive sensitivity on ANT	-	-87	-	dBm	Guaranteed by design simulation
F <sub>R</sub>	Module frequency range	2400	-	2480	MHz	-
G <sub>P</sub>	Peak gain	-	0.5	-	dBi	-
G <sub>Avg</sub>	Average gain	-	-0.5	-	dBi	-
RL	Return loss	-	-10.5	-	dB	-

Table 9 through Table 48 list the module level electrical characteristics for the CYBLE-01201X-X0. All specifications are valid for -40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 9. CYBLE-01201X-X0 DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>DD1</sub>	Power supply input voltage	1.8	-	5.5	V	With regulator enabled
V <sub>DD2</sub>	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
V <sub>DDR1</sub>	Radio supply voltage (radio on)	1.9	-	5.5	V	-
V <sub>DDR2</sub>	Radio supply voltage (radio off)	1.71	-	5.5	V	-
<b>Active Mode, V<sub>DD</sub> = 1.71 V to 5.5 V</b>						
I <sub>DD3</sub>	Execute from flash; CPU at 3 MHz	-	1.7	-	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD4</sub>	Execute from flash; CPU at 3 MHz	-	-	-	mA	T = -40 °C to 85 °C
I <sub>DD5</sub>	Execute from flash; CPU at 6 MHz	-	2.5	-	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD6</sub>	Execute from flash; CPU at 6 MHz	-	-	-	mA	T = -40 °C to 85 °C
I <sub>DD7</sub>	Execute from flash; CPU at 12 MHz	-	4	-	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V

**Table 9. CYBLE-01201X-X0 DC Specifications (continued)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>DD8</sub>	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 85 °C
I <sub>DD9</sub>	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD10</sub>	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
I <sub>DD11</sub>	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD12</sub>	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
<b>Sleep Mode, V<sub>DD</sub> = 1.8 V to 5.5 V</b>						
I <sub>DD13</sub>	IMO on	–	–	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V, SYSCLK = 3 MHz
<b>Sleep Mode, V<sub>DD</sub> and V<sub>DDR</sub> = 1.9 V to 5.5 V</b>						
I <sub>DD14</sub>	ECO on	–	–	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V, SYSCLK = 3 MHz
<b>Deep-Sleep Mode, V<sub>DD</sub> = 1.8 V to 3.6 V</b>						
I <sub>DD15</sub>	WDT with WCO on	–	1.5	–	μA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD16</sub>	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
I <sub>DD17</sub>	WDT with WCO on	–	–	–	μA	T = 25 °C, V <sub>DD</sub> = 5 V
I <sub>DD18</sub>	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
<b>Deep-Sleep Mode, V<sub>DD</sub> = 1.71 V to 1.89 V (Regulator Bypassed)</b>						
I <sub>DD19</sub>	WDT with WCO on	–	–	–	μA	T = 25 °C
I <sub>DD20</sub>	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
<b>Hibernate Mode, V<sub>DD</sub> = 1.8 V to 3.6 V</b>						
I <sub>DD27</sub>	GPIO and reset active	–	150	–	nA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD28</sub>	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
<b>Hibernate Mode, V<sub>DD</sub> = 3.6 V to 5.5 V</b>						
I <sub>DD29</sub>	GPIO and reset active	–	–	–	nA	T = 25 °C, V <sub>DD</sub> = 5 V
I <sub>DD30</sub>	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
<b>Stop Mode, V<sub>DD</sub> = 1.8 V to 3.6 V</b>						
I <sub>DD33</sub>	Stop-mode current (V <sub>DD</sub> )	–	20	–	nA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD34</sub>	Stop-mode current (V <sub>DDR</sub> )	–	40	–	nA	T = 25 °C, V <sub>DDR</sub> = 3.3 V
I <sub>DD35</sub>	Stop-mode current (V <sub>DD</sub> )	–	–	–	nA	T = –40 °C to 85 °C
I <sub>DD36</sub>	Stop-mode current (V <sub>DDR</sub> )	–	–	–	nA	T = –40 °C to 85 °C, V <sub>DDR</sub> = 1.9 V to 3.6 V
<b>Stop Mode, V<sub>DD</sub> = 3.6 V to 5.5 V</b>						
I <sub>DD37</sub>	Stop-mode current (V <sub>DD</sub> )	–	–	–	nA	T = 25 °C, V <sub>DD</sub> = 5 V
I <sub>DD38</sub>	Stop-mode current (V <sub>DDR</sub> )	–	–	–	nA	T = 25 °C, V <sub>DDR</sub> = 5 V
I <sub>DD39</sub>	Stop-mode current (V <sub>DD</sub> )	–	–	–	nA	T = –40 °C to 85 °C
I <sub>DD40</sub>	Stop-mode current (V <sub>DDR</sub> )	–	–	–	nA	T = –40 °C to 85 °C

**Table 10. AC Specifications**



Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>CPU</sub>	CPU frequency	DC	–	48	MHz	1.71 V ≤ V <sub>DD</sub> ≤ 5.5 V
T <sub>SLEEP</sub>	Wakeup from Sleep mode	–	0	–	μs	Guaranteed by characterization
T <sub>DEEPSLEEP</sub>	Wakeup from Deep-Sleep mode	–	–	25	μs	24-MHz IMO. Guaranteed by characterization
T <sub>HIBERNATE</sub>	Wakeup from Hibernate mode	–	–	2	ms	Guaranteed by characterization
T <sub>STOP</sub>	Wakeup from Stop mode	–	–	2	ms	XRES wakeup

## GPIO

**Table 11. GPIO DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>IH</sub> <sup>[7]</sup>	Input voltage HIGH threshold	0.7 × V <sub>DD</sub>	–	–	V	CMOS input
	LVTTL input, V <sub>DD</sub> < 2.7 V	0.7 × V <sub>DD</sub>	–	–	V	–
	LVTTL input, V <sub>DD</sub> ≥ 2.7 V	2.0	–	–	V	–
V <sub>IL</sub>	Input voltage LOW threshold	–	–	0.3 × V <sub>DD</sub>	V	CMOS input
	LVTTL input, V <sub>DD</sub> < 2.7 V	–	–	0.3 × V <sub>DD</sub>	V	–
	LVTTL input, V <sub>DD</sub> ≥ 2.7 V	–	–	0.8	V	–
V <sub>OH</sub>	Output voltage HIGH level	V <sub>DD</sub> – 0.6	–	–	V	I <sub>OH</sub> = 4 mA at 3.3-V V <sub>DD</sub>
	Output voltage HIGH level	V <sub>DD</sub> – 0.5	–	–	V	I <sub>OH</sub> = 1 mA at 1.8-V V <sub>DD</sub>
V <sub>OL</sub>	Output voltage LOW level	–	–	0.6	V	I <sub>OL</sub> = 8 mA at 3.3-V V <sub>DD</sub>
	Output voltage LOW level	–	–	0.6	V	I <sub>OL</sub> = 4 mA at 1.8-V V <sub>DD</sub>
	Output voltage LOW level	–	–	0.4	V	I <sub>OL</sub> = 3 mA at 3.3-V V <sub>DD</sub>
R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	–
R <sub>PULLDOWN</sub>	Pull-down resistor	3.5	5.6	8.5	kΩ	–
I <sub>IL</sub>	Input leakage current (absolute value)	–	–	2	nA	25 °C, V <sub>DD</sub> = 3.3 V
I <sub>IL_CTBM</sub>	Input leakage on CTBm input pins	–	–	4	nA	–
C <sub>IN</sub>	Input capacitance	–	–	7	pF	–
V <sub>HYSTTL</sub>	Input hysteresis LVTTL	25	40	–	mV	V <sub>DD</sub> > 2.7 V
V <sub>HYSCMOS</sub>	Input hysteresis CMOS	0.05 × V <sub>DD</sub>	–	–	1	–
I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	–	–	100	μA	–
I <sub>TOT_GPIO</sub>	Maximum total source or sink chip current	–	–	200	mA	–

**Note**

7. V<sub>IH</sub> must not exceed V<sub>DD</sub> + 0.2 V.

**Table 12. GPIO AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>RISEF</sub>	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V <sub>DD</sub> , C <sub>LOAD</sub> = 25 pF
T <sub>FALLF</sub>	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V <sub>DD</sub> , C <sub>LOAD</sub> = 25 pF
T <sub>RISES</sub>	Rise time in Slow-Strong mode	10	–	60	ns	3.3-V V <sub>DD</sub> , C <sub>LOAD</sub> = 25 pF
T <sub>FALLS</sub>	Fall time in Slow-Strong mode	10	–	60	ns	3.3-V V <sub>DD</sub> , C <sub>LOAD</sub> = 25 pF
F <sub>GPIOOUT1</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V Fast-Strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOOUT2</sub>	GPIO F <sub>OUT</sub> ; 1.7 V ≤ V <sub>DD</sub> ≤ 3.3 V Fast-Strong mode	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOOUT3</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V Slow-Strong mode	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOOUT4</sub>	GPIO F <sub>OUT</sub> ; 1.7 V ≤ V <sub>DD</sub> ≤ 3.3 V Slow-Strong mode	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOIN</sub>	GPIO input operating frequency 1.71 V ≤ V <sub>DD</sub> ≤ 5.5 V	–	–	48	MHz	90/10% V <sub>IO</sub>

**Table 13. OVT GPIO DC Specifications (P5\_0 and P5\_1 Only)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>IL</sub>	Input leakage (absolute value). V <sub>IH</sub> > V <sub>DD</sub>	–	–	10	μA	25°C, V <sub>DD</sub> = 0 V, V <sub>IH</sub> = 3.0 V
V <sub>OL</sub>	Output voltage LOW level	–	–	0.4	V	I <sub>OL</sub> = 20 mA, V <sub>DD</sub> > 2.9 V

**Table 14. OVT GPIO AC Specifications (P5\_0 and P5\_1 Only)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>RISE_OVFS</sub>	Output rise time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V <sub>DD</sub> =3.3 V
T <sub>FALL_OVFS</sub>	Output fall time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V <sub>DD</sub> =3.3 V
T <sub>RISESS</sub>	Output rise time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V <sub>DD</sub> = 3.3 V
T <sub>FALLSS</sub>	Output fall time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V <sub>DD</sub> = 3.3 V
F <sub>GPIOOUT1</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOOUT2</sub>	GPIO F <sub>OUT</sub> ; 1.71 V ≤ V <sub>DD</sub> ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle

## XRES

**Table 15. XRES DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>IH</sub>	Input voltage HIGH threshold	0.7 × V <sub>DD</sub>	–	–	V	CMOS input
V <sub>IL</sub>	Input voltage LOW threshold	–	–	0.3 × V <sub>DD</sub>	V	CMOS input
R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	–
C <sub>IN</sub>	Input capacitance	–	3	–	pF	–
V <sub>HYSXRES</sub>	Input voltage hysteresis	–	100	–	mV	–
I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	–	–	100	μA	–

**Table 16. XRES AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>RESETWIDTH</sub>	Reset pulse width	1	–	–	μs	–

*Temperature Sensor*

**Table 17. Temperature Sensor Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>SENSACC</sub>	Temperature-sensor accuracy	–5	±1	5	°C	–40 to +85 °C

*SAR ADC*

**Table 18. SAR ADC DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_RES	Resolution	–	–	12	bits	
A_CHNIS_S	Number of channels - single-ended	–	–	8		8 full-speed <sup>[8]</sup>
A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O <sup>[8]</sup>
A-MONO	Monotonicity	–	–	–		Yes
A_GAINERR	Gain error	–	–	±0.1	%	With external reference
A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V <sub>REF</sub>
A_ISAR	Current consumption	–	–	1	mA	
A_VINS	Input voltage range - single-ended	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	
A_VIND	Input voltage range - differential	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	
A_INRES	Input resistance	–	–	2.2	kΩ	
A_INCAP	Input capacitance	–	–	10	pF	
VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of V <sub>bg</sub> (1.024 V)

**Table 19. SAR ADC AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_PSRR	Power-supply rejection ratio	70	–	–	dB	Measured at 1-V reference
A_CMRR	Common-mode rejection ratio	66	–	–	dB	
A_SAMP	Sample rate	–	–	1	Msps	
Fsarintref	SAR operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution
A_SNR	Signal-to-noise ratio (SNR)	65	–	–	dB	F <sub>IN</sub> = 10 kHz
A_BW	Input bandwidth without aliasing	–	–	A_SAMP/2	kHz	
A_INL	Integral nonlinearity. V <sub>DD</sub> = 1.71 V to 5.5 V, 1 Msps	–1.7	–	2	LSB	V <sub>REF</sub> = 1 V to V <sub>DD</sub>
A_INL	Integral nonlinearity. V <sub>DDD</sub> = 1.71 V to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	V <sub>REF</sub> = 1.71 V to V <sub>DD</sub>

**Note**

8. A maximum of eight single-ended ADC Channels can be accomplished only if the AMUX Buses are not being used for other functionality (e.g. CapSense). If the AMUX Buses are being used for other functions, then the maximum number of single-ended ADC channels is six. Similarly, if the AMUX Buses are being used for other functionality, then the maximum number of differential ADC channels is three.

**Table 19. SAR ADC AC Specifications** (continued)

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
A_INL	Integral nonlinearity. $V_{DD} = 1.71\text{ V}$ to $5.5\text{ V}$ , 500 ksp/s	-1.5	-	1.7	LSB	$V_{REF} = 1\text{ V}$ to $V_{DD}$
A_dnl	Differential nonlinearity. $V_{DD} = 1.71\text{ V}$ to $5.5\text{ V}$ , 1 Msps	-1	-	2.2	LSB	$V_{REF} = 1\text{ V}$ to $V_{DD}$
A_DNL	Differential nonlinearity. $V_{DD} = 1.71\text{ V}$ to $3.6\text{ V}$ , 1 Msps	-1	-	2	LSB	$V_{REF} = 1.71\text{ V}$ to $V_{DD}$
A_DNL	Differential nonlinearity. $V_{DD} = 1.71\text{ V}$ to $5.5\text{ V}$ , 500 ksp/s	-1	-	2.2	LSB	$V_{REF} = 1\text{ V}$ to $V_{DD}$
A_THD	Total harmonic distortion	-	-	-65	dB	$F_{IN} = 10\text{ kHz}$

CSD

**CSD Block Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
$V_{CSD}$	Voltage range of operation	1.71	-	5.5	V	
IDAC1	DNL for 8-bit resolution	-1	-	1	LSB	
IDAC1	INL for 8-bit resolution	-3	-	3	LSB	
IDAC2	DNL for 7-bit resolution	-1	-	1	LSB	
IDAC2	INL for 7-bit resolution	-3	-	3	LSB	
SNR	Ratio of counts of finger to noise	5	-	-	Ratio	Capacitance range of 9 pF to 35 pF, 0.1-pF sensitivity. Radio is not operating during the scan
$I_{DAC1\_CRT1}$	Output current of IDAC1 (8 bits) in High range	-	612	-	$\mu\text{A}$	
$I_{DAC1\_CRT2}$	Output current of IDAC1 (8 bits) in Low range	-	306	-	$\mu\text{A}$	
$I_{DAC2\_CRT1}$	Output current of IDAC2 (7 bits) in High range	-	305	-	$\mu\text{A}$	
$I_{DAC2\_CRT2}$	Output current of IDAC2 (7 bits) in Low range	-	153	-	$\mu\text{A}$	



## Digital Peripherals

### Timer

**Table 20. Timer DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$I_{TIM1}$	Block current consumption at 3 MHz	–	–	42	$\mu\text{A}$	16-bit timer
$I_{TIM2}$	Block current consumption at 12 MHz	–	–	130	$\mu\text{A}$	16-bit timer
$I_{TIM3}$	Block current consumption at 48 MHz	–	–	535	$\mu\text{A}$	16-bit timer

**Table 21. Timer AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{TIMFREQ}$	Operating frequency	$F_{CLK}$	–	48	MHz	
$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{TIMRES}$	Timer resolution	$T_{CLK}$	–	–	ns	
$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{TENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{TIMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{TIMRESEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

### Counter

**Table 22. Counter DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$I_{CTR1}$	Block current consumption at 3 MHz	–	–	42	$\mu\text{A}$	16-bit counter
$I_{CTR2}$	Block current consumption at 12 MHz	–	–	130	$\mu\text{A}$	16-bit counter
$I_{CTR3}$	Block current consumption at 48 MHz	–	–	535	$\mu\text{A}$	16-bit counter

**Table 23. Counter AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{CTRFREQ}$	Operating frequency	$F_{CLK}$	–	48	MHz	
$T_{CTRPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRES}$	Counter Resolution	$T_{CLK}$	–	–	ns	
$T_{CENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

Pulse Width Modulation (PWM)

**Table 24. PWM DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>PWM1</sub>	Block current consumption at 3 MHz	–	–	42	μA	16-bit PWM
I <sub>PWM2</sub>	Block current consumption at 12 MHz	–	–	130	μA	16-bit PWM
I <sub>PWM3</sub>	Block current consumption at 48 MHz	–	–	535	μA	16-bit PWM

**Table 25. PWM AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>PWMFREQ</sub>	Operating frequency	F <sub>CLK</sub>	–	48	MHz	
T <sub>PWMPWINT</sub>	Pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>PWMEXT</sub>	Pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>PWMKILLINT</sub>	Kill pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>PWMKILLEXT</sub>	Kill pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>PWMEINT</sub>	Enable pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>PWMENEXT</sub>	Enable pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>PWMRESWINT</sub>	Reset pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>PWMRESWEXT</sub>	Reset pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	

LCD Direct Drive

**Table 26. LCD Direct Drive DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>LCDLOW</sub>	Operating current in low-power mode	–	17.5	–	μA	16 × 4 small segment display at 50 Hz
C <sub>LCDCAP</sub>	LCD capacitance per segment/common driver	–	500	5000	pF	
LCD <sub>OFFSET</sub>	Long-term segment offset	–	20	–	mV	
I <sub>LCDOP1</sub>	LCD system operating current V <sub>BIAS</sub> = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz at 25 °C
I <sub>LCDOP2</sub>	LCD system operating current V <sub>BIAS</sub> = 3.3 V	–	2	–	mA	32 × 4 segments 50 Hz at 25 °C

**Table 27. LCD Direct Drive AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>LCD</sub>	LCD frame rate	10	50	150	Hz	

## Serial Communication

**Table 28. Fixed I<sup>2</sup>C DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>I2C1</sub>	Block current consumption at 100 kHz	–	–	50	μA	–
I <sub>I2C2</sub>	Block current consumption at 400 kHz	–	–	155	μA	–
I <sub>I2C3</sub>	Block current consumption at 1 Mbps	–	–	390	μA	–
I <sub>I2C4</sub>	I <sup>2</sup> C enabled in Deep-Sleep mode	–	–	1.4	μA	–

**Table 29. Fixed I<sup>2</sup>C AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>I2C1</sub>	Bit rate	–	–	400	kHz	–

**Table 30. Fixed UART DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>UART1</sub>	Block current consumption at 100 kbps	–	–	55	μA	–
I <sub>UART2</sub>	Block current consumption at 1000 kbps	–	–	312	μA	–

**Table 31. Fixed UART AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>UART</sub>	Bit rate	–	–	1	Mbps	–

**Table 32. Fixed SPI DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>SPI1</sub>	Block current consumption at 1 Mbps	–	–	360	μA	–
I <sub>SPI2</sub>	Block current consumption at 4 Mbps	–	–	560	μA	–
I <sub>SPI3</sub>	Block current consumption at 8 Mbps	–	–	600	μA	–

**Table 33. Fixed SPI AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>SPI</sub>	SPI operating frequency (master; 6x over sampling)	–	–	8	MHz	–

**Table 34. Fixed SPI Master Mode AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>DMO</sub>	MOSI valid after SCLK driving edge	–	–	18	ns	–
T <sub>DSI</sub>	MISO valid before SCLK capturing edge Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
T <sub>HMO</sub>	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

**Table 35. Fixed SPI Slave Mode AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>DMI</sub>	MOSI valid before SCLK capturing edge	40	–	–	ns	–
T <sub>DSO</sub>	MISO valid after SCLK driving edge	–	–	42 + 3 × T <sub>CPU</sub>	ns	–
T <sub>DSO_ext</sub>	MISO Valid after SCLK driving edge in external clock mode. V <sub>DD</sub> < 3.0 V	–	–	50	ns	–

**Table 35. Fixed SPI Slave Mode AC Specifications** (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>HSD</sub>	Previous MISO data hold time	0	–	–	ns	
T <sub>SSELSCK</sub>	SSEL valid to first SCK valid edge	100	–	–	ns	

## Memory

**Table 36. Flash DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>PE</sub>	Erase and program voltage	1.71	–	5.5	V	–
T <sub>WS48</sub>	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
T <sub>WS32</sub>	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
T <sub>WS16</sub>	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

**Table 37. Flash AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>ROWWRITE</sub> <sup>[9]</sup>	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
T <sub>ROWERASE</sub> <sup>[9]</sup>	Row erase time	–	–	13	ms	–
T <sub>ROWPROGRAM</sub> <sup>[9]</sup>	Row program time after erase	–	–	7	ms	–
T <sub>BULKERASE</sub> <sup>[9]</sup>	Bulk erase time (128 KB)	–	–	35	ms	–
T <sub>DEVPROG</sub> <sup>[9]</sup>	Total device program time	–	–	25	seconds	–
F <sub>END</sub>	Flash endurance	100 K	–	–	cycles	–
F <sub>RET</sub>	Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles	20	–	–	years	–
F <sub>RET2</sub>	Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles	10	–	–	years	–

**Note**

9. It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.



## System Resources

### Power-on-Reset (POR)

**Table 38. POR DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>RISEIPOR</sub>	Rising trip voltage	0.80	–	1.45	V	–
V <sub>FALLIPOR</sub>	Falling trip voltage	0.75	–	1.40	V	–
V <sub>IPORHYST</sub>	Hysteresis	15	–	200	mV	–

**Table 39. POR AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>PPOR_TR</sub>	Precision power-on reset (PPOR) response time in Active and Sleep modes	–	–	1	µs	–

**Table 40. Brown-Out Detect**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>FALLPPOR</sub>	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	–
V <sub>FALLDPSLP</sub>	BOD trip voltage in Deep Sleep	1.4	–	–	V	–

**Table 41. Hibernate Reset**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>HBRTRIP</sub>	BOD trip voltage in Hibernate	1.1	–	–	V	–

### Voltage Monitors (LVD)

**Table 42. Voltage Monitor DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>LVI1</sub>	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
V <sub>LVI2</sub>	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
V <sub>LVI3</sub>	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
V <sub>LVI4</sub>	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
V <sub>LVI5</sub>	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
V <sub>LVI6</sub>	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
V <sub>LVI7</sub>	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
V <sub>LVI8</sub>	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
V <sub>LVI9</sub>	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
V <sub>LVI10</sub>	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
V <sub>LVI11</sub>	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
V <sub>LVI12</sub>	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
V <sub>LVI13</sub>	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
V <sub>LVI14</sub>	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
V <sub>LVI15</sub>	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
V <sub>LVI16</sub>	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
LVI_IDD	Block current	–	–	100	µA	–

**Table 43. Voltage Monitor AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>MONTRIP</sub>	Voltage monitor trip time	–	–	1	μs	–

*SWD Interface*

**Table 44. SWD Interface Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>SWDCLK1</sub>	3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
F <sub>SWDCLK2</sub>	1.71 V ≤ V <sub>DD</sub> ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
T <sub>SWDI_SETUP</sub>	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T <sub>SWDI_HOLD</sub>	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T <sub>SWDO_VALID</sub>	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
T <sub>SWDO_HOLD</sub>	T = 1/f SWDCLK	1	–	–	ns	–

*Internal Main Oscillator*

**Table 45. IMO DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>IMO1</sub>	IMO operating current at 48 MHz	–	–	1000	μA	–
I <sub>IMO2</sub>	IMO operating current at 24 MHz	–	–	325	μA	–
I <sub>IMO3</sub>	IMO operating current at 12 MHz	–	–	225	μA	–
I <sub>IMO4</sub>	IMO operating current at 6 MHz	–	–	180	μA	–
I <sub>IMO5</sub>	IMO operating current at 3 MHz	–	–	150	μA	–

**Table 46. IMO AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>IMOTOL3</sub>	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
F <sub>IMOTL3</sub>	IMO startup time	–	12	–	μs	–

*Internal Low-Speed Oscillator*

**Table 47. ILO DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>ILO2</sub>	ILO operating current at 32 kHz	–	0.3	1.05	μA	–

**Table 48. ILO AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>STARTILO1</sub>	ILO startup time	–	–	2	ms	–
F <sub>ILOTRIM1</sub>	32-kHz trimmed frequency	15	32	50	kHz	–

**Table 49. Recommended ECO Trim Value**

Parameter	Description	Value	Details/Conditions
ECO <sub>TRIM</sub>	24-MHz trim value (firmware configuration)	0x0000BCBC	Recommended trim value that needs to be loaded to register CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG