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CYBLE-013025-00
CYBLE-013030-00

EZ-BLE™ WICED Module

General Description

The CYBLE-0130XX-00 is a fully integrated Bluetooth® Low Energy (BLE) wireless module solution. The CYBLE-0130XX-00 includes an onboard crystal oscillator, passive components, flash memory, and the Cypress CYW20737 silicon device. Refer to the CYW20737 datasheet for additional details on the capabilities of the silicon device used in this module.

The CYBLE-0130XX-00 supports peripheral functions (ADC and PWM), as well as serial communication (UART, SPI, I^2C). The CYBLE-0130XX-00 includes a royalty-free BLE stack compatible with Bluetooth 4.1 in a 14.5 × 19.2 × 2.25 mm package.

The CYBLE-013025-00 includes 128 KB of onboard serial flash memory and is designed for standalone operation. The CYBLE-013030-00 does not contain onboard flash, requiring an external host to control the module via HCI commands or an external host to perform a RAM upload procedure, where the uploaded code will then execute from RAM. The CYBLE-013030-00 can also interface to external flash on the host board.

The CYBLE-0130XX-00 is fully qualified by Bluetooth SIG and is targeted at applications requiring cost-optimized BLE wireless connectivity. The CYBLE-013025-00 is footprint compatible[1] with the Cypress CYBLE-x120xx-00 module family.

Module Description

- Module size: 14.52 mm × 19.20 mm × 2.25 mm
- Bluetooth LE 4.1 listed single-mode module
  - QDID: 96386
  - Declaration ID: D035307
- Certified to FCC, ISED, MIC, and CE regulations
- Castelated solder pad connections for ease-of-use
- 128 KB on-module serial flash memory (CYBLE-013025-00)
- 60-KB SRAM memory
- Up to 14 GPIOs
- Temperature range: –30 °C to +85 °C
- Cortex-M3 32-bit processor
- Supports RSA encryption/decryption and key exchange mechanisms (up to 4 kbit)
- Maximum TX output power: +4.0 dbm
- RX Receive Sensitivity: –94 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution

Power Consumption

- One-second interval average: 120 uA
- Advertising Only Current (20-ms interval): 2.7 mA
- Cypress CYW20737 silicon low-power mode support
  - Sleep: 50-µA typical
  - Deep Sleep (HIDOFF): 1.5-µA typical

Functional Capabilities

- 10-bit auxiliary ADC with nine analog channels
- Serial communications interface (compatible with Philips® I2C slaves)
- Serial peripheral interface (SPI) support for both master and slave modes
- Four dedicated PWM blocks
- BLE protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
- Programmable output power from –20 dbm to +4 dBm (steps of ± 4 dBm)

Benefits

CYBLE-0130XX-00 provides all necessary components required to operate BLE communication standards.

- Proven hardware design ready to use
- Cost optimized for applications without space constraints
- Nonvolatile memory for self-sufficient operation (CYBLE-013025-00 only)
- Over-the-air update capable for in-field updates (CYBLE-013025-00 only)
- Bluetooth SIG qualified with QDID and Declaration ID
- Fully certified module eliminates the time needed for design, development, and certification processes
- WICED™ SMART provides an easy-to-use integrated design environment (IDE) to configure, develop, and program a BLE application
- Pre-programmed EZ-Serial firmware platform to allow for easy-to-use out of the box Bluetooth Low Energy connectivity

Note

1. CYBLE-0130XX-00 global connections (Power, Ground, XRES, etc) are pad compatible with the CYBLE-x120xx-00 family of modules. Available GPIO and functions may not be 100% compatible with your design. A review of the pad location and function within your design should be complete to determine if the CYBLE-013025-00 is completely pad-compatible to the CYBLE-x120xx-00 modules.

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

- Overview: EZ-BLE Module Portfolio, Module Roadmap
- EZ-BLE WICED Product Overview
- CYW20737 BLE Silicon Datasheet
- Development Kits:
  - CYBLE-013025-EVAL CYBLE-013025-00 Evaluation Board
- Test and Debug Tools:
  - CYSmart, Bluetooth LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth LE Test and Debug Tool (Android/iOS Mobile App)
- Knowledge Base Article
  - KBA97095 - EZ-BLE Module Placement
  - KBA219623 - RF Regulatory Certifications for CYBLE-013025-00 and CYBLE-013030-00 EZ-BLE™ WICED Modules
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
  - KBA218122 - 3D Model Fils for EZ-BLE/EZ-BT Modules
  - KBA220379 - Platform Files for CYBLE-013025-EVAL
  - KBA222505 - Downloading into the CYBLE-013025-00 module.

Two Easy-To-Use Design Environments to Get You Started Quickly

Wireless Connectivity for Embedded Devices Smart (WICED Smart) Software Development Kit (SDK)

Cypress's WICED® Smart Version 2.2.3 (Wireless Connectivity for Embedded Devices) is a full-featured platform with proven Software Development Kits (SDKs) and turnkey hardware solutions from partners to readily enable Wi-Fi and Bluetooth connectivity in system design.

The WICED Smart SDK includes the tools and software needed to create BLE peripheral and central devices for a wide range of products. The SDK is available as a standalone compressed file or as a separate installer bundled with the WICED Integrated Development Environment.

EZ-Serial™ Firmware Platform

The EZ-Serial Firmware Platform provides a simple way to access the most common hardware and communication features needed in BLE applications. EZ-Serial implements an intuitive API protocol over the UART interface and exposes various status and control signals through the module's GPIOs, making it easy to add BLE functionality quickly to existing designs.

Use a simple serial terminal and evaluation kit to begin development without requiring an IDE.

EZ-BLE modules are pre-flashed with the EZ-Serial Firmware Platform. If you do not have EZ-Serial pre-loaded on your module, you can download each EZ-BLE module's firmware images on the EZ-Serial webpage.

Technical Support

- Cypress Community: Whether you are a customer, partner, or a developer interested in the latest Cypress innovations, the Cypress Developer Community offers you a place to learn, share, and engage with both Cypress experts and other embedded engineers around the world.
- Frequently Asked Questions (FAQs): Learn more about our BLE ECO System.
- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

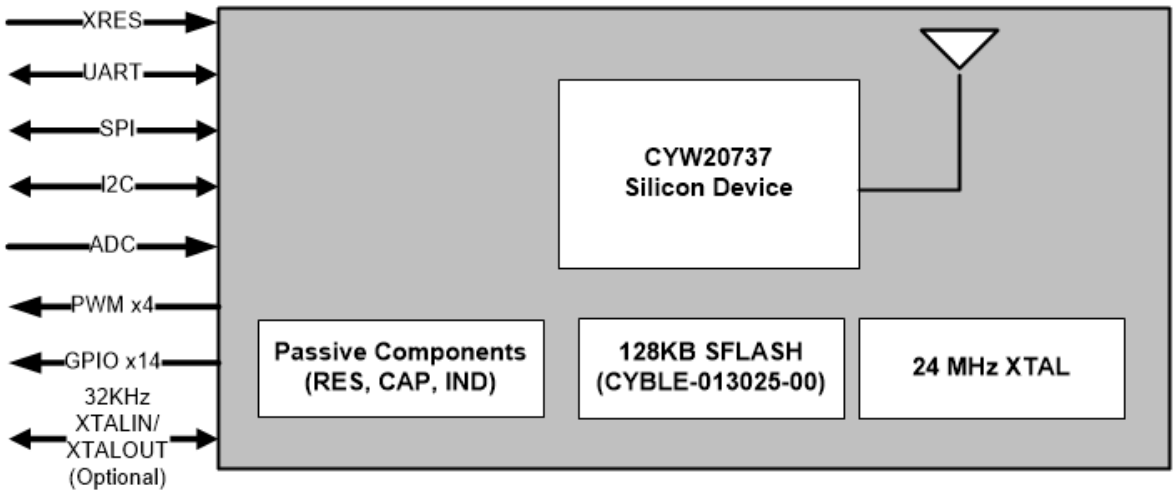
Contents

Overview

Functional Block Diagram

Figure 1 illustrates the CYBLE-0130XX-00 functional block diagram.

Figure 1. Functional Block Diagram



Module Description

The CYBLE-0130XX-00 module is a complete module designed to be soldered to the application's main board.

Module Dimensions and Drawing

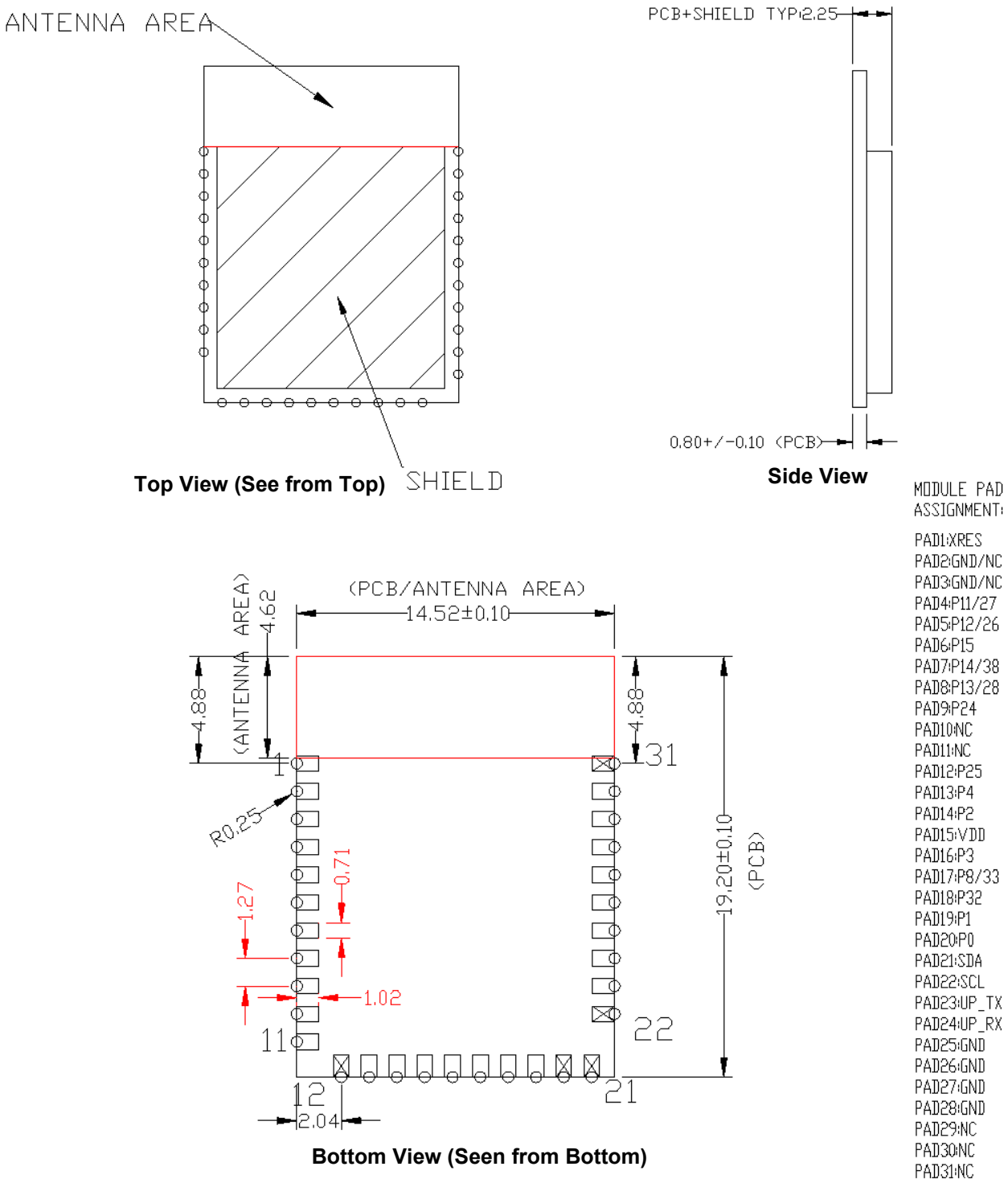
Cypress reserves the right to select components from various vendors to achieve the Bluetooth module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in Figure 2 on page 5. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	14.52 ± 0.10 mm
	Width (Y)	19.50 ± 0.10 mm
Antenna connection location dimensions	Length (X)	14.52 mm
	Width (Y)	4.80 mm
PCB thickness	Height (H)	0.80 ± 0.10 mm
Shield height	Height (H)	1.45 mm typical
Maximum component height	Height (H)	1.45 mm typical
Total module thickness (bottom of module to highest component)	Height (H)	2.25 mm typical

See Figure 2 for the CYBLE-0130XX-00 mechanical reference drawing.

Figure 2. Module Mechanical Drawing[2, 3]



Notes
2. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see "Recommended Host PCB Layout" on page 7.
3. The CYBLE-013025-00 includes castellated pad connections, denoted as the circular openings at the pad location above.

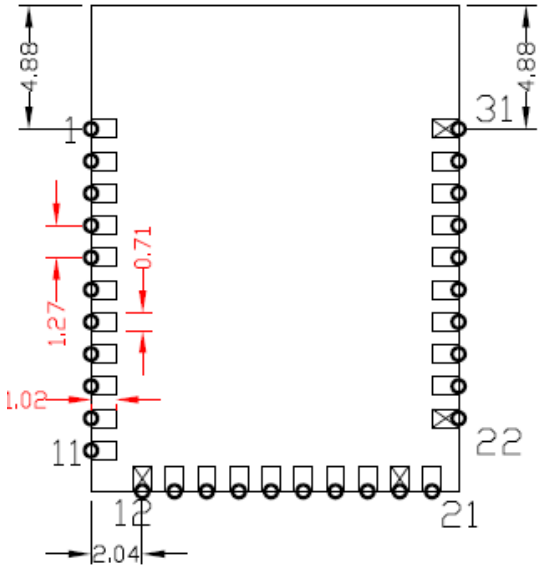
Pad Connection Interface

As shown in the bottom view of Figure 2 on page 5, the CYBLE-0130XX-00 connects to the host board via solder pads on the backside of the module. Table 2 and Figure 3 detail the solder pad length, width, and pitch dimensions of the CYBLE-0130XX-00 module.

Table 2. Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	31	Solder Pads	1.02 mm	0.71 mm	1.27 mm

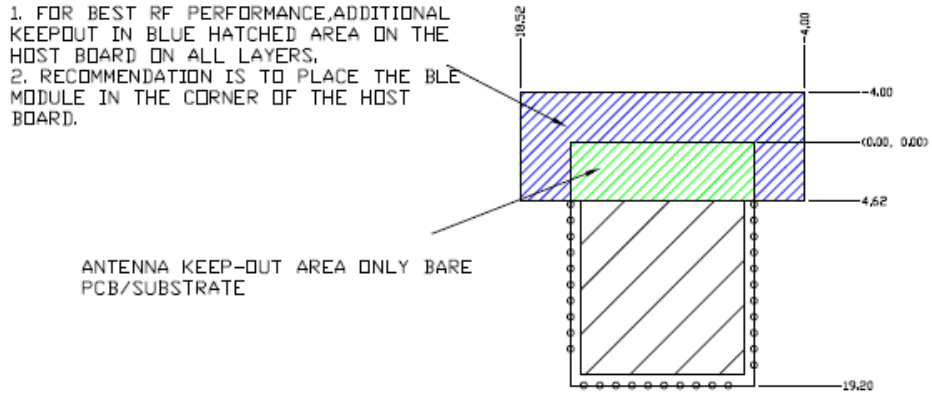
Figure 3. Solder Pad Dimensions (Seen from Bottom



To maximize RF performance, the host layout should follow these recommendations:

1. Antenna Area Keepout: The host board directly below the antenna area of the Cypress module (see Figure 2 on page 5) must contain no ground or signal traces. This keep out area requirement applies to all layers of the host board.
2. Module Placement: The ideal placement of the Cypress Bluetooth module is in a corner of the host board with the PCB trace antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2. Refer to AN96841 for module placement best practices.

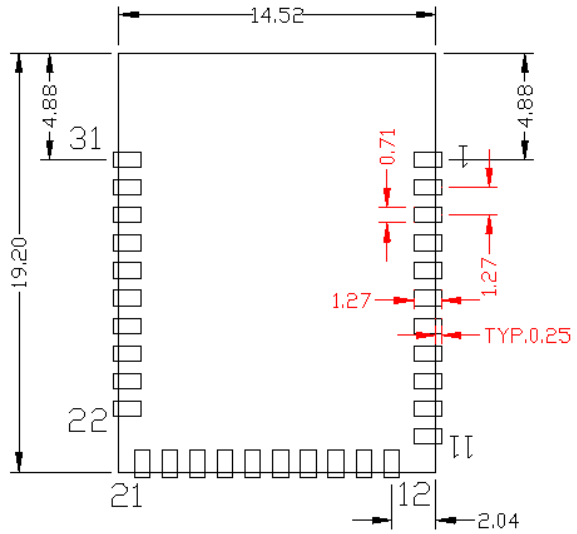
Figure 4. Recommended Host PCB Keep Out Area Around the CYBLE-0130XX-00 Antenna



Recommended Host PCB Layout

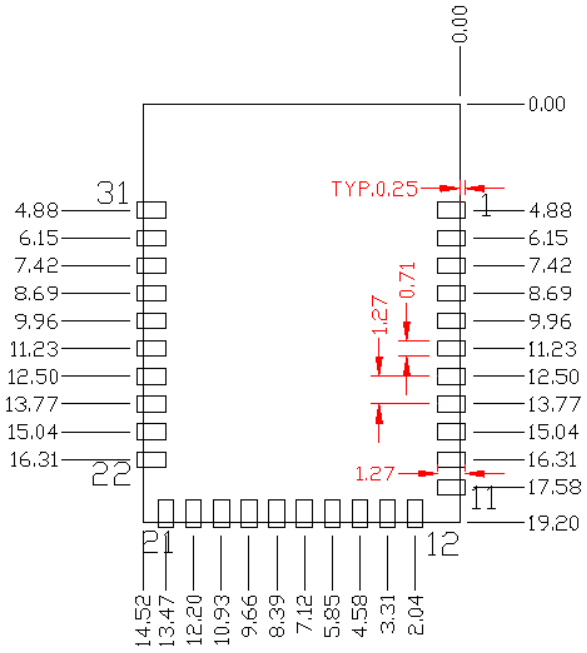
Figure 5, Figure 6, Figure 7, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-0130XX-00. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.635 mm from center of the pad on either side) shown in Figure 7 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 5, Figure 6, or Figure 7. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 5. CYBLE-0130XX-00 Host Layout (Dimensioned)



Top View (Seen on Host PCB)

Figure 6. CYBLE-0130XX-00 Host Layout (Relative to Origin)



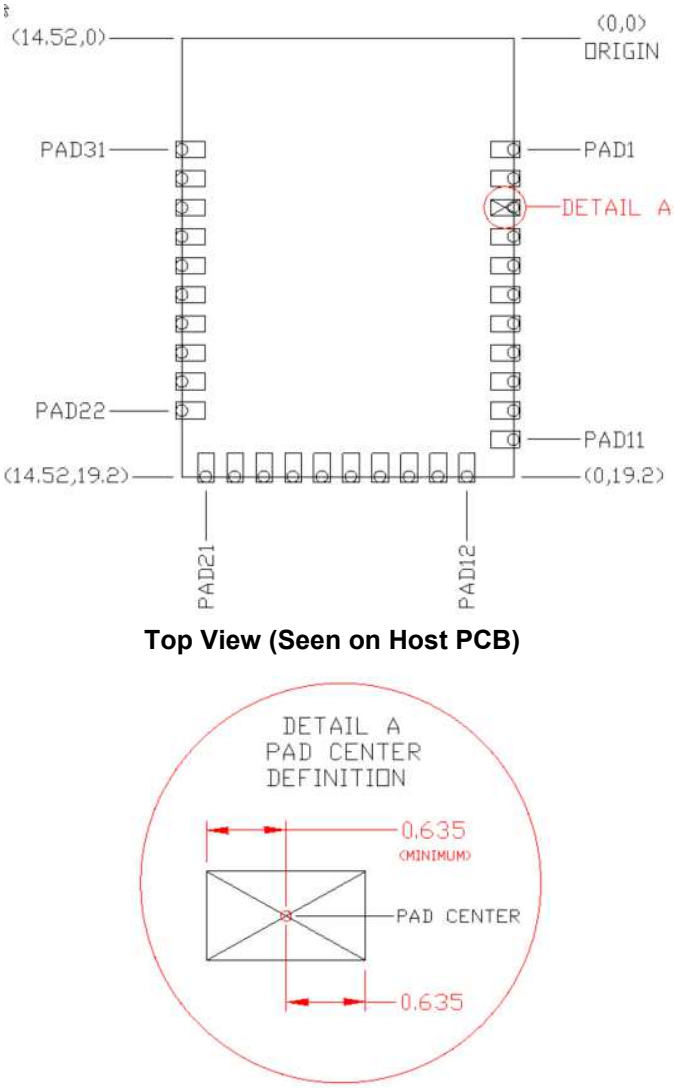
Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBLE-0130XX-00. All dimensions are referenced to the center of the solder pad. Refer to Figure 6 for the location of each module solder pad.

Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Dimension from Origin (mils)
1	(0.39, 4.88)	(15.35, 192.13)
2	(0.39, 6.15)	(15.35, 242.13)
3	(0.39, 7.42)	(15.35, 292.13)
4	(0.39, 8.69)	(15.35, 342.13)
5	(0.39, 9.96)	(15.35, 392.13)
6	(0.39, 11.23)	(15.35, 442.13)
7	(0.39, 12.50)	(15.35, 492.13)
8	(0.39, 13.77)	(15.35, 542.13)
9	(0.39, 15.04)	(15.35, 592.13)
10	(0.39, 16.31)	(15.35, 642.13)
11	(0.39, 17.58)	(15.35, 692.13)
12	(2.04, 18.82)	(80.31, 740.94)
13	(3.31, 18.82)	(130.31, 740.94)
14	(4.58, 18.82)	(180.31, 740.94)
15	(5.85, 18.82)	(230.31, 740.94)
16	(7.12, 18.82)	(280.31, 740.94)
17	(8.39, 18.82)	(330.31, 740.94)
18	(9.66, 18.82)	(380.31, 740.94)
19	(10.93, 18.82)	(430.31, 740.94)
20	(12.20, 18.82)	(480.31, 740.94)
21	(13.47, 18.82)	(530.31, 740.94)
22	(14.14, 16.31)	(556.69, 642.12)
23	(14.14, 15.04)	(556.69, 592.12)
24	(14.14, 13.77)	(556.69, 542.12)
25	(14.14, 12.50)	(556.69, 492.12)
26	(14.14, 11.23)	(556.69, 442.12)
27	(14.14, 9.96)	(556.69, 392.12)
28	(14.14, 8.69)	(556.69, 342.12)
29	(14.14, 7.42)	(556.69, 292.12)
30	(14.14, 6.15)	(556.69, 242.12)
31	(14.14, 4.88)	(556.69, 192.12)

Figure 7. Solder Pad Reference Location



Top View (Seen on Host PCB)

Module Connections

Table 4 and Table 5 detail the solder pad connection definitions and available functions for the pad connections for the CYBLE-013025-00 and CYBLE-013030-00 respectively. Table 4 and Table 5 lists the solder pads on the CYBLE-0130XX-00 modules, the silicon device pin, and denotes what functions are available for each solder pad.

Table 4. CYBLE-013025-00 Solder Pad Connection Definitions

Pad	Pad Name	UART	SPI[4]	I2C	ADC	PWM	CLK/XTAL	GPIO	Other
1	XRES	External Reset (Active Low)							
2	GND/NC	Ground/No Connect							
3	GND/NC	Ground/No Connect							
4	P11/27[5]		SPI2_MOSI (P27) (master/slave)		✓ (P11)	PWM1 (P27)	XTALI32K (P11)	✓	
5	P12/26[5]		SPI2_CS (P26) (slave)		✓ (P12))	PWM0 (P26)	XTALO32K (P12)	✓	
6	P15				✓			✓	SWDIO
7	P14/38[5]		SPI2_MOSI (P38) (master/slave)		✓ (P14/P38)	PWM2 (P14)		✓	
8	P13/28[5]				✓ (P13/P28)	PWM3 (P13) PWM2 (P28)		✓	
9	P24	PUART_TX	SPI2_CLK (master/slave)					✓	
10	NC	Not Connect							
11	NC	Not Connect							
12	P25	PUART_RX	SPI2_MISO (master/slave)					✓	
13	P4	PUART_RX	SPI2_MOSI (master/slave)					✓	
14	P2	PUART_RX	SPI2_MOSI (master)/ SPI2_CS (slave)					✓	
15	VDD	VDD (2.3 V ~ 3.63 V)							
16	P3	PUART_CTS	SPI2_CLK (master/slave)					✓	
17	P8/33[5]	No Connect (Used for on-module memory SPI interface for CYBLE-013025-00)							
18	P32	No Connect (Used for on-module memory SPI interface for CYBLE-013025-00)							
19	P1	PUART_RTS	SPI2_MISO (master/slave)		✓			✓	
20	P0	PUART_TX	SPI2_MOSI (master/slave)		✓			✓	
21	SDA			I2C_SDA				✓	
22	SCL			I2C_SCL				✓	
23	UP_TX	UART_TXD						✓	
24	UP_RX	UART_RXD						✓	
25	GND	Ground							
26	GND	Ground							
27	GND	Ground							
28	GND	Ground							
29	NC	Not Connect							
30	NC	Not Connect							
31	NC	Not Connect							

Notes
4. The CYBLE-013025-00 contains a single SPI (SPI2) peripheral supporting both master or slave configurations. SPI1 is used for on-module serial memory interface.
5. The chip pin for this connection is dual-bonded. Use of the internal chip super-mux is required to configure the desired output signal on these connections.

Table 5. CYBLE-013030-00 Solder Pad Connection Definitions

Pad	Pad Name	UART	SPI[6]	I2C	ADC	PWM	CLK/XTAL	GPIO	Other
1	XRES	External Reset (Active Low)							
2	GND/NC	Ground/No Connect							
3	GND/NC	Ground/No Connect							
4	P11/27[7]		SPI2_MOSI (P27) (master/slave)		✓ (P11)	PWM1 (P27)	XTALI32K (P11)	✓	
5	P12/26[7]		SPI1_MISO (P26, Master) SPI2_CS (P26, slave)		✓ (P12))	PWM0 (P26)	XTALO32K (P12)	✓	
6	P15				✓			✓	SWDIO
7	P14/38[7]		SPI2_MOSI (P38) (master/slave)		✓ (P14/P38)	PWM2 (P14)		✓	
8	P13/28[7]				✓ (P13/P28)	PWM3 (P13) PWM2 (P28)		✓	
9	P24	PUART_TX	SPI1_MISO (master) SPI2_CLK (master/slave)					✓	
10	NC	Not Connect							
11	NC	Not Connect							
12	P25	PUART_RX	SPI2_MISO (master/slave)					✓	
13	P4	PUART_RX	SPI2_MOSI (master)					✓	
14	P2	PUART_RX	SPI2_MOSI (master)/ SPI2_CS (slave)					✓	
15	VDD	VDD (1.62V - 3.63V)							
16	P3	PUART_CTS	SPI2_CLK (master/slave)					✓	
17	P8/33[6]	PUART_RX (P33)	SPI2_MOSI (P33) (slave) SPI1_CS (P33) (master)		✓ (P8/P33)		ACLK1 (P33)	✓	
18	P32	PUART_TX	SPI1_MISO (master) SPI2_CS (slave)		✓		ACLK0	✓	
19	P1	PUART_RTS	SPI2_MISO (master/slave)		✓			✓	
20	P0	PUART_TX	SPI2_MOSI (master/slave)		✓			✓	
21	SDA		SPI1_MOSI (master)	I2C_SDA				✓	
22	SCL		SP1_CLK (master)	I2C_SCL				✓	
23	UP_TX	UART_TXD						✓	
24	UP_RX	UART_RXD						✓	
25	GND	Ground							
26	GND	Ground							
27	GND	Ground							
28	GND	Ground							
29	NC	Not Connect							
30	NC	Not Connect							
31	NC	Not Connect							

Notes

6. The CYBLE-013030-00 contains two SPI peripherals, SPI1 and SPI2. SPI1 supports only master mode, whereas SPI2 supports masters or slave modes. The connections shown in Table 5 detail the SPI function for the given mode shown in parenthesis. If external memory is used with the CYBLE-013030-00, then SPI1 should be used as the interface..
7. The chip pin for this connection is dual-bonded. Use of the internal chip super-mux is required to configure the desired output signal on these connections.

Connections and Optional External Components

Power Connections (VDD)

The CYBLE-0130XX-00 contains one power supply connection, VDD, which accepts a supply input range of 2.3 V to 3.63 V (CYBLE-013025-00) or 1.62 V to 3.63 V (CYBLE-013030-00). Table 14 provides these specifications. The maximum power supply ripple for this power connection is 100 mV, as shown in Table 14.

It is not required to add any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included, but is not necessary. If used, the ferrite bead should be positioned as close as possible to the module connection. If used, the recommended ferrite bead value is 330 Ω, 100 MHz.

External Reset (XRES)

The CYBLE-0130XX-00 has an integrated power-on reset circuit, which completely resets all circuits to a known power on state. This action can also be evoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYBLE-0130XX-00 module (solder pad 1). The CYBLE-0130XX-00 module does not require an external pull-up resistor on the XRES input

During power-on operation, the XRES connection to the CYBLE-0130XX-00 is required to be held low 50 ms after the VDD power supply input to the module is stable. This can be accomplished in the following ways:

- The host device should connect a GPIO to the XRES of Cypress CYBLE-0130XX-00 module and pull XRES low until VDD is stable. XRES is recommended to be released 50 ms after VDD is stable.
- If the XRES connection of the CYBLE-0130XX-00 module is not used in the application, a 0.47-µF capacitor may be connected to the XRES solder pad of the CYBLE-0130XX-00 to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the VDD power supply ramp time of the system. The capacitor value should result in an XRES release timing of 50 ms after VDD stability.
- The XRES release may be controlled by a external voltage detection circuit. XRES should be released 50 ms after VDD is stable.

Refer to Figure 10 on page 19 for XRES operating and timing requirements during power on events.

Dual-Bonded GPIO Connections

The CYBLE-013030-00 contains five GPIOs that are dual-bonded at the silicon level (four such pins exist on the CYBLE-013025-00). Solder pads 4, 5, 7, 8, and 17 are the module connections with dual-bonded silicon I/O. If any of these dual-bonded GPIO are used, only the functionality and features for one of these port pins may be used. The desired port pin should be configured in the WICED SMART SDK. For details on the features and functions that each of these dual-bonded GPIOs provide, refer to Table 4 and Table 5. For additional information on all available GPIOs, refer to GPIO Port on page 22.

External 32-kHz Clock/Crystal Oscillator Input

The CYBLE-0130XX-00 provides the option to connect an external 32-kHz crystal oscillator or clock input instead of using the internal Local Oscillator (LO). Solder pads 4 and 5 of the CYBLE-0130XX-00 module provide this connection option. Note that these connections are also dual-bonded GPIOs, requiring the appropriate GPIO to be selected to enable external clocking functionality. The specific pins required are as follows:

- Module Solder Pad 4, Silicon GPIO P11 - Must be assigned as XTALI32K (Crystal Input terminal)
- Module Solder Pad 5, Silicon GPIO P12 - Must be assigned as XTALO32K (Crystal Output terminal)

This option may be desired for customers who wish to achieve minimum power consumption in their application. Refer to 32-kHz Crystal Oscillator (Optional) on page 21 for details on the requirements for an external 32-kHz input to the CYBLE-0130XX-00.

Using CYBLE-013030-00 with External Flash

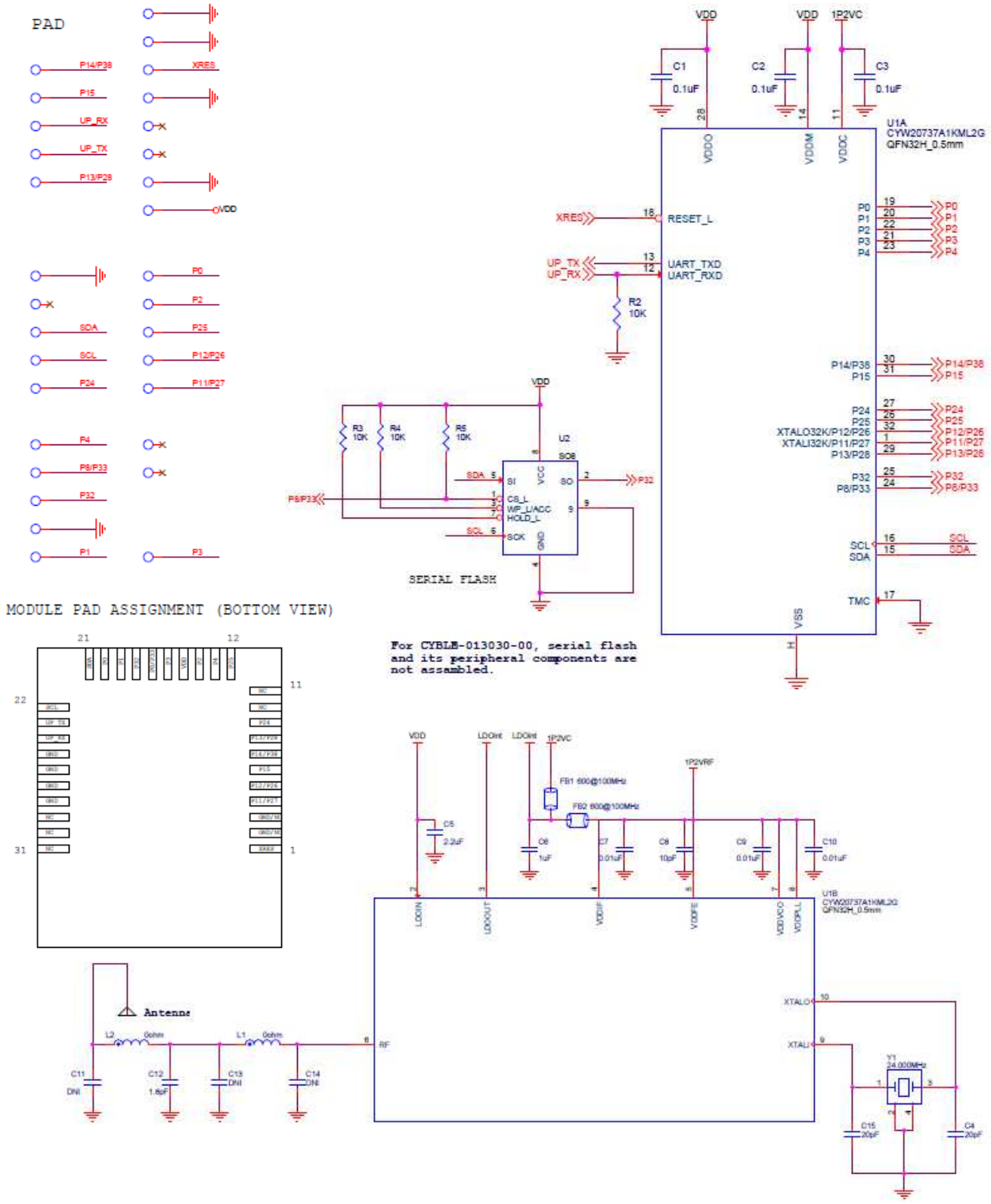
The CYBLE-013030-00 does not contain any on-module nonvolatile memory. If desired, the CYBLE-013030-00 can be used with an external memory device (EEPROM or SFLASH). If EEPROM is used as an external memory device with I^2C interface, module solder pads 21 (SDA) and 22 (SCL) must be used as the I^2C interface.

If using external SFLASH as the memory interface, SPI1 (master) must be used as the interface to the SFLASH device. The specific GPIO required and the applicable SPI signal is listed below. These are the same signals used for the SFLASH interface on the CYBLE-013025-00.

1. SPI signal MOSI: Module Solder Pad 21, silicon GPIO SDA
2. SPI signal MISO: Module Solder Pad 18, silicon GPIO P32
3. SPI Signal CLK: Module Solder Pad 22, silicon GPIO SCL
4. SPI Signal CS: Module Solder Pad 17, silicon GPIO P8

Figure 8 illustrates the CYBLE-0130XX-00 schematic.

Figure 8. CYBLE-0130XX-00 Schematic Diagram



Critical Components List

Table 6 details the critical components used in the CYBLE-0130XX-00 module.

Table 6. Critical Component List

Component	Reference Designator	Description
Silicon	U1	32-pin QFN BLE Silicon Device - CYW20737
Silicon	U2	8-pin TDF8N, 128K Serial Flash (CYBLE-013025-00)
Crystal	Y1	24.000 MHz, 12PF

Antenna Design

Table 7 details the trace antenna used in the CYBLE-0130XX-00 module. For more information, see Table 7.

Table 7. Trace Antenna Specifications

Item	Description
Frequency Range	2400–2500 MHz
Peak Gain	–0.5 dBi
Return Loss	10 dB minimum

Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for a high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and data routing for all connections. It also buffers data that passes through it, handles data flow control, schedules ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase TX/RX data reliability and security before sending over the air:

- Receive Functions: symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening.
- Transmit Functions: data framing, FEC generation, HEC generation, CRC generation, link key generation, data encryption, and data whitening.

Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number depending on the link controller state, Bluetooth clock, and device address.

E0 Encryption

The encryption key and the encryption engine are implemented using dedicated hardware to reduce software complexity and provide minimal processor intervention.

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the Link Control Unit (LCU). This layer consists of the Command Controller, which takes software commands, and other controllers that are activated or configured by the Command Controller to perform the link control tasks. Each task performs a different Bluetooth link controller state. STANDBY and CONNECTION are the two major states. In addition, there are four substates: page, page scan, inquiry, and inquiry scan.

Adaptive Frequency Hopping

The CYBLE-0130XX-00 gathers link quality statistics on a channel-by-channel basis to facilitate channel assessment and channel map selection. The link quality is determined by using both RF and baseband signal processing to provide a more accurate frequency hop map.

Bluetooth Low Energy Profiles

The CYBLE-0130XX-00 supports Bluetooth Low Energy (BLE), including the following profiles that are supported[8] in ROM:

- Battery status
- Blood pressure monitor
- Find me
- Heart rate monitor
- Proximity
- Thermometer
- Weight scale
- Time
- Alliance for Wireless Power (A4WP) wireless charging
- Automation profile
- Support for secure OTA (external memory required for CYBLE-013030-00)

The following additional profiles can be supported[8] from RAM:

- Blood glucose monitor
- Temperature alarm
- Location
- Custom profile

Test Mode Support

The CYBLE-0130XX-00 supports Bluetooth Test mode, as described in the Bluetooth Low Energy specification.

Security

CYBLE-0130XX-00 provides mechanisms for implementing security and authentication schemes using:

- RSA (Public Key Cryptography)
- X.509 (excluding parsing)
- Hash functions: MD5, SHA-1, SHA-224, SHA-256, SHA-384, SHA-512
- Message authentication code: HMAC MD5, HMAC SHA-1

Note
8. Full qualification and use of these profiles may require FW updates from Cypress. Some of these profiles are under development/approval at the Bluetooth SIG and conformity with the final approved version is pending. Contact your local representative for updates and the latest list of profiles.

ADC Port

The CYBLE-0130XX-00 contains a 16-bit ADC (effective number of bits is 10).

Additionally:

- There are nine analog input channels in the 31-pad module
- The following GPIOs can be used as ADC inputs (module pad number denoted in [ ]):
  - P0 [Pad 20]
  - P1 [Pad 19]
  - P8/P33 (select only one[9]) [Pad 17]
  - P11 on P11/P27[10] pin [Pad 4]
  - P12 on P12/28[10] pin [Pad 5]
  - P13/P28[9] (select only one) [Pad 8]
  - P14/P38[9] (select only one) [Pad 7]
  - P15 [Pad 6]
  - P32 [Pad 18]
- The conversion time is 10 us.
- There is a built-in reference with supply- or bandgap-based reference modes.
- The maximum conversion rate is 187 kHz.
- There is a rail-to-rail input swing.

The ADC consists of an analog ADC core that performs the actual analog-to-digital conversion and digital hardware that processes the output of the ADC core into valid ADC output samples.

The ADC input range is selectable by firmware control:

- When an input range of 0~3.6 V is used, the input impedance is 3 MW.
- When an input range of 0~2.4 V is used, the input impedance is 1.84 MW.
- When an input range of 0~1.2 V is used, the input impedance is 680 kW.

ADC modes are defined in Table 8.

Table 8. ADC Modes

Mode	Effective Number of Bits (Typical)	Maximum Sampling Rate (kHz)	Latency[11] (us)
0	13	5.859	171
1	12.6	11.7	85
2	12	46.875	21
3	11.5	93.75	11
4	10	187	5

Notes
9. Either signal on these dual-bonded connections may be used for ADC functionality.
10. Only the specified port-pin connection may be used for ADC functionality (for example, only a P11 configuration on module pad 4 (P11/P27) may be used for ADC functionality.
11. Settling time after switching channels.

Serial Peripheral Interface

The CYBLE-0130XX-00 has two independent SPI interfaces, SPI1 and SPI2. One is a master-only (SPI1) interface and the other can be either a master or a slave (SPI2). Each interface has a 16-byte transmit buffer and a 16-byte receive buffer. The CYBLE-013025-00 has one SPI interface available to the user (SPI2). SPI1 is used as the on-board SFLASH interface on the CYBLE-013025-00. CYBLE-013030-00 has both SPI interfaces available to the user. If an external SFLASH memory is used, SPI1 should be used as the interface to the memory device.

The CYBLE-0130XX-00 can act as an SPI master device that supports 1.8 V or 3.3 V SPI slaves. The CYBLE-0130XX-00 can also act as an SPI slave device that supports a 1.8 V or 3.3 V SPI master. Table 9, Table 10, and Table 11 details the available signal connections on BLE silicon device for each SPI function. The module solder pad number for each silicon connection is shown in Table 4 and Table 5.

Table 9 details the available SPI master mode connections when a SPI serial flash connection is present (detault for the CYBLE-013025-00, and optional for the CYBLE-013030-00). Table 10 details the available SPI master mode connections when there is no SPI serial flash connected to the module (only the case for the CYBLE-013030-00). Table 11 details the available SPI slave mode connections under no restrictions.

Table 9. CYBLE-0130XX-00 SPI1 (Master Mode)

Pin Name	SPI_CLK	SPI_MOSI	SPI_MISO[12]	SPI_CS[13]
Configured Pin Name	SCL [Pad 22]	SDA [Pad 21]	P32 [Pad 18]	P33[14] [Pad 17]

Table 10. CYBLE-0130XX-00 SPI2 (Master Mode)

Pin Name	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS[15]
Configured Pin Name	P3 [Pad 16]	P0 [Pad 20]	P1 [Pad 19]	–
	P24 [Pad 9]	P4 [Pad 13]	P25 [Pad 12]	–
	–	P27 [Pad 4]	–	–

Table 11. CYBLE-0130XX-00 SPI2 (Slave Mode)

Pin Name	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS
Configured Pin Name	P3 [Pad 16]	P0 [Pad 20]	P1 [Pad 19]	P2 [Pad 14]
	P24 [Pad 9]	P27 [Pad 4]	P25 [Pad 12]	P26 [Pad 5]
	–	P33 [Pad 17]	–	P32 [Pad 18]

Notes
12. SPI1 MISO should always be P32 (solder pad 18). Boot ROM of the silicon device does not configure any others.
13. Any GPIO can be used as SPI_CS when SPI1 is in master mode, and when the SPI slave is not a serial flash.
14. P33 (solder pad 17) is always SPI_CS when a serial flash is used for nonvolatile storage. This is also the case for the CYBLE-013025-00.
15. Any available GPIO can be used as SPI_CS when SPI2 is in master mode.

Microprocessor Unit

The CYBLE-0130XX-00 microprocessor unit (µPU) executes software from the link control (LC) layer up to the application layer components. The microprocessor is based on an ARM® Cortex® M3, 32-bit RISC processor. The µPU has 320 KB of ROM for program storage and boot-up, 60 KB of RAM for scratch-pad data, and patch RAM code. The SoC has a total storage of 380 KB, including RAM and ROM.

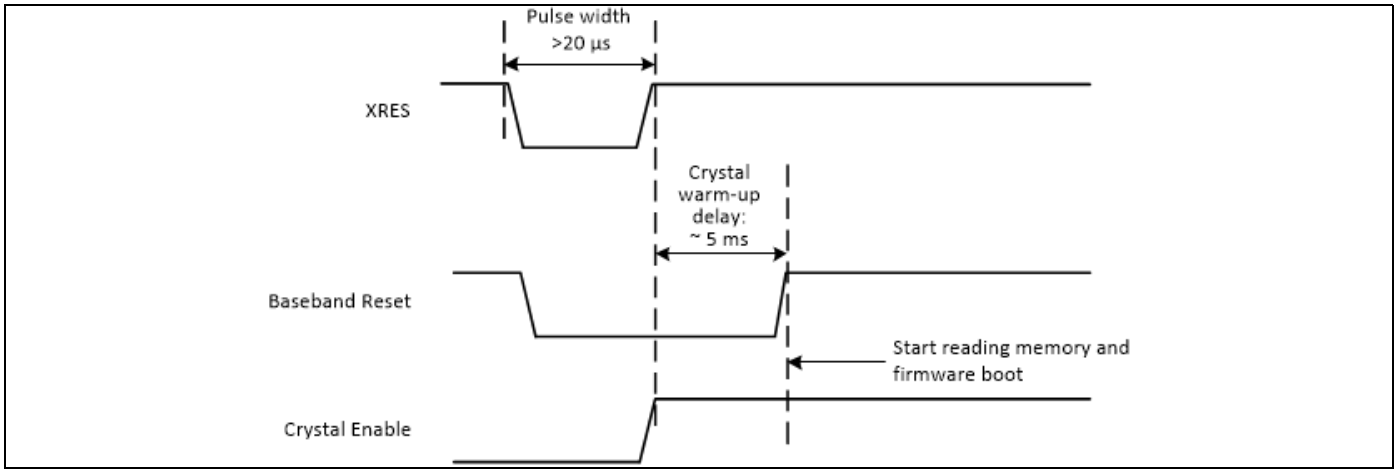
The internal boot ROM provides power-on reset flexibility, which enables the same device to be used in different HID applications with an external serial EEPROM or with an external serial flash memory. At power-up, the lowest layer of the protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes and feature additions. The device also supports the integration of user applications.

External Reset (XRES)

The CYBLE-0130XX-00 has an integrated power-on reset circuit that completely resets all circuits to a known power-on state. An external active low reset signal, XRES, can be used to put the CYBLE-0130XX-00 in the reset state.

Figure 9. External Reset (XRES) Timing

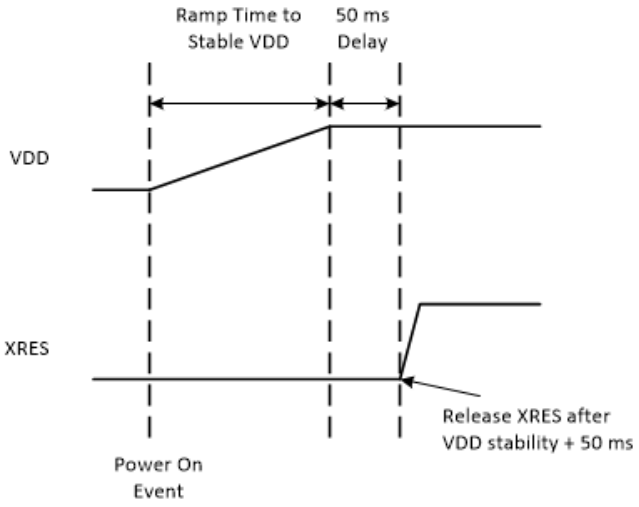


External Reset (XRES) Recommended External Components and Power On Operation

During a power-on event, the XRES line of the CYBLE-0130XX-00 is required to be held low 50 ms after the VDD power supply input to the module is stable. Refer to Figure 10 for the Power On XRES timing operation. This power-on operation can be accomplished in the following ways:

- A host device should connect a GPIO to the XRES of Cypress CYBLE-0130XX-00 module and pull XRES low until VDD is stable. XRES can be released after VDD is stable.
- If the XRES connection of the CYBLE-0130XX-00 module is not used in the application, a 0.47-µF capacitor may be connected to the XRES solder pad of the CYBLE-0130XX-00.
- The XRES release timing can also be controlled via a external voltage detection circuit.

Figure 10. Power-On External Reset (XRES) Operation



Integrated Radio Transceiver

The CYBLE-0130XX-00 has an integrated radio transceiver that is optimized for 2.4-GHz Bluetooth wireless systems. It has been designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. It is fully compliant with Bluetooth Radio Specification 4.1 and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

The CYBLE-0130XX-00 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4-GHz ISM band.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

Power Amplifier

The CYBLE-0130XX-00 has an integrated power amplifier (PA) that can transmit up to +4 dBm for class 2 operation.

Receiver Path

The receiver path uses a low IF scheme to down convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, and an extended dynamic range to ensure reliable operation in the noisy 2.4-GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYBLE-0130XX-00 to be used in most applications without off-chip filtering.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYBLE-0130XX-00 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator (LO)

The accuracy of the local oscillator is ±250 ppm. The CYBLE-0130XX-00 is designed to use the LO for sleep mode operation and power savings.

Additional power consumption savings can be achieved by connecting an accurate external crystal oscillator to the CYBLE-0130XX-00 module. If used, the external crystal oscillator connects to Pads 4 (P11 - input) and 5 (P12 - output) of the CYBLE-0130XX-00. Refer to 32-kHz Crystal Oscillator (Optional) on page 21 for more details.

Calibration

The CYBLE-0130XX-00 radio transceiver features a self-contained automated calibration scheme. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration compensates for filter, matching network, and amplifier gain and phase characteristics to yield radio performance within 2% of what is optimal. Calibration takes process and temperature variations into account, and it takes place transparently during normal operation and hop setting times.

Internal LDO Regulator

The CYBLE-0130XX-00 has an integrated 1.2-V LDO regulator that provides power to the digital and RF circuits. The 1.2-V LDO regulator operates from a 2.3 V to 3.63 V (CYBLE-013025-00) or 1.62 V to 3.63 V (CYBLE-013030-00) input supply with a 30-mA maximum load current.

Peripheral Transport Unit

Broadcom Serial Communications Interface

The CYBLE-0130XX-00 provides a 2-pin master BSC interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I^2C slave devices. The BSC does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by the BSC:

- 100 kHz
- 400 kHz
- 800 kHz (not a standard I^2C-compatible speed.)
- 1 MHz (Compatibility with high-speed I^2C-compatible devices is not guaranteed.)

The following transfer types are supported by the BSC:

- Read (Up to 16 bytes can be read.)
- Write (Up to 16 bytes can be written.)
- Read-then-Write (Up to 16 bytes can be read and up to 16 bytes can be written.)
- Write-then-Read (Up to 16 bytes can be written and up to 16 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the CYBLE-0130XX-00 are required on both the SCL and SDA pins for proper operation. The CYBLE-013025-00 does allow for I^2C operation, even though the SDA and SCL connections are used for on-board memory interface. WICED Smart SDK Version 2.2.3 must be used for I^2C operation to work on the CYBLE-013025-00.

UART Interface

The UART is a standard 2-wire interface (RX and TX) and has adjustable baud rates from 9600 bps to 1.5 Mbps. The baud rate can be selected via a vendor-specific UART HCI command. The interface supports the Bluetooth 3.0 UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

Both high and low baud rates can be supported by running the UART clock at 24 MHz.

The CYBLE-0130XX-00 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

Clock Frequencies

Crystal Oscillator

The CYBLE-0130XX-00 has an integrated 24-MHz crystal on the module. There is no need to add an additional crystal oscillator.

Peripheral Block

The peripheral blocks of the CYBLE-0130XX-00 all run from a single 128 kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case, in that it may drop its clock request line even when enabled, and then reassert the clock request line if a keypress is detected.

32-kHz Crystal Oscillator (Optional)

The use of an external 32-kHz crystal oscillator is optional for the CYBLE-0130XX-00 module. Figure 11 shows the 32-kHz crystal (XTAL) oscillator with external components and Table 12 list the oscillator's characteristics. It is a standard Pierce oscillator using a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis was added to eliminate any chatter when the input is around the threshold of the comparator and is ~100 mV. This circuit can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at similar frequency. The default component values are: R1 = 10 MΩ, C1 = C2 = ~10 pF. The values of C1 and C2 are used to fine-tune the oscillator.

Figure 11. 32 kHz Oscillator Block Diagram

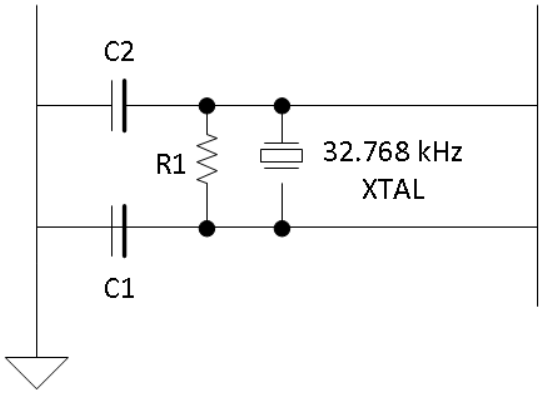


Table 12. XTAL Oscillator Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Crystal dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	–	500	ms
XTAL drive level	P_{drv}	For crystal selection	0.5	–	–	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	–	–	1.3	pF

If used, the external crystal oscillator connects to Pad 4 (P11 - input) and Pad 5 (P12 - output) of the CYBLE-0130XX-00. Refer to Table 4 and Table 5 for more details on the available functions for each solder pad connections.

GPIO Port

The CYBLE-0130XX-00 has 14 GPIOs, which can be used for Serial Communication, I/O control, and other GPIO functionality. All GPIOs support programmable pull-up and pull-down resistors, and all support a 2 mA drive strength except P26, P27, and P28, which provide a 16 mA drive strength at 3.3-V supply. The following GPIOs are available:

- P0-P4
- P8/P33 only available for CYBLE-013030-00
- P11/P27 (Dual bonded, only one of two is available)
- P12/P26 (Dual bonded, only one of two is available)
- P13/P28 (Dual bonded, only one of two is available)
- P14/P38 (Dual bonded, only one of two is available)
- P15
- P24
- P25
- P32 - only available for CYBLE-013030-00

For a description of the capabilities of all GPIOs, see Table 4 and Table 5.

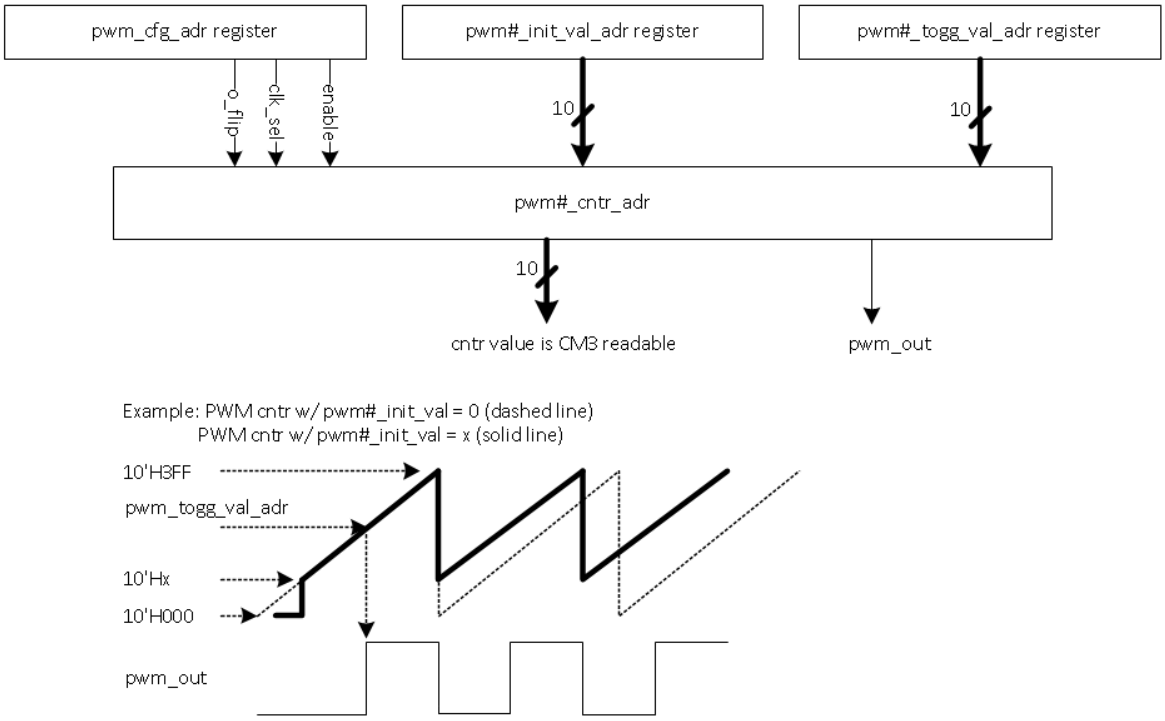
PWM

The CYBLE-0130XX-00 has four PWMs. The PWM module consists of the following:

- PWM0-3
- The following GPIOs can be mapped as PWMs; module pad assignments are shown in Table 4 and Table 5:
  - P26 on P12/P26 [Pad 5]
  - P27 on P11/P27 [Pad 4]
  - P14 on P14/P38 [Pad 7]
  - P13 on P13/P28 [Pad 8]
- PWM0-3: Each of the four PWM channels contains the following registers:
  - 10-bit initial value register (read/write)
  - 10-bit toggle register (read/write)
  - 10-bit PWM counter value register (read)
- PWM configuration register shared among PWM0-3 (read/write). This 12-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 12 shows the structure of one PWM.

Figure 12. PWM Block Diagram



Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4-GHz transceiver, which then processes the power-down functions accordingly.

Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in deep sleep (HIDOFF) mode.

BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the CYBLE-0130XX-00 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYBLE-0130XX-00 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF (Deep Sleep) mode
- Timed Deep Sleep mode

The CYBLE-0130XX-00 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

- In HIDOFF (Deep Sleep) mode, the CYBLE-0130XX-00 baseband and core are powered off by disabling power to LDOOUT. The VDDO domain remains powered up and will turn the remainder of the module on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

Electrical Characteristics

Table 13 shows the maximum electrical rating for voltages referenced to VDD pin.

Table 13. Maximum Electrical Rating

Rating	Symbol	Value	Unit
VDD	–	3.8	V
Voltage on input or output pin	–	VSS – 0.3 to VDD + 0.3	V
Operating ambient temperature range	Topr	–30 to +85	°C
Storage temperature range	Tstg	–40 to +125	°C

Table 14 shows the power supply characteristics for the range T_J = 0 to 125 °C.

Table 14. Power Supply

Parameter	Description	Minimum[16]	Typical	Maximum[16]	Unit
V_{DD}	Power Supply Input (CYBLE-013025-00)	2.30	–	3.63	V
	Power Supply Input (CYBLE-013030-00)	1.62	–	3.63	V
V_{DD_RIPPLE}	Maximum power supply ripple for V_{DD} input voltage	–	–	100	mV

Table 15 shows the specifications for the ADC characteristics.

Table 15. ADC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Number of Input channels	–	–	–	9	–	–
Channel switching rate	f_{ch}	–	–	–	133.33	kch/s
Input signal range	V_{inp}	–	0	–	3.63	V
Reference settling time	–	Changing refsel	7.5	–	–	µs
Input resistance	R_{inp}	Effective, single ended	–	500	–	kΩ
Input capacitance	C_{inp}	–	–	–	5	pF
Conversion rate	f_C	–	5.859	–	187	kHz
Conversion time	T_C	–	5.35	–	170.7	µs
Resolution	R	–	–	16	–	bits
Effective number of bits	–	In specified performance range	–	See Table 8 on page 16	–	
Absolute voltage measurement error	–	Using on-chip ADC firmware driver	–	±2	–	%
Current	I	$I_{avdd1p2} + I_{avdd3p3}$	–	–	1	mA
Power	P	–	–	1.5	–	mW
Leakage current	$I_{leakage}$	T = 25 °C	–	–	100	nA
Power-up time	$T_{powerup}$	–	–	–	200	µs
Integral nonlinearity[17]	INL	In guaranteed performance range	–	–	1	LSB
Differential nonlinearity[17]	DNL	In guaranteed performance range	–	–	1	LSB

Notes
16. Overall performance degrades beyond minimum and maximum supply voltages.
17. LSBs are expressed at the 10-bit level.