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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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CYBLE-212006-01
CYBLE-202007-01
CYBLE-202013-11

EZ-BLE™ PRoC™ XR Module

General Description

The CYBLE-2X20XX-X1 is a Bluetooth® Low Energy (BLE) wireless module solution. The CYBLE-2X20XX-X1 is a turnkey solution and includes onboard crystal oscillators, passive components, and the Cypress PRoC™ BLE. Refer to the CYBL1XX7X datasheet for additional details on the capabilities of the PRoC BLE device used on this module.

The CYBLE-2X20XX-X1 supports a number of peripheral functions (ADC, timers, counters, PWM) and serial communication protocols (I^2C, UART, SPI) through its programmable architecture. The CYBLE-2X20XX-X1 includes a royalty-free BLE stack compatible with Bluetooth 4.2 and provides up to 19 GPIOs in a 15.0 × 23.0 × 2.0 mm package.

The CYBLE-2X20XX-X1 is offered in two certified versions (CYBLE-212006-01 and CYBLE-202007-01), as well as an uncertified version (CYBLE-202013-11). The CYBLE-212006-01 includes an integrated trace antenna. The CYBLE-202007-01 supports an external antenna via a u-FL connector. The CYBLE-202013-11 supports an external antenna through a RF solder pad output. The CYBLE-202013-11 does not include a RF shield and is not regulatory certified.

Module Description

- Module size: 15.00 mm × 23.00 mm × 2.00 mm
- Extended Range:
  - Up to 400 meters bidirectional communication[1,2]
  - Up to 450 meters in beacon only mode[1]
- Bluetooth 4.2 qualified single-mode module
  - QDID: 88957
  - Declaration ID: D032786
- Footprint compatible options for integrated antenna or antenna-less design options
- Certified to FCC, IC, MIC, KC, and CE regulations (CYBLE-212006-01 and CYBLE-202007-01 only)
- Castelated solder pad connections for ease-of-use
- 256-KB flash memory, 32-KB SRAM memory
- Up to 19 GPIOs
- Industrial temperature range: –40 °C to +85 °C
- 32-bit processor (0.9 DMIPS/MHz) operating up to 48 MHz
- Watchdog timer with dedicated internal low-speed oscillator

Power Consumption

- Maximum TX output power: +7.5 dbm
- RX Receive Sensitivity: –93 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution
- TX current consumption
  - BLE silicon: 15.6 mA (radio only, 0 dbm)
  - RFX2401C: 27 mA (PA/LNA only, +7.5 dBm)
- RX current consumption
  - BLE silicon: 16.4 mA (radio only, 0 dbm)
  - RFX2401C: 8.0 mA (PA/LNA only)
- Cypress CYBL1XX7X silicon low power mode support
  - Deep Sleep: 1.3 µA with watch crystal oscillator (WCO) on
  - Hibernate: 150 nA with SRAM retention
  - Stop: 60 nA with XRES wakeup

Functional Capabilities

- Up to 18 capacitive sensors for buttons or sliders
- 12-bit, 1-Msps SAR ADC with internal reference, sample-and-hold (S/H), and channel sequencer
- Two serial communication blocks (SCBs) supporting I^2C (master/slave), SPI (master/slave), or UART
- Four dedicated 16-bit timer, counter, or PWM blocks (TCPWMs)
- LCD drive supported on all GPIOs (common or segment)
- Programmable low voltage detect (LVD) from 1.8 V to 4.5 V
- I^2S master interface
- BLE protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
- Switches between Central and Peripheral roles on-the-go
- Standard BLE profiles and services for interoperability
- Custom profile and service for specific use cases

Benefits

CYBLE-2X20XX-X1 is provided as a turnkey solution, including all necessary hardware required to use BLE communication standards.

- Proven hardware design ready to use
- Cost optimized for applications without space constraint
- Reprogrammable architecture
- Fully certified module eliminates the time needed for design, development and certification
- Bluetooth SIG qualified with QDID and Declaration ID
- Flexible communication protocol support
- PSoC Creator™ provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test a BLE application

Notes
1. Connection range tested module-to-module in full line-of-sight environment, free of obstacles or interferance sources with output power of +7.5 dBm.
2. Specified as EZ-BLE XR module to module range. Mobile phone connection range will decrease based on the PA/LNA performance of the mobile phone used.

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

- Overview: EZ-BLE Module Portfolio, Module Roadmap
- EZ-BLE PRoC Product Overview
- PRoC BLE Silicon Datasheet
- Application notes: Cypress offers a number of BLE application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with EZ-BLE modules are:
  - AN96841 - Getting Started with EZ-BLE Module
  - AN94020 - Getting Started with PRoC BLE
  - AN97060 - PSoC® 4 BLE and PRoC™ BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91162 - Creating a BLE Custom Profile
  - AN91184 - PSoC 4 BLE - Designing BLE Applications
  - AN92584 - Designing for Low Power and Estimating Battery Life for BLE Applications
  - AN85951 - PSoC® 4 CapSense® Design Guide
  - AN95089 - PSoC® 4/PRoC™ BLE Crystal Oscillator Selection and Tuning Techniques
  - AN91445 - Antenna Design and RF Layout Guidelines
- Technical Reference Manual (TRM):
  - PRoC® BLE Technical Reference Manual
- Knowledge Base Articles
  - KBA212334 - Pin Mapping Differences Between the EZ-BLE PRoC® Evaluation Boards (CYBLE-212006-EVAL/CY-BLE-202007-EVAL/CYBLE-202013-EVAL) and the BLE Pioneer Kit (CY8CKIT-042-BLE)
  - KBA97095 - EZ-BLE™ Module Placement
  - KBA216380 - RF Regulatory Certifications for CY-BLE-212006-01 and CYBLE-202007-01 EZ-BLE™ PRoC® XR Modules
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
- Development Kits:
  - CYBLE-212006-EVAL, CYBLE-212006-01 Eval Board
  - CYBLE-202007-EVAL, CYBLE-202007-01 Eval Board
  - CYBLE-202013-EVAL, CYBLE-202013-11 Eval Board
  - CY8CKIT-042-BLE, Bluetooth® Low Energy Pioneer Kit
  - CY8CKIT-002, PSoC® MiniProg3 Program and Debug Kit
- Test and Debug Tools:
  - CYSmart, Bluetooth® LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)

Two Easy-To-Use Design Environments to Get You Started Quickly

PSoC® Creator™ Integrated Design Environment (IDE)

PSoC Creator is an Integrated Design Environment (IDE) that enables concurrent hardware and firmware editing, compiling and debugging of PSoC 3, PSoC 4, PSoC 5LP, PSoC 4 BLE, PRoC BLE and EZ-BLE module systems with no code size limitations. PSoC peripherals are designed using schematic capture and simple graphical user interface (GUI) with over 120 pre-verified, production-ready PSoC Components™.

PSoC Components are analog and digital “virtual chips,” represented by an icon that users can drag-and-drop into a design and configure to suit a broad array of application requirements.

Bluetooth Low Energy Component

The Bluetooth Low Energy Component inside PSoC Creator provides a comprehensive GUI-based configuration window that lets you quickly design BLE applications. The Component incorporates a Bluetooth Core Specification v4.2 compliant BLE protocol stack and provides API functions to enable user applications to interface with the underlying Bluetooth Low Energy Sub-System (BLESS) hardware via the stack.

EZ-Serial™ BLE Firmware Platform

The EZ-Serial Firmware Platform provides a simple way to access the most common hardware and communication features needed in BLE applications. EZ-Serial implements an intuitive API protocol over the UART interface and exposes various status and control signals through the module’s GPIOs, making it easy to add BLE functionality quickly to existing designs.

Use a simple serial terminal and evaluation kit to begin development without requiring an IDE. Refer to the EZ-Serial webpage for User Manuals and instructions for getting started as well as detailed reference materials.

EZ-BLE modules are pre-flashed with the EZ-Serial Firmware Platform. If you do not have EZ-Serial pre-loaded on your module, you can download each EZ-BLE module’s firmware images on the EZ-Serial webpage.

Technical Support

- Frequently Asked Questions (FAQs): Learn more about our BLE ECO System.
- Forum: See if your question is already answered by fellow developers on the PSoC 4 BLE and PRoC BLE forums.
- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

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Overview

Module Description

The CYBLE-2X20XX-X1 module is a complete module designed to be soldered to the applications main board.

Module Dimensions and Drawing

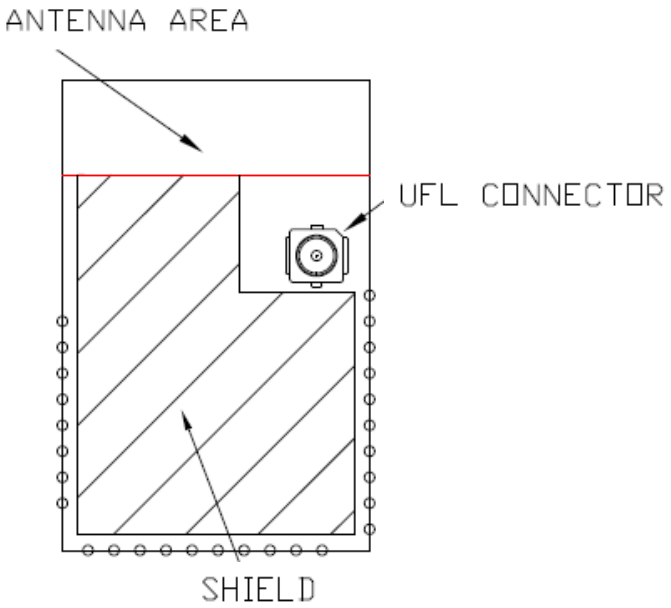
Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will still guarantee that all height restrictions of the component area are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in Figure 1. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

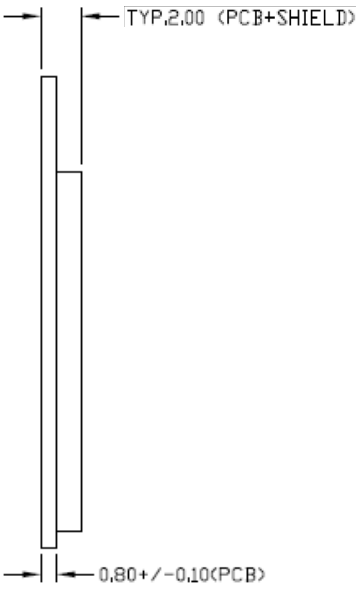
Dimension Item		Specification
Module dimensions	Length (X)	15.00 ± 0.15 mm
	Width (Y)	23.00 ± 0.15 mm
Antenna location dimensions	Length (X)	15.00 ± 0.15 mm
	Width (Y)	4.65 ± 0.15 mm
PCB thickness	Height (H)	0.80 ± 0.10 mm
Shield height	Height (H)	1.20 ± 0.10 mm
Maximum component height	Height (H)	1.20 mm typical (shield) - CYBLE-212006-01 1.25 mm typical (connector) - CYBLE-202007-01 0.75mm typical (crystal) - CYBLE-202013-11
Total module thickness (bottom of module to highest component)	Height (H)	2.00 mm typical - CYBLE-212006-01 2.05 mm typical - CYBLE-202007-01 1.55 mm typical - CYBLE-202013-11

See Figure 1 on page 5 for the mechanical reference drawing for CYBLE-2X20XX-X1.

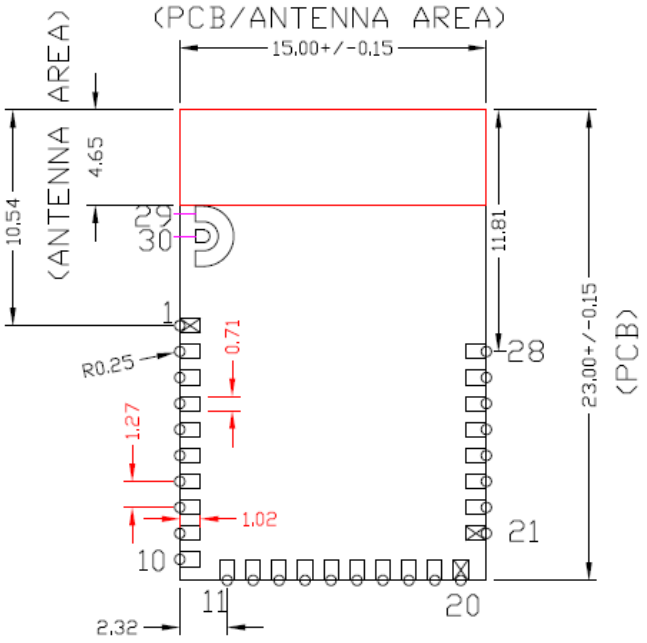
Figure 1. Module Mechanical Drawing



Top View



Side View



MODULE PAD ASSIGNMENT:

PAD1:GND
PAD2:XRES
PAD3:P4.0
PAD4:P3.7
PAD5:P3.6
PAD6:P3.5
PAD7:P3.4
PAD8:VREF
PAD9:P2.6
PAD10:P2.4
PAD11:P2.3
PAD12:P2.2
PAD13:P2.0
PAD14:P1.7
PAD15:P1.6
PAD16:P1.5
PAD17:P1.4
PAD18:P0.7
PAD19:P1.0
PAD20:P0.4
PAD21:P0.5
PAD22:VDD
PAD23:P0.6
PAD24:GND
PAD25:GND
PAD26:GND
PAD27:GND
PAD28:VDDR
PAD29:GND-for 202013 only
PAD30:ANT-for 202013 only

Bottom View

Note
3. No metal or traces should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see Figure 3, Figure 4, Figure 5, and Figure 6 and Table 3.

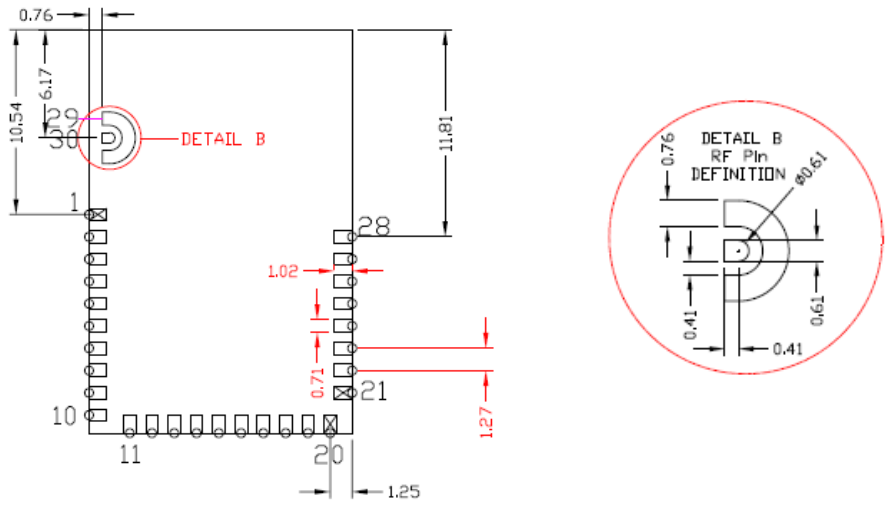
Pad Connection Interface

As shown in the bottom view of Figure 1 on page 5, the CYBLE-2X20XX-X1 connects to the host board via solder pads on the backside of the module. Table 2 and Figure 2 detail the solder pad length, width, and pitch dimensions of the CYBLE-2X20XX-X1 module.

Table 2. Solder Pad Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	30	Solder Pads	1.02 mm	0.71 mm	1.27 mm

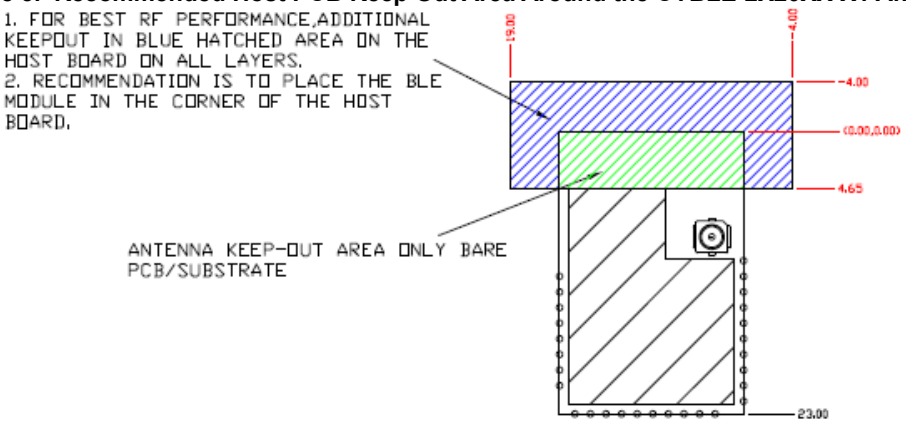
Figure 2. Solder Pad Dimensions (Seen from Bottom)



To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE module is in a corner of the host board with the trace antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2. Refer to AN96841 for module placement best practices.
2. To maximize RF performance, the area immediately around the Cypress BLE module trace antenna should contain an additional keep out area, where no grounding or signal trace are contained. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in Figure 3 (dimensions are in mm).

Figure 3. Recommended Host PCB Keep Out Area Around the CYBLE-2X20XX-X1 Antenna

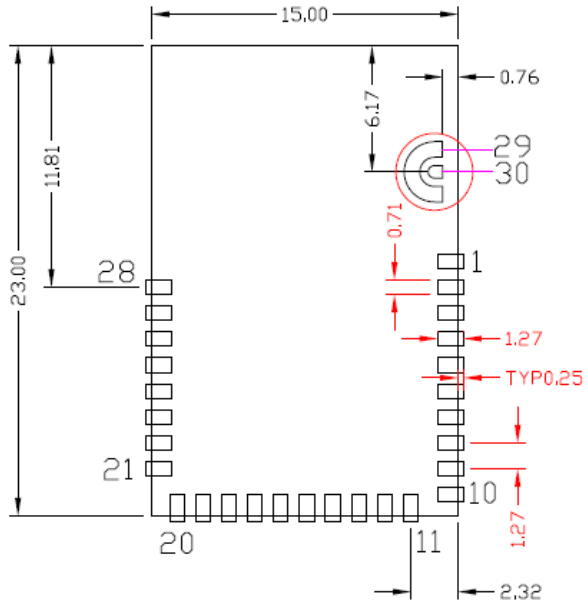


Host PCB Keep Out Area Around Trace Antenna

Recommended Host PCB Layout

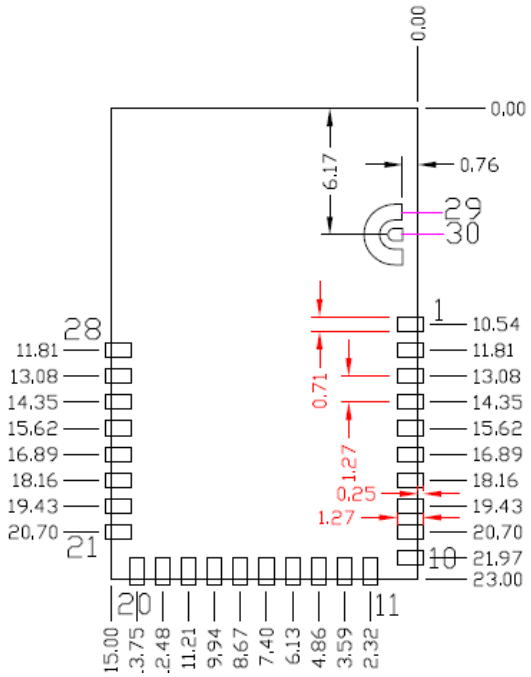
Figure 4, Figure 5, Figure 6, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-212006-01. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.635 mm from center of the pad on either side) shown in Figure 6 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 4, Figure 5, or Figure 6. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 4. Host Layout Pattern for CYBLE-2X20XX-X1



Top View (Seen on Host PCB)

Figure 5. Module Pad Location from Origin



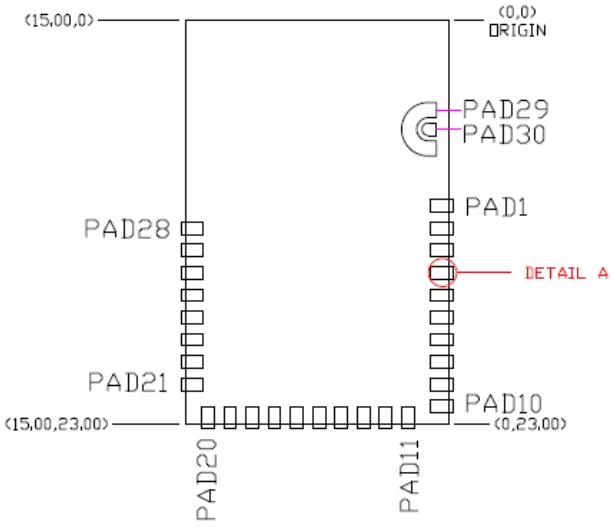
Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBLE-2X20XX-X1. All dimensions are referenced to the center of the solder pad. Refer to Figure 6 for the location of each module solder pad.

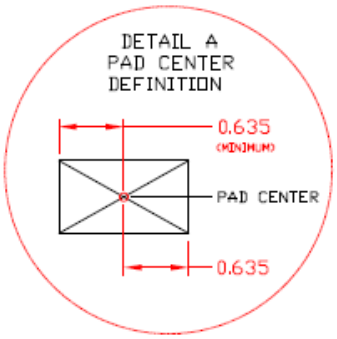
Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Orign (mm)	Dimension from Orign (mils)
1	(0.38, 10.54)	(14.96, 414.96)
2	(0.38, 11.81)	(14.96, 464.96)
3	(0.38, 13.08)	(14.96, 514.96)
4	(0.38, 14.35)	(14.96, 564.96)
5	(0.38, 15.62)	(14.96, 614.96)
6	(0.38, 16.89)	(14.96, 664.96)
7	(0.38, 18.16)	(14.96, 714.96)
8	(0.38, 19.43)	(14.96, 764.96)
9	(0.38, 20.70)	(14.96, 814.96)
10	(0.38, 21.97)	(14.96, 864.96)
11	(2.32, 22.62)	(91.34, 890.55)
12	(3.59, 22.62)	(141.34, 890.55)
13	(4.86, 22.62)	(191.34, 890.55)
14	(6.13, 22.62)	(241.34, 890.55)
15	(7.40, 22.62)	(291.34, 890.55)
16	(8.67, 22.62)	(341.34, 890.55)
17	(9.94, 22.62)	(391.34,8 90.55)
18	(11.21, 22.62)	(441.34, 890.55)
19	(12.48, 22.62)	(491.34, 890.55)
20	(13.75, 22.62)	(541.34, 890.55
21	(14.62, 20.70)	(575.59, 814.96)
22	(14.62, 19.43)	(575.59, 764.96)
23	(14.62, 18.16)	(575.59, 714.96)
24	(14.62, 16.89)	(575.59, 664.96)
25	(14.62, 15.62)	(575.59, 614.96)
26	(14.62, 14.35)	(575.59, 564.96)
27	(14.62, 13.08)	(575.59, 514.96)
28	(14.62, 11.81)	(575.59, 464.96)
29	See Figure 2	See Figure 2
30	See Figure 2	See Figure 2

Figure 6. Solder Pad Reference Location



Top View (Seen on Host PCB)



Digital and Analog Capabilities and Connections

Table 4 details the solder pad connection definitions and available functions for each connection pad. Table 4 lists the solder pads on CYBLE-2X20XX-X1, the BLE device port-pin, and denotes whether the function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

Table 4. Solder Pad Connection Definitions

Solder Pad Number	Device Port Pin	UART	SPI	I²C	TCPWM[4,5]	Cap-Sense	WCO Out	ECO Out	LCD	SWD	GPIO
1	GND	Ground Connection									
2	XRES	External Reset Hardware Connection Input									
3	P4.0[6]	✓(SCB1_RTS)	✓(SCB1_MOSI)		✓(TCPWM0_P)	✓(C_{MOD})			✓		✓
4	P3.7	✓(SCB1_CTS)			✓(TCPWM)	✓(Sensor)	✓		✓		✓
5	P3.6	✓(SCB1_RTS)			✓(TCPWM)	✓(Sensor)			✓		✓
6	P3.5	✓(SCB1_TX)		✓(SCB1_SCL)	✓(TCPWM)	✓(Sensor)			✓		✓
7	P3.4	✓(SCB1_RX)		✓(SCB1_SDA)	✓(TCPWM)	✓(Sensor)			✓		✓
8	V_{REF}	Reference Voltage Input (Optional)									
9	P2.6				✓(TCPWM)	✓(Sensor)			✓		✓
10	P2.4				✓(TCPWM)	✓(Sensor)			✓		✓
11	P2.3				✓(TCPWM)	✓(Sensor)	✓		✓		✓
12	P2.2		✓(SCB0_SS3)		✓(TCPWM)	✓(Sensor)			✓		✓
13	P2.0		✓(SCB0_SS1)		✓(TCPWM)	✓(Sensor)			✓		✓
14	P1.7	✓(SCB0_CTS)	✓(SCB0_SCLK		✓(TCPWM)	✓(Sensor)			✓		✓
15	P1.6	✓(SCB0_RTS)	✓(SCB0_SS0)		✓(TCPWM)	✓(Sensor)			✓		✓
16	P1.5	✓(SCB0_TX)	✓(SCB0_MISO)	✓(SCB0_SCL)	✓(TCPWM)	✓(Sensor)			✓		✓
17	P1.4	✓(SCB0_RX)	✓(SCB0_MOSI)	✓(SCB0_SDA)	✓(TCPWM)	✓(Sensor)			✓		✓
18	P0.7	✓(SCB0_CTS)	✓(SCB0_SCLK		✓(TCPWM)	✓(Sensor)			✓	✓(SWDCLK)	✓
19	P1.0				✓(TCPWM)	✓(Sensor)			✓		✓
20	P0.4	✓(SCB0_RX)	✓(SCB0_MOSI)	✓(SCB0_SDA)	✓(TCPWM)	✓(Sensor)		✓	✓		✓
21	P0.5	✓(SCB0_TX)	✓(SCB0_MISO)	✓(SCB0_SCL)	✓(TCPWM)	✓(Sensor)			✓		✓
22	V_{DD}	Digital Power Supply Input (1.8 to 5.5V)									
23	P0.6	✓(SCB0_RTS)	✓(SCB0_SS0)		✓(TCPWM)	✓(Sensor)			✓	✓(SWDIO)	✓
24	GND[7]	Ground Connection									
25	GND	Ground Connection									
26	GND	Ground Connection									
27	GND	Ground Connection									
28	V_{DDR}	Radio Power Supply (2V to 3.6V)									
29	GND	RF Ground Connection for use with CYBLE-202013-11 only; No Connect for CYBLE-212006-01 and CYBLE-202007-01									
30	ANT	RF Pin to External Antenna for use with CYBLE-202013-11 only; No Connect for CYBLE-212006-01 and CYBLE-202007-01									

Notes

4. TCPWM: Timer, Counter, and Pulse Width Modulator. If supported, the pad can be configured to any of these peripheral functions.
5. TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on port 4 are direct and can only be used with the specified TCPWM block and polarity specified above.
6. When using the capacitive sensing functionality, Pad 3 (P4.0) must be connected to a C_{MOD} capacitor (located off of Cypress BLE Module). The value of this capacitor is 2.2 nF and should be placed as close to the module as possible.
7. The main board needs to connect all GND connections (Pad 24/25/26/27) on the module to the common ground of the system.
8. If the I²S feature is used in the design, the I²S pins shall be dynamically routed to the appropriate available GPIO by PSoC Creator.

Power Supply Connections and Recommended External Components

Power Connections

The CYBLE-2X20XX-X1 contains two power supply connections, VDD and VDDR. The VDD connection supplies power for both digital and analog device operation. The VDDR connection supplies power for the device radio.

VDD accepts a supply range of 1.71 V to 5.5 V. VDDR accepts a supply range of 2.0 V to 3.6 V. These specifications can be found in Table 12. The maximum power supply ripple for both power connections on the module is 100 mV, as shown in Table 10.

The power supply ramp rate of VDD must be equal to or greater than that of VDDR.

Connection Options

Two connection options are available for any application:

1. Single supply: Connect VDD and VDDR to the same supply.
2. Independent supply: Power VDD and VDDR separately.

External Component Recommendation

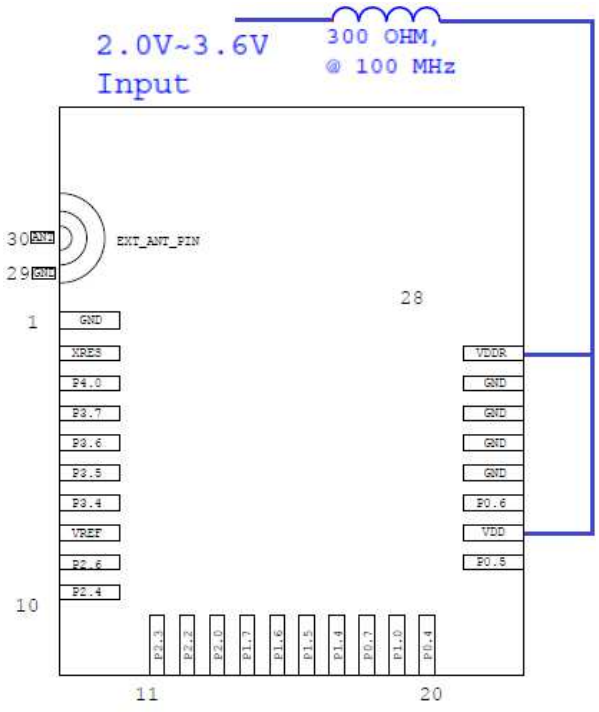
In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

Figure 7 details the recommended host schematic options for a single supply scenario. The use of one or two ferrite beads will depend on the specific application and configuration of the CYBLE-2X20XX-X1.

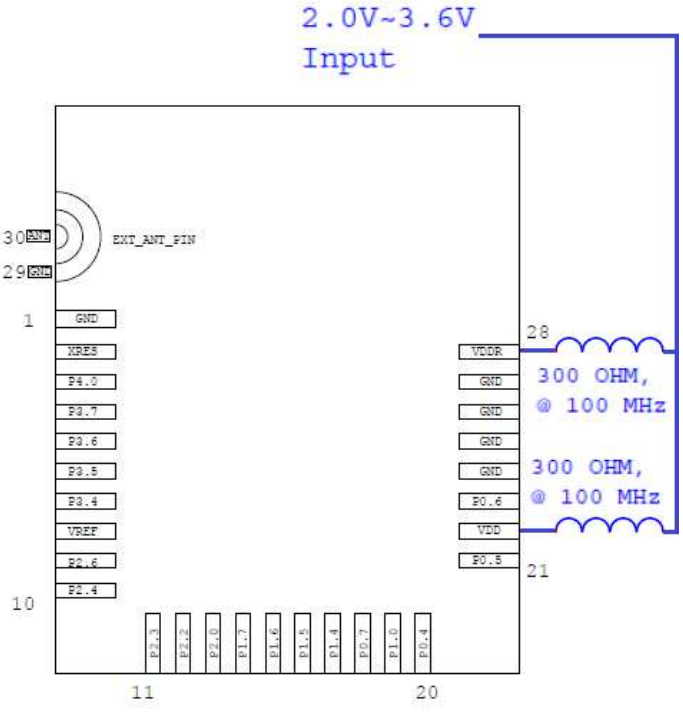
Figure 8 details the recommended host schematic for an independent supply scenario.

The recommended ferrite bead value is 330 Ω, 100 MHz. (Murata BLM21PG331SN1D).

Figure 7. Recommended Host Schematic Options for a Single Supply Option

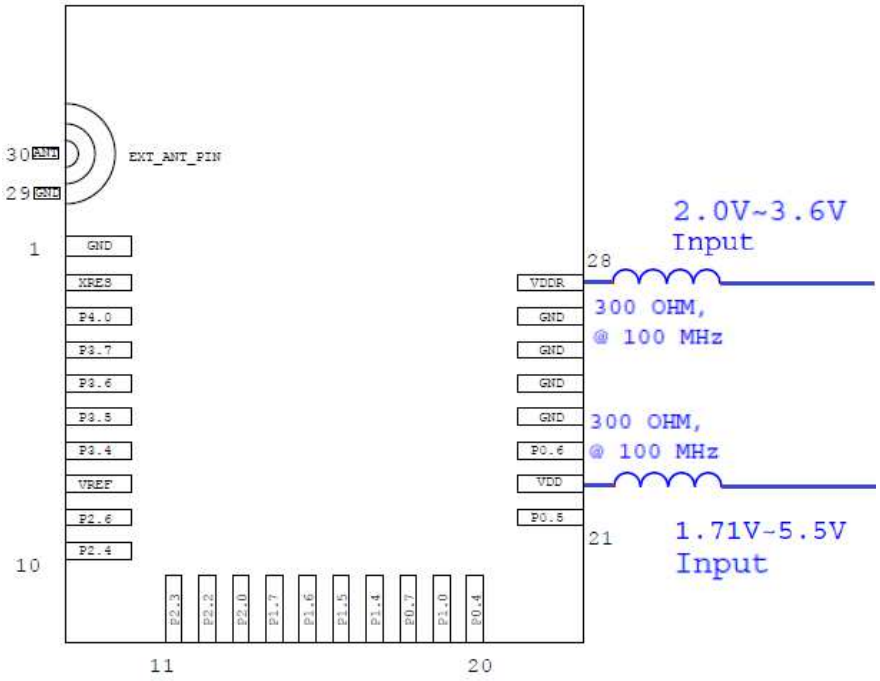


Single Ferrite Bead Option (Seen from Bottom)



Two Ferrite Bead Option (Seen from Bottom)

Figure 8. Recommended Host Schematic for an Independent Supply Option

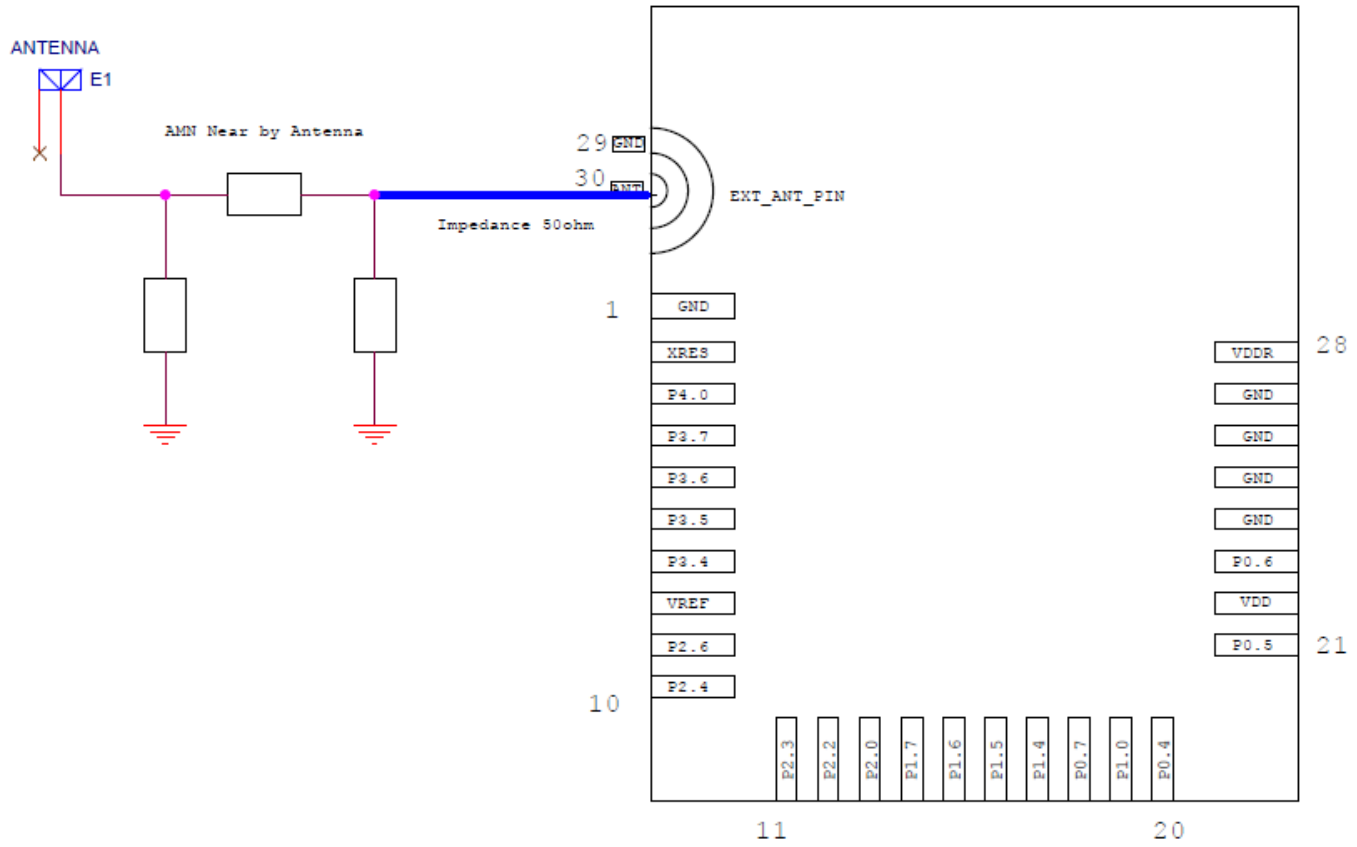


Independent Power Supply Option (Seen from Bottom)

Antenna Matching Network Requirements for CYBLE-202013-11

The CYBLE-202013-11 module requires ANT and GND connections to an external antenna via the RF pad connections on the module (Pads 29 and 30). To optimize RF performance, an Antenna Matching Network (AMN) is required to be placed between the ANT connection (Pad 29) and the antenna used in the final design. Figure 9 details the recommended Pi topology circuit footprint to use for the Antenna Matching Network.

Figure 9. Recommended Antenna Matching Network for CYBLE-202013-11 Module



Module Pad Assignments Seen from Bottom View

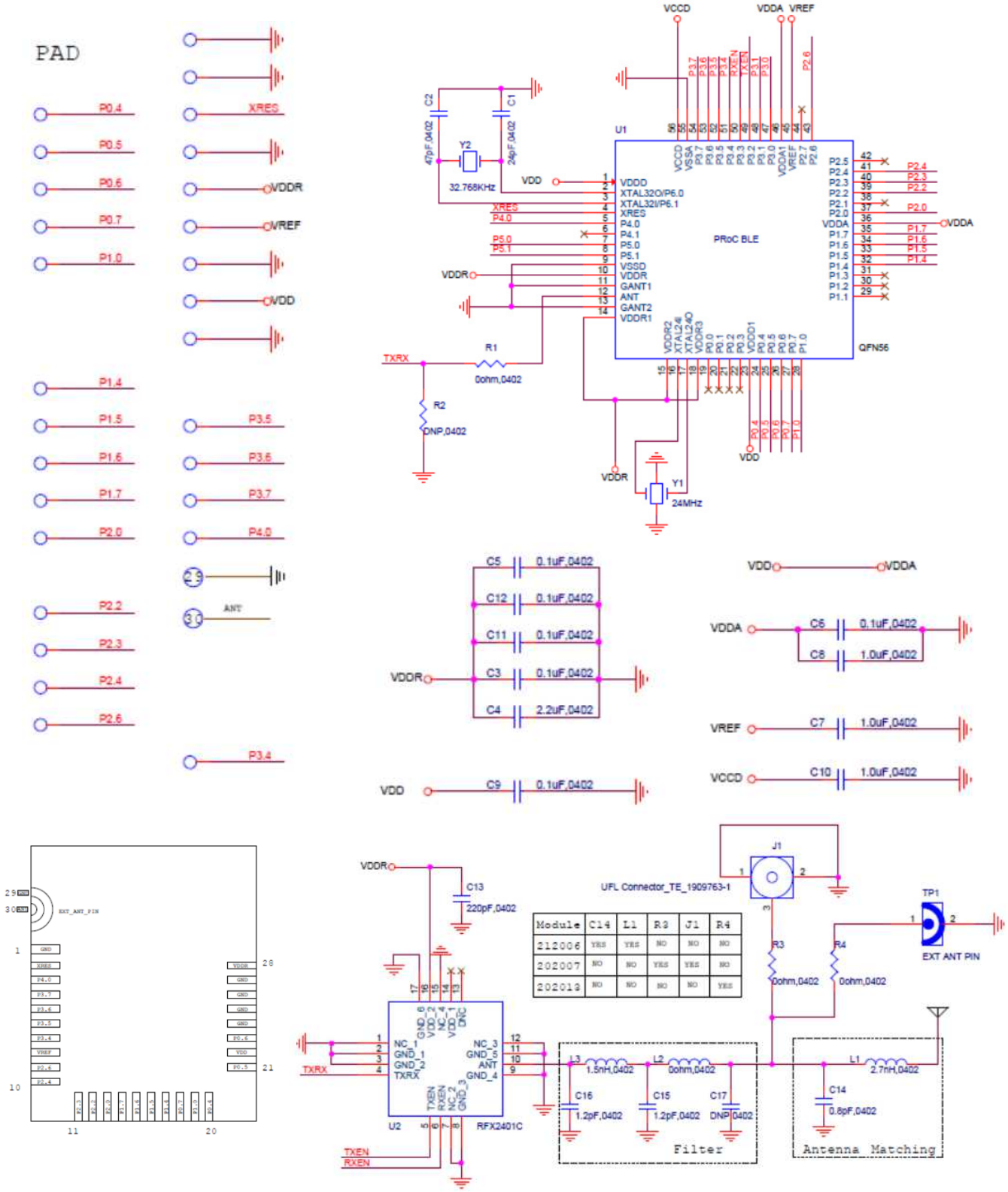
Denotes a component footprint representing either a capacitor, inductor, or 0 Ohm resistor.

The design guidelines that should be followed when completing the Antenna Matching Network are as follows:

- The AMN should be placed close to the antenna on the main board.
- Routing to the AMN from the ANT pad on the module must be controlled to an impedance of 50 Ω.
- The final AMN circuit may contain only a single component, or all three components shown above. The final number and type of components will be determined based on the actual design of the system, and the final values for each component can be determined through tuning the AMN. For details on how to properly tune an AMN, refer to the application note, AN91445.

The CYBLE-2X20XX-X1 schematic is shown in Figure 10.

Figure 10. CYBLE-2X20XX-X1 Schematic Diagram



Critical Components List

Table 5 details the critical components used in the CYBLE-2X20XX-X1 module.

Table 5. Critical Component List

Component	Reference Designator	Description
Silicon	U1	56-pin QFN Programmable Radio-on-Chip (PRoC) with BLE
Crystal	Y1	24.000 MHz, 12PF
Crystal	Y2	32.768 kHz, 12.5PF

Antenna Design

Table 6 details trace antenna used in the CYBLE-212006-01 module. For more information, see Table 11.

Table 6. Trace Antenna Specifications

Item	Description
Frequency Range	2402 – 2480 MHz
Peak Gain	-0.5 dBi typical
Return Loss	10 dB minimum

Qualified Antenna for CYBLE-202007-01 and CYBLE-202013-11

The CYBLE-202007-01 module has been designed to work with a standard 2.2 dBi dipole antenna. Any antenna of equivalent or less gain can be used without additional application and testing for FCC regulations. Table 7 details the approved antennas for the CYBLE-202007-01 module for BLE operation. These antennas may also be used for the CYBLE-202013-11 module, however all FCC and other regulatory testing will be required.

Table 7. Qualified Antenna

Manufacturer	Part Number	Gain
Antenova	B4844-01	2.2 dBi
RFlink	RF21C01228A	2.0 dBi
Pulse	W1030	2.0 dBi

Power Amplifier (PA) and Low Noise Amplifier (LNA)

Table 8 details the PA/LNA that is used on the CYBLE-2X20XX-X1 module. For more information, see Table 11.

Table 8. Power Amplifier/Low Noise Amplifier Details

Item	Description
PA/LNA Manufacturer	Skyworks Inc.
PA/LNA Part Number	RFX2401C
Power Supply Range	2.0 V to 3.6 V

Table 9 details the power consumption of the integrated PA/LNA used on the CYBLE-2X20XX-X1 module. Table 9 only details the current consumption of the RFX2401C PA/LNA. VDD= 3.3 V, TA = +25 °C, measured on the RFX2401C evaluation board, unless otherwise noted.

Table 9. Power Amplifier/Low Noise Amplifier Current Consumption Specifications

Parameter	Test Condition	Min	Typical	Max	Unit
Tx High Power Current	Pout = +20 dBm	–	90	–	mA
Tx Quiescent Current	No RF applied	–	17	–	mA
Rx Quiescent Current	No RF applied	–	8	–	mA

Enabling Extended Range Feature

The CYBLE-2X20XX-X1 modules come with an integrated Power Amplifier/Low Noise Amplifier to allow for extended communication range of up to 400 meters full line-of-sight. This section describes the firmware steps required to enable extended range operation of the CYBLE-2X20XX-X1 modules.

The Skyworks RFX2401C PA/LNA is controlled by PRoC BLE and uses two GPIOs:

1. One GPIO to control the PA enable (P3[2]). The PA enable GPIO is controlled directly by the BLE Link Layer.
2. One GPIO to control the LNA enable (P3[3]). The LNA enable GPIO is controlled directly by the BLE Link Layer.

Ensure that the PRoC BLE silicon device “Adv/Scan TX Power Level (dBm)” and “Connection TX Power Level (dBm)” in the BLE Component are both set to -12 dBm[9]

To enable the extended range functionality, follow the steps outlined below.

1. Open your project's *main.c* file and write the following code to define the register at the top of the code.

```
/* define the test register to switch the PA/LNA hardware control pins */
#define     CYREG_SRSS_TST_DDFT_CTRL    0x40030008
```

2. Locate/add the event “CYBLE_EVT_STACK_ON" in the application code and insert the following two lines of code to enable the Skyworks RFX2401C.

```
/* Mandatory events to be handled by BLE application code */
case CYBLE_EVT_STACK_ON:
  /* Configure the Link Layer to automatically switch PA control pin P3[2] and LNA control pin P3[3] */
  CY_SET_XTND_REG32((void CYFAR *)(CYREG_BLE_BLESS_RF_CONFIG), 0x0331);
  CY_SET_XTND_REG32((void CYFAR *)(CYREG_SRSS_TST_DDFT_CTRL), 0x80000302);
```

Low Power Operation

The CYBLE-2X20XX-X1 module is already optimized for low power operation when in high output power, high gain mode. The Cypress BLE Link Layer will automatically enable TX high power operation, as well as RX high gain operation. When the radio TX or RX operation is not in use (that is, Sleep), the PA/LNA will be set to shutdown mode by the BLE Link Layer. This occurs during sleep modes of the Cypress PRoC BLE silicon device.

To learn more about optimizing the Cypress PRoC BLE power consumption, refer to AN92584: Designing for Low Power and Estimating Battery Life for BLE Applications.

Note
9. The CYBLE-212006-01 module is certified for FCC, IC, CE, MIC and KC regulations at an output power of +7.5 dBm. To achieve this output power, RF_{O2} (PRoC BLE silicon PA level) must be set to the -12 dBm setting in firmware. Settings higher than this will result in higher output power than specified in the CYBLE-212006-01 certifications.

Electrical Specification

Table 10 details the absolute maximum electrical characteristics for the Cypress BLE module.

Table 10. CYBLE-2X20XX-X1 Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD_ABS}	Analog, digital, or radio supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	6	V	Absolute maximum
V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute maximum
V_{DD_RIPPLE}	Maximum power supply ripple for V_{DD} and V_{DDR} input voltage	–	–	100	mV	3.0V supply Ripple frequency of 100 kHz to 750 kHz
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} +0.5	V	Absolute maximum
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute maximum
$I_{GPIO\_injection}$	GPIO injection current: Maximum for V_{IH} > V_{DD} and minimum for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute maximum current injected per pin
LU	Pin current for latch up	–200		200	mA	–

Table 11 details the RF characteristics for the Cypress BLE module.

Table 11. CYBLE-2X20XX-X1 RF Performance Characteristics

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
RF_O	RF output power on ANT	1		7.5	dBm	Configurable via silicon register settings
RX_S	RF receive sensitivity on ANT	–	–93	–	dBm	Measured value (CYBLE-212006-01)
F_R	Module frequency range	2402	–	2480	MHz	–
G_P	Peak gain	–	–0.5	–	dBi	–
RL	Return loss	–	–10	–	dB	–

Table 12 through Table 51 list the module level electrical characteristics for the CYBLE-2X20XX-X1. All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 12. CYBLE-2X20XX-X1 DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DD1}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
V_{DD2}	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
V_{DDR1}	Radio supply voltage (radio on)	2.0	–	3.6	V	Restricted by RFX2401C
V_{DDR2}	Radio supply voltage (radio off)	2.0	–	3.6	V	–
Active Mode, V_{DD} = 1.71 V to 5.5 V						
I_{DD3}	Execute from flash; CPU at 3 MHz	–	1.7	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD4}	Execute from flash; CPU at 3 MHz	–	–	–	mA	T = –40 °C to 85 °C
I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD6}	Execute from flash; CPU at 6 MHz	–	–	–	mA	T = –40 °C to 85 °C
I_{DD7}	Execute from flash; CPU at 12 MHz	–	4	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD8}	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 85 °C

Table 12. CYBLE-2X20XX-X1 DC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
Sleep Mode, V_{DD} = 1.8 to 5.5 V						
I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, V_{DD} = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 to 5.5 V						
I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, V_{DD} = 3.3 V, SYSCLK = 3 MHz
Deep-Sleep Mode, V_{DD} = 1.8 to 3.6 V						
I_{DD15}	WDT with WCO on	–	1.5	–	µA	T = 25 °C, V_{DD} = 3.3 V
I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
I_{DD17}	WDT with WCO on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep-Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)						
I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.8 to 3.6 V						
I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3 V
I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 3.6 to 5.5 V						
I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.8 to 3.6 V						
I_{DD33}	Stop-mode current (V_{DD})	–	20	–	nA	T = 25 °C, V_{DD} = 3.3 V
I_{DD34}	Stop-mode current (V_{DDR})	–	40	–-	nA	T = 25 °C, V_{DDR} = 3.3 V
I_{DD35}	Stop-mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
I_{DD36}	Stop-mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C, V_{DDR} = 1.9 V to 3.6 V
Stop Mode, V_{DD} = 3.6 to 5.5 V						
I_{DD37}	Stop-mode current (V_{DD})	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
I_{DD38}	Stop-mode current (V_{DDR})	–	–	–	nA	T = 25 °C, V_{DDR} = 5 V
I_{DD39}	Stop-mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
I_{DD40}	Stop-mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C

Table 13. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
$T_{DEEPSLEEP}$	Wakeup from Deep-Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization
$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	2	ms	Guaranteed by characterization
T_{STOP}	Wakeup from Stop mode	–	–	2	ms	XRES wakeup

GPIO

Table 14. GPIO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}[10]	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS input
	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}	–	–	V	–
	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	–	V	–
V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS input
	LVTTL input, V_{DD} < 2.7 V	–	–	0.3 × V_{DD}	V	–
	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	–
V_{OH}	Output voltage HIGH level	V_{DD} –0.6	–	–	V	I_{OH} = 4 mA at 3.3-V V_{DD}
	Output voltage HIGH level	V_{DD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DD}
V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3.3-V V_{DD}
	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DD}
	Output voltage LOW level	–	–	0.4	V	I_{OL} = 3 mA at 3.3-V V_{DD}
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.3 V
I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
C_{IN}	Input capacitance	–	–	7	pF	–
V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DD} > 2.7 V
$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DD}	–	–	1	–
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Note
10. V_{IH} must not exceed V_{DD} + 0.2 V.

Table 15. GPIO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISEF}	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
T_{FALLF}	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
T_{RISES}	Rise time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
T_{FALLS}	Fall time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT2}$	GPIO Fout; 1.7 V≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V Slow-Strong mode	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT4}$	GPIO Fout; 1.7 V ≤ V_{DD} ≤ 3.3 V Slow-Strong mode	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
F_{GPIOIN}	GPIO input operating frequency 1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

Table 16. OVT GPIO DC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{IL}	Input leakage (absolute value). V_{IH} > V_{DD}	–	–	10	µA	25°C, V_{DD} = 0 V, V_{IH} = 3.0 V
V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 20 mA, V_{DD} > 2.9 V

Table 17. OVT GPIO AC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISE_OVFS}	Output rise time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD} = 3.3 V
T_{FALL_OVFS}	Output fall time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD} = 3.3 V
T_{RISESS}	Output rise time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V_{DD} = 3.3 V
T_{FALLSS}	Output fall time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V_{DD} = 3.3 V
$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle

XRES

Table 18. XRES DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
C_{IN}	Input capacitance	–	3	–	pF	–
$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

Table 19. XRES AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–

Temperature Sensor

Table 20. Temperature Sensor Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{SENSACC}$	Temperature-sensor accuracy	–5	±1	5	°C	–40 °C to +85 °C

SAR ADC

Table 21. SAR ADC DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_RES	Resolution	–	–	12	bits	
A_CHNIS_S	Number of channels - single-ended	–	–	6		6 full-speed[11]
A-CHNKS_D	Number of channels - differential	–	–	3		Diff inputs use neighboring I/O[11]
A-MONO	Monotonicity	–	–	–		Yes
A_GAINERR	Gain error	–	–	±0.1	%	With external reference
A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}
A_ISAR	Current consumption	–	–	1	mA	
A_VINS	Input voltage range - single-ended	V_{SS}	–	V_{DDA}	V	
A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	
A_INRES	Input resistance	–	–	2.2	kΩ	
A_INCAP	Input capacitance	–	–	10	pF	
VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of Vbg (1.024 V)

Note
11. A maximum of six single-ended ADC Channels can be accomplished only if the AMUX Buses are not being used for other funcitonality (e.g. CapSense). If the AMUX Buses are being used for other functions, then the maximum number of single-ended ADC channels is four. Similarly, if the AMUX Buses are being used for other functionality, then the maximum number of differential ADC channels is two.

Table 22. SAR ADC AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_PSRR	Power-supply rejection ratio	70	–	–	dB	Measured at 1-V reference
A_CMRR	Common-mode rejection ratio	66	–	–	dB	
A_SAMP	Sample rate	–	–	1	Msps	
Fsarintref	SAR operating speed without external ref. bypass	–	–	100	Ksps	12-bit resolution
A_SNR	Signal-to-noise ratio (SNR)	65	–	–	dB	F_{IN} = 10 kHz
A_BW	Input bandwidth without aliasing	–	–	A_SAMP/2	kHz	
A_INL	Integral nonlinearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 V to V_{DD}
A_INL	Integral nonlinearity. V_{DDD} = 1.71 V to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 V to V_{DD}
A_INL	Integral nonlinearity. V_{DD} = 1.71 V to 5.5 V, 500 Ksps	–1.5	–	1.7	LSB	V_{REF} = 1 V to V_{DD}
A_dnl	Differential nonlinearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}
A_DNL	Differential nonlinearity. V_{DD} = 1.71 V to 3.6 V, 1 Msps	–1	–	2	LSB	V_{REF} = 1.71 V to V_{DD}
A_DNL	Differential nonlinearity. V_{DD} = 1.71 V to 5.5 V, 500 Ksps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}
A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz

CSD

CSD Block Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{CSD}	Voltage range of operation	1.71	–	5.5	V	–
IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	–
IDAC1	INL for 8-bit resolution	–3	–	3	LSB	–
IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	–
IDAC2	INL for 7-bit resolution	–3	–	3	LSB	–
SNR	Ratio of counts of finger to noise	5	–	–	Ratio	Capacitance range of 9 pF to 35 pF, 0.1-pF sensitivity. Radio is not operating during the scan
I_{DAC1_CRT1}	Output current of IDAC1 (8 bits) in High range	–	612	–	µA	–
I_{DAC1_CRT2}	Output current of IDAC1 (8 bits) in Low range	–	306	–	µA	–
I_{DAC2_CRT1}	Output current of IDAC2 (7 bits) in High range	–	305	–	µA	–
I_{DAC2_CRT2}	Output current of IDAC2 (7 bits) in Low range	–	153	–	µA	–

Digital Peripherals

Timer

Table 23. Timer DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{TIM1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit timer
I_{TIM2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit timer
I_{TIM3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit timer

Table 24. Timer AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{TIMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
T_{TIMRES}	Timer resolution	T_{CLK}	–	–	ns	
$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{TENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{TIMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{TIMRESEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

Counter

Table 25. Counter DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{CTR1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit counter
I_{CTR2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit counter
I_{CTR3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit counter

Table 26. Counter AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{CTRFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
$T_{CTRPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
$T_{CTRPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
T_{CTRES}	Counter Resolution	T_{CLK}	–	–	ns	–
$T_{CENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
$T_{CENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
$T_{CTRRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
$T_{CTRRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

Pulse Width Modulation (PWM)

Table 27. PWM DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{PWM1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit PWM
I_{PWM2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit PWM
I_{PWM3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit PWM

Table 28. PWM AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{PWMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
$T_{PWMPWINT}$	Pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
T_{PWMEXT}	Pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
$T_{PWMKILLINT}$	Kill pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
$T_{PWMKILLEXT}$	Kill pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
$T_{PWMEINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
$T_{PWMENEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
$T_{PWMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
$T_{PWMRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

LCD Direct Drive

Table 29. LCD Direct Drive DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{LCDLOW}	Operating current in low-power mode	–	17.5	–	µA	16 × 4 small segment display at 50 Hz
C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
I_{LCDOP1}	LCD system operating current, V_{BIAS} = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz at 25 °C
I_{LCDOP2}	LCD system operating current, V_{BIAS} = 3.3 V	–	2	–	mA	32 × 4 segments 50 Hz at 25 °C

Table 30. LCD Direct Drive AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{LCD}	LCD frame rate	10	50	150	Hz	–

Serial Communication

Table 31. Fixed I²C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
I_{I2C2}	Block current consumption at 400 kHz	–	–	155	µA	–
I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
I_{I2C4}	I²C enabled in Deep-Sleep mode	–	–	1.4	µA	–

Table 32. Fixed I²C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{I2C1}	Bit rate	–	–	400	kHz	

Table 33. Fixed UART DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{UART1}	Block current consumption at 100 kbps	–	–	55	µA	–
I_{UART2}	Block current consumption at 1000 kbps	–	–	312	µA	–

Table 34. Fixed UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{UART}	Bit rate	–	–	1	Mbps	–

Table 35. Fixed SPI DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	–
I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	–

Table 36. Fixed SPI AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{SPI}	SPI operating frequency (master; 6x over sampling)	–	–	8	MHz	–

Table 37. Fixed SPI Master Mode AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{DMO}	MOSI valid after SCLK driving edge	–	–	18	ns	–
T_{DSI}	MISO valid before SCLK capturing edge Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 38. Fixed SPI Slave Mode AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{DMI}	MOSI valid before SCLK capturing edge	40	–	–	ns	
T_{DSO}	MISO valid after SCLK driving edge	–	–	$42 + 3 \times T_{CPU}$	ns	
T_{DSO_ext}	MISO Valid after SCLK driving edge in external clock mode. $V_{DD} < 3.0$ V	–	–	50	ns	
T_{HSO}	Previous MISO data hold time	0	–	–	ns	
$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	

Memory

Table 39. Flash DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{PE}	Erase and program voltage	1.71	–	5.5	V	–
T_{WS48}	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
T_{WS32}	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
T_{WS16}	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

Table 40. Flash AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{ROWWRITE}$[12]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
$T_{ROWERASE}$[12]	Row erase time	–	–	13	ms	–
$T_{ROWPROGRAM}$[12]	Row program time after erase	–	–	7	ms	–
$T_{BULKERASE}$[12]	Bulk erase time (256 KB)	–	–	35	ms	–
$T_{DEVPROG}$[12]	Total device program time	–	–	25	seconds	–
F_{END}	Flash endurance	100 K	–	–	cycles	–
F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	–
F_{RET2}	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	–

System Resources

Power-on-Reset (POR)

Table 41. POR DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	–
$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.40	V	–
$V_{IPORHYST}$	Hysteresis	15	–	200	mV	–

Table 42. POR AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{PPOR_TR}	Precision power-on reset (PPOR) response time in Active and Sleep modes	–	–	1	µs	–

Table 43. Brown-Out Detect

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	–
$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.4	–	–	V	–

Table 44. Hibernate Reset

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{HBRTRIP}$	BOD trip voltage in Hibernate	1.1	–	–	V	–

Note
12. It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.