Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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General Description

The Cypress CYBLE-222005-00 is a fully certified and qualified module supporting Bluetooth® Low Energy (BLE) wireless communication. The CYBLE-222005-00 is a turnkey solution and includes onboard crystal oscillators, chip antenna, passive components, and Cypress PRoC™ BLE. Refer to the CYBL1XX7X datasheet for additional details on the capabilities of the PRoC BLE device used on this module.

The CYBLE-222005-00 supports a number of peripheral functions (ADC, timers, counters, PWM) and serial communication protocols (I^{2}C, UART, SPI) through its programmable architecture. The CYBLE-222005-00 includes a royalty-free BLE stack compatible with Bluetooth 4.1 and provides up to 16 GPIOs in a small 10 × 10 × 1.80 mm package.

The CYBLE-222005-00 is a complete solution and an ideal fit for applications requiring BLE wireless connectivity.

Module Description

- Module size: 10.0 mm × 10.0 mm × 1.80 mm (with shield)
- Drop-in compatible with CYBLE-022001-00 and includes additional V$_{REF}$ input
- 256-KB flash memory, 32-KB SRAM memory
- Up to 16 GPIOs configurable as open drain high/low, pull-up/pull-down, HI-Z analog, HI-Z digital, or strong output
- Bluetooth 4.1 qualified single-mode module
  - QDID: 79920
  - Declaration ID: D029884
- Certified to FCC, IC, MIC, KC, and CE regulations
  - FCC ID: WAP2005
  - IC ID: 7922A-2005
  - MIC ID: 203-JN0495
  - KC ID: MSIP-CRM-Cyp-2005
- Industrial temperature range: –40 °C to +85 °C
- 32-bit processor (0.9 DMIPS/MHz) with single-cycle 32-bit multiply, operating at up to 48 MHz
- Watchdog timer with dedicated internal low-speed oscillator (ILO)
- Two-pin SWD for programming

Power Consumption

- TX output power: –18 dbm to +3 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution
- TX current consumption of 15.6 mA (radio only, 0 dbm)
- RX current consumption of 16.4 mA (radio only)

- Low power mode support
  - Deep Sleep: 1.3 µA with watch crystal oscillator (WCO) on
  - Hibernate: 150 nA with SRAM retention
  - Stop: 60 nA with XRES wakeup

Functional Capabilities

- Up to 15 capacitive sensors for buttons or sliders with best-in-class signal-to-noise ratio (SNR) and liquid tolerance
- 12-bit, 1-Msps SAR ADC with internal reference, sample-and-hold (S/H), and channel sequencer
- Two serial communication blocks (SCBs) supporting I^{2}C (master/slave), SPI (master/slave), or UART
- Four dedicated 16-bit timer, counter, or PWM blocks (TCPWMs)
- Programmable low voltage detect (LVD) from 1.8 V to 4.5 V
- I^{2}S master interface
- Bluetooth Low Energy protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
- Switches between Central and Peripheral roles on-the-go
- Standard Bluetooth Low Energy profiles and services for interoperability
- Custom profile and service for specific use cases

Benefits

The CYBLE-222005-00 module is provided as a turnkey solution, including all necessary hardware required to use BLE communication standards.

- Proven, qualified, and certified hardware design ready to use
- Small footprint (10 × 10 mm × 1.80 mm), perfect for space constrained applications
- Reprogrammable architecture
- Fully certified module eliminates the time needed for design, development and certification processes
- Bluetooth SIG qualified with QDID and Declaration ID (D029647)
- Flexible communication protocol support
- PSoC Creator™ provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test a BLE application

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

- Overview: EZ-BLE Module Portfolio, Module Roadmap
- EZ-BLE PRoC Product Overview
- PRoC BLE Silicon Datasheet
- Application notes: Cypress offers a number of BLE application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with EZ-BLE modules are:
  - ❑ AN96841 - Getting Started with EZ-BLE Module
  - ❑ AN94020 - Getting Started with PRoC BLE
  - ❑ AN97060 - PSoC® 4 BLE and PRoC™ BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - ❑ AN91162 - Creating a BLE Custom Profile
  - ❑ AN91184 - PSoC 4 BLE - Designing BLE Applications
  - ❑ AN92584 - Designing for Low Power and Estimating Battery Life for BLE Applications
  - ❑ AN85951 - PSoC® 4 CapSense® Design Guide
  - ❑ AN95089 - PSoC® 4/PRoC™ BLE Crystal Oscillator Selection and Tuning Techniques
  - ❑ AN91445 - Antenna Design and RF Layout Guidelines
- Technical Reference Manual (TRM):
  - ❑ PRoC® BLE Technical Reference Manual
- Knowledge Base Articles
  - ❑ KBA04069 - Pin Mapping Differences Between the EZ-BLE™ PRoC™ Evaluation Board (CYBLE-222005-EVAL) and the BLE Pioneer Kit (CY8CKIT-042-BLE)
  - ❑ KBA97095 - EZ-BLE™ Module Placement
  - ❑ KBA210559 - RF Regulatory Certifications for EZ-BLE™ PRoC™ Module CYBLE-222005-00 - KBA210559
  - ❑ KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - ❑ KBA210802 - Queries on BLE Qualification and Declaration Processes
- Development Kits:
  - ❑ CYBLE-222005-EVAL - CYBLE-222005-00 Evaluation Board
  - ❑ CY8CKIT-042-BLE - Bluetooth® Low Energy (BLE) Pioneer Kit
  - ❑ CY8CKIT-002 - PSoC® MiniProg3 Program and Debug Kit
- Test and Debug Tools:
  - ❑ CYSmart - Bluetooth® LE Test and Debug Tool (Windows)
  - ❑ CYSmart Mobile - Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)

Two Design Environments to Get You Started Quickly

PSoC® Creator™ Integrated Design Environment (IDE)

PSoC Creator is an Integrated Design Environment (IDE) that enables concurrent hardware and firmware editing, compiling and debugging of PSoC 3, PSoC 4, PSoC 5LP, PSoC 4 BLE, PRoC BLE, and EZ-BLE module systems with no code size limitations. PSoC peripherals are designed using schematic capture and simple graphical user interface (GUI) with over 120 pre-verified, production-ready PSoC Components™.

PSoC Components are analog and digital "virtual chips," represented by an icon that users can drag-and-drop into a design and configure to suit a broad array of application requirements.

Bluetooth Low Energy Component

The Bluetooth Low Energy Component inside PSoC Creator provides a comprehensive GUI-based configuration window that lets you quickly design BLE applications. The Component incorporates a Bluetooth Core Specification v4.1 compliant BLE protocol stack and provides API functions to enable user applications to interface with the underlying Bluetooth Low Energy Sub-System (BLESS) hardware via the stack.

EZ-Serial™ BLE Firmware Platform

The EZ-Serial Firmware Platform provides a simple way to access the most common hardware and communication features needed in BLE applications. EZ-Serial implements an intuitive API protocol over the UART interface and exposes various status and control signals through the module's GPIOs, making it easy to add BLE functionality quickly to existing designs.

Use a simple serial terminal and evaluation kit to begin development without requiring an IDE. Refer to the EZ-Serial webpage for User Manuals and instructions for getting started as well as detailed reference materials.

EZ-BLE modules are pre-flashed with the EZ-Serial Firmware Platform. If you do not have EZ-Serial pre-loaded on your module, you can download each EZ-BLE module's firmware images on the EZ-Serial webpage.

Technical Support

- Frequently Asked Questions (FAQs): Learn more about our BLE ECO System.
- Forum: See if your question is already answered by fellow developers on the PSoC 4 BLE and PRoC BLE forums.
- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

Contents

Overview

Module Description

The CYBLE-222005-00 module is a complete module designed to be soldered to the applications main board.

Module Dimensions and Drawing

Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will still guarantee that all height restrictions of the component area are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in Figure 1. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	10.00 ± 0.15 mm
	Width (Y)	10.00 ± 0.15 mm
Antenna location dimensions	Length (X)	7.00 ± 0.15 mm
	Width (Y)	5.00 ± 0.15 mm
PCB thickness	Height (H)	0.50 ± 0.10 mm
Shield height	Height (H)	1.10 ± 0.10 mm
Maximum component height	Height (H)	1.30 mm typical (chip antenna)
Total module thickness (bottom of module to highest component)	Height (H)	1.80 mm typical

See Figure 1 on page 5 for the mechanical reference drawing for CYBLE-222005-00.

Figure 1. Module Mechanical Drawing

ANTENNA H:1.30(TYPICAL)

SHIELD

Top View

0.50±0.10 (PCB)

TYP. 1.60 (SHIELD+PCB)

Side View

10.00±0.15
(PCB)

7.00
(ANTENNA AREA)

5.00
(ANTENNA AREA)

6.22

10.00±0.15
(PCB)

1

0.41

1.64

0.762

0.71

22

19

0.81

MODULE PAD ASSIGNMENT:

PAD1:GND
PAD2:P4.1
PAD3:P5.1
PAD4:P5.0
PAD5:VDDR
PAD6:VREF
PAD7:P1.6
PAD8:P0.7
PAD9:P0.4
PAD10:P0.5
PAD11:GND
PAD12:P0.6
PAD13:P1.7
PAD14:VDD
PAD15:XRES
PAD16:P3.5
PAD17:P3.4
PAD18:P3.7
PAD19:P1.4
PAD20:P1.5
PAD21:P3.6
PAD22:P4.0

Bottom View

Note
1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see "Recommended Host PCB Layout" on page 7.

Pad Connection Interface

As shown in the bottom view of Figure 1 on page 5, the CYBLE-222005-00 connects to the host board via solder pads on the back of the module. Table 2 and Figure 2 detail the solder pad length, width, and pitch dimensions of the CYBLE-222005-00 module.

Table 2. Solder Pad Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	22	Solder Pads	0.71 mm	0.41 mm	0.76 mm

Figure 2. Solder Pad Dimensions (Seen from Bottom)
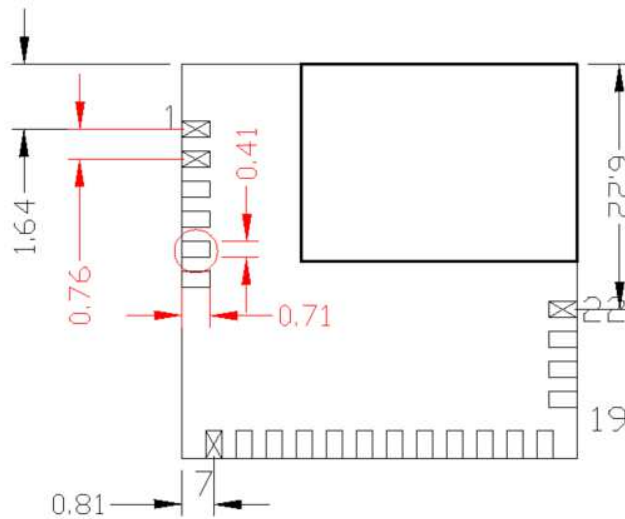
To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE module is in a corner of the host board with the chip antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2. Refer to AN96841 for module placement best practices.

2. To maximize RF performance, the area immediately around the Cypress BLE module chip antenna should contain an additional keep out area, where no grounding or signal traces are contained. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in Figure 3 (dimensions are in mm).

Figure 3. Recommended Host PCB Keep Out Area Around the CYBLE-222005-00 Chip Antenna

1. FOR BEST RF PERFORMANCE,ADDITIONAL KEEPOUT IN BLUE HATCHED AREA ON THE HOST BOARD ON ALL LAYERS.
2. RECOMMENDATION IS TO PLACE THE BLE MODULE IN THE CORNER OF THE HOST BOARD.

MODULE OUTLINE
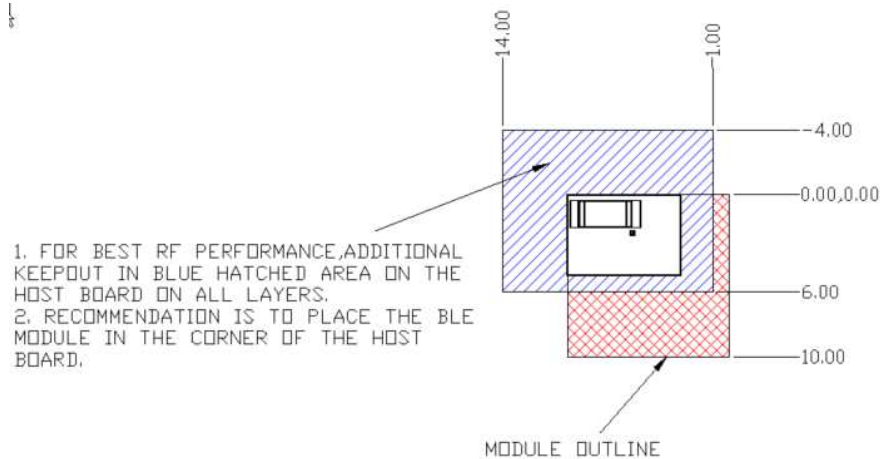
Host PCB Keep Out Area Around Chip Antenna

Recommended Host PCB Layout

Figure 4, Figure 5, Figure 6, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-222005-00. Dimensions are in millimeters unless otherwise noted. Pad length of 0.91 mm (0.455 mm from center of the pad on either side) shown in Figure 6 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 4, Figure 5, or Figure 6. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 4. Host Layout Pattern for CYBLE-222005-00
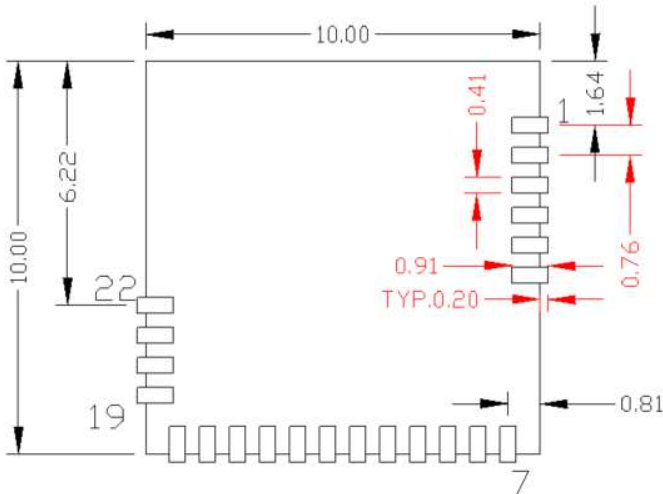
Top View (Seen on Host PCB)

Figure 5. Module Pad Location from Origin
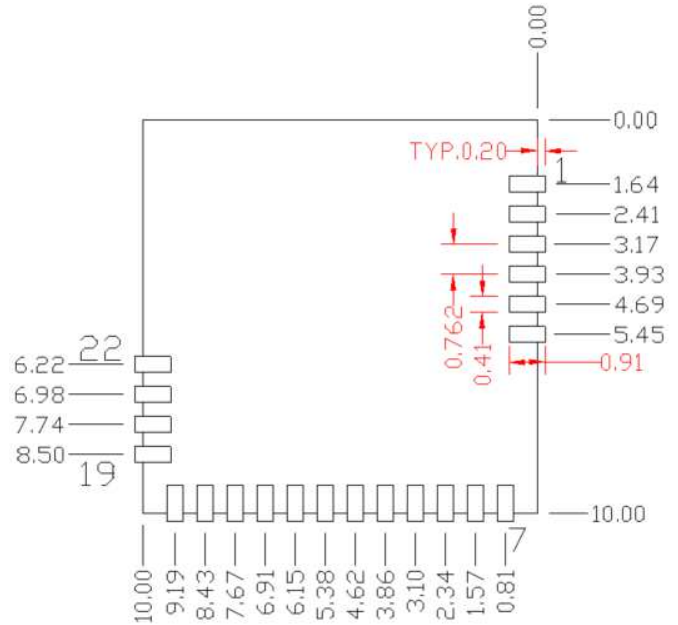
Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBLE-222005-00. All dimensions are referenced to the center of the solder pad. Refer to Figure 6 for the location of each module solder pad.

Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Orign (mm)	Dimension from Orign (mils)
1	(0.26, 1.64)	(10.24, 64.57)
2	(0.26, 2.41)	(10.24, 94.88)
3	(0.26, 3.17)	(10.24, 124.80)
4	(0.26, 3.93)	(10.24, 154.72)
5	(0.26, 4.69)	(10.24, 184.65)
6	(0.26, 5.45)	(10.24, 214.57)
7	(0.81, 9.74)	(31.89, 383.46)
8	(1.57, 9.74)	(61.81, 383.46)
9	(2.34, 9.74)	(92.13, 383.46)
10	(3.10, 9.74)	(122.05, 383.46)
11	(3.86, 9.74)	(151.97, 383.46)
12	(4.62, 9.74)	(181.89, 383.46)
13	(5.38, 9.74)	(211.81, 383.46)
14	(6.15, 9.74)	(242.13, 383.46)
15	(6.91, 9.74)	(272.05, 383.46)
16	(7.67, 9.74)	(301.97, 383.46)
17	(8.43, 9.74)	(331.89, 383.46)
18	(9.19, 9.74)	(361.81, 383.46)
19	(9.75, 8.50)	(383.86, 334.65)
20	(9.75, 7.74)	(383.86, 304.72)
21	(9.75, 6.98)	(383.86, 274.80)
22	(9.75, 6.22)	(383.86, 244.88)

Figure 6. Solder Pad Reference Location
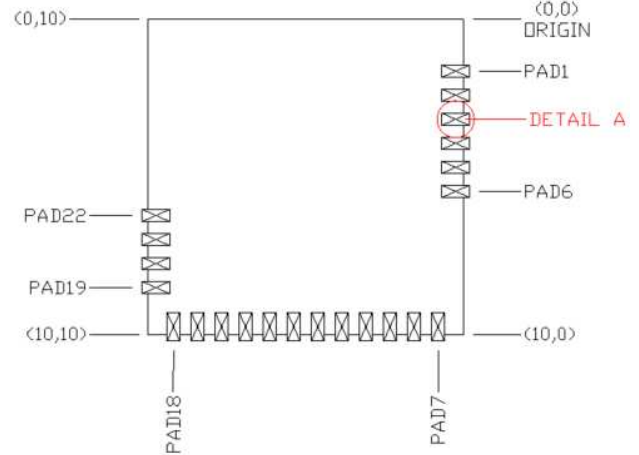
Top View (Seen on Host PCB)
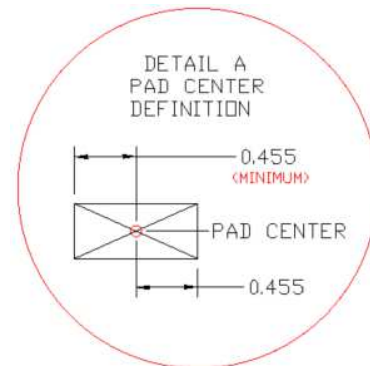
Digital and Analog Capabilities and Connections

Table 4 details the solder pad connection definitions and available functions for each connection pad. Table 4 lists the solder pads on CYBLE-222005-00, the BLE device port-pin, and denotes whether the function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

Table 4. Solder Pad Connection Definitions

Solder Pad Number	Device Port Pin	UART	SPI	I^{2}C	TCPWM[2,3]	CapSense	WCO OUT	ECO OUT	LCD	SWD	GPIO
1	GND[4]	Ground Connection									
2	P4.1[5]	✓ (SCB1_CTS)	✓ (SCB1_MISO)		✓ (TCPWM0_N)	✓ (Sensor/ C$_{TANK}$)			✓		✓
3	P5.1	✓ (SCB1_TX)	✓ (SCB1_SCLK)	✓ (SCB1_SCL)	✓ (TCPWM3_N)	✓		✓	✓		✓
4	P5.0	✓ (SCB1_RX)	✓ (SCB1_SS0)	✓ (SCB1_SDA)	✓ (TCPWM3_P)	✓			✓		✓
5	V$_{DDR}$	Radio Power Supply (1.9V to 5.5V)									
6	V$_{REF}$[6]	Voltage Reference Input (Optional)									
7	P1.6	✓ (SCB0_RTS)	✓ (SCB0_SS0)		✓ (TCPWM)	✓ (Sensor)			✓		✓
8	P0.7	✓ (SCB0_CTS)	✓ (SCB0_SCLK)		✓ (TCPWM)	✓			✓	✓ (SWDCLK)	✓
9	P0.4	✓ (SCB0_RX)	✓ (SCB0_MOSI)	✓ (SCB0_SDA)	✓ (TCPWM)	✓		✓	✓		✓
10	P0.5	✓ (SCB0_TX)	✓ (SCB0_MISO)	✓ (SCB0_SCL)	✓ (TCPWM)	✓			✓		✓
11	GND	Ground Connection									
12	P0.6	✓ (SCB0_RTS)	✓ (SCB0_SS0)		✓ (TCPWM)	✓			✓	✓ (SWDIO)	✓
13	P1.7	✓ (SCB0_CTS)	✓ (SCB0_SCLK)		✓ (TCPWM)	✓ (Sensor)			✓		✓
14	V$_{DD}$	Digital Power Supply Input (1.71 to 5.5V)									
15	XRES	External Reset Hardware Connection Input									
16	P3.5	✓ (SCB1_TX)		✓ (SCB1_SCL)	✓ (TCPWM)	✓			✓		✓
17	P3.4	✓ (SCB1_RX)		✓ (SCB1_SDA)	✓ (TCPWM)	✓			✓		✓
18	P3.7	✓ (SCB1_CTS)			✓ (TCPWM)	✓	✓		✓		✓
19	P1.4	✓ (SCB0_RX)	✓ (SCB0_MOSI)	✓ (SCB0_SDA)	✓ (TCPWM)	✓			✓		✓
20	P1.5	✓ (SCB0_TX)	✓ (SCB0_MISO)	✓ (SCB0_SCL)	✓ (TCPWM)	✓			✓		✓
21	P3.6	✓ (SCB1_RTS)			✓ (TCPWM)	✓			✓		✓
22	P4.0[7]	✓ (SCB1_RTS)	✓ (SCB1_MOSI)		✓ (TCPWM0_P)	✓ (C$_{MOD}$)			✓		✓

Notes
2. TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
3. TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.
4. The main board needs to connect both GND connections (Pad 1 and Pad 10) on the module to the common ground of the system.
5. When using the capacitive sensing functionality, Pad 2 (P4.1) can be connected to a C$_{TANK}$ capacitor (located off of Cypress BLE Module). C$_{Tank}$ should be used if implementing a shield layer on the capacitive sensor. If used, this capacitor should be placed as close to the module as possible.
6. Analog block functionality is augmented for the user with the external V$_{REF}$ input. The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor.
7. When using the capacitive sensing functionality, Pad 22 (P4.0) must be connected to a C$_{MOD}$ capacitor (located off of Cypress BLE Module). The value of this capacitor is 2.2 nF and should be placed as close to the module as possible.
8. If the I^{2}S feature is used in the design, the I^{2}S pins shall be dynamically routed to the appropriate available GPIO by PSoC Creator

Power Supply Connections and Recommended External Components

Power Connections

The CYBLE-222005-00 contains two power supply connections, VDD and VDDR. The VDD connection supplies power for both digital and analog device operation. The VDDR connection supplies power for the device radio.

VDD accepts a supply range of 1.71 V to 5.5 V. VDDR accepts a supply range of 1.9 V to 5.5 V. These specifications can be found in Table 9. The maximum power supply ripple for both power connections on the module is 100 mV, as shown in Table 7.

The power supply ramp rate of VDD must be equal to or greater than that of VDDR.

Connection Options

Two connection options are available for any application:

1. Single supply: Connect VDD and VDDR to the same supply.

2. Independent supply: Power VDD and VDDR separately.

External Component Recommendation

In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

Figure 7 details the recommended host schematic options for a single supply scenario. The use of one or two ferrite beads will depend on the specific application and configuration of the CYBLE-222005-00.

Figure 8 details the recommended host schematic for an independent supply scenario.

The recommended ferrite bead value is 330 Ω, 100 MHz. (Murata BLM21PG331SN1D).

Figure 7. Recommended Host Schematic Options for a Single Supply Option

Single Ferrite Bead Option (Seen from Bottom)

Two Ferrite Bead Option (Seen from Bottom)
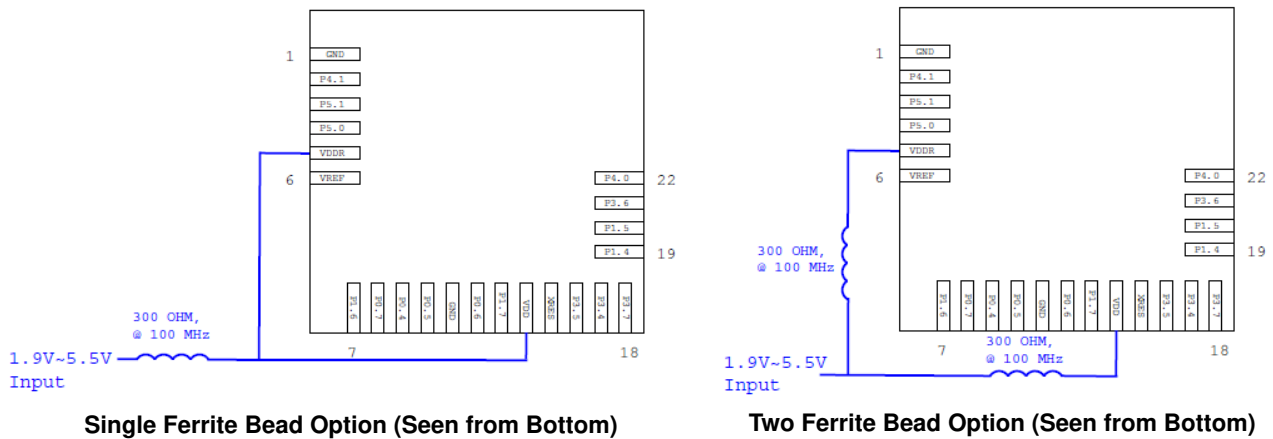
Figure 8. Recommended Host Schematic for an Independent Supply Option

Independent Power Supply Option (Seen from Bottom)
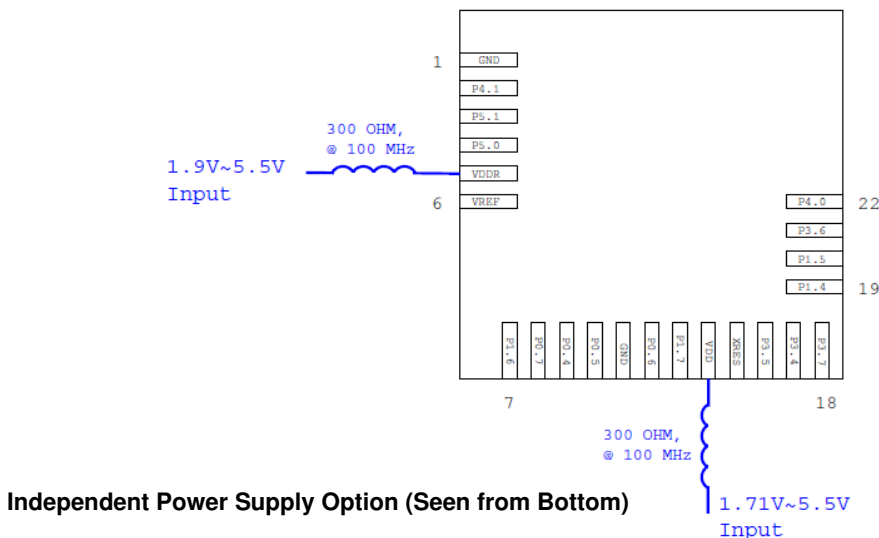
The CYBLE-222005-00 schematic is shown in Figure 9.

Figure 9. CYBLE-222005-00 Schematic Diagram
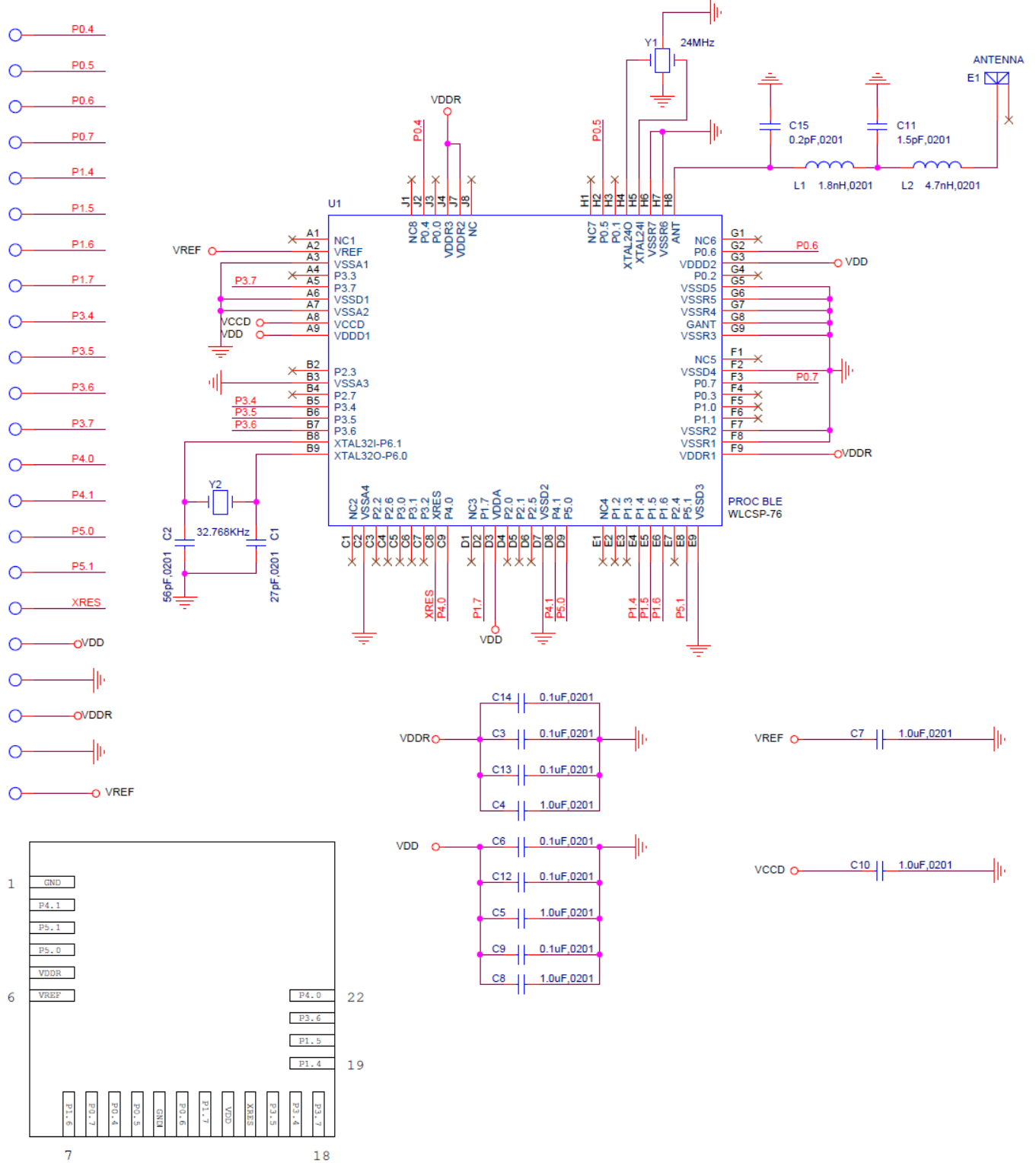
Critical Components List

Table 5 details the critical components used in the CYBLE-222005-00 module.

Table 5. Critical Component List

Component	Reference Designator	Description
Silicon	U1	76-pin WLCSP Programmable Radio-on-Chip (PRoC) with BLE
Crystal	Y1	24.000 MHz, 10PF
Crystal	Y2	32.768 kHz, 12.5PF
Antenna	E1	2.4–2.5 GHz chip antenna

Antenna Design

Table 6 details the chip antenna used in the CYBLE-222005-00 module. The specifications listed are according to the vendor's datasheet. The Cypress module performance improves many of these characteristics. For more information, see Table 8.

Table 6. Chip Antenna Specifications

Item	Description
Chip Antenna Manufacturer	Johanson Technology Inc.
Chip Antenna Part Number	2450AT18B100
Frequency Range	2400–2500 MHz
Peak Gain	0.5-dBi typical
Average Gain	–0.5-dBi typical
Return Loss	9.5-dB minimum

Electrical Specification

details the absolute maximum electrical characteristics for the Cypress BLE module.

Table 7. CYBLE-222005-00 Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD_ABS}	Analog, digital, or radio supply relative to V_{SS} ($V_{SSD} = V_{SSA}$)	−0.5	–	6	V	Absolute maximum
V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	−0.5	–	1.95	V	Absolute maximum
V_{DDD_RIPPLE}	Maximum power supply ripple for V_{DD} and V_{DDR} input voltage	–	–	100	mV	3.0V supply Ripple frequency of 100 kHz to 750 kHz
V_{GPIO_ABS}	GPIO voltage	−0.5	–	V_{DD} +0.5	V	Absolute maximum
I_{GPIO_ABS}	Maximum current per GPIO	−25	–	25	mA	Absolute maximum
$I_{GPIO\_injection}$	GPIO injection current: Maximum for $V_{IH} > V_{DD}$ and minimum for $V_{IL} < V_{SS}$	−0.5	–	0.5	mA	Absolute maximum current injected per pin
LU	Pin current for latch up	−200		200	mA	–

details the RF characteristics for the Cypress BLE module.

Table 8. CYBLE-222005-00 RF Performance Characteristics

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
RF_O	RF output power on ANT	−18	0	3	dBm	Configurable via register settings
RX_S	RF receive sensitivity on ANT	–	−87	–	dBm	Guaranteed by design simulation
F_R	Module frequency range	2400	–	2480	MHz	–
G_P	Peak gain	–	0.5	–	dBi	–
G_{Avg}	Average gain	–	−0.5	–	dBi	–
RL	Return loss	–	−10.5	–	dB	–

through list the module level electrical characteristics for the CYBLE-222005-00. All specifications are valid for −40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 9. CYBLE-222005-00 DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DD1}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
V_{DD2}	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
V_{DDR1}	Radio supply voltage (radio on)	1.9	–	5.5	V	–
V_{DDR2}	Radio supply voltage (radio off)	1.71	–	5.5	V	–
Active Mode, V_{DD} = 1.71 V to 5.5 V						
I_{DD3}	Execute from flash; CPU at 3 MHz	–	1.7	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD4}	Execute from flash; CPU at 3 MHz	–	–	–	mA	T = −40 °C to 85 °C
I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD6}	Execute from flash; CPU at 6 MHz	–	–	–	mA	T = −40 °C to 85 °C
I_{DD7}	Execute from flash; CPU at 12 MHz	–	4	–	mA	T = 25 °C, V_{DD} = 3.3 V

Table 9. CYBLE-222005-00 DC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I$_{DD8}$	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 85 °C
I$_{DD9}$	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V$_{DD}$ = 3.3 V
I$_{DD10}$	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
I$_{DD11}$	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V$_{DD}$ = 3.3 V
I$_{DD12}$	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
Sleep Mode, V$_{DD}$ = 1.8 V to 5.5 V						
I$_{DD13}$	IMO on	–	–	–	mA	T = 25 °C, V$_{DD}$ = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V$_{DD}$ and V$_{DDR}$ = 1.9 V to 5.5 V						
I$_{DD14}$	ECO on	–	–	–	mA	T = 25 °C, V$_{DD}$ = 3.3 V, SYSCLK = 3 MHz
Deep-Sleep Mode, V$_{DD}$ = 1.8 V to 3.6 V						
I$_{DD15}$	WDT with WCO on	–	1.5	–	µA	T = 25 °C, V$_{DD}$ = 3.3 V
I$_{DD16}$	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
I$_{DD17}$	WDT with WCO on	–	–	–	µA	T = 25 °C, V$_{DD}$ = 5 V
I$_{DD18}$	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep-Sleep Mode, V$_{DD}$ = 1.71 V to 1.89 V (Regulator Bypassed)						
I$_{DD19}$	WDT with WCO on	–	–	–	µA	T = 25 °C
I$_{DD20}$	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Hibernate Mode, V$_{DD}$ = 1.8 V to 3.6 V						
I$_{DD27}$	GPIO and reset active	–	150	–	nA	T = 25 °C, V$_{DD}$ = 3.3 V
I$_{DD28}$	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V$_{DD}$ = 3.6 V to 5.5 V						
I$_{DD29}$	GPIO and reset active	–	–	–	nA	T = 25 °C, V$_{DD}$ = 5 V
I$_{DD30}$	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V$_{DD}$ = 1.8 V to 3.6 V						
I$_{DD33}$	Stop-mode current (V$_{DD}$)	–	20	–	nA	T = 25 °C, V$_{DD}$ = 3.3 V
I$_{DD34}$	Stop-mode current (V$_{DDR}$)	–	40	-–	nA	T = 25 °C, V$_{DDR}$ = 3.3 V
I$_{DD35}$	Stop-mode current (V$_{DD}$)	–	–	–	nA	T = –40 °C to 85 °C
I$_{DD36}$	Stop-mode current (V$_{DDR}$)	–	–	–	nA	T = –40 °C to 85 °C, V$_{DDR}$ = 1.9 V to 3.6 V
Stop Mode, V$_{DD}$ = 3.6 V to 5.5 V						
I$_{DD37}$	Stop-mode current (V$_{DD}$)	–	–	–	nA	T = 25 °C, V$_{DD}$ = 5 V
I$_{DD38}$	Stop-mode current (V$_{DDR}$)	–	–	–	nA	T = 25 °C, V$_{DDR}$ = 5 V
I$_{DD39}$	Stop-mode current (V$_{DD}$)	–	–	–	nA	T = –40 °C to 85 °C
I$_{DD40}$	Stop-mode current (V$_{DDR}$)	–	–	–	nA	T = –40 °C to 85 °C

Table 10. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71\ V \leq V_{DD} \leq 5.5\ V$
T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
$T_{DEEPSLEEP}$	Wakeup from Deep-Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization
$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	2	ms	Guaranteed by characterization
T_{STOP}	Wakeup from Stop mode	–	–	2	ms	XRES wakeup

GPIO

Table 11. GPIO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}[9]	Input voltage HIGH threshold	$0.7 \times V_{DD}$	–	–	V	CMOS input
	LVTTL input, $V_{DD} < 2.7\ V$	$0.7 \times V_{DD}$	–	–	V	–
	LVTTL input, $V_{DD} \geq 2.7\ V$	2.0	–	–	V	–
V_{IL}	Input voltage LOW threshold	–	–	$0.3 \times V_{DD}$	V	CMOS input
	LVTTL input, $V_{DD} < 2.7\ V$	–	–	$0.3 \times V_{DD}$	V	–
	LVTTL input, $V_{DD} \geq 2.7\ V$	–	–	0.8	V	–
V_{OH}	Output voltage HIGH level	$V_{DD} - 0.6$	–	–	V	I_{OH} = 4 mA at 3.3-V V_{DD}
	Output voltage HIGH level	$V_{DD} - 0.5$	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DD}
V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3.3-V V_{DD}
	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DD}
	Output voltage LOW level	–	–	0.4	V	I_{OL} = 3 mA at 3.3-V V_{DD}
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.3 V
I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
C_{IN}	Input capacitance	–	–	7	pF	–
V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DD} > 2.7 V
$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–	1	–
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Note
9. V_{IH} must not exceed V_{DD} + 0.2 V.

Table 12. GPIO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISEF}	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
T_{FALLF}	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
T_{RISES}	Rise time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
T_{FALLS}	Fall time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT2}$	GPIO Fout; 1.7 V≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V Slow-Strong mode	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT4}$	GPIO Fout; 1.7 V ≤ V_{DD} ≤ 3.3 V Slow-Strong mode	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
F_{GPIOIN}	GPIO input operating frequency 1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

Table 13. OVT GPIO DC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{IL}	Input leakage (absolute value). V_{IH} > V_{DD}	–	–	10	µA	25°C, V_{DD} = 0 V, V_{IH} = 3.0 V
V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 20 mA, V_{DD} > 2.9 V

Table 14. OVT GPIO AC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISE_OVFS}	Output rise time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
T_{FALL_OVFS}	Output fall time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
T_{RISESS}	Output rise time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V_{DD} = 3.3 V
T_{FALLSS}	Output fall time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V_{DD} = 3.3 V
$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle

XRES

Table 15. XRES DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
C_{IN}	Input capacitance	–	3	–	pF	–
$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

Table 16. XRES AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–

SAR ADC

Table 17. SAR ADC DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_RES	Resolution	–	–	12	bits	
A_CHNIS_S	Number of channels - single-ended	–	–	6		6 full-speed[10]
A-CHNKS_D	Number of channels - differential	–	–	3		Diff inputs use neighboring I/O[10]
A-MONO	Monotonicity	–	–	–		Yes
A_GAINERR	Gain error	–	–	±0.1	%	With external reference
A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}
A_ISAR	Current consumption	–	–	1	mA	
A_VINS	Input voltage range - single-ended	V_{SS}	–	V_{DDA}	V	
A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	
A_INRES	Input resistance	–	–	2.2	kΩ	
A_INCAP	Input capacitance	–	–	10	pF	
VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of Vbg (1.024 V)

Table 18. SAR ADC AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_PSRR	Power-supply rejection ratio	70	–	–	dB	Measured at 1-V reference
A_CMRR	Common-mode rejection ratio	66	–	–	dB	
A_SAMP	Sample rate	–	–	1	Msps	
Fsarintref	SAR operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution
A_SNR	Signal-to-noise ratio (SNR)	65	–	–	dB	F_{IN} = 10 kHz
A_BW	Input bandwidth without aliasing	–	–	A_SAMP/2	kHz	
A_INL	Integral nonlinearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 V to V_{DD}
A_INL	Integral nonlinearity. V_{DDD} = 1.71 V to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 V to V_{DD}
A_INL	Integral nonlinearity. V_{DD} = 1.71 V to 5.5 V, 500 ksps	–1.5	–	1.7	LSB	V_{REF} = 1 V to V_{DD}
A_dnl	Differential nonlinearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}

Note

10. A maximum of six single-ended ADC Channels can be accomplished only if the AMUX Buses are not being used for other funcitonality (e.g. CapSense). If the AMUX Buses are being used for other functionality, then the maximum number of single-ended ADC channels is four. Similarly, if the AMUX Buses are being used for other functonalty, then the maximum number of differential ADC channels is two.

Table 18. SAR ADC AC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_DNL	Differential nonlinearity. V_{DD} = 1.71 V to 3.6 V, 1 Msps	–1	–	2	LSB	V_{REF} = 1.71 V to V_{DD}
A_DNL	Differential nonlinearity. V_{DD} = 1.71 V to 5.5 V, 500 ksps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}
A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz

CSD

CSD Block Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{CSD}	Voltage range of operation	1.71	–	5.5	V	
IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SNR	Ratio of counts of finger to noise	5	–	–	Ratio	Capacitance range of 9 pF to 35 pF, 0.1-pF sensitivity. Radio is not operating during the scan
I_{DAC1_CRT1}	Output current of IDAC1 (8 bits) in High range	–	612	–	µA	
I_{DAC1_CRT2}	Output current of IDAC1 (8 bits) in Low range	–	306	–	µA	
I_{DAC2_CRT1}	Output current of IDAC2 (7 bits) in High range	–	305	–	µA	
I_{DAC2_CRT2}	Output current of IDAC2 (7 bits) in Low range	–	153	–	µA	

Digital Peripherals

Timer

Table 19. Timer DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{TIM1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit timer
I_{TIM2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit timer
I_{TIM3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit timer

Table 20. Timer AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{TIMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
T_{TIMRES}	Timer resolution	T_{CLK}	–	–	ns	
$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{TENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{TIMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{TIMRESEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

Counter

Table 21. Counter DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{CTR1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit counter
I_{CTR2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit counter
I_{CTR3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit counter

Table 22. Counter AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{CTRFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
$T_{CTRPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
T_{CTRES}	Counter Resolution	T_{CLK}	–	–	ns	
$T_{CENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

Pulse Width Modulation (PWM)

Table 23. PWM DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{PWM1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit PWM
I_{PWM2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit PWM
I_{PWM3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit PWM

Table 24. PWM AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{PWMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
$T_{PWMPWINT}$	Pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
T_{PWMEXT}	Pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMKILLINT}$	Kill pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMKILLEXT}$	Kill pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMEINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMENEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

LCD Direct Drive

Table 25. LCD Direct Drive DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID228	I_{LCDLOW}	Operating current in low-power mode	–	17.5	–	µA	16 × 4 small segment display at 50 Hz
SID229	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	
SID230	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	
SID231	I_{LCDOP1}	LCD system operating current V_{BIAS} = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz at 25 °C
SID232	I_{LCDOP2}	LCD system operating current V_{BIAS} = 3.3 V	–	2	–	mA	32 × 4 segments 50 Hz at 25 °C

Table 26. LCD Direct Drive AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID233	F_{LCD}	LCD frame rate	10	50	150	Hz	

Serial Communication

Table 27. Fixed I^{2}C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
I_{I2C2}	Block current consumption at 400 kHz	–	–	155	µA	–
I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
I_{I2C4}	I^{2}C enabled in Deep-Sleep mode	–	–	1.4	µA	–

Table 28. Fixed I^{2}C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{I2C1}	Bit rate	–	–	400	kHz	

Table 29. Fixed UART DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{UART1}	Block current consumption at 100 kbps	–	–	55	µA	–
I_{UART2}	Block current consumption at 1000 kbps	–	–	312	µA	–

Table 30. Fixed UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{UART}	Bit rate	–	–	1	Mbps	–

Table 31. Fixed SPI DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	–
I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	–

Table 32. Fixed SPI AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{SPI}	SPI operating frequency (master; 6x over sampling)	–	–	8	MHz	–

Table 33. Fixed SPI Master Mode AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{DMO}	MOSI valid after SCLK driving edge	–	–	18	ns	–
T_{DSI}	MISO valid before SCLK capturing edge Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 34. Fixed SPI Slave Mode AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{DMI}	MOSI valid before SCLK capturing edge	40	–	–	ns	
T_{DSO}	MISO valid after SCLK driving edge	–	–	$42 + 3 \times T_{CPU}$	ns	
T_{DSO_ext}	MISO Valid after SCLK driving edge in external clock mode. $V_{DD} < 3.0$ V	–	–	50	ns	
T_{HSO}	Previous MISO data hold time	0	–	–	ns	
$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	

Memory

Table 35. Flash DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{PE}	Erase and program voltage	1.71	–	5.5	V	–
T_{WS48}	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
T_{WS32}	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
T_{WS16}	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

Table 36. Flash AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{ROWWRITE}$[11]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
$T_{ROWERASE}$[11]	Row erase time	–	–	13	ms	–
$T_{ROWPROGRAM}$[11]	Row program time after erase	–	–	7	ms	–
$T_{BULKERASE}$[11]	Bulk erase time (256 KB)	–	–	35	ms	–
$T_{DEVPROG}$[11]	Total device program time	–	–	25	seconds	–
F_{END}	Flash endurance	100 K	–	–	cycles	–
F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	–
F_{RET2}	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	–

System Resources

Power-on-Reset (POR)

Table 37. POR DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V$_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	–
V$_{FALLIPOR}$	Falling trip voltage	0.75	–	1.40	V	–
V$_{IPORHYST}$	Hysteresis	15	–	200	mV	–

Table 38. POR AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T$_{PPOR\_TR}$	Precision power-on reset (PPOR) response time in Active and Sleep modes	–	–	1	µs	–

Table 39. Brown-Out Detect

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V$_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	–
V$_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.4	–	–	V	–

Table 40. Hibernate Reset

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V$_{HBRTRIP}$	BOD trip voltage in Hibernate	1.1	–	–	V	–

Voltage Monitors (LVD)

Table 41. Voltage Monitor DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V$_{LVI1}$	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
V$_{LVI2}$	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
V$_{LVI3}$	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
V$_{LVI4}$	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
V$_{LVI5}$	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
V$_{LVI6}$	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
V$_{LVI7}$	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
V$_{LVI8}$	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
V$_{LVI9}$	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
V$_{LVI10}$	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
V$_{LVI11}$	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
V$_{LVI12}$	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
V$_{LVI13}$	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
V$_{LVI14}$	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
V$_{LVI15}$	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
V$_{LVI16}$	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
LVI_IDD	Block current	–	–	100	µA	–

Note
11. It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

Table 42. Voltage Monitor AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T$_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	–

SWD Interface

Table 43. SWD Interface Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_SWDCLK1	3.3 V ≤ V$_{DD}$ ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
F_SWDCLK2	1.71 V ≤ V$_{DD}$ ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

Internal Main Oscillator

Table 44. IMO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I$_{IMO1}$	IMO operating current at 48 MHz	–	–	1000	µA	–
I$_{IMO2}$	IMO operating current at 24 MHz	–	–	325	µA	–
I$_{IMO3}$	IMO operating current at 12 MHz	–	–	225	µA	–
I$_{IMO4}$	IMO operating current at 6 MHz	–	–	180	µA	–
I$_{IMO5}$	IMO operating current at 3 MHz	–	–	150	µA	–

Table 45. IMO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F$_{IMOTOL3}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
F$_{IMOTOL3}$	IMO startup time	–	12	–	µs	–

Internal Low-Speed Oscillator

Table 46. ILO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I$_{ILO2}$	ILO operating current at 32 kHz	–	0.3	1.05	µA	–

Table 47. ILO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T$_{STARTILO1}$	ILO startup time	–	–	2	ms	–
F$_{ILOTRIM1}$	32-kHz trimmed frequency	15	32	50	kHz	–

Table 48. Recommended ECO Trim Value

Parameter	Description	Value	Details/Conditions
ECO$_{TRIM}$	24-MHz trim value (firmware configuration)	0x0000A0A0	Recommended trim value that needs to be loaded to register CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG

BLE Subsystem

Table 49. BLE Subsystem

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
RF Receiver Specification						
RXS, IDLE	RX sensitivity with idle transmitter	–	–89	–	dBm	
	RX sensitivity with idle transmitter excluding Balun loss	–	–91	–	dBm	Guaranteed by design simulation
RXS, DIRTY	RX sensitivity with dirty transmitter	–	–87	–70	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
RXS, HIGHGAIN	RX sensitivity in high-gain mode with idle transmitter	–	–91	–	dBm	
PRXMAX	Maximum input power	–10	–1	–	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
CI1	Cochannel interference, Wanted signal at –67 dBm and Interferer at FRX	–	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI2	Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±1 MHz	–	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI3	Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±2 MHz	–	–29	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI4	Adjacent channel interference Wanted signal at –67 dBm and Interferer at ≥FRX ±3 MHz	–	–39	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI5	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (F_{IMAGE})	–	–20	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI3	Adjacent channel interference Wanted signal at –67 dBm and Interferer at Image frequency (F_{IMAGE} ± 1 MHz)	–	–30	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
OBB1	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 30–2000 MHz	–30	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
OBB2	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2003–2399 MHz	–35	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
OBB3	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2484–2997 MHz	–35	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
OBB4	Out-of-band blocking, Wanted signal a –67 dBm and Interferer at F = 3000–12750 MHz	–30	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
IMD	Intermodulation performance Wanted signal at –64 dBm and 1-Mbps BLE, third, fourth, and fifth offset channel	–50	–	–	dBm	RF-PHY Specification (RCV-LE/CA/05/C)
RXSE1	Receiver spurious emission 30 MHz to 1.0 GHz	–	–	–57	dBm	100-kHz measurement bandwidth ETSI EN300 328 V1.8.1