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CYBLE-224110-00

EZ-BLE™ PSoC® XT/XR Module

General Description

The Cypress CYBLE-224110-00 is a fully certified and qualified module supporting Bluetooth® Low Energy (BLE) wireless communication. The CYBLE-224110-00 is a turnkey solution that includes onboard power amplifier (PA), low noise amplifier (LNA), crystal oscillators, chip antenna, passive components, and the Cypress PSoC® 4 BLE. Refer to the PSoC® 4 BLE datasheet for additional details on the capabilities of the PSoC® 4 BLE device used on this module.

The EZ-BLE™ PSoC® XT/XR module provides extended industrial temperature operation (XT) as well as extended communication range (XR). The EZ-BLE XT/XR module is a scalable and reconfigurable platform architecture, combining programmable and reconfigurable analog and digital blocks with flexible automatic routing. The CYBLE-224110-00 also includes digital programmable logic, high-performance analog-to-digital conversion (ADC), opamps with comparator mode, and standard communication and timing peripherals. The CYBLE-224110-00 includes a royalty-free BLE stack compatible with Bluetooth 4.1.

Module Description

- Module size: 9.5 mm × 15.4 mm × 1.80 mm (with shield)
- Extended range:
  - Up to 400 meters bidirectional communication[1,2]
  - Up to 450 meters in beacon-only mode[1]
- Extended industrial temperature range: –40 °C to +105 °C
- Up to 25 GPIOs
- 256-KB flash memory, 32-KB SRAM memory
- Bluetooth 4.1 qualified single-mode module
  - QDID: 82951
  - Declaration ID: D030799
- Certified to FCC, CE, MIC, KC, and IC regulations
- 32-bit processor (0.9 DMIPS/MHz), operating at up to 48 MHz
- Watchdog timer with dedicated internal low-speed oscillator
- Two-pin SWD for programming

Power Consumption

- TX output power: –18 dbm to +9.5 dbm
- RX Receive Sensitivity: –95 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution
- 1-second connection interval with PA/LNA active: 26.3 µA
- TX current consumption:
  - BLE silicon: 15.6 mA (radio only, 0 dbm)
  - SE2438T: 20 mA (PA/LNA only, +9.5 dBm)
- RX current consumption of 16.4 mA (radio only)
  - BLE silicon: 16.4 mA (radio only)
  - SE2438T: 5.5 mA (PA/LNA only)
- Low power mode support
  - Deep Sleep: 1.3 µA with watch crystal oscillator (WCO) on
  - Hibernate: 150 nA with SRAM retention
  - Stop: 60 nA with XRES wakeup

Integrated PA/LNA

- Supports output power of +9.5 dBm and RX_S of –95 dBm

Programmable Analog

- Four opamps with reconfigurable high-drive external and high-bandwidth internal drive, comparator modes, and ADC input buffering capability; can operate in Deep-Sleep mode
- 12-bit, 1-Msps SAR ADC with differential and single-ended modes; channel sequencer with signal averaging
- Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
- One low-power comparator that operates in Deep-Sleep mode

Programmable Digital

- Four programmable logic blocks called universal digital blocks, (UDBs), each with eight macrocells and datapath
- Cypress-provided peripheral Component library, user-defined state machines, and Verilog input

Capacitive Sensing

- Cypress CapSense Sigma-Delta (CSD) provides best-in-class SNR (> 5:1) and liquid tolerance

Segment LCD Drive

- LCD drive supported on all GPIOs (common or segment)
- Operates in Deep-Sleep mode with four bits per pin memory

Serial Communication

- Two independent runtime reconfigurable serial communication blocks (SCBs) with I^2C, SPI, or UART functionality

Timing and Pulse-Width Modulation

- Four 16-bit timer, counter, pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes

Up to 25 Programmable GPIOs

- Any GPIO pin can be CapSense, LCD, analog, or digital
- Two overvoltage-tolerant (OVT) pins; drive modes, strengths, and slew rates are programmable

Notes
1. Connection range tested module-to-module in full line-of-sight environment, free of obstacles or interferance sources with output power of +9.5 dBm.
2. Specified as EZ-BLE XT/XR module to module range. Mobile phone connection will decrease based on the PA/LNA performance of the mobile phone used.

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

- Overview: EZ-BLE Module Portfolio, Module Roadmap
- EZ-BLE PSoC Product Overview
- PSoC 4 BLE Silicon Datasheet
- Application notes: Cypress offers a number of BLE application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with EZ-BLE modules are:
  - AN96841 - Getting Started with EZ-BLE Module
  - AN94020 - Getting Started with PSoC® 4 BLE
  - AN97060 - PSoC® 4 BLE and PRoC™ BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91162 - Creating a BLE Custom Profile
  - AN91184 - PSoC 4 BLE - Designing BLE Applications
  - AN92584 - Designing for Low Power and Estimating Battery Life for BLE Applications
  - AN85951 - PSoC® 4 CapSense® Design Guide
  - AN95089 - PSoC® 4/PRoC™ BLE Crystal Oscillator Selection and Tuning Techniques
  - AN91445 - Antenna Design and RF Layout Guidelines
- Technical Reference Manual (TRM):
  - PSoC® 4 BLE Technical Reference Manual
  - PSOC(R) 4 BLE Registers Technical Reference Manual
- Knowledge Base Article
  - KBA212334 - Pin Mapping Differences Between the EZ-BLE™ PSoC™ Evaluation Board (CY-BLE-224110-EVAL) and the BLE Pioneer Kit (CY8CKIT-042-BLE)
  - KBA97095 - EZ-BLE™ Module Placement
  - KBA213260 - RF Regulatory Certifications for CY-BLE-224110-00 and CYBLE-224116-01 EZ-BLE™ PSoC® XT/XR Modules
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
- Development Kits:
  - CYBLE-224110-EVAL, CYBLE-224110-00 Evaluation Board
  - CY8CKIT-042-BLE, Bluetooth® Low Energy (BLE) Pioneer Kit
  - CY8CKIT-002, PSoC® MiniProg3 Program and Debug Kit
- Test and Debug Tools:
  - CYSmart, Bluetooth® LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)

Two Design Environments to Get You Started Quickly

PSoC® Creator™ Integrated Design Environment (IDE)

PSoC Creator is an Integrated Design Environment (IDE) that enables concurrent hardware and firmware editing, compiling, and debugging of PSoC 3, PSoC 4, PSoC 5LP, PSoC 4 BLE, PRoC BLE, and EZ-BLE module systems with no code size limitations. PSoC peripherals are designed using schematic capture and simple graphical user interface (GUI) with over 120 pre-verified, production-ready PSoC Components™.

PSoC Components are analog and digital “virtual chips,” represented by an icon that users can drag-and-drop into a design and configure to suit a broad array of application requirements.

Bluetooth Low Energy Component:

The Bluetooth Low Energy Component inside PSoC Creator provides a comprehensive GUI-based configuration window that lets you quickly design BLE applications. The Component incorporates a Bluetooth Core Specification v4.1 compliant BLE protocol stack and provides API functions to enable user applications to interface with the underlying Bluetooth Low Energy Sub-System (BLESS) hardware via the stack.

EZ-Serial™ BLE Firmware Platform

The EZ-Serial Firmware Platform provides a simple way to access the most common hardware and communication features needed in BLE applications. EZ-Serial implements an intuitive API protocol over the UART interface and exposes various status and control signals through the module’s GPIOs, making it easy to add BLE functionality quickly to existing designs.

Use a simple serial terminal and evaluation kit to begin development without requiring an IDE. Refer to the EZ-Serial webpage for User Manuals and instructions for getting started as well as detailed reference materials. EZ-BLE modules are pre-flashed with the EZ-Serial Firmware Platform. If EZ-Serial is not pre-loaded on your module, you can download each EZ-BLE module’s firmware images on the EZ-Serial webpage.

Technical Support

- Frequently Asked Questions (FAQs): Learn more about our BLE ECO System.
- Forum: See if your question is already answered by fellow developers on the PSoC 4 BLE and PRoC BLE forums.

Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

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Overview

Module Description

The CYBLE-224110-00 is an integrated wireless module designed to be soldered to the main host board.

Module Dimensions and Drawing

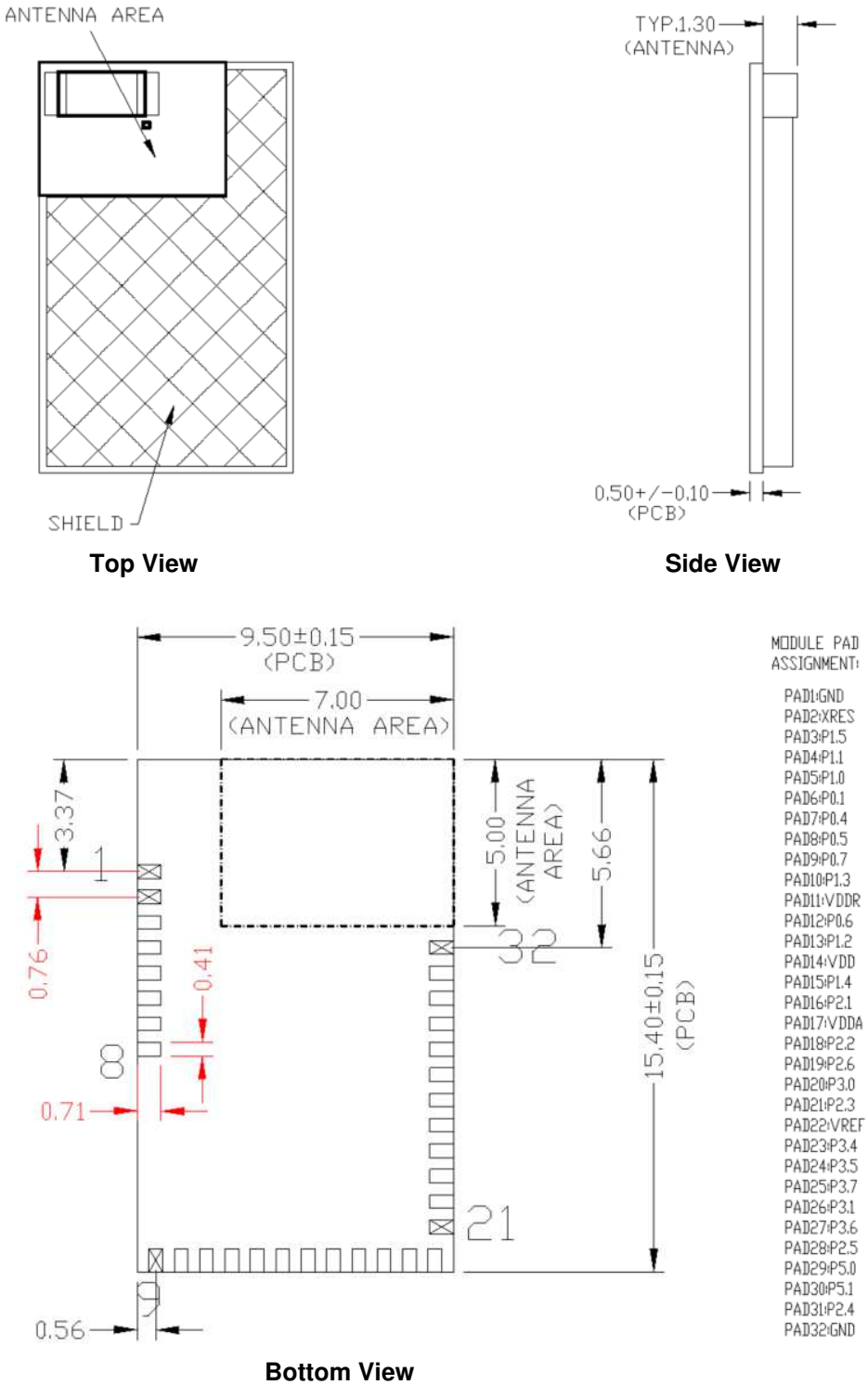
Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will guarantee that all height restrictions of the component area are maintained. Designs should be completed with the physical dimensions shown in the mechanical drawings in Figure 1. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	9.50 ± 0.15 mm
	Width (Y)	15.40 ± 0.15 mm
Antenna location dimensions	Length (X)	7.00 mm
	Width (Y)	5.00 mm
PCB thickness	Height (H)	0.50 ± 0.10 mm
Shield height	Height (H)	1.10 ± 0.10 mm
Maximum component height	Height (H)	1.30 mm typical (chip antenna)
Total module thickness (bottom of module to highest component)	Height (H)	1.80 mm typical

See Figure 1 on page 5 for the mechanical reference drawing for CYBLE-224110-00.

Figure 1. Module Mechanical Drawing



Top View **Side View**

Bottom View

Note

3. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see Figure 3, Figure 4, Figure 5, and Figure 6 and Table 3.

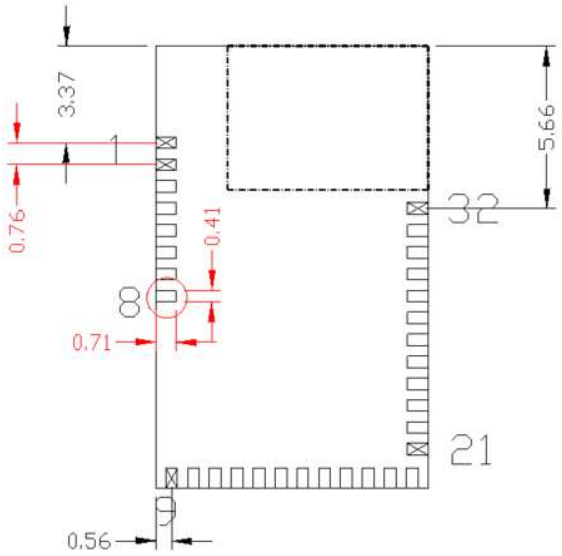
Pad Connection Interface

As shown in the bottom view of Figure 1 on page 5, the CYBLE-224110-00 connects to the host board via solder pads on the back of the module. Table 2 and Figure 2 detail the solder pad length, width, and pitch dimensions of the CYBLE-224110-00 module.

Table 2. Solder Pad Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	32	Solder Pads	0.71 mm	0.41 mm	0.76 mm

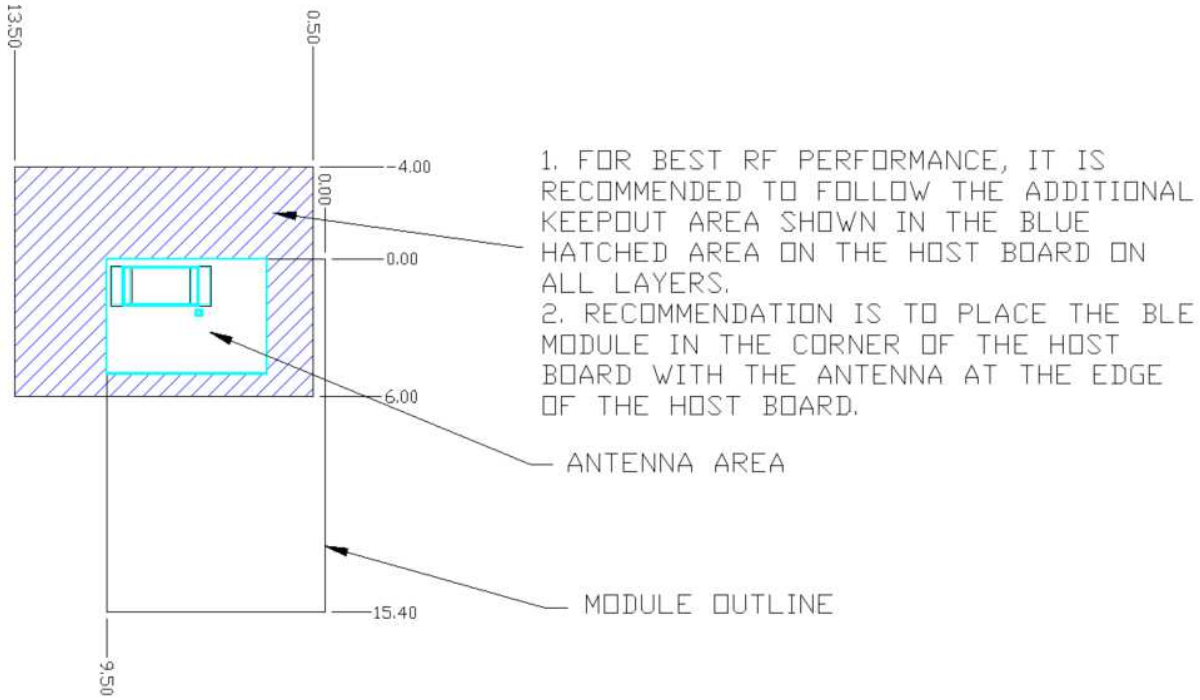
Figure 2. Solder Pad Dimensions (Seen from Bottom)



To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE module is in a corner of the host board with the antenna located on the edge of the host board. This placement minimizes the additional recommended keep-out area shown in item 2. Refer to AN96841 for module placement best practices.
2. To maximize RF performance, the area immediately around the Cypress BLE module trace antenna should contain an additional keep-out area, where no grounding or signal traces are contained. The keep-out area applies to all layers of the host board. The recommended dimensions of the host PCB keep-out area are shown in Figure 3 (dimensions are in mm).

Figure 3. Recommended Host PCB Keep-Out Area Around the CYBLE-224110-00 Trace Antenna



Host PCB Keep-Out Area Around Trace Antenna

Recommended Host PCB Layout

Figure 4, Figure 5, Figure 6, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-224110-00. Dimensions are in millimeters unless otherwise noted. The minimum recommended host PCB pad length is 0.91 mm (0.455 mm from center of the pad to either side) is recommended as shown in Figure 6. The host PCB layout pattern can be completed using either Figure 4, Figure 5, or Figure 6. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 4. Host Layout Pattern for CYBLE-224110-00

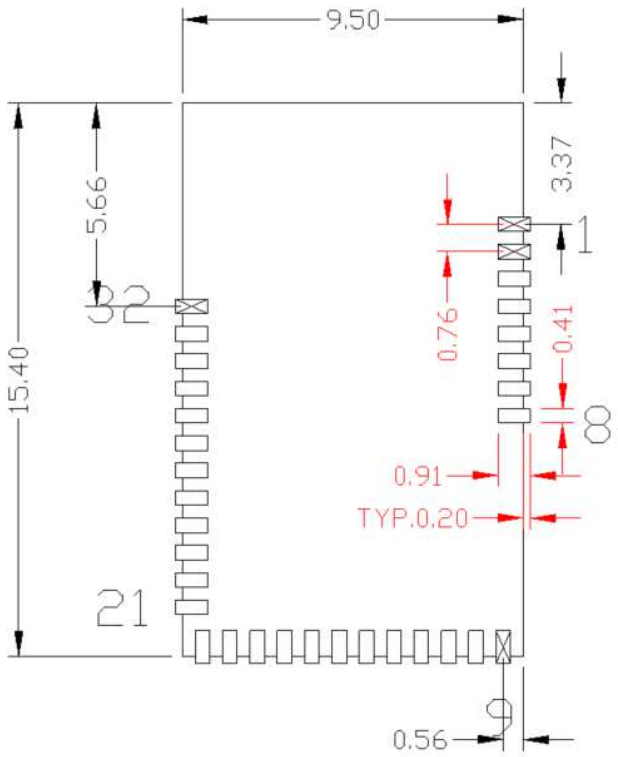


Figure 5. Module Pad Location from Origin

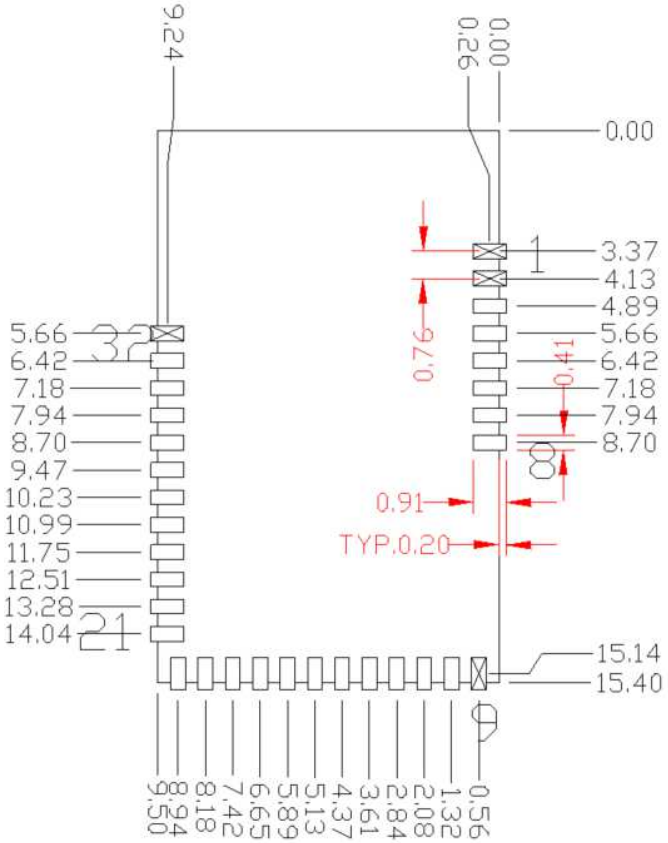


Table 3 provides the center location for each solder pad on the CYBLE-224110-00. All dimensions are referenced to the center of the solder pad. Refer to Figure 6 for the location of each module solder pad.

Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Dimension from Origin (mils)
1	(0.26, 3.37)	(10.24, 132.68)
2	(0.26, 4.13)	(10.24, 162.68)
3	(0.26, 4.89)	(10.24, 192.68)
4	(0.26, 5.66)	(10.24, 222.68)
5	(0.26, 6.42)	(10.24, 252.68)
6	(0.26, 7.18)	(10.24, 282.68)
7	(0.26, 7.94)	(10.24, 312.68)
8	(0.26, 8.70)	(10.24, 342.68)
9	(0.56, 15.14)	(22.05, 596.06)
10	(1.32,15.14)	(51.97, 596.06)
11	(2.08, 15.14)	(81.89, 596.06)
12	(2.84,15.14)	(111.81, 596.06)
13	(3.61, 15.14)	(142.13, 596.06)
14	(4.37, 15.14)	(172.13, 596.06)
15	(5.13, 15.14)	(202.13, 596.06)
16	(5.89, 15.14)	(231.89, 596.06)
17	(6.65,15.14)	(261.81, 596.06)
18	(7.42, 15.14)	(292.13, 596.06)
19	(8.18, 15.14)	(322.05, 596.06)
20	(8.94, 15.14)	(351.97, 596.06)
21	(9.24, 14.04)	(363.78, 552.76)
22	(9.24, 13.28)	(363.78, 522.83)
23	(9.24, 12.51)	(363.78,492.52)
24	(9.24, 11.75)	(363.78, 462.60)
25	(9.24,10.99)	(363.78, 432.68)
26	(9.24,10.23)	(363.78, 402.76)
27	(9.24, 9.47)	(363.78, 372.83)
28	(9.24, 8.70)	(363.78, 342.52)
29	(9.24, 7.94)	(363.78, 312.60)
30	(9.24, 7.18)	(363.78, 282.68)
31	(9.24, 6.42)	(363.78, 252.76)
32	(9.24,5.66)	(363.78, 222.83)

Figure 6. Solder Pad Reference Location

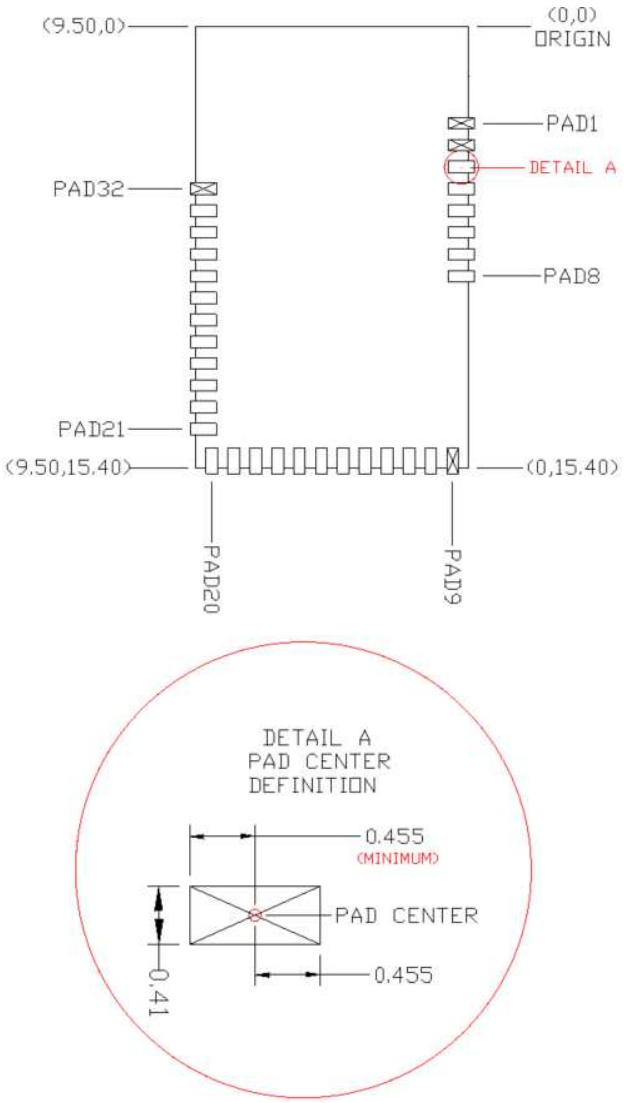


Table 4 and Table 5 detail the solder pad connection definitions and available functions for each connection pad. Table 4 lists the solder pads on CYBLE-224110-00, the BLE device port-pin, and denotes whether the digital function shown is available for each solder pad. Table 5 denotes whether the analog function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

.

Table 4. Digital Peripheral Capabilities

Pad Number	Device Port Pin	UART	SPI	I²C	TCPWM[4,5]	Cap-Sense	WCO Out	ECO OUT	LCD	SWD	GPIO
1	GND[5]	Ground Connection									
2	XRES	External Reset Hardware Connection Input									
3	P1.5	✓(SCB0_TX)	✓(SCB0_MISO)	✓(SCB0_SCL)	✓(TCPWM)	✓			✓		✓
4	P1.1		✓(SCB1_SS1)		✓(TCPWM)	✓			✓		✓
5	P1.0				✓(TCPWM)	✓			✓		✓
6	P0.1	✓(SCB1_TX)	✓(SCB1_MISO)	✓(SCB1_SCL)	✓(TCPWM)	✓			✓		✓
7	P0.4	✓(SCB0_RX)	✓(SCB0_MOSI)	✓(SCB0_SDA)	✓(TCPWM)	✓		✓	✓		✓
8	P0.5	✓(SCB0_TX)	✓(SCB0_MISO)	✓(SCB0_SCL)	✓(TCPWM)	✓			✓		✓
9	P0.7	✓(SCB0_CTS)	✓(SCB0_SCLK)		✓(TCPWM)	✓			✓	✓ (SWDCLK)	✓
10	P1.3		✓(SCB1_SS3)		✓(TCPWM)	✓			✓		✓
11	V_{DDR}	Radio Power Supply (2.0V to 3.6V)									
12	P0.6	✓(SCB0_RTS)	✓(SCB0_SS0)		✓(TCPWM)	✓			✓	✓ (SWDIO)	✓
13	P1.2		✓(SCB1_SS2)		✓(TCPWM)	✓			✓		✓
14	V_{DD}	Digital Power Supply Input (1.71 to 5.5V)									
15	P1.4	✓(SCB0_RX)	✓(SCB0_MOSI)	✓(SCB0_SDA)	✓(TCPWM)	✓			✓		✓
16	P2.1		✓(SCB0_SS2)		✓(TCPWM)	✓			✓		✓
17	V_{DDA}	Analog Power Supply Input (1.71 to 5.5V)									
18	P2.2		✓(SCB0_SS3)		✓(TCPWM)	✓			✓		✓
19	P2.6				✓(TCPWM)	✓			✓		✓
20	P3.0	✓(SCB0_RX)		✓(SCB0_SDA)	✓(TCPWM)	✓			✓		✓
21	P2.3				✓(TCPWM)	✓	✓		✓		✓
22	V_{REF}	Reference Voltage Input									
23	P3.4	✓(SCB1_RX)		✓(SCB1_SDA)	✓(TCPWM)	✓			✓		✓
24	P3.5	✓(SCB1_TX)		✓(SCB1_SCL)	✓(TCPWM)	✓			✓		✓
25	P3.7	✓(SCB1_CTS)			✓(TCPWM)	✓	✓		✓		✓
26	P3.1	✓(SCB0_TX)		✓(SCB0_SCL)	✓(TCPWM)	✓			✓		✓
27	P3.6	✓(SCB1_RTS)			✓(TCPWM)	✓			✓		✓
28	P2.5				✓(TCPWM)	✓			✓		✓
29	P5.0	✓(SCB1_RX)	✓(SCB1_SS0)	✓(SCB1_SDA)	✓(TCPWM3_P)	✓			✓		✓
30	P5.1	✓(SCB1_TX)	✓(SCB1_SCLK)	✓(SCB1_SCL)	✓(TCPWM3_N)	✓		✓	✓		✓
31	P2.4				✓(TCPWM)	✓			✓		✓
32	GND[5]	Ground Connection									

Notes
4. TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
5. The main board needs to connect both GND connections (Pad 1 and Pad 32) on the module to the common ground of the system.

.

Table 5. Analog Peripheral Capabilities

Pad Number	Device Port Pin	SARMUX	OPAMP	LPCOMP
1	GND[5]	Ground Connection		
2	XRES	External Reset Hardware Connection Input		
3	P1.5		✓(CTBm1_OA1_INP)	
4	P1.1		✓(CTBm1_OA0_INN)	
5	P1.0		✓(CTBm1_OA0_INP)	
6	P0.1			
7	P0.4			✓(COMP1_INP)
8	P0.5			✓(COMP1_INN)
9	P0.7			
10	P1.3		✓(CTBm1_OA1_OUT)	
11	V_{DDR}	Radio Power Supply (2.0V to 3.6V)		
12	P0.6			
13	P1.2		✓(CTBm1_OA0_OUT)	
14	VDD	Digital Power Supply Input (1.71 to 5.5V)		
15	P1.4		✓(CTBm1_OA1_INN)	
16	P2.1		✓(CTBm0_OA0_INN)	
17	V_{DDA}	Analog Power Supply Input (1.71 to 5.5V)		
18	P2.2		✓(CTBm0_OA0_OUT)	
19	P2.6		✓(CTBm0_OA0_INP)	
20	P3.0	✓		
21	P2.3		✓(CTBm0_OA1_OUT)	
22	VREF	Reference Voltage Input (Optional)		
23	P3.4	✓		
24	P3.5	✓		
25	P3.7	✓		
26	P3.1	✓		
27	P3.6	✓		
28	P2.5		✓(CTBm0_OA1_INP)	
29	P5.0			
30	P5.1			
31	P2.4		✓(CTBm0_OA1_INN)	
32	GND	Ground Connection		

Power Supply Connections and Recommended External Components

Power Connections

The CYBLE-224110-00 contains three power supply connections: VDD, VDDA, and VDDR. The VDD and VDDA connections supply power for the digital and analog device operation respectively. VDDR supplies power for the device radio and PA/LNA.

VDD and VDDA accept a supply range of 1.71 V to 5.5 V. VDDR accepts a supply range of 2.0 V to 3.6 V. These specifications can be found in Table 13. The maximum power supply ripple for both power connections on the module is 100 mV, as shown in Table 11.

The power supply ramp rate of VDD and VDDA must be equal to or greater than that of VDDR when the radio is used.

Connection Options

Two connection options are available for any application:

1. Single supply: Connect VDD, VDDA, and VDDR to the same supply.
2. Independent supply: Power VDD, VDDA, and VDDR separately.

External Component Recommendation

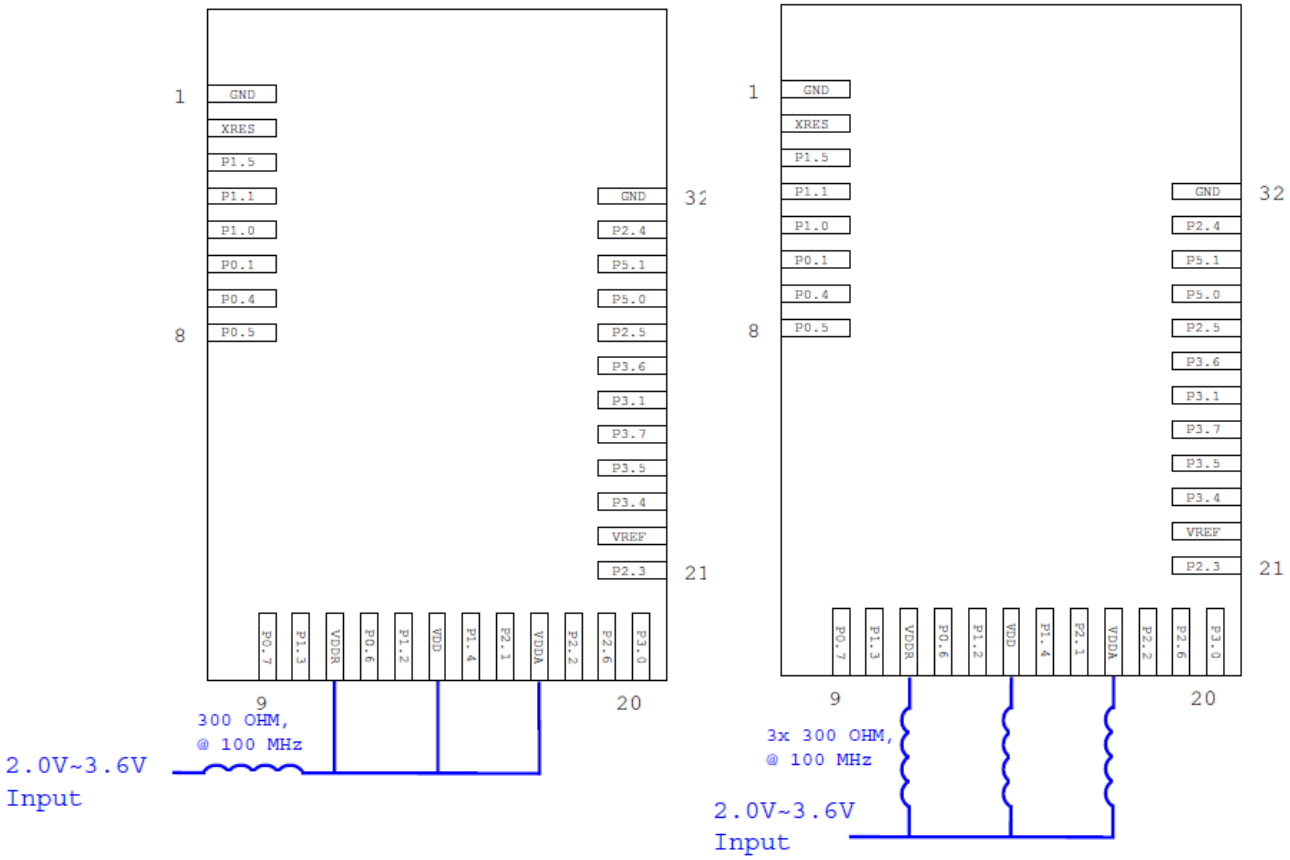
In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

Figure 7 details the recommended host schematic options for a single supply scenario. The use of one or three ferrite beads will depend on the specific application and configuration of the CYBLE-224110-00.

Figure 8 details the recommended host schematic for an independent supply scenario.

The recommended ferrite bead value is 330 Ω, 100 MHz. (Murata BLM21PG331SN1D).

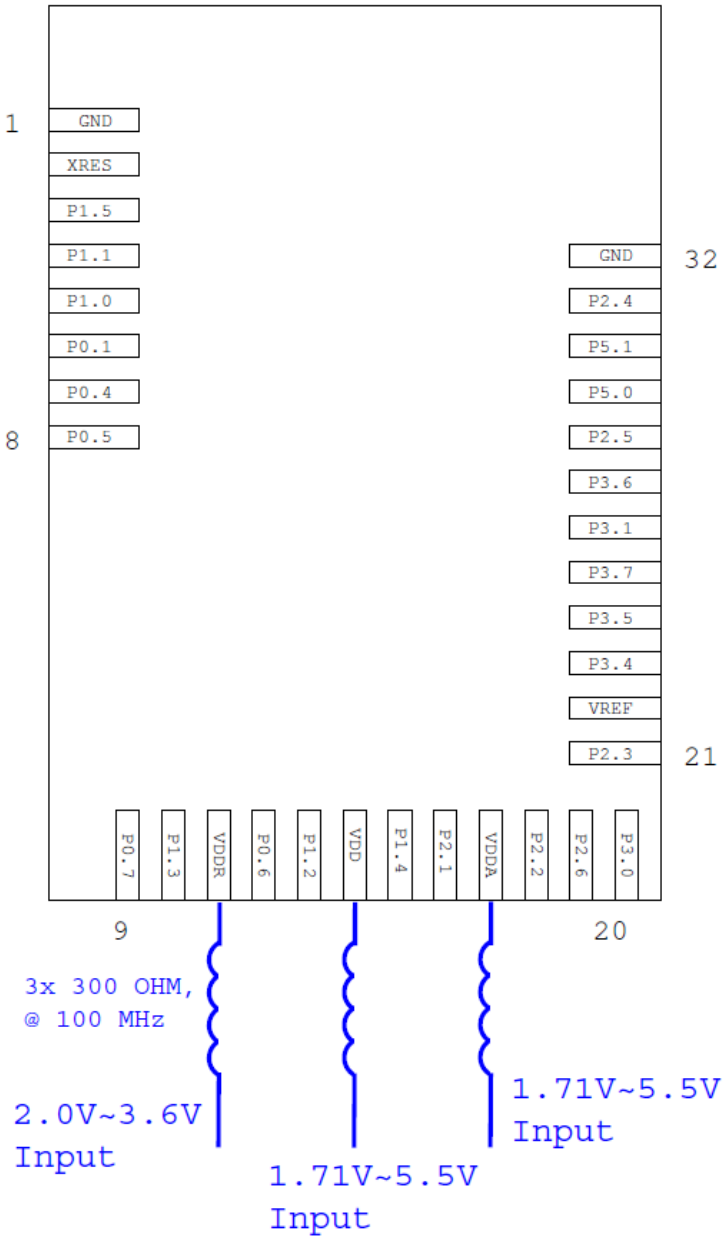
Figure 7. Recommended Host Schematic Options for a Single Supply Option



Single Ferrite Bead Option

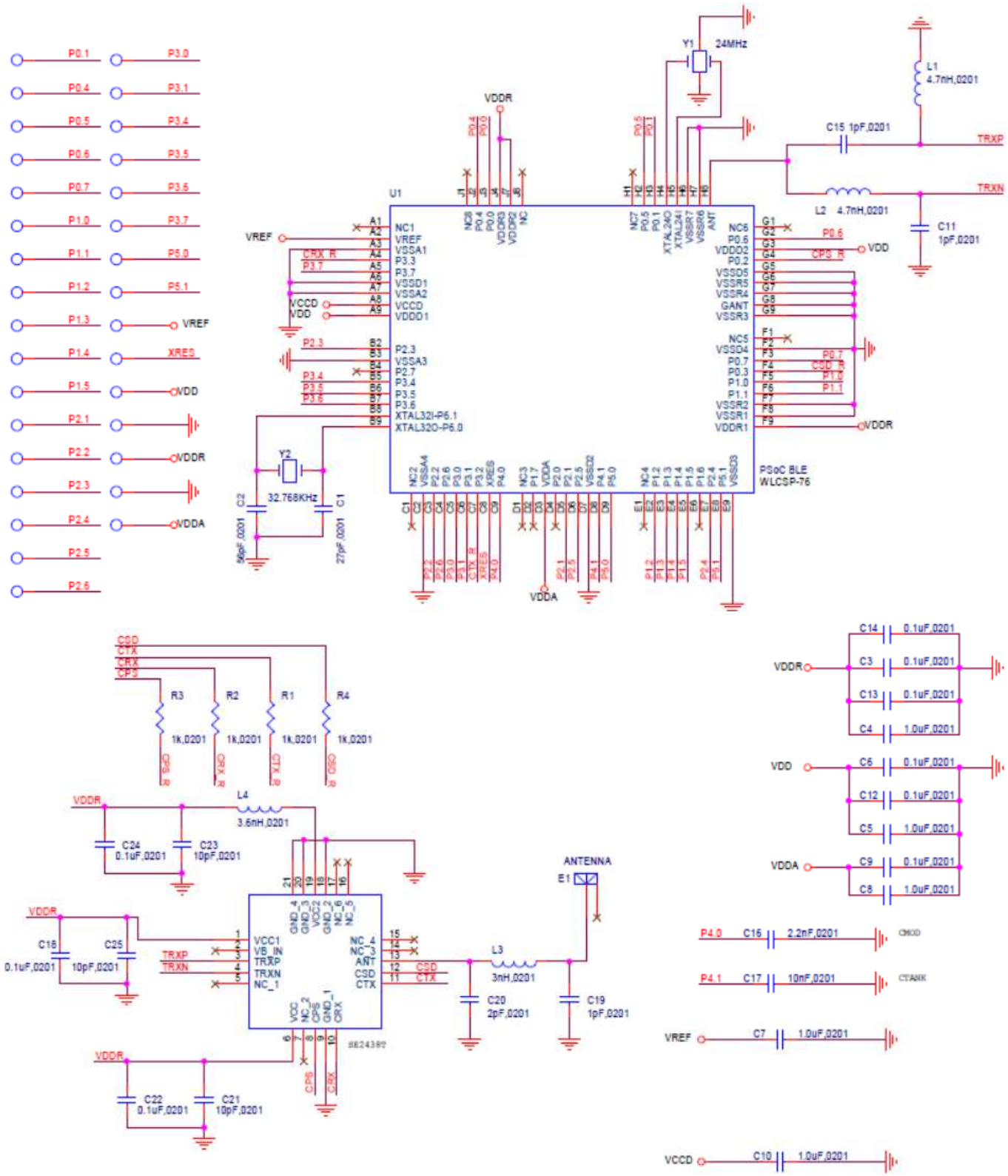
Three Ferrite Bead Option

Figure 8. Recommended Host Schematic for an Independent Supply Option



The CYBLE-224110-00 schematic is shown in Figure 9.

Figure 9. CYBLE-224110-00 Schematic Diagram



Critical Components List

Table 6 details the critical components used in the CYBLE-224110-00 module.

Table 6. Critical Component List

Component	Reference Designator	Description
Silicon	U1	76-pin WLCSP Programmable System-on-Chip (PSoC) with BLE
Crystal	Y1	24.000 MHz, 10PF
Crystal	Y2	32.768 kHz, 12.5PF

Antenna Design

Table 7 details the antenna used on the CYBLE-224110-00 module. The Cypress module performance improves many of these characteristics. For more information, see Table 12.

Table 7. Chip Antenna Specifications

Item	Description
Chip Antenna Manufacturer	Johanson Technology Inc.
Chip Antenna Part Number	2450AT18B100
Frequency Range	2400 – 2500 MHz
Peak Gain	0.5 dBi typical
Average Gain	-0.5 dBi typical
Return Loss	9.5 dB minimum

Power Amplifier (PA) and Low Noise Amplifier (LNA)

Table 8 details the PA/LNA that is used on the CYBLE-224110-00 module. For more information, see Table 12.

Table 8. Power Amplifier/Low Noise Amplifier Details

Item	Description
PA/LNA Manufacturer	Skyworks Inc.
PA/LNA Part Number	SE2438T
Power Supply Range	2.0V ~ 3.6V

Table 9 details the power consumption of the integrated PA/LNA used on the CYBLE-224110-00 module. Table 9 only details the current consumption of the SE2438T PA/LNA. VDDR = 3 V, T_A = +25 „°C, measured on the SE2438T evaluation board, unless otherwise noted.

Table 9. Power Amplifier/Low Noise Amplifier Current Consumption Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Total supply current	I_{CC}_Tx14	Tx mode P_{OUT} = +14 dBm	–	33	–	mA
Total supply current	I_{CC}_Tx12	Tx mode P_{OUT} = +12 dBm	–	25	–	mA
Total supply current	I_{CC}_Tx10	Tx mode P_{OUT} = +10 dBm	–	20	–	mA
Quiescent current	I_{CQ}_Tx	No RF	–	6	–	mA
Total supply current	I_{CC}_R_{XHG}	Rx Low Noise Amplifier (LNA) High Gain mode	–	5.5	–	mA
Total supply current	I_{CC}_R_{XLG}	Rx LNA Low Gain mode	–	2.7	–	mA
Total supply current	I_{CC}_$R_{XBypass}$	Rx Bypass mode	–	–	10	µA
Sleep supply current	I_{CC}_OFF	No RF	–	0.05	1.0	µA

Enabling Extended Range Feature

The CYBLE-224110-00 module comes with an integrated power amplifier/low-noise amplifier to allow for extended communication range of up to 400 meters full line-of-sight. This section describes the firmware steps required to enable extended range operation of the CYBLE-224110-00 module. For detailed step-by-step instructions, refer to Appendix B.2.3.2 in the application note, Getting Started with EZ-BLE Module.

The Skyworks SE2438T PA/LNA is controlled by PSoC4 BLE and uses four pins:

1. Two pins for the radio enable (CPS - P0[2], CSD - P0[3]). The CPS and CSD pins are controlled in the firmware application code of the CYBLE-224110-00.
2. One pin to control the PA enable (P3[2]). The PA enable pin is controlled directly by the BLE Link Layer.
3. One pin to control the LNA enable (P3[3]). The LNA enable pin is controlled directly by the BLE Link Layer.
4. Ensure that the PSoC® 4 BLE silicon device “Adv/Scan TX Power Level (dBm)” and “Connection TX Power Level (dBm)” in the BLE component are both set to -6 dBm[6].

To enable the extended range functionality, follow these steps:

1. "Drag and drop two "Digital Output Pin" components from the Component Catalog to the schematic page in PSoC Creator
2. "Double-click the pins and rename them as CPS and CSD. The HW connection option in the component configuration should be unchecked as these are Firmware GPIOs.
3. "To configure the CPS and CSD pins, open your project's Design-Wide Resources file (for example, "Project_Name.cydwr") from your Workspace Explorer and click the "Pins" tab. The "Pins" tab is used to select the physical device connections for the outputs (CPS, CSD). These pins are connected to the enable pins of the Skyworks SE2438T Power Amplifier. For the extended range operation to function, it is required to configure the CPS and CSD pins to P0[2] and P0[3] respectively.
4. "Open your project's main.c file and write the following code to define the register at the top of the code.

```
/* define the test register to switch the PA/LNA hardware control pins */
#define     CYREG_SRSS_TST_DDFT_CTRL    0x40030008
```

5. Locate/add the event “CYBLE_EVT_STACK_ON" in the application code and insert the following four lines of code to enable the Skyworks SE2438T.

```
/* Mandatory events to be handled by BLE application code */
case CYBLE_EVT_STACK_ON:
/* Enable the Skyworks SE2438T PA/LNA */
    CSD_Write(1);
    CPS_Write(1);

  /* Configure the Link Layer to automatically switch PA control pin P3[2] and LNA control pin P3[3] */
 CY_SET_XTND_REG32((void CYFAR *)(CYREG_BLE_BLESS_RF_CONFIG), 0x0331);
 CY_SET_XTND_REG32((void CYFAR *)(CYREG_SRSS_TST_DDFT_CTRL), 0x80000302);
```

Note

6. The CYBLE-224110-00 module is certified for FCC, IC, CE, MIC, and KC regulations at an output power of +9.5 dBm. To achieve this output power, RF_{O2} (PSoC 4 BLE silicon PA level) must be set to the -6 dBm setting in firmware. Settings higher than this will result in higher output power than specified in the CYBLE-224110-00 certifications.

Power Saving Measures with PA/LNA Operation

The section will describe power saving measures available for controlling the integrated PA/LNA on the CYBLE-224110-00 module.

Table 10 lists the states available through via the CSD and CPS logic control signals.

Table 10. PA/LNA Logic Controls and Power Modes

PA/LNA Mode	CSD (P0[3]) Logic State	CPS (P0[2]) Logic State	Description
0	0	0	All Off. Lowest Power Mode PA and LNA are off
1	0	1	Standby Mode Recommended mode for low power operation
2	1	0	TX and RX Bypass Mode
3	1	1	High Power TX and High Gain RX

Power Optimization Tips with Extended Range Functionality

If left in High Power TX and High Gain RX mode continuously, the integrated PA/LNA on the CYBLE-224110-00 module will draw more current than desired. Optimizing the average power consumption of the CYBLE-224110-00 module can be accomplished via the CSD and CPS logic control signals explained in Enabling Extended Range Feature and shown in Table 10.

To minimize power consumption of a BLE solution that is using the extended range feature of the CYBLE-224110-00, the PA/LNA should be set to either Mode 0 (All Off) or Mode 1 (Standby). Transitioning the PA/LNA from Mode 3 (High Power and High Gain) to either Mode 0 or 1 needs to be taken care of in the application firmware. The recommendations below should be followed when changing modes of the PA/LNA on the CYBLE-224110-00 module.

1. To set the PA/LNA to a low power mode, either Power Mode 0 or Power Mode 1 should be entered just before the BLE application firmware transitions the PSoC® 4 BLE silicon device to a Sleep or Deep Sleep mode. To execute the transition of the PA/LNA to a lower power mode, the following code should be used in the low power routine in the application firmware. Power Mode 0 and Power Mode 1 PA/LNA commands are both shown.

```
/* Set the Skyworks SE2438T PA/LNA to Power Mode 0 (All Off)*/
    CSD_Write(0);
    CPS_Write(0);
```

```
/* Set the Skyworks SE2438T PA/LNA to Power Mode 1 (Standby)*/
    CSD_Write(0);
    CPS_Write(1);
```

2. When the BLE system is transitioning to Active mode (that is, waking from low power mode) and extended range functionality is required, it is necessary to enable the PA/LNA to Power Mode 3. Enabling the PA/LNA should be the first action completed when the PSoC® 4 BLE silicon device transitions from a low power mode to active mode. Enabling the PA/LNA to Power Mode 3 can be completed using the following commands in the wakeup routine of the application firmware.

```
/* Set the Skyworks SE2438T PA/LNA to Power Mode 3 (High Power and High Gain)*/
    CSD_Write(1);
    CPS_Write(1);
```

3. Power Mode 2 (TX/RX Bypass) is not recommended for typical low power mode use. The Bypass mode should be considered if a transition from Extended Range functionality to short-range communication is desired on-the-fly. Transitions from Active mode to Bypass mode are only recommended after a BLE event has completed and no RF activity is in process.

Electrical Specification

Table 11 details the absolute maximum electrical characteristics for the Cypress BLE module.

Table 11. CYBLE-224110-00 Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DD_ABS}	V_{DD} or V_{DDA} supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	6	V	Absolute maximum
V_{DDR_ABS}	V_{DDR} supply relative to V_{SS} (V_{SSD} = V_{SSA})	-0.3	–	3.6	V	Restricted by SE2438T
V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute maximum
V_{DD_RIPPLE}	Maximum power supply ripple for V_{DD}, V_{DDA} and V_{DDR} input voltage	–	–	100	mV	3.0V supply Ripple frequency of 100 kHz to 750 kHz
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} +0.5	V	Absolute maximum
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute maximum
$I_{GPIO\_injection}$	GPIO injection current: Maximum for V_{IH} > V_{DD} and minimum for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute maximum current injected per pin
LU	Pin current for latch up	–200		200	mA	–

Table 12 details the RF characteristics for the Cypress BLE module.

Table 12. CYBLE-224110-00 RF Performance Characteristics

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
RF_{O1}[7]	RF output power on ANT PA active	–3.5	0	9.5	dBm	Configurable via register settings. PA active. RF_{O2} = –6 dBm PA/LNA active.
RF_{O2}	RF output power on ANT PA bypassed	-18	0	3	dBm	PSoC 4 BLE Silicon. Configurable via register settings. PA in bypass mode.
RX_{S1}	RF receive sensitivity on ANT LNA active	–	–95	–	dBm	Measured value
RX_{S2}	RF receive sensitivity on ANT LNA bypassed	–	–87	–	dBm	Measured value
F_R	Module frequency range	2402	–	2480	MHz	–
G_P	Peak gain	–	– 0.5	–	dBi	–
RL	Return loss	–	–10	–	dB	–

Table 13 through Table 55 list the module-level electrical characteristics for the CYBLE-224110-00. All specifications are valid for –40 °C ≤ TA ≤ 105 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 13. CYBLE-224110-00 DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DD1}	Power supply input voltage (V_{DD} = V_{DDA})	1.8	–	5.5	V	–
V_{DD2}	Power supply input voltage unregulated (V_{DD} = V_{DDA})	1.71	1.8	1.89	V	Internally unregulated supply
V_{DD3}	Power supply input voltage (V_{DD} = V_{DDA} = V_{DDR})	2.0	–	3.6	V	Restricted by SE2438T
V_{DDR1}	Radio supply voltage (radio on)	2.0	–	3.6	V	Restricted by SE2438T
V_{DDR2}	Radio supply voltage (radio off)	2.0	–	3.6	V	Restricted by SE2438T

Note

7. The CYBLE-224110-00 module is certified for FCC, IC, CE, MIC, and KC regulations at an output power of +9.5 dBm. To achieve this output power, RF_{O2} must be set to the –6 dBm setting in firmware. Settings higher than this will result in higher output power than specified in the CYBLE-224110-00 certifications.

Table 13. CYBLE-224110-00 DC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Active Mode, V_{DD} = 1.71 V to 5.5 V						
I_{DD3}	Execute from flash; CPU at 3 MHz	–	1.7	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD4}	Execute from flash; CPU at 3 MHz	–	–	–	mA	T = –40 °C to 105 °C
I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD6}	Execute from flash; CPU at 6 MHz	–	–	–	mA	T = –40 °C to 105 °C
I_{DD7}	Execute from flash; CPU at 12 MHz	–	4	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD8}	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 105 °C
I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 105 °C
I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 105 °C
Sleep Mode, V_{DD} and V_{DDR} = 2.0 to 3.6 V, PA/LNA in All Off mode						
I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, V_{DD} = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 2.0 to 3.6 V, PA/LNA in All Off mode						
I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, V_{DD} = 3.3 V, SYSCLK = 3 MHz
Deep-Sleep Mode, V_{DD} and V_{DDR} = 2.0 to 3.6 V, PA/LNA in All Off mode						
I_{DD15}	WDT with WCO on	–	2.3	–	µA	T = 25 °C, V_{DD} = 3.3 V
I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Deep-Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed) and V_{DDR} = 2.0 to 3.6 V, PA/LNA in All Off mode						
I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} and V_{DDR} = 2.0 to 3.6 V, PA/LNA in All Off mode						
I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3 V
I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C
Hibernate Mode, V_{DD} = 3.6 to 5.5 V and V_{DDR} = 2.0 to 3.6 V, PA/LNA in All Off mode						
I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 105 °C
Stop Mode, V_{DD} = 1.71 to 3.6 V and V_{DDR} = 2.0 to 3.6 V, PA/LNA in All Off						
I_{DD33}	Stop-mode current (V_{DD})	–	20	–	nA	T = 25 °C, V_{DD} = 3.3 V
I_{DD34}	Stop-mode current (V_{DDR})	–	540	–-	nA	T = 25 °C, V_{DDR} = 3.3 V
I_{DD35}	Stop-mode current (V_{DD})	–	–	–	nA	T = –40 °C to 105 °C
I_{DD36}	Stop-mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 105 °C, V_{DDR} = 2.0 V to 3.6 V

Table 13. CYBLE-224110-00 DC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Stop Mode, V_{DD} = 3.6 to 5.5 V and V_{DDR} = 2.0 to 3.6 V, PA/LNA in All Off mode						
I_{DD37}	Stop-mode current (V_{DD})	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
I_{DD38}	Stop-mode current (V_{DDR})	–	–	–	nA	T = 25 °C, V_{DDR} = 3.6 V PA/LNA in All Off mode
I_{DD39}	Stop-mode current (V_{DD})	–	–	–	nA	T = –40 °C to 105 °C
I_{DD40}	Stop-mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 105 °C

Table 14. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
$T_{DEEPSLEEP}$	Wakeup from Deep-Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization
$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	2	ms	Guaranteed by characterization
T_{STOP}	Wakeup from Stop mode	–	–	2	ms	Guaranteed by characterization

GPIO

Table 15. GPIO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}[8]	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS input
	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}	–	–	V	–
	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	–	V	–
V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS input
	LVTTL input, V_{DD} < 2.7 V	–	–	0.3 × V_{DD}	V	–
	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	–
V_{OH}	Output voltage HIGH level	V_{DD} –0.6	–	–	V	I_{OH} = 4 mA at 3.3-V V_{DD}
	Output voltage HIGH level	V_{DD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DD}
V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3.3-V V_{DD}
	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DD}
	Output voltage LOW level	–	–	0.4	V	I_{OL} = 3 mA at 3.3-V V_{DD}
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.3 V
I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
C_{IN}	Input capacitance	–	–	7	pF	–
V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DD} > 2.7 V
$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DD}	–	–	1	–
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Note
8. V_{IH} must not exceed V_{DD} + 0.2 V.

Table 16. GPIO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISEF}	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DD}, C_{LOAD} = 25 pF
T_{FALLF}	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DD}, C_{LOAD} = 25 pF
T_{RISES}	Rise time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DD}, C_{LOAD} = 25 pF
T_{FALLS}	Fall time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DD}, C_{LOAD} = 25 pF
$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
$F_{GPIOUT2}$	GPIO Fout; 1.7 V≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V Slow-Strong mode	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
$F_{GPIOUT4}$	GPIO Fout; 1.7 V ≤ V_{DD} ≤ 3.3 V Slow-Strong mode	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
F_{GPIOIN}	GPIO input operating frequency 1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

Table 17. OVT GPIO DC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{IL}	Input leakage (absolute value). V_{IH} > V_{DD}	–	–	10	µA	25°C, V_{DD} = 0 V, V_{IH} = 3.0 V
V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 20 mA, V_{DD} > 2.9 V

Table 18. OVT GPIO AC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISE_OVFS}	Output rise time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
T_{FALL_OVFS}	Output fall time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
T_{RISESS}	Output rise time in Slow-Strong mode	10	–	60	ns	25-pF load, 10%-90%, V_{DD} = 3.3 V
T_{FALLSS}	Output fall time in Slow-Strong mode	10	–	60	ns	25-pF load, 10%-90%, V_{DD} = 3.3 V
$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25-pF load, 60/40 duty cycle
$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25-pF load, 60/40 duty cycle

XRES

Table 19. XRES DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
C_{IN}	Input capacitance	–	3	–	pF	–
$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

Table 20. XRES AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–

Analog Peripherals

Opamp

Table 21. Opamp Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{DD} (Opamp Block Current. V_{DD} = 1.8 V. No Load)						
I_{DD_HI}	Power = high	–	1000	1300	µA	
I_{DD_MED}	Power = medium	–	500	–	µA	
I_{DD_LOW}	Power = low	–	250	350	µA	
GBW (Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V)						
GBW_HI	Power = high	6	–	–	MHz	
GBW_MED	Power = medium	4	–	–	MHz	
GBW_LO	Power = low	–	1	–	MHz	
I_{OUT_MAX} (V_{DDA} ≥ 2.7 V, 500 mV from Rail)						
$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
I_{OUT} (V_{DDA} = 1.71 V, 500 mV from Rail)						
$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
V_{IN}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	
V_{CM}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	
V_{OUT} (V_{DDA} ≥ 2.7 V)						
V_{OUT_1}	Power = high, I_{LOAD}=10 mA	0.5	–	V_{DDA} – 0.5	V	
V_{OUT_2}	Power = high, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	
V_{OUT_3}	Power = medium, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	
V_{OUT_4}	Power = low, I_{LOAD}=0.1 mA	0.2	–	V_{DDA} – 0.2	V	
V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode

Table 21. Opamp Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode
$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
CMRR	DC	65	70	–	dB	V_{DD} = 3.6 V, High-power mode
PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V_{DD} = 3.6 V
Noise						
V_{N1}	Input referred, 1 Hz–1 GHz, power = high	–	94	–	µVrms	
V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
V_{N3}	Input referred, 10 kHz, power = high	–	28	–	nV/rtHz	
V_{N4}	Input referred, 100 kHz, power = high	–	15	–	nV/rtHz	
C_{LOAD}	Stable up to maximum load. Performance specs at 50 pF	–	–	125	pF	
Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V	6	–	–	V/µs	
T_op_wake	From disable to enable, no external RC dominating	–	300	–	µs	
Comp_mode (Comparator Mode; 50-mV Drive, $T_{RISE} = T_{FALL}$ (Approx.)						
T_{PD1}	Response time; power = high	–	150	–	ns	
T_{PD2}	Response time; power = medium	–	400	–	ns	
T_{PD3}	Response time; power = low	–	2000	–	ns	
Vhyst_op	Hysteresis	–	10	–	mV	
Deep-Sleep Mode (Deep-Sleep mode operation is only guaranteed for V_{DDA} > 2.5 V)						
GBW_DS	Gain bandwidth product	–	50	–	kHz	
IDD_DS	Current	–	15	–	µA	
Vos_DS	Offset voltage	–	5	–	mV	
Vos_dr_DS	Offset voltage drift	–	20	–	µV/°C	
Vout_DS	Output voltage	0.2	–	V_{DD}–0.2	V	
Vcm_DS	Common mode voltage	0.2	–	V_{DD}–1.8	V	

Table 22. Comparator DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	
$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±6	mV	
$V_{OFFSET3}$	Input offset voltage, ultra-low-power mode	–	±12	–	mV	
V_{HYST}	Hysteresis when enabled	–	10	35	mV	
V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DD} – 0.1	V	Modes 1 and 2
V_{ICM2}	Input common mode voltage in low-power mode	0	–	V_{DD}	V	
V_{ICM3}	Input common mode voltage in ultra low-power mode	0	–	V_{DD} –1.15	V	
CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DD} \geq 2.7$ V

Table 22. Comparator DC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
CMRR	Common mode rejection ratio	42	–	–	dB	$V_{DD} \leq 2.7$ V
I_{CMP1}	Block current, normal mode	–	–	400	µA	
I_{CMP2}	Block current, low-power mode	–	–	100	µA	
I_{CMP3}	Block current in ultra-low-power mode	–	6	–	µA	
Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	

Table 23. Comparator AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RESP1}	Response time, normal mode, 50-mV overdrive	–	38	–	ns	50-mV overdrive
T_{RESP2}	Response time, low-power mode, 50-mV overdrive	–	70	–	ns	50-mV overdrive
T_{RESP3}	Response time, ultra-low-power mode, 50-mV overdrive	–	2.3	–	µs	200-mV overdrive $V_{DD} \geq 2.6$ V for Temp < 0 °C $V_{DD} \geq 1.8$ V for Temp ≥ 0 °C

Temperature Sensor

Table 24. Temperature Sensor Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{SENSACC}$	Temperature-sensor accuracy	–5	±1	5	°C	–40 to +85 °C

SAR ADC

Table 25. SAR ADC DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_RES	Resolution	–	–	12	bits	
A_CHNIS_S	Number of channels - single-ended	–	–	8		8 full-speed[9]
A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O[9]
A-MONO	Monotonicity	–	–	–		Yes
A_GAINERR	Gain error	–	–	±0.1	%	With external reference
A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}
A_ISAR	Current consumption	–	–	1	mA	
A_VINS	Input voltage range - single-ended	V_{SS}	–	V_{DDA}	V	
A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	
A_INRES	Input resistance	–	–	2.2	kΩ	
A_INCAP	Input capacitance	–	–	10	pF	
VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of Vbg (1.024 V)

Note
9. A maximum of eight single-ended ADC Channels can be accomplished only if the AMUX Buses are not being used for other funcitonality (e.g. CapSense). If the AMUX Buses are being used for other functionality, then the maximum number of single-ended ADC channels is six. Similarly, if the AMUX Buses are being used for other functionalty, then the maximum number of differential ADC channels is three.

Table 26. SAR ADC AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
A_PSRR	Power-supply rejection ratio	70	–	–	dB	Measured at 1-V reference
A_CMRR	Common-mode rejection ratio	66	–	–	dB	
A_SAMP	Sample rate	–	–	1	Msps	
Fsarintref	SAR operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution
A_SNR	Signal-to-noise ratio (SNR)	65	–	–	dB	F_{IN} = 10 kHz
A_BW	Input bandwidth without aliasing	–	–	A_SAMP/2	kHz	
A_INL	Integral nonlinearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 V to V_{DD}
A_INL	Integral nonlinearity. V_{DDD} = 1.71 V to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 V to V_{DD}
A_INL	Integral nonlinearity. V_{DD} = 1.71 V to 5.5 V, 500 ksps	–1.5	–	1.7	LSB	V_{REF} = 1 V to V_{DD}
A_dnl	Differential nonlinearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}
A_DNL	Differential nonlinearity. V_{DD} = 1.71 V to 3.6 V, 1 Msps	–1	–	2	LSB	V_{REF} = 1.71 V to V_{DD}
A_DNL	Differential nonlinearity. V_{DD} = 1.71 V to 5.5 V, 500 ksps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}
A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz

CSD

CSD Block Specifications

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
V_{CSD}	Voltage range of operation	1.71	–	5.5	V	
IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SNR	Ratio of counts of finger to noise	5	–	–	Ratio	Capacitance range of 9 pF to 35 pF, 0.1-pF sensitivity. Radio is not operating during the scan
I_{DAC1_CRT1}	Output current of IDAC1 (8 bits) in High range	–	612	–	µA	
I_{DAC1_CRT2}	Output current of IDAC1 (8 bits) in Low range	–	306	–	µA	
I_{DAC2_CRT1}	Output current of IDAC2 (7 bits) in High range	–	305	–	µA	
I_{DAC2_CRT2}	Output current of IDAC2 (7 bits) in Low range	–	153	–	µA	