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CYBT-343026-01

EZ-BT™ WICED® Module

General Description

The CYBT-343026-01 is a fully integrated Bluetooth® Smart Ready wireless module. The CYBT-343026-01 includes an onboard crystal oscillator, passive components, flash memory, and the Cypress CYW20706 silicon device. Refer to the CYW20706 datasheet for additional details on the capabilities of the silicon device used in this module.

The CYBT-343026-01 supports peripheral functions (ADC and PWM), UART, I^2C, and SPI communication, and a PCM/I2S audio interface. The CYBT-343026-01 includes a royalty-free Bluetooth stack compatible with Bluetooth 5.0 in a 12.0 × 15.5 × 1.95 mm package.

The CYBT-343026-01 includes 512 KB of onboard serial flash memory and is designed for standalone operation. The CYBT-343026-01 uses an integrated power amplifier to achieve Class I or Class II output power capability.

The CYBT-343026-01 is fully qualified by Bluetooth SIG and is targeted at applications requiring cost optimized Bluetooth wireless connectivity.

Module Description

- Module size: 12.00 mm × 15.50 mm × 1.95 mm
- Bluetooth 5.0 Qualified Smart Ready module
  - QDID: 99198
  - Declaration ID: D035378
- Certified to FCC, ISED, MIC, and CE regulations
- Castelated solder pad connections for ease-of-use
- 512-KB on-module serial flash memory
- Up to 11 GPIOs
- Temperature range: –30 °C to +85 °C
- Cortex-M3 32-bit processor
- Maximum TX output power
  - +12 dbm for Bluetooth Classic
  - +9 dBm for Bluetooth Low Energy
    - BLE connection range of up to 250 meters at 9 dBm[1]
- RX Receive Sensitivity:
  - Bluetooth Classic:
    - –93.5 dBm at 1 Mbps, GFSK
    - –95.5 dBm at 2 Mbps, π/4-DQPSK
    - –89.5 dBm at 3 Mbps, 8-DPSK
  - –96.5 dBm for Bluetooth Low Energy

Power Consumption

- Enhanced Data Rate (EDR) at 8 dBm
  - Peak TX current: 52.5 mA
  - Peak RX current consumption: 26.4 mA
- Bluetooth Low Energy (BLE) at 0 dBm
  - 1-second interval BLE ADV average current consumption: 315 uA
- Low power mode support
  - Deep Sleep: 2.69 uA

Functional Capabilities

- Σ-Δ ADC for audio (12 bits) and DC measurement (10 bits)
- Serial Communications interface compatible with I^2C slaves
- Serial Peripheral Interface (SPI) support for both master and slave modes
- HCI interface through UART
- PCM/I2S Audio interface
- Two-wire Global Coexistence Interface (GCI)
- Integrated peripherals such as PWM, ADC
- Programmable output power control
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Bluetooth wideband speech support

Benefits

CYBT-343026-01 provides all necessary components required to operate BLE and/or BR/EDR communication standards.

- Proven hardware design ready to use
- Dual-mode operation eliminates the need for multiple modules
- Cost optimized for applications without space constraints
- Nonvolatile memory for self-sufficient operation and Over-the-air updates
- Bluetooth SIG Listed with QDID and Declaration ID
- Fully certified module eliminates the time needed for design, development and certification processes
- WICED® Studio provides an easy-to-use integrated design environment (IDE) to configure, develop, and program a Bluetooth application

Note

1. Connection range tested module-to-module in full line-of-sight environment, free of obstacles or interference sources with output power of +9.0 dBm. Actual range will vary based on end product design, environment, receive sensitivity and transmit output power of the central device.

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

References

- Overview: EZ-BLE/BT Module Portfolio, Module Roadmap
- CYW20706 BT Silicon Datasheet
- Development Kits:
  - CYBT-343026-EVAL, CYBT-343026-01 Evaluation Board
- Test and Debug Tools:
  - CYSmart, Bluetooth® LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)
- Knowledge Base Article
  - KBA97095 - EZ-BLE™ Module Placement
  - KBA213260- RF Regulatory Certifications for CYBT-343026-01 EZ-BT™ WICED Modules
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
  - KBA218122 - 3D Model Files for EZ-BLE/EZ-BT Modules
  - KBA221025 - Platform Files for CYBT-343026-EVAL
  - KBA223428 - Programming an EZ-BT WICED Module

Development Environments

Wireless Connectivity for Embedded Devices (WICED) Studio Software Development Kit (SDK)

Cypress' WICED® (Wireless Connectivity for Embedded Devices) is a full-featured platform with proven Software Development Kits (SDKs) and turnkey hardware solutions from partners to readily enable Wi-Fi and Bluetooth® connectivity in system design.

WICED Studio is the only SDK for the Internet of Things (IoT) that combines Wi-Fi and Bluetooth into a single integrated development environment. In addition to providing WICED APIs and an application framework designed to abstract complexity, WICED Studio also leverages many common industry standards.

Technical Support

- Cypress Community: Whether you're a customer, partner or a developer interested in the latest Cypress innovations, the Cypress Developer Community offers you a place to learn, share and engage with both Cypress experts and other embedded engineers around the world.
- Frequently Asked Questions (FAQs): Learn more about our Bluetooth ECO System.
- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

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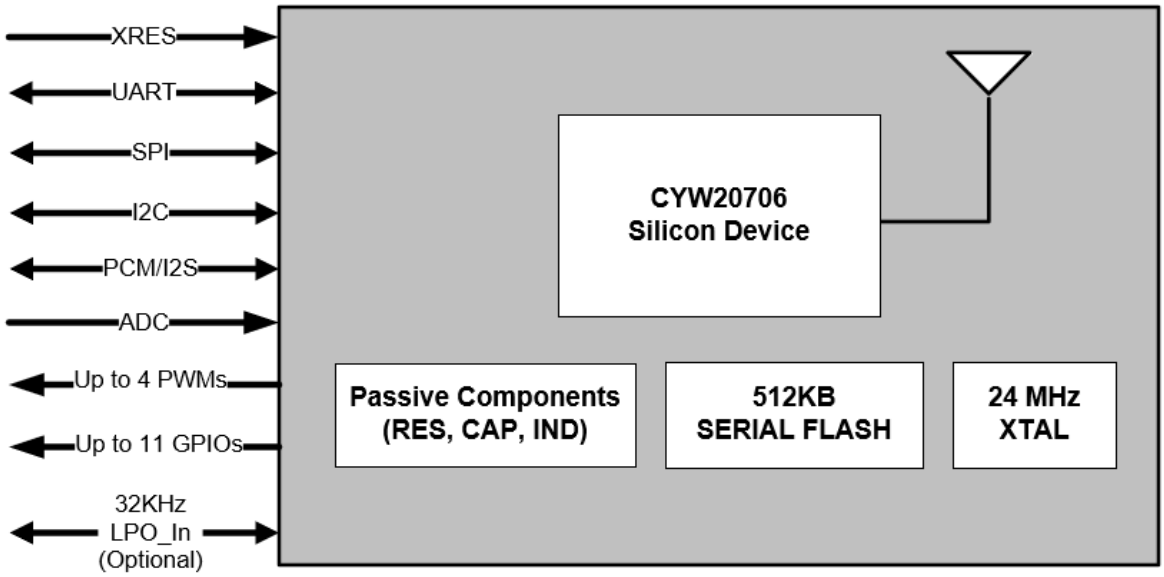
Overview

Functional Block Diagram

Figure 1 illustrates the CYBT-343026-01 functional block diagram.

Figure 1. Functional Block Diagram (GPIOs)



Module Description

The CYBT-343026-01 module is a complete module designed to be soldered to the application's main board.

Module Dimensions and Drawing

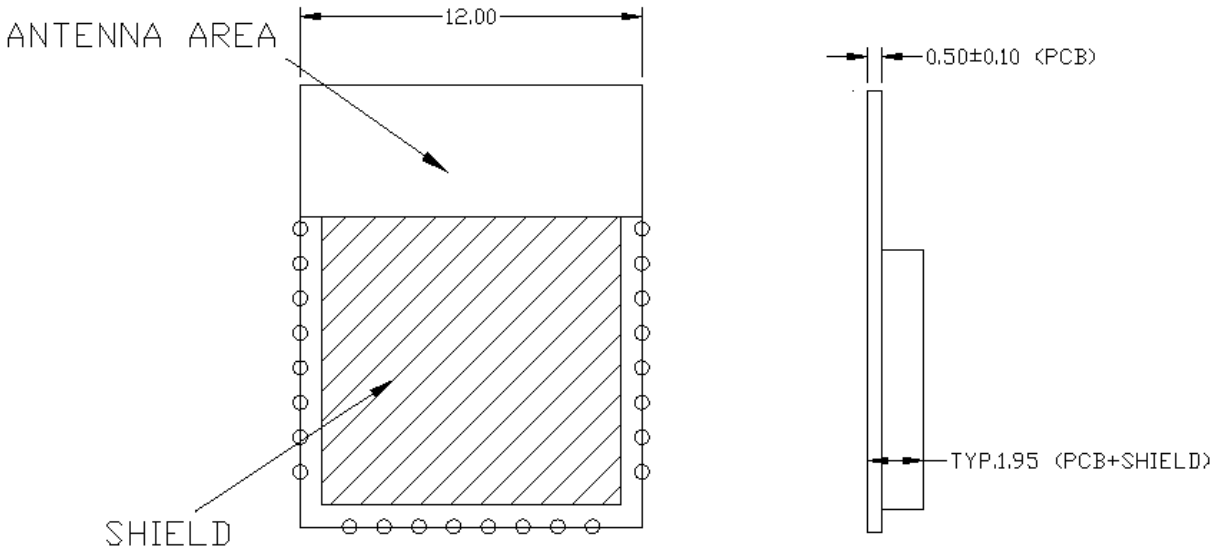
Cypress reserves the right to select components from various vendors to achieve the Bluetooth module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in Figure 2 on page 5. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	12.00 ± 0.15 mm
	Width (Y)	15.50 ± 0.15 mm
Antenna connection location dimensions	Length (X)	12.0 mm
	Width (Y)	4.62 mm
PCB thickness	Height (H)	0.50 ± 0.05 mm
Shield height	Height (H)	1.45 mm typical
Maximum component height	Height (H)	1.45 mm typical
Total module thickness (bottom of module to highest component)	Height (H)	1.95 mm typical

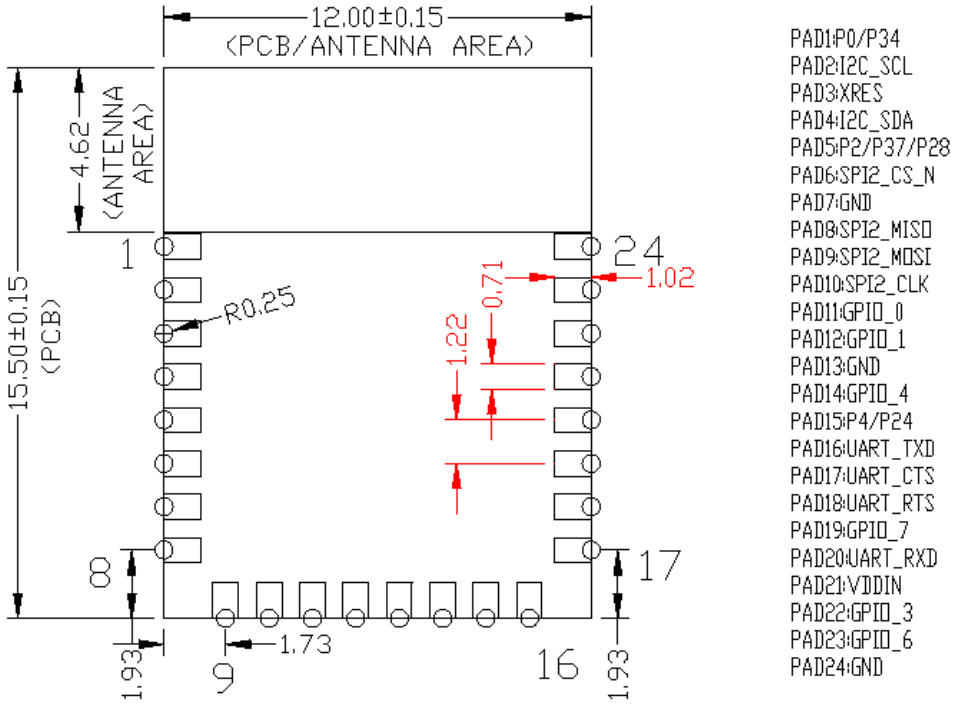
See Figure 2 for the mechanical reference drawing for CYBT-343026-01.

Figure 2. Module Mechanical Drawing[2, 3]



Top View (Seen from Top)

Side View



Bottom View

Notes
2. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see "Recommended Host PCB Layout" on page 7.
3. The CYBT-343026-01 includes castellated pad connections, denoted as the circular openings at the pad location above.

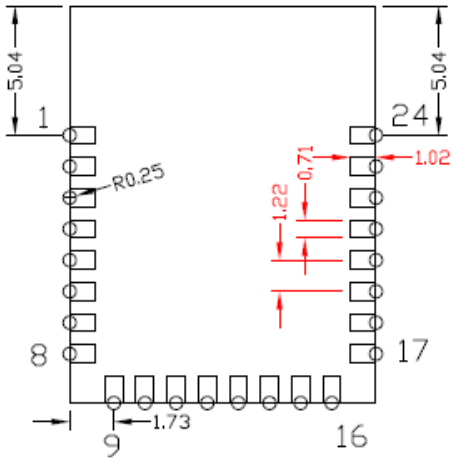
Pad Connection Interface

As shown in the bottom view of Figure 2 on page 5, the CYBT-343026-01 connects to the host board via solder pads on the backside of the module. Table 2 and Figure 3 detail the solder pad length, width, and pitch dimensions of the CYBT-343026-01 module.

Table 2. Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	24	Solder Pads	1.02 mm	0.71 mm	1.22 mm

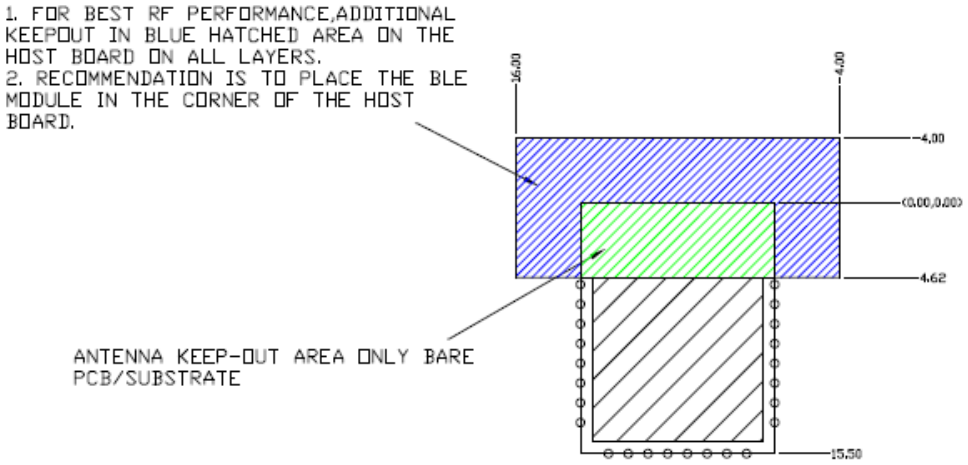
Figure 3. Solder Pad Dimensions (Seen from Bottom



To maximize RF performance, the host layout should follow these recommendations:

1. Antenna Area Keepout: The host board directly below the antenna area of the Cypress module (see Figure 2 on page 5) must contain no ground or signal traces. This keep out area requirement applies to all layers of the host board.
2. Module Placement: The ideal placement of the Cypress Bluetooth module is in a corner of the host board with the PCB trace antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2. Refer to AN96841 for module placement best practices.

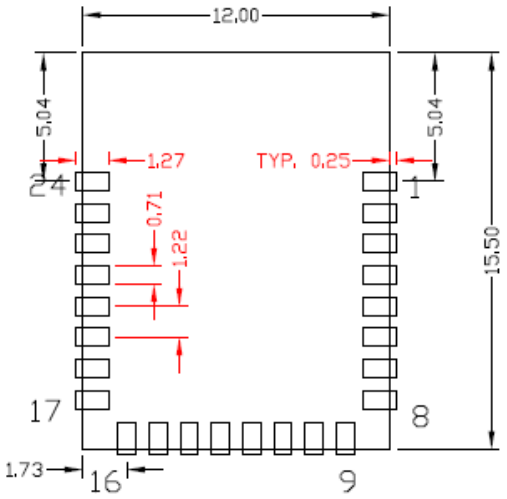
Figure 4. Recommended Host PCB Keep Out Area Around the CYBT-343026-01 Antenna



Recommended Host PCB Layout

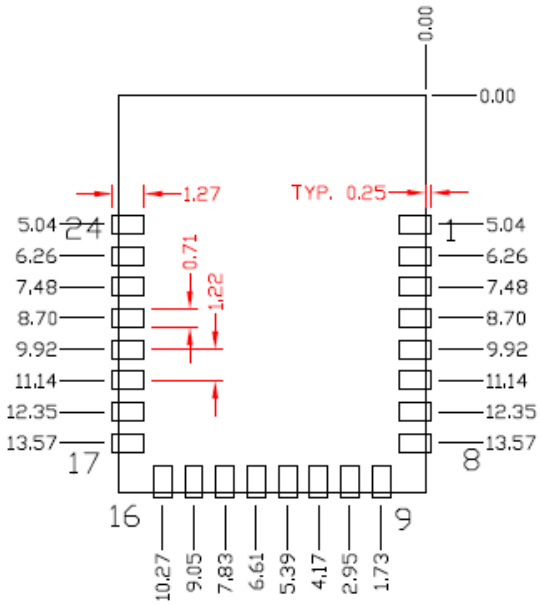
Figure 5, Figure 6, Figure 7, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBT-343026-01. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.635 mm from center of the pad on either side) shown in Figure 7 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 5, Figure 6, or Figure 7. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 5. CYBT-343026-01 Host Layout (Dimensioned)



Top View (Seen on Host PCB)

Figure 6. CYBT-343026-01 Host Layout (Relative to Origin)



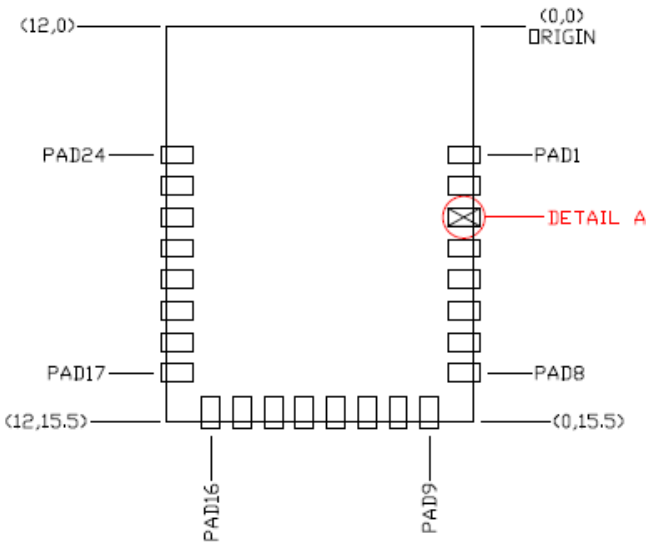
Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBT-343026-01. All dimensions are referenced to the center of the solder pad. Refer to Figure 7 for the location of each module solder pad.

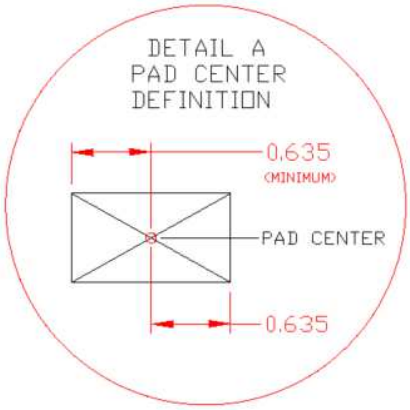
Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Dimension from Origin (mils)
1	(0.38, 5.04)	(14.96, 198.42)
2	(0.38, 6.26)	(14.96, 246.46)
3	(0.38, 7.48)	(14.96, 294.49)
4	(0.38, 8.70)	(14.96, 342.52)
5	(0.38, 9.92)	(14.96, 390.55)
6	(0.38, 11.14)	(14.96, 438.58)
7	(0.38, 12.35)	(14.96, 486.22)
8	(0.38, 13.57)	(14.96, 534.25)
9	(1.73, 15.11)	(68.11, 594.88)
10	(2.95, 15.11)	(116.14, 594.88)
11	(4.17, 15.11)	(164.17, 594.88)
12	(5.39, 15.11)	(212.20, 594.88)
13	(6.61, 15.11)	(260.24, 594.88)
14	(7.83, 15.11)	(308.27, 594.88)
15	(9.05, 15.11)	(356.30, 594.88)
16	(10.27, 15.11)	(404.33, 594.88)
17	(11.62, 13.57)	(457.48, 534.25)
18	(11.62, 12.35)	(457.48, 486.22)
19	(11.62, 11.14)	(457.48, 438.58)
20	(11.62, 9.92)	(457.48, 390.55)
21	(11.62, 8.70)	(457.48, 342.52)
22	(11.62, 7.48)	(457.48, 294.49)
23	(11.62, 6.26)	(457.48, 246.46)
24	(11.62, 5.04)	(457.48, 198.42)

Figure 7. Solder Pad Reference Location



Top View (Seen on Host PCB)



Module Connections

Table 4 details the solder pad connection definitions and available functions for the pad connections for the CYBT-343026-01 module. Table 4 lists the solder pads on the CYBT-343026-01 module, the silicon device pin, and denotes what functions are available for each solder pad.

Table 4. CYBT-343026-01 Solder Pad Connection Definitions

Pad	Pad Name	Silicon Pin Name	Silicon Port-Pin Name	UART	SPI[4,5]	I2C	ADC	COEX	CLK/ XTAL	GPIO	Other
1	P0/P34	C8	PCM_Sync/ I2S_WS/P0/P34	PUART_TX/P0 PUART_RX/P34	SPI1_MOSI/P0 (master/slave)		IN29/P0 IN5/P34			✓	PCM_Sync I2S_WS
2	I2C_SCL	A8	I2S_DO/ PCM_Out/P3/ P29/P35	PUART_CTS/ P3 or P35	SPI1_CLK/P3 (master/slave)	SCL SDA/ P35	IN4/P35 IN10/29			✓ (P3/P29 /P35)	I2S_DO PCM_Out PWM3 (P29)
3	XRES	RESET _N	RESET_N	External Reset (Active Low)							
4	I2C_SDA	C7	PCM_IN/ I2S_DI/P12			SDA	IN23/P12			✓ (P12)	PCM_IN I2S_DI
5	P2/P37/P28	B7	PCM_CLK/ I2S_CLK/P2/ P28/P37	PUART_RX/P2	SPI1_CS(slave)/P2 SPI1_MOSI(master)/P2 SPI1_MISO(slave)/P37	SCL/ P37	IN11/P28 IN2/P37		ACLK1 /P37	✓	PWM2 (P28) I2S_CLK PCM_CLK
6	SPI2_CS_N	D7	N/A	No Connect (Used for on-module memory SPI interface for CYBT-343026-01)							
7	GND	GND	GND	Ground							
8	SPI2_MISO	D8	N/A	No Connect (Used for on-module memory SPI interface for CYBT-343026-01)							
9	SPI2_MOSI	E8	N/A	No Connect (Used for on-module memory SPI interface for CYBT-343026-01)							
10	SPI2_CLK	E7	N/A	No Connect (Used for on-module memory SPI interface for CYBT-343026-01)							
11	GPIO_0	F8	BT_GPIO_0/ P36/P38		SPI1_CLK/P36 SPI1_MOSI/P38 (master/slave)		IN3/P36 IN1/P38		ACLK0 /P36	✓ (DevWa ke)	
12	GPIO_1	F7	BT_GPIO_1/ P25/P32	PUART_RX/P25 PUART_TX/P32	SPI1_MISO/P25 (master/slave) SPI1_CS/P32 (slave)		IN7/P32		ACLK0 /P32	✓ (HostWa ke)	
13	GND	GND	GND	Ground							
14	GPIO_4	D6	BT_GPIO_4/P6/ P31/LPO_IN	PUART_RTS/P6 PUART_TX/P31	SPI1_CS/P6 (slave)		IN8/P31			✓	Ext LPO In
15	P4/P24	G8	BT_CLK_REQ/ P4/P24	PUART_RX/P4 PUART_TX/P24	SPI1_MOSI/P4 (master/slave) SPI1_CLK/P24 (master/slave)					✓ (CLK_R EQ)	
16	UART_TXD	F4	BT_UART_TXD	HCI UART Transmit Data							
17	UART_CTS	G4	BT_UART_CTS	HCI UART Clear To Send Input							
18	UART_RTS	F3	BT_UART_RTS	HCI UART Request To Send Output							
19	GPIO_7	C6	BT_GPIO_7/ P30	PUART_RTS/ P30			IN9/P30	✓ (GCI_SE CI_OUT)		✓	
20	UART_RXD	F5	BT_UART_RXD	HCI UART Receive Data							
21	VDDIN	G1	VDDIN	VDDIN (2.3V ~ 3.6V)							
22	GPIO_3	C5	BT_GPIO_3/ P27/P33	PUART_RX/P33	SPI1_MOSI/P27 (master/slave) SPI1_MOSI/P33 (slave)		IN6/P33		ACLK1 /P33	✓	PWM1 (P27)
23	GPIO_6	B6	BT_GPIO_6/ P11/P26		SPI1_CS/P26 (slave)		IN24/P11	✓ (GCI_SE CI_IN)		✓	PWM0 (P26)
24	GND	GND	GND	Ground							

Notes

4. The CYBT-343026-01 contains a single SPI (SPI1) peripheral supporting both master or slave configurations. SPI2 is used for on-module serial memory interface.
5. In Master mode, any available GPIO can be configured as SPI1_CS. This function is not explicitly shown in Table 4.

Connections and Optional External Components

Power Connections (VDDIN)

The CYBT-343026-01 contains one power supply connection, VDDIN, that accepts a supply input range of 2.3 V to 3.6 V for CYBT-343026-01. Table 11 provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in Table 11.

It is not required to place any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included, but is not necessary. If used, the ferrite bead should be positioned as close as possible to the module pin connection and the recommended ferrite bead value is 330 Ω, 100 MHz.

Considerations and Optional Components for Brown Out (BO) Conditions

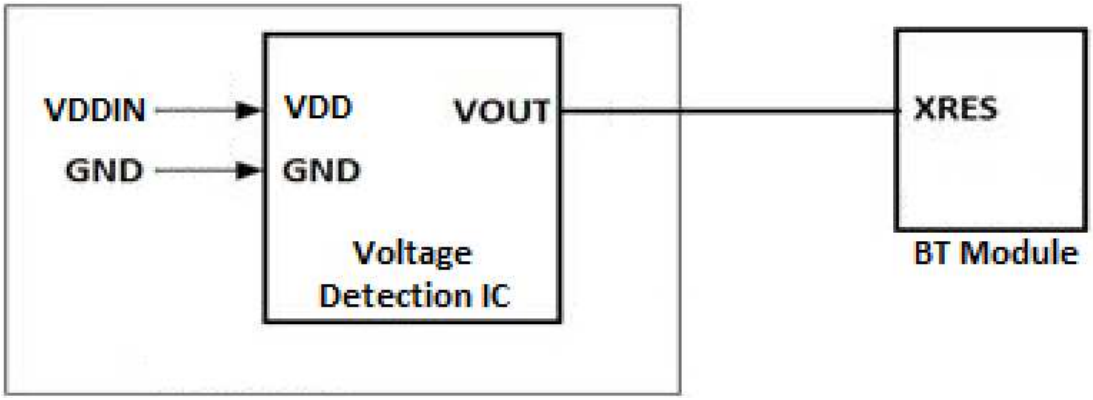
Power supply design must be completed to ensure that the CYBT-343026-01 module does not encounter a Brown Out condition, which can lead to unexpected functionality, or module lock-up. A Brown Out condition may be met if power supply provided to the module during power up or reset is in the following range:

$$V_{IL} \leq VDDIN \leq V_{IH}$$

Refer to Table 12 for the V_{IL} and V_{IH} specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (that is, battery installation, high-value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brown Out voltage range from occurring during power removal. Refer to Figure 8 for the recommended circuit design when using an external voltage detection IC.

Figure 8. Reference Circuit Block Diagram for External Voltage Detection IC



In the event that the module does encounter a Brown Out condition, and is operating erratically or not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brown Out conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brown Out condition.

External Reset (XRES)

The CYBT-343026-01 has an integrated power-on reset circuit, which completely resets all circuits to a known power-on state. This action can also be evoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYBT-343026-01 module (solder pad 3). The CYBT-343026-01 module does not require an external pull-up resistor on the XRES input

During power-on operation, the XRES connection to the CYBT-343026-01 is required to be held low 50 ms after the VDD power supply input to the module is stable. This can be accomplished in the following ways:

- The host device should connect a GPIO to the XRES of the Cypress CYBT-343026-01 module and pull XRES low until VDD is stable. XRES is recommended to be released 50 ms after VDDIN is stable.
- If the XRES connection of the CYBT-343026-01 module is not used in the application, a 10-µF capacitor may be connected to the XRES solder pad of the CYBT-343026-01 to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the VDDIN power supply ramp time of the system. The capacitor value should result in an XRES release timing of 50 ms after VDDIN stability.
- The XRES release timing may be controlled by a external voltage detection IC. XRES should be released 50 ms after VDD is stable.

Refer to Figure 11 on page 17 for XRES operating and timing requirements during power-on events.

Multiple-Bonded GPIO Connections

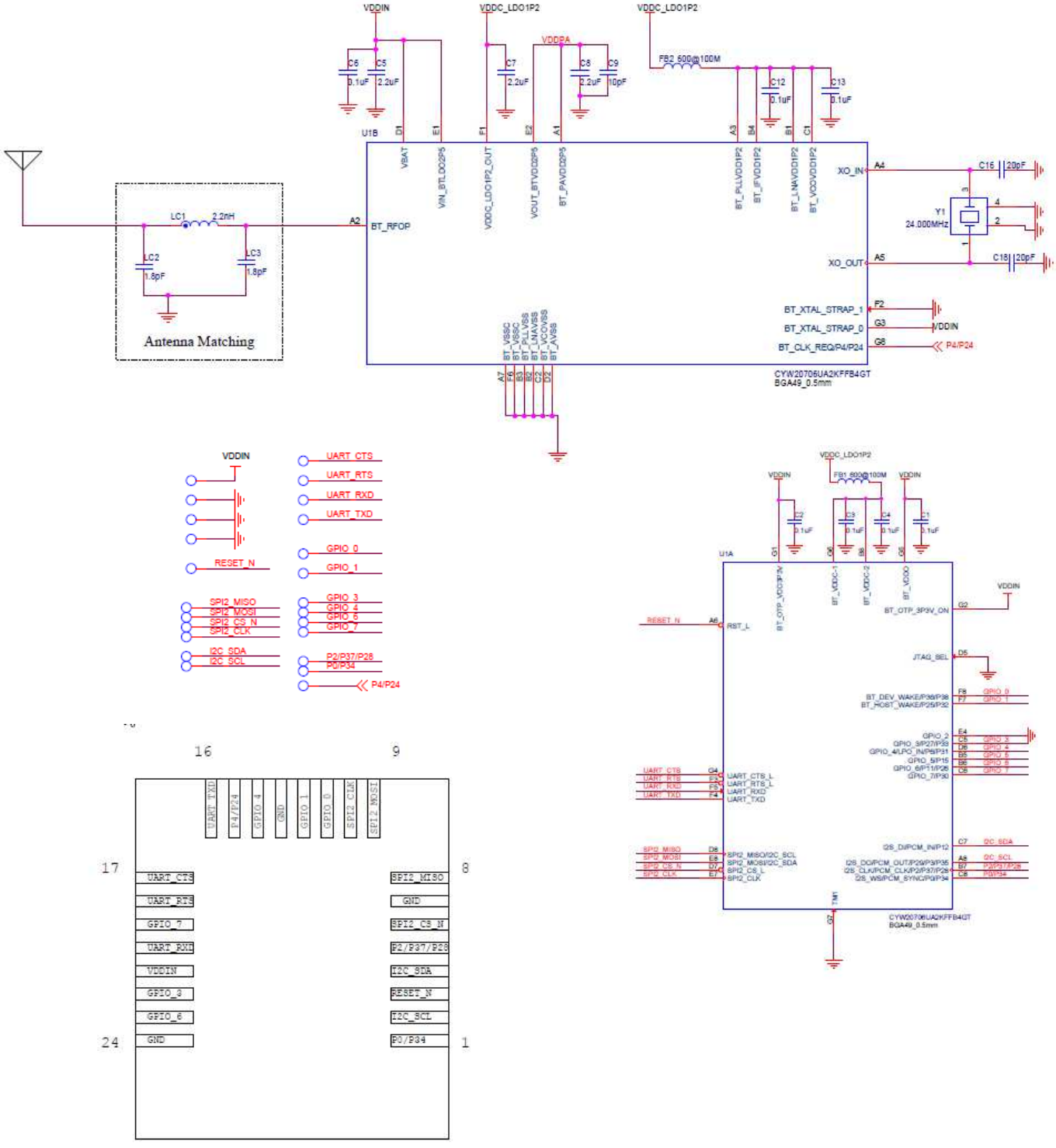
The CYBT-343026-01 contains GPIOs, which are multiple-bonded at the silicon level. If any of these dual-bonded GPIOs are used, only the functionality and features for one of these port pins may be used. The desired port pin should be configured in the WICED Studio SDK. For details on the features and functions that each of these multiple-bonded GPIOs provide, refer to Table 4.

The following list details the multiple-bonded GPIOs available on the CYBT-343026-01 module:

- PAD 1 P0/34: I2S_WS_PCM_SYNC/P0/P34 (triple bonded; only one of four is available)
- PAD 2 I2C_SCL: I2S_PCM_OUT/P3/P29/P35 (quadruple bonded; only one of four is available)
- PAD 4 I2C_SDA: I2S_PCM_IN/P12 (dual bonded; only one of two is available)
- PAD 5 P2/P37/P28: I2S_PCM_CLK/P2/P28/P37 (quadruple bonded; only one of four is available)
- PAD 11 GPIO_0: GPIO_0/P36/P38 (triple bonded; only one of three is available)
- PAD 12 GPIO_1: GPIO_1/P25/P32 (triple bonded; only one of three is available)
- PAD 14 GPIO_4: GPIO_4/LPO_IN/P6/P31 (quadruple bonded; only of four is available)
- PAD 15 P4/P24: BT_CLK_REQ/P4/P24 (triple bonded; only one of three is available)
- PAD 19 GPIO_7: GPIO_7/P30 (Dual bonded; only one of two is available)
- PAD 22 GPIO_3: GPIO_3/P27/P33 (triple bonded; only one of three is available)
- PAD 23 GPIO_6: GPIO_6/P11/P26 (triple bonded; only one of three is available)

Figure 9 illustrates the CYBT-343026-01 schematic.

Figure 9. CYBT-343026-01 Schematic Diagram



MODULE PAD ASSIGNMENT (BOTTOM VIEW)

Critical Components List

Table 5 details the critical components used in the CYBT-343026-01 module.

Table 5. Critical Component List

Component	Reference Designator	Description
Silicon	U1	49-pin FBGA BT/BLE Silicon Device - CYW20706
Silicon	U2	8-pin TDF8N, 512K Serial Flash
Crystal	Y1	24.000 MHz, 12PF

Antenna Design

Table 6 details the trace antenna used in the CYBT-343026-01 module.

Table 6. Trace Antenna Specifications

Item	Description
Frequency Range	2400–2500 MHz
Peak Gain	–0.5 dBi typical
Return Loss	10 dB minimum

Functional Description

Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL and TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types. The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Table 7. Bluetooth Features

Bluetooth 1.0	Bluetooth 1.2	Bluetooth 2.0
Basic Rate	Interlaced Scans	EDR 2 Mbps and 3 Mbps
SCO	Adaptive Frequency Hopping	–
Paging and Inquiry	eSCO	–
Page and Inquiry Scan	–	–
Sniff	–	–
Bluetooth 2.1	**Bluetooth 3.0**	**Bluetooth 4.0**
Secure Simple Pairing	Unicast Connectionless Data	Bluetooth Low Energy
Enhanced Inquiry Response	Enhanced Power Control	–
Sniff Subrating	eSCO	–
Bluetooth 4.1	**Bluetooth 4.2**	
Low Duty Cycle Advertising	Data Packet Length Extension	
Dual Mode	LE Secure Connection	
LE Link Layer Topology	Link Layer Privacy	

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state in the Bluetooth Link Controller.

- States:
  - Standby
  - Connection
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff
  - Advertising
  - Scanning

Test Mode Support

The CYBT-343026-01 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYBT-343026-01 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment.

Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth clock, and device address.

Microcontroller Unit

The microprocessor unit in CYBT-343026-01 runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is based on the Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The microprocessor also includes 848 KB of ROM memory for program storage and boot ROM, 352 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

NVRAM Configuration Data and Storage

NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The CYBT-343026-01 uses SPI Serial Flash for NVRAM storage.

One-Time Programmable Memory

The microprocessor unit in CYBT-343026-01 includes 2 KB of one-time programmable (OTP) memory allow manufacturing customization and to avoid the need for an on-board NVRAM. If customization is not required, then the OTP does not need to be programmed. Whether the OTP is programmed or not, to save power it is disabled when the boot process is complete. The OTP is designed to store a minimal amount of information. Aside from OTP data, most user configuration information will be downloaded to RAM after the CYBT-343026-01 boots and is ready for host transport communication.

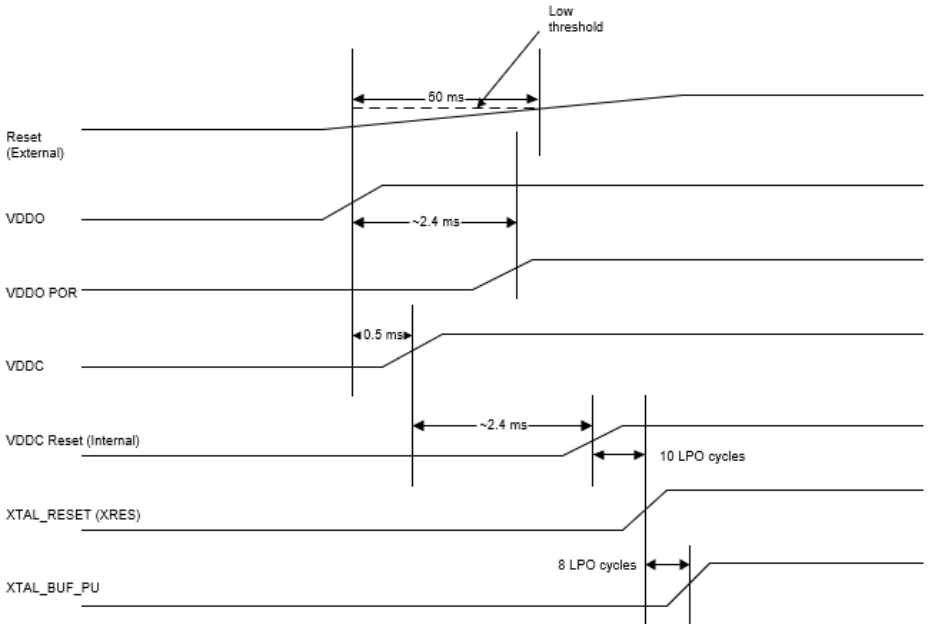
The OTP contents are limited to:

- Parameters required prior to downloading the user configuration to RAM.
- Parameters unique to each part and each customer (for example, the Bluetooth device address and/or the software license key).
- VDDIN for the module must be kept to 3.0 V to 3.6 V power supply range if OTP is used in the application.

External Reset (XRES)

The CYBT-343026-01 has an integrated power-on reset circuit that completely resets all circuits to a known power-on state. An external active low reset signal, XRES, can be used to put the CYBT-343026-01 in the reset state. The XRES pin has an internal pull-up resistor and, in most applications, it does not require anything to be connected to it.

Figure 10. External Reset Internal Timing

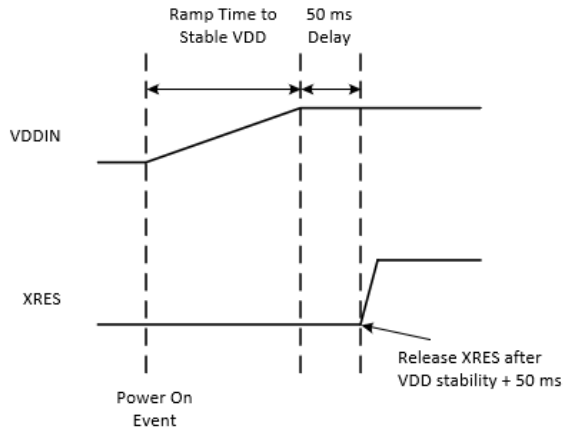


External Reset (XRES) Recommended External Components and Proper Operation

During a power-on event, the XRES line of the CYBT-343026-01 is required to be held low 50 ms after the VDD power supply input to the module is stable. Refer to Figure 11 for the Power-On XRES timing operation. This power-on operation can be accomplished in the following ways:

- A host device should connect a GPIO to the XRES of the Cypress CYBT-343026-01 module and pull XRES low until VDD is stable. XRES can be released after VDD is stable.
- If the XRES connection of the CYBT-343026-01 module is not used in the application, a 10-µF capacitor may be connected to the XRES solder pad of the CYBT-343026-01.
- The XRES release timing can also be controlled via an external voltage detection circuit.

Figure 11. Power-On External Reset (XRES) Operation



Integrated Radio Transceiver

The CYBT-343026-01 has an integrated radio transceiver that has been optimized for use in 2.4-GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. The CYBT-343026-01 is fully compliant with the Bluetooth Radio Specification and enhanced data rate (EDR) specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

The CYBT-343026-01 a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4-GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the BLE specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

Receiver Path

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYBT-343026-01 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYBT-343026-01 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation sub-block employs an architecture for high immunity to LO pulling during PA operation. The CYBT-343026-01 uses an internal loop filter.

Calibration

The CYBT-343026-01 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration tunes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops, and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Internal LDO

The microprocessor in CYBT-343026-01 uses two LDOs – one for 1.2 V and the other for 2.5 V. The 1.2-V LDO provides power to the baseband and radio and the 2.5-V LDO powers the PA.

Collaborative Coexistence

The CYBT-343026-01 provides extensions and collaborative coexistence to the standard Bluetooth AFH for direct communication with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously in a single device. The device supports industry-standard coexistence signaling, including 802.15.2, and supports Cypress and third-party WLAN solutions.

Global Coexistence Interface

The CYBT-343026-01 supports the proprietary Cypress Global Coexistence Interface (GCI) which is a 2-wire interface.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over GCI_SECI_IN and GCI_SECI_OUT a two-wire interface, one serial input (GCI_SECI_IN), and one serial output (GCI_SECI_OUT). The pad configuration registers must be programmed to choose the digital I/O pins that serve the GCI_SECI_IN and GCI_SECI_OUT function.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronization upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

SECI I/O

The microprocessor in CYBT-343026-01 has dedicated GCI_SECI_IN (PAD 23/GPIO_6) and GCI_SECI_OUT (PAD19/GPIO_7) pins. Refer to Table 4, which detail the module solder pad number used for SECI I/O.

Peripheral and Communication Interfaces

I²C Communication Interface

The CYBT-343026-01 provides a 2-pin master I²C interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. This interface is compatible with I²C slave devices. I²C does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by the I²C:

- 100 kHz
- 400 kHz
- 800 kHz (not a standard I²C-compatible speed.)
- 1 MHz (Compatibility with high-speed I²C-compatible devices is not guaranteed.)

The following transfer types are supported by the I²C:

- Read (Up to 127 bytes can be read)
- Write (Up to 127 bytes can be written)
- Read-then-Write (Up to 127 bytes can be read and up to 127 bytes can be written)
- Write-then-Read (Up to127 bytes can be written and up to 127 bytes can be read)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pad (I2C_SCL) and data pad 2 (I2C_SDA) are both open-drain I/O pins. Pull-up resistors, external to the CYBT-343026-01, are required on both the SCL and SDA pad for proper operation.

HCI UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 38400 bps to 4 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYBT-343026-01 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 4 Mbps. The baud rate of the CYBT-343026-01UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Table 8 contains example values to generate common baud rates with a 24-MHz UART clock.

Table 8. Common Baud Rate Examples, 24 MHz Clock

Baud Rate (bps)	Baud Rate Adjustment		Mode	Error (%)
	High Nibble	Low Nibble		
4M	0xFF	0xF4	High rate	0.00
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16
38400	0x01	0x00	Normal	0.00

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYBT-343026-01 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Peripheral UART Interface

The CYBT-343026-01 has a second UART that may be used to interface to other peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each signal as shown in Table 9

Table 9. CYBT-343026-01 Peripheral UART

Signal Name	PUART_TX	PUART_RX	PUART_CTS_N	PUART_RTS_N
PUART Port Configuration #1	P0	P2	P3	P6
PUART Port Configuration #2	P31	P33	P35	P30

Serial Peripheral Interface

The CYBT-343026-01 has two independent SPI interfaces. One is a master-only interface (SPI2) and the other (SPI1) can be either a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYBT-343026-01 has optional I/O ports that can be configured individually and separately for each functional pin. The CYBT-343026-01 acts as an SPI master device that supports 3.3 V SPI slaves. In master mode, refer to Table 4 to identify the solder pads available for SPI1_MISO, SPI1_MOSI, and SPI1_CLK connections. NOTE: In master mode, any available GPIO can be assigned as SPI1_CS.

The CYBT-343026-01 can also act as an SPI slave device that supports a 3.3 V SPI master. For SPI1 slave mode, refer to Table 4 to identify the solder pads available for SPI1 slave mode connections.

SPI voltage depends on V_{DDIN}; therefore, V_{DDIN} should be set to 3.3 V for SPI communication.

PCM Interface

The CYBT-343026-01 includes a PCM interface that shares pins with the I^2S interface. The PCM Interface on the CYBT-343026-01 can connect to linear PCM codec devices in master or slave mode. In master mode, the CYBT-343026-01 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYBT-343026-01.

Slot Mapping

The CYBT-343026-01 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The CYBT-343026-01 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The CYBT-343026-01 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYBT-343026-01 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

Clock Frequencies

The CYBT-343026-01 has an integrated 24-MHz crystal on the module. There is no need to add an additional crystal oscillator.

GPIO Port

The CYBT-343026-01 has nine GPIOs besides two I^2C pads. All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3 V or 4 mA at 1.8 V, except chips P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3 V.

The following GPIOs are available on the module pads:

- PAD 1 P0/34: I2S_WS_PCM_SYNC/P0/P34 (triple bonded; only one of four is available)
- PAD 2 I2C_SCL: I2S_PCM_OUT/P3/P29/P35 (quadruple bonded; only one of four is available)
- PAD 4 I2C_SDA: I2S_PCM_IN/P12 (dual bonded; only one of two is available)
- PAD 5 P2/P37/P28: I2S_PCM_CLK/P2/P28/P37 (quadruple bonded; only one of four is available)
- PAD 11 GPIO_0: GPIO_0/P36/P38 (triple bonded; only one of three is available)
- PAD 12 GPIO_1: GPIO_1/P25/P32 (triple bonded; only one of three is available)
- PAD 14 GPIO_4: GPIO_4/LPO_IN/P6/P31 (quadruple bonded; only of four is available)
- PAD 15 P4/P24: BT_CLK_REQ/P4/P24 (triple bonded; only one of three is available)
- PAD 19 GPIO_7: GPIO_7/P30 (Dual bonded; only one of two is available)
- PAD 22 GPIO_3: GPIO_3/P27/P33 (triple bonded; only one of three is available)
- PAD 23 GPIO_6: GPIO_6/P11/P26 (triple bonded; only one of three is available)

Refer to Table 4 to determine what GPIOs can be configured as ADC Inputs.

NOTE: Any available GPIO can be used for SPI1_CS when in master mode.

Port 26–Port 29 in PAD 23/PAD 22/PAD 5/PAD 2

P[26:29] in PAD 23/PAD 22/PAD 5/PAD 2 consists of four pins. All pins are capable of sinking up to 16 mA for LEDs. These pins also have PWM functionality, which can be used for LED dimming.

For a description of the capabilities of all GPIOs, see Table 4.

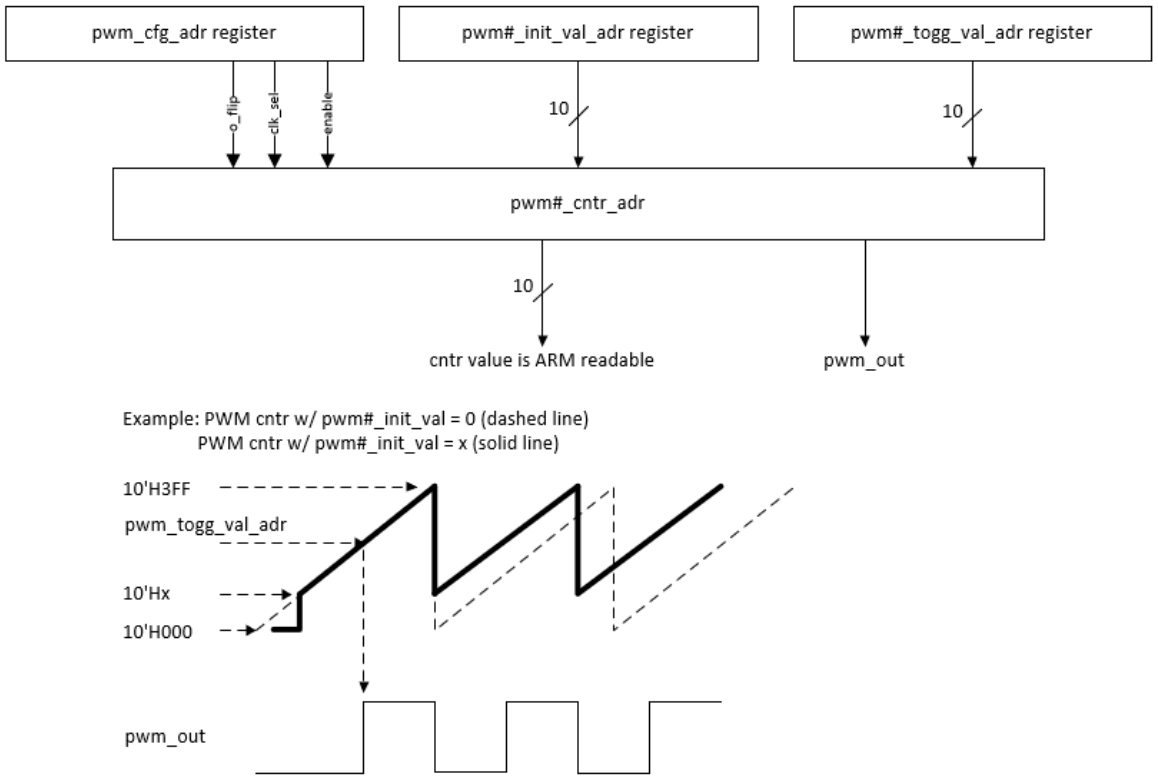
PWM

The CYBT-343026-01 has four PWMs. The PWM module consists of the following:

- PWM0-3
- The following GPIOs can be mapped as PWMs (the module pad is shown in [ ]):
  - PWM0: P26 on P11/P26 [Pad 23]
  - PWM1: P27 on P33/P27 [Pad 22]
  - PWM2: P28 on P2/P37/P28 [Pad 5]
  - PWM3: P29 on P3/P35/P29/I2C_SCL [Pad 2]
- PWM1-4: Each of the four PWM channels contains the following registers:
  - 10-bit initial value register (read/write)
  - 10-bit toggle register (read/write)
  - 10-bit PWM counter value register (read)
- PWM configuration register shared among PWM1-4 (read/write). This 12-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 12 shows the structure of one PWM.

Figure 12. PWM Block Diagram



Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4-GHz transceiver, which then processes the power-down functions accordingly.

Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in deep sleep (HIDOFF) mode.

BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the CYBT-343026-01 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYBT-343026-01 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF (Deep Sleep) mode

The CYBT-343026-01 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

In HIDOFF (Deep Sleep) mode, the CYBT-343026-01 baseband and core are powered off by disabling power to LDOOUT. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

Electrical Characteristics

Table 10 shows the maximum electrical rating for voltages referenced to V_{DDIN} pad.

Table 10. Maximum Electrical Rating

Rating	Symbol	Value	Unit
V_{DDIN}	–	3.795	V
Voltage on input or output pin	–	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating ambient temperature range	T_{opr}	–30 to +85	°C
Storage temperature range	T_{stg}	–40 to +85	°C

Table 11 shows the power supply characteristics for the range T_J = 0 to 125 °C.

Table 11. Power Supply

Parameter	Description	Minimum[6]	Typical	Maximum[6]	Unit
V_{DDIN}	Power Supply Input (CYBT-343026-01)	2.3	–	3.6	V
V_{DDIN_RIPPLE}	Maximum Power Supply Ripple for V_{DDIN} input voltage	–	–	100	mV

Table 12 shows the specifications for the digital voltage levels.

Table 12. Digital Voltage Levels

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.8	V
Input high voltage	V_{IH}	2.0	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	V_{DDIN} – 0.4	–	–	V
Input capacitance (V_{DDMEM} domain)	C_{IN}	–	–	0.4	pF

Table 13 shows the current consumption measurements

Table 13. Bluetooth, BLE, BR and EDR Current Consumption

Parameter	Description	Silicon or Module Parameter	Output Power Level/Class	Typ	Unit
Bluetooth Classic (BR, EDR)					
3DM5/3DH5	HCI control mode	Silicon	Class 1	37.1	mA
DM1/DH1	HCI control mode	Silicon	Class 1	32.2	mA
DM3/DH3	HCI control mode	Silicon	Class 1	38.2	mA
DM5/DH5	HCI control mode	Silicon	Class 1	38.5	mA
RX_{1M_BR}	Peak receive (1 Mbps) current level when receiving a basic rate packet (radio only)	Silicon	Class 1	26.4	mA
TX_{1M_BR}	Peak transmit (1 Mbps) current level when transmitting a basic rate packet (radio only)	Silicon	10 dBm	60.3	mA
RX_{23M_EDR}	Peak receive (EDR) current level when receiving a 2 or 3 Mbps rate packet (radio only)	Silicon	Class 1	26.4	mA
TX_{23M_EDR}	Peak transmit (EDR) current level when transmitting a 2 or 3 Mbps rate packet (radio only)	Silicon	8 dBm	52.5	mA

Note
6. Overall performance degrades beyond minimum and maximum supply voltages.The voltage range specified is determined by the minimum and maximum operating voltage of the SPI Serial Flash included on the module.