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PRELIMINARY

CYBT-423028-02

EZ-BT™ WICED® Module

General Description

The CYBT-423028-02 is a dual-mode Bluetooth® BR/EDR and Low Energy (BLE) wireless module solution. The CYBT-423028-02 includes onboard crystal oscillators, passive components, and the Cypress CYW20719 silicon device.

The CYBT-423028-02 supports a number of peripheral functions (ADC, PWM), as well as multiple serial communication protocols (UART, SPI, I^2C, I^2S/PCM). The CYBT-423028-02 includes a royalty-free BLE stack compatible with Bluetooth 5.0 in a small 11.0 × 11.0 × 1.70mm module form-factor.

The CYBT-423028-02 includes an integrated chip antenna, is qulaified by Bluetooth SIG, and includes regulatory certification approval for FCC, ISED, MIC, and CE.

Module Description

- Module size: 11.00 mm × 11.00 mm × 1.70 mm
- Complies with Bluetooth Core Specification version 5.0 and includes support for BR, EDR 2/3 Mbps, eSCO, BLE, and LE 2 Mbps features.
  - QDID: TBD
  - Declaration ID: TBD
- Certified to FCC, ISED, MIC, and CE standards
- 1024-KB flash memory, 512-KB SRAM memory
- Extended Industrial temperature range: –30 °C to +85 °C
- Integrated ARM Cortex-M4 microprocessor core with floating point unit (FPU)

RF Characteristics

- Maximum TX output power: +4.0 dbm
- RX Receive Sensitivity: –95.5 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution

Power Consumption

- TX current consumption
  - BLE silicon: 5.6 mA (MCU + radio only, 0 dbm)
- RX current consumption
  - Bluetooth silicon: 5.9 mA (MCU + radio only)
- Cypress CYW20719 silicon low power mode support
  - PDS: 61 µA with 512 KB SRAM retention
  - SDS: 1.6 uA
  - HIDOFF (External Interrupt): 400 nA

Functional Capabilities

- 1x ADC with (10-bit ENoB for DC measurement and 12-bit ENoB for Audio measurement) with 11 channels.
- 1x HCI UART for programming and HCI
- 1x peripheral UART (PUART)
- 2x SPI (master or slave mode) blocks (SPI, Quad SPI, and MIPI DBI-C)
- 1x I^2C master/slave and 1x I^2C master only
- I^2S/PCM audio interfaces
- Up to 6 16-bit PWMs
- Watchdog Timer
- Bluetooth Basic Rate (BR) and Enhanced Data Rate (EDR) Support
- BLE protocol stack supporting generic access profile (GAP) Central, Peripheral, or Broadcaster roles
- Hardware Security Engine

Benefits

CYBT-423028-02 is fully integrated and certified solution that provides all necessary components required to operate Bluetooth communication standards.

- Proven hardware design ready to use
- Ultra-flexible supermux I/O designs allows maximum flexibility for GPIO function assignment
- Large non-volatile memory for complex application development
- Over-the-air update capable for development or field updates
- Bluetooth SIG qualified with QDID and Declaration ID
- WICED™ Studio provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test your Bluetooth application

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

References

- Overview: EZ-BLE/EZ-BT Module Portfolio, Module Roadmap
- Development Kits:
  - CYBT-423028-EVAL, CYBT-423028-02 Evaluation Board
  - CYW920719Q40EVB-01, Evaluation Kit for CYW20719 silicon device
- Test and Debug Tools:
  - CYSmart, Bluetooth® LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)
- Knowledge Base Article
  - KBA97095 - EZ-BLE™ Module Placement
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
  - KBA218122 - 3D Model Files for EZ-BLE/EZ-BT Modules
  -

Development Environments

Wireless Connectivity for Embedded Devices (WICED) Studio Software Development Kit (SDK)

Cypress' WICED® (Wireless Connectivity for Embedded Devices) is a full-featured platform with proven Software Development Kits (SDKs) and turnkey hardware solutions from partners to readily enable Wi-Fi and Bluetooth® connectivity in system design.

WICED Studio is the only SDK for the Internet of Things (IoT) that combines Wi-Fi and Bluetooth into a single integrated development environment. In addition to providing WICED APIs and an application framework designed to abstract complexity, WICED Studio also leverages many common industry standards.

Technical Support

- Cypress Community: Whether you're a customer, partner or a developer interested in the latest Cypress innovations, the Cypress Developer Community offers you a place to learn, share and engage with both Cypress experts and other embedded engineers around the world.
- Frequently Asked Questions (FAQs): Learn more about our Bluetooth ECO System.
- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

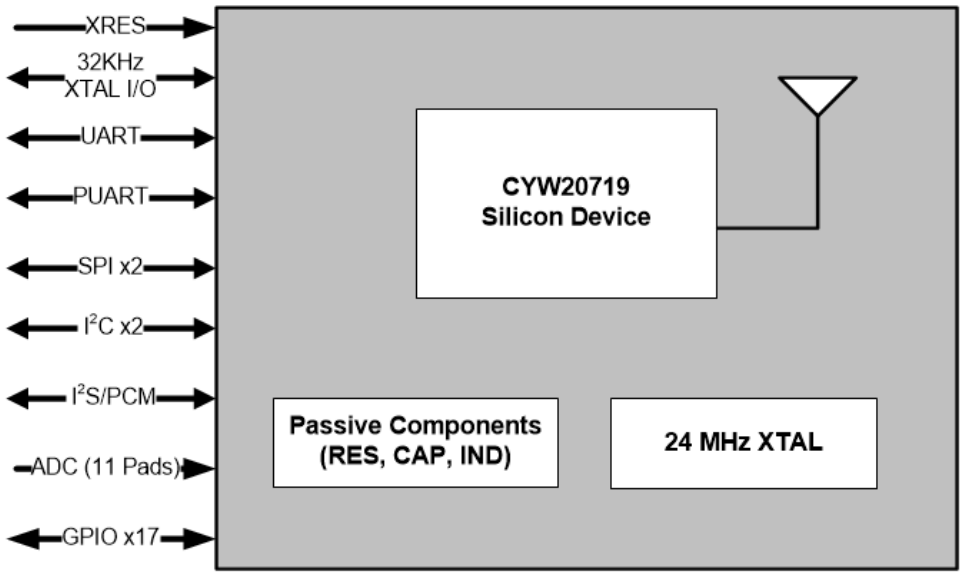
Contents

Overview

Functional Block Diagram

Figure 1 illustrates the CYBT-423028-02 functional block diagram.

Figure 1. Functional Block Diagram



Note: General Purpose Input/Output pins shown in Figure 1 are configuratble to any specified input or output function in the SuperMux table detailed in Table 5 in the Module Connections section.

Note: Connections shown in the above block diagram are maximum number of connections per function. The total number of GPIOs available on the CYBT-423028-02 is 17.

Module Description

The CYBT-423028-02 module is a complete module designed to be soldered to the applications main board.

Module Dimensions and Drawing

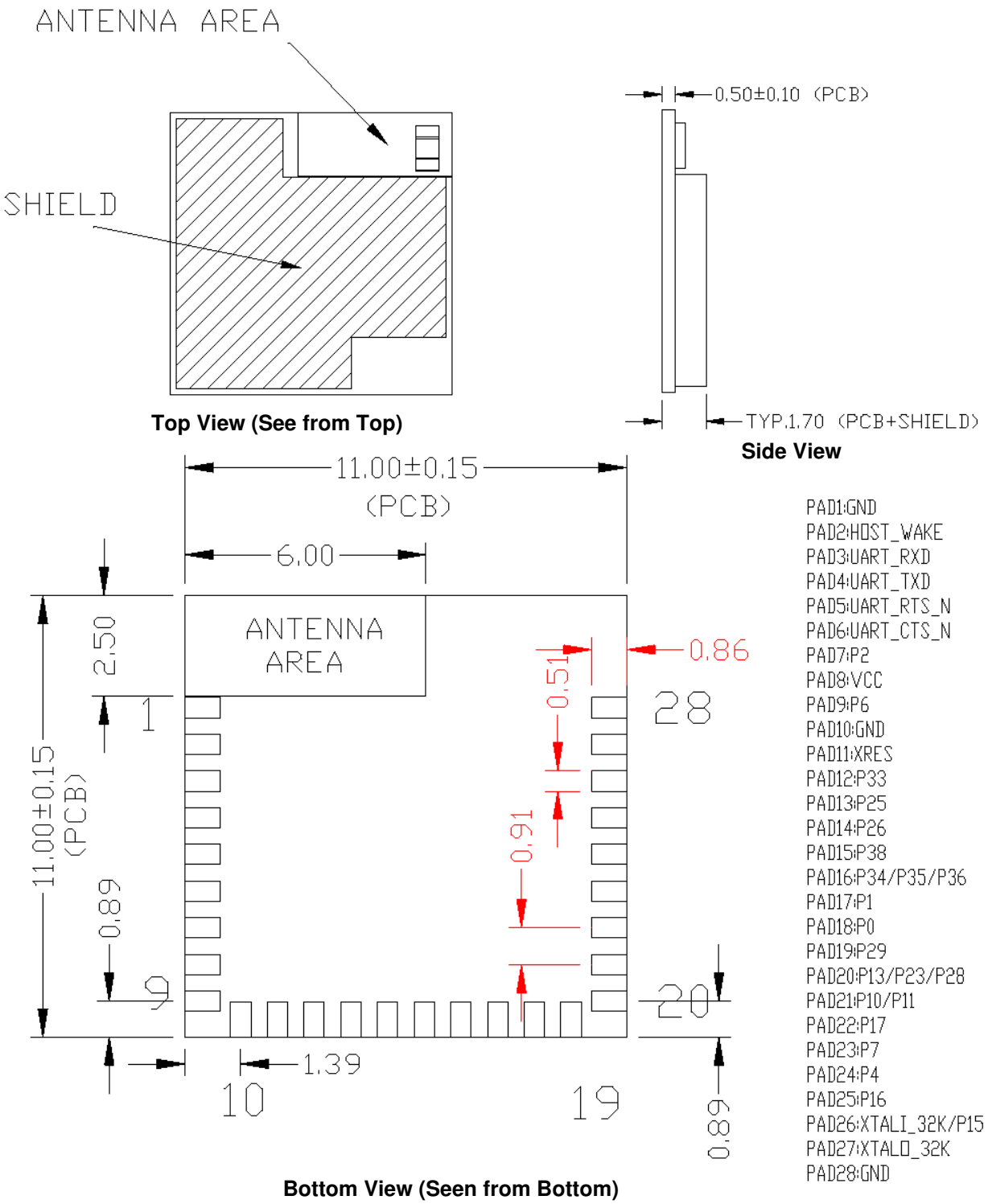
Cypress reserves the right to select components from various vendors to achieve the Bluetooth module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Any changes to the current BOM for the CYBT-423028-02 will not be made until approval is provided by the end customer for this product. The CYBT-423028-02 will be held within the physical dimensions shown in the mechanical drawings in Figure 2 on page 5. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	11.00 ± 0.15 mm
	Width (Y)	11.00 ± 0.15 mm
Antenna location dimensions	Length (X)	6.00 mm
	Width (Y)	2.50 mm
PCB thickness	Height (H)	0.50 ± 0.10 mm
Shield height	Height (H)	1.20 mm
Maximum component height	Height (H)	0.60 mm typical
Total module thickness (bottom of module to top of shield)	Height (H)	1.70 mm typical

See Figure 2 for the mechanical reference drawing for CYBT-423028-02.

Figure 2. Module Mechanical Drawing



Notes
1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see "Recommended Host PCB Layout" on page 7.

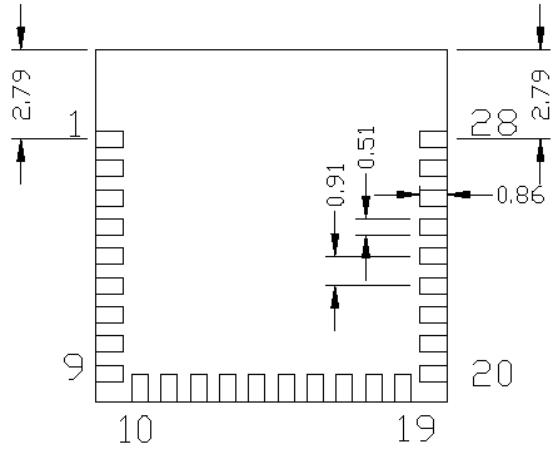
Pad Connection Interface

As shown in the bottom view of Figure 2 on page 5, the CYBT-423028-02 has 28 connections to a host board via solder pads (SP). Table 2 and Figure 3 detail the solder pad length, width, and pitch dimensions of the CYBT-423028-02 module.

Table 2. Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	28	Solder Pad	0.86 mm	0.51 mm	0.91 mm

Figure 3. Solder Pad Dimensions (Seen from Bottom)

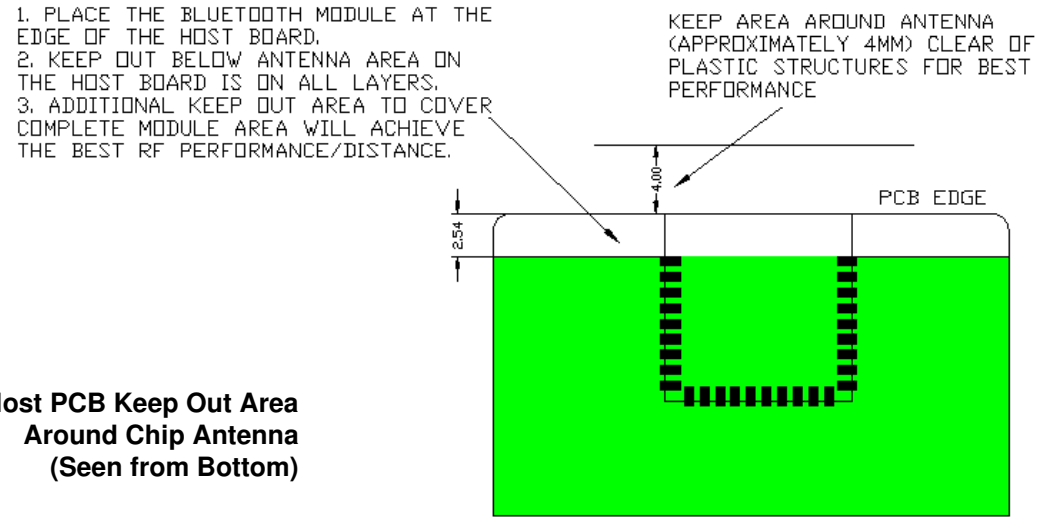


Solder Pad Connections (Seen from Bottom)

To maximize RF performance, the host layout should follow these recommendations:

1. Antenna Area Keepout: The host board directly below the antenna area of the Cypress module (see Figure 2 on page 5) must contain no ground or signal traces. This keep out area requirement applies to all layers of the host board.
2. Module Placement: The ideal placement of the Cypress Bluetooth module is in a corner of the host board with the chip antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 3 below. Please refer to AN96841 for module placement best practices.
3. Optional Keepout: To maximize RF performance, the area immediately around the Cypress Bluetooth module chip antenna may contain an additional keep out area, where there are no grounding or signal traces. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in Figure 4 (dimensions are in mm).

Figure 4. Optional Additional Host PCB Keep Out Area Around the CYBT-423028-02 Chip Antenna

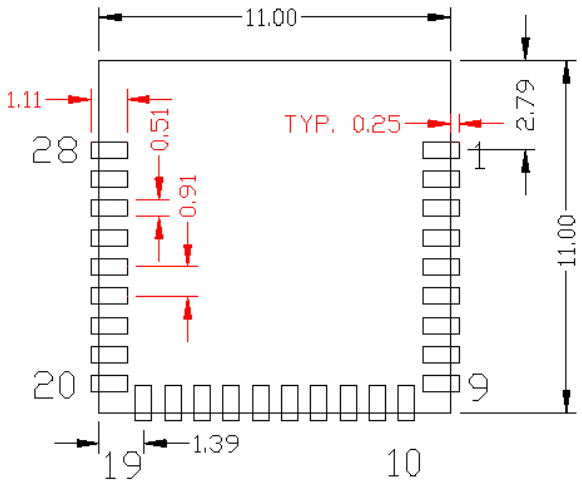


Optional Host PCB Keep Out Area Around Chip Antenna (Seen from Bottom)

Recommended Host PCB Layout

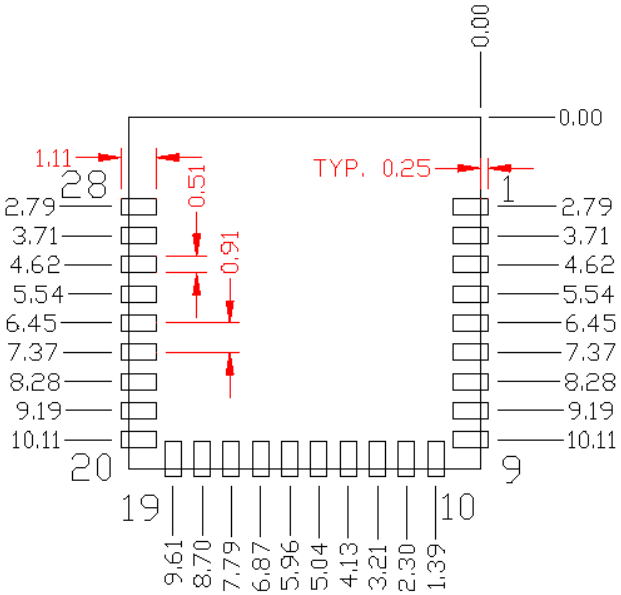
Figure 5, Figure 6, Figure 7, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBT-423028-02. Dimensions are in millimeters unless otherwise noted. Pad length of 1.11 mm (0.56 mm from center of the pad on either side) shown in Figure 7 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 5, Figure 6, or Figure 7. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 5. CYBT-423028-02 Host Layout (Dimensioned)



Top View (Seen on Host PCB)

Figure 6. CYBT-423028-02 Host Layout (Relative to Origin)



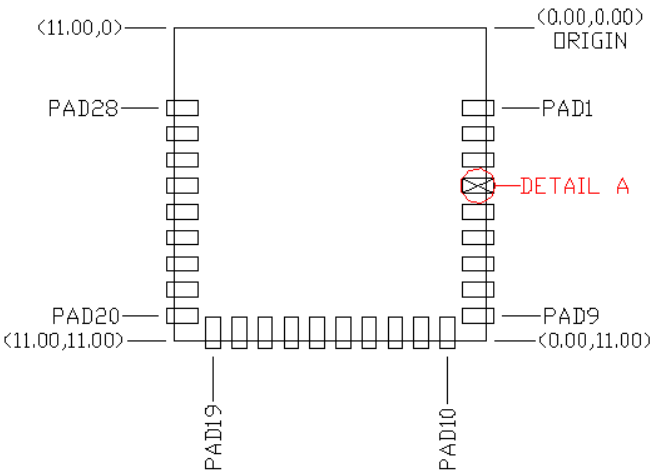
Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBT-423028-02. All dimensions are referenced to the center of the solder pad. Refer to Figure 7 for the location of each module solder pad.

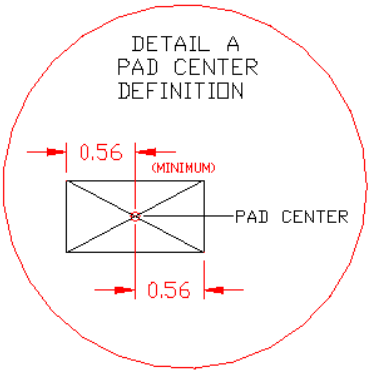
Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Dimension from Origin (mils)
1	(0.31, 2.79)	(12.20, 109.84)
2	(0.31, 3.71)	(12.20, 146.06)
3	(0.31, 4.62)	(12.20, 181.89)
4	(0.31, 5.54)	(12.20, 218.11)
5	(0.31, 6.45)	(12.20, 253.94)
6	(0.31, 7.37)	(12.20, 290.16)
7	(0.31, 8.28)	(12.20, 325.98)
8	(0.31, 9.19)	(12.20, 361.81)
9	(0.31, 10.11)	(12.20, 398.03)
10	(1.39,10.69)	(54.72, 420.87)
11	(2.30,10.69)	(90.55, 420.87)
12	(3.21,10.69)	(126.38, 420.87)
13	(4.13,10.69)	(162.60, 420.87)
14	(5.04,10.69)	(198.42, 420.87)
15	(5.96,10.69)	(234.65, 420.87)
16	(6.87,10.69)	(270.47, 420.87)
17	(7.79,10.69)	(306.69, 420.87)
18	(8.70,10.69)	(342.52, 420.87)
19	(9.61,10.69)	(378.35, 420.87)
20	(10.69,10.11)	(420.87, 398.03)
21	(10.69,9.19)	(420.87, 361.81)
22	(10.69,8.28)	(420.87, 325.98)
23	(10.69,7.37)	(420.87, 290.16)
24	(10.69,6.45)	(420.87, 253.94)
25	(10.69,5.54)	(420.87, 218.11)
26	(10.69,4.62)	(420.87, 181.89)
27	(10.69,3.71)	(420.87, 146.06)
28	(10.69,2.79)	(420.87, 109.84)

Figure 7. Solder Pad Reference Location



Top View (Seen on Host PCB)



Module Connections

Table 4 details the solder pad connection definitions and available functions for each connection pad. The GPIO connections available on the CYBT-423028-02 can be configured to any of the input or output functions listed in Table 5. Table 4 specifies any function that is required to be used on a specific solder pad, and also identifies GPIOs that can be configured using the SuperMux.

Table 4. CYBT-423028-02 Solder Pad Connection Definitions

Pad	Pad Name	Silicon Pin Name	XTALI/O	ADC	GPIO	SuperMux Capable[2]
1	GND	GND	Ground			
2	HOST_WAKE	BT_HOST_WAKE	A signal from the CYBT-423028-02 module to the host indicating that the Bluetooth device requires attention.			
3	UART_RXD	BT_UART_RXD	UART (HCI UART) Receive Data Only			
4	UART_TXD	BT_UART_TXD	UART (HCI UART) Transmit Data Only			
5	UART_RTS_N	BT_UART_RTS_N	UART (HCI UART) Request To Send Output Only			
6	UART_CTS_N	BT_UART_CTS_N	UART (HCI UART) Clear To Send Input Only			
7	P2	P2	-	-	✓	✓ see Table 5
8	VCC	VDDIO	Power Supply Input (1.76V ~ 3.63V)			
9	P6	P6	-	-	✓	✓ see Table 5
10	GND	GND	Ground			
11	XRES	RST_N	External Reset (Active Low)			
12	P33	P33	-	IN6	✓	✓ see Table 5
13	P25	P25	-	-	✓	✓ see Table 5
14	P26	P26	-	-	✓	✓ see Table 5
15	P38	P38	-	IN1	✓	✓ see Table 5
16	P34/P35/P36	P34 P35 P36	-	IN5 (P34) IN4 (P35) IN3 (P36)	✓ (P34/P35/P36)	✓ see Table 5
17	P1	P1	-	IN28	✓	✓ see Table 5
18	P0	P0	-	IN29	✓	✓ see Table 5
19	P29	P29	-	IN10	✓	✓ see Table 5
20	P13/P23/P28	P13 P23 P28	-	IN22 (P13) IN12 (P23) IN11 (P28)	✓(P13/P23/P28)	✓ see Table 5
21	P10/P11	P10 P11	-	IN25 (P10) IN24 (P11)	✓ (P10/P11)	✓ see Table 5
22	P17	P17	-	IN18	✓	✓ see Table 5
23	P7	P7	-	-	✓	-
24	P4	P4	-	-	✓	-
25	P16	P16	-	IN19	✓	-
26	XTALI_32K/ P15[3]	XTALI_32K P15	External Oscillator Input (32KHz)	IN20 (P15)	✓(P15)	✓(P15), see Table 5
27	XTALO_32K	XTALO_32K	External Oscillator Output (32KHz)	-	-	-
28	GND	GND	Ground			

Table 5 details the available Input and Output functions that are configurable to any solder pad in Table 4 that are marked as SuperMux capable.

Note
2. The CYBT-423028-02 can configure GPIO connections to any Input/Output function described in Table 5.
3. P15 should not be driven high externally while the part is held in reset (it can be floating or driven low). Failure to do so may cause some current to flow through P15 until the device comes out of reset.

Table 5. GPIO SuperMux Input and Output Functions

Function	Input or Output	Function Type	GPIOs Required	Function Connection Description
SWD	Input	Serial Communication and Debug	2	SWDCK, Serial Wire Debugger Clock
	Input/Output			SWDIO, Serial Wire Debugger I/O
SPI 1	Input/Output	Serial Communication (Master or Slave)	4 ~ 8	SPI 1 Clock
				SPI 1 Chip Select
				SPI 1 MOSI
				SPI 1 MISO
				SPI 1 I/O 2 (Quad SPI)
				SPI 1 I/O 3 (Quad SPI)
				SPI 1 Interrupt
	Output			SPI 1 DCX (DBI-C DCX 8-bit mode)
SPI 2	Input/Output	Serial Communication (Master or Slave)	4 ~ 8	SPI 2 Clock
				SPI 2 Chip Select
				SPI 2 MOSI
				SPI 2 MISO
				SPI 2 I/O 2 (Quad SPI)
				SPI 2 I/O 3 (Quad SPI)
				SPI 2 Interrupt
	Output			SPI 2 DCX (DBI-C DCX 8-bit mode)
PUART	Input	Serial Communication Input	4	Peripheral UART RX
				Peripheral UART CTS
	Output	Serial Communication Output		Peripheral UART TX
				Peripheral UART RTS
I^2C	Input/Output	Serial Communication (Master or Slave)	2	I2C Clock
				I2C Data
I^2C 2	Input/Output	Serial Communication (Master or Slave)	2	I2C 2 Clock
				I2C 2 Data
PCM In	Input	Audio Input Communication	3	PCM Input
				PCM Clock
				PCM Sync
PCM Out	Output	Audio Output Communication	3	PCM Output
				PCM Clock
				PCM Sync
I^2S In	Input	Audio Input Communication	3	I2S DI, Data Input
				I2S WS, Word Select
				I2S Clock
I^2S Out	Output	Audio Output Communication	3	I2S DO, Data Output
				I2S WS, Word Select
				I2S Clock
PDM	Input	Microphone	1 ~ 2	PDM Input Channel 1
				PDM Input Channel 2
PWM	Output	Pulse Width Modulator	1 ~ 6	PWM Channel 0
				PWM Channel 1
				PWM Channel 2
				PWM Channel 3
				PWM Channel 4
				PWM Channel 5

Function	Input or Output	Function Type	GPIOs Required	Function Connection Description
ACLK	Output	Auxiliary Clock	1 ~ 2	Auxiliary Clock 0 (ACLK0)
				Auxiliary Clock 1 (ACLK1)
HIDOFF	Output	HID-OFF Indicator	1	HID-OFF Indicator to host

Connections and Optional External Components

Power Connections (VDD)

The CYBT-423028-02 contains one power supply connection, VDD.

VDD accepts a supply input of 1.76 V to 3.63 V. Table 12 provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in Table 12.

Considerations and Optional Components for Brown Out (BO) Conditions

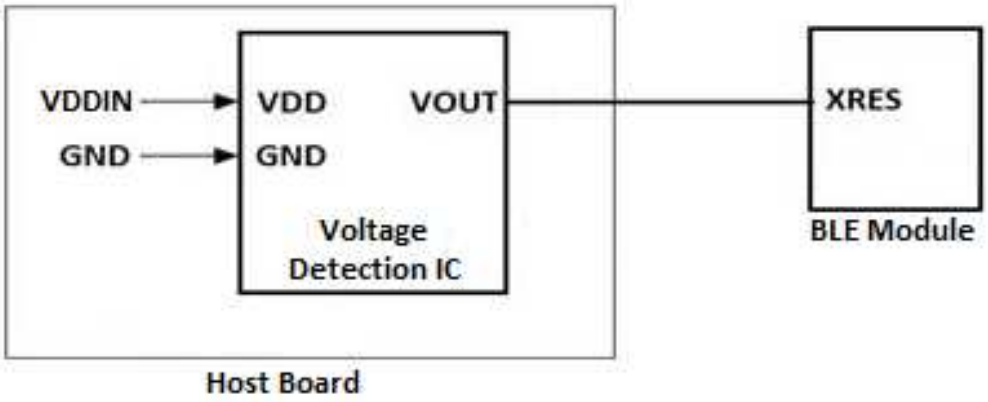
Power supply design must be completed to ensure that the CYBT-423028-02 module does not encounter a Brown Out condition, which can lead to unexpected functionality, or module lock up. A Brown Out condition may be met if power supply provided to the module during power up or reset is in the range shown below:

$$V_{IL} \leq VDD \leq V_{IH}$$

Refer to Table 16 for the V_{IL} and V_{IH} specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (i.e. battery installation, high value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brown Out voltage range from occurring during power removal. Please refer to Figure 8 for the recommended circuit design when using an external voltage detection IC.

Figure 8. Reference Circuit Block Diagram for External Voltage Detection IC



In the event that the module does encounter a Brown Out condition, and is operating erratically or not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brown Out conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brown Out condition.

External Reset (XRES)

The CYBT-423028-02 has an integrated power-on reset circuit which completely resets all circuits to a known power on state. This action can also be evoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYBT-423028-02 module (solder pad 11). The CYBT-423028-02 module does not require an external pull-up resistor on the XRES input

During power on operation, the XRES connection to the CYBT-423028-02 is required to be held low 50 ms after the VDD power supply input to the module is stable. This can be accomplished in the following ways:

- The host device can connect a GPIO to the XRES of Cypress CYBT-423028-02 module and pull XRES low until VDD is stable. XRES is recommended to be released 50 ms after VDD is stable.
- If the XRES connection of the CYBT-423028-02 module is not used in the application, a 0.33 uF capacitor may be connected to the XRES solder pad of the CYBT-423028-02 in order to delay the XRES release. The capacitor value for this recommended imple-

mentation is approximate, and the exact value may differ depending on the VDD power supply ramp time of the system. The capacitor value should result in an XRES release timing of at least 50 ms after VDD stability.

- The XRES release timing may be controlled by a external voltage detection IC. XRES should be released 50 ms after VDD is stable.

Refer to Figure 11 on page 18 for XRES operating and timing requirements during power on events.

HCI UART Connections

The recommendations in this section apply to the HCI UART (Solder Pads 3, 4, 5, and 6). For full UART functionality, all UART signals must be connected to the Host device. If full UART functionality is not being used, and only UART RXD and TXD are desired or capable, then the following connection considerations should be followed for UART RTS and CTS:

- UART RTS: Can be left floating, pulled low, or pulled high. RTS is not critical for initial firmware uploading at power on.
- UART CTS: Must be pulled low to bypass flow control and to ensure that continuous data transfers are made from the host to the module.

External Component Recommendation

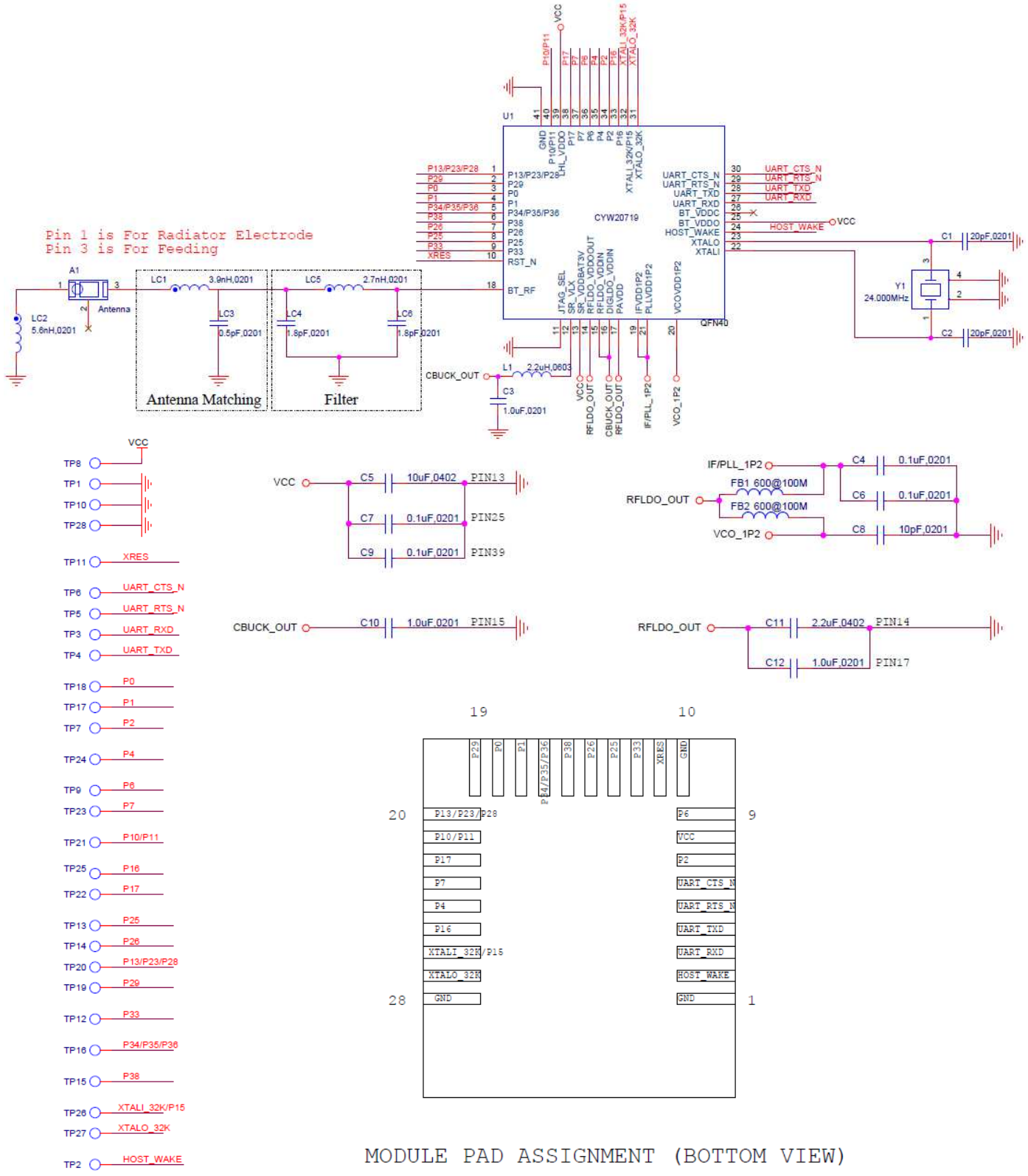
Power Supply Circuitry

It is not required to place any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included. The ferrite bead should be positioned as close as possible to the module pad connection.

If used, the recommended ferrite bead value is 330 Ω, 100 MHz. (Murata BLM21PG331SN1D).

Figure 9 illustrates the CYBT-423028-02 schematic.

Figure 9. CYBT-423028-02 Schematic Diagram



Critical Components List

Table 6 details the critical components used in the CYBT-423028-02 module.

Table 6. Critical Component List

Component	Reference Designator	Description
Silicon	U2	40-pin QFN Bluetooth Silicon Device - CYW20719
Chip Antenna	A1	Antenna, 2.4 GHz
Crystal	Y1	24.000 MHz, 12PF

Antenna Design

Table 7 details the chip antenna used in the CYBT-423028-02 module.

Table 7. Chip Antenna Specifications

Item	Description
Frequency Range	2400 – 2500 MHz
Peak Gain	-1.0 dBi typical
Return Loss	10.0 dB typical

Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It prioritizes and schedules all RX/TX activities including adv, paging, scanning, and servicing of connections. In addition to these functions, it independently handles the host controller interface (HCI) including all commands, events, and data flowing over HCI. The core also handles symbol timing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), authentication, data encryption/decryption, and data whitening/dewhitening.

Table 8. Bluetooth Features

Bluetooth 1.0	Bluetooth 1.2	Bluetooth 2.0
Basic Rate	Interlaced Scans	EDR 2 Mbps and 3 Mbp
SCO	Adaptive Frequency Hopping	–
Paging and Inquiry	eSCO	–
Page and Inquiry Scan	–	–
Sniff	–	–
Bluetooth 2.1	**Bluetooth 3.0**	**Bluetooth 4.0**
Secure Simple Pairing	Unicast Connectionless Data	Bluetooth Low Energy
Enhanced Inquiry Response	Enhanced Power Control	–
Sniff Subrating	eSCO	–
Bluetooth 4.1	**Bluetooth 4.2**	**Bluetooth 5.0**
Low Duty Cycle Advertising	Data Packet Length Extension	LE 2 Mbps
Dual Mode	LE Secure Connection	Slot Availability Mask
LE Link Layer Topology	Link Layer Privacy	High Duty Cycle Advertising

BQB and Regulatory Testing Support

The CYBT-423028-02 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loop back tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYBT-423028-02 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

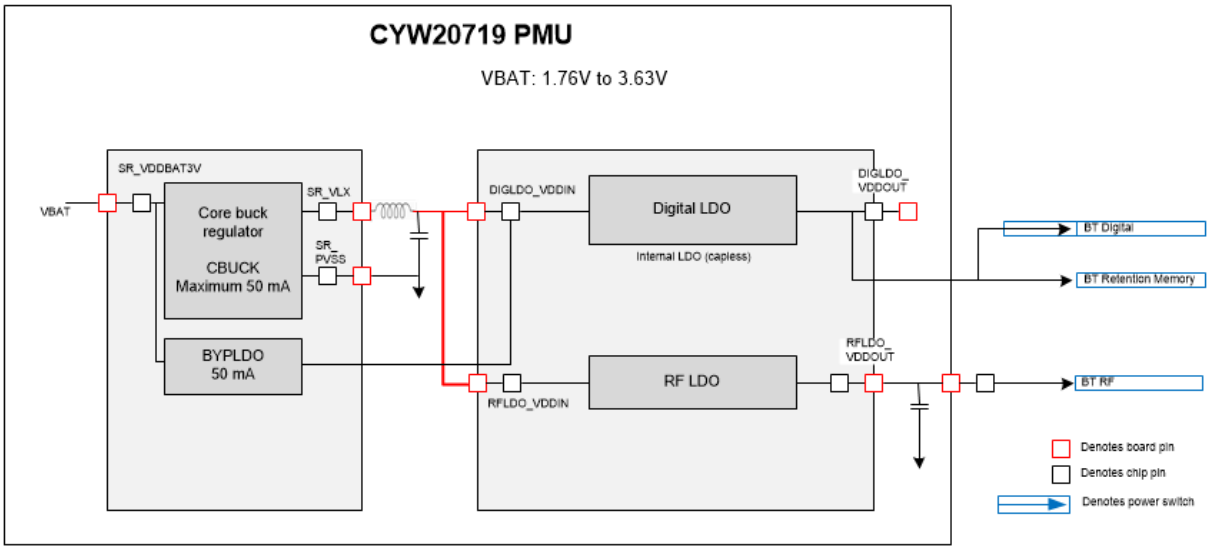
- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

Power Management Unit

Figure 10 shows the CYW20719 power management unit (PMU) block diagram. The CYW20719 includes an integrated buck regulator, a bypass LDO, a capless LDO for digital circuits and a separate LDO for RF. The bypass LDO automatically takes over from the buck once V_{bat} supply falls below 2.1V.

The voltage levels shown in this figure are the default settings; the firmware may change voltage levels based on operating conditions.

Figure 10. Default Usage Mode



Integrated Radio Transceiver

The CYBT-423028-02 has an integrated radio transceiver that has been designed to provide low power operation in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with Bluetooth Radio Specification 3.0 and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

CYBT-423028-02 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

Power Amplifier

The CYBT-423028-02 has an integrated power amplifier (PA) that can transmit up to +4 dBm for class 2 operation.

Receiver Path

The receiver path uses a low IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, and an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYBT-423028-02 to be used in most applications without off-chip filtering.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYBT-423028-02 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The CYBT-423028-02 uses an internal loop filter.

Microcontroller Unit

The CYBT-423028-02 includes a Cortex M4 processor with 2 MB of ROM, 448 KB of data RAM, 64 KB of patch RAM, and 1 MB of on-chip flash. The CM4 has a maximum speed of 96 MHz. CYBT-423028-02 supports execution from on-chip flash (OCF).

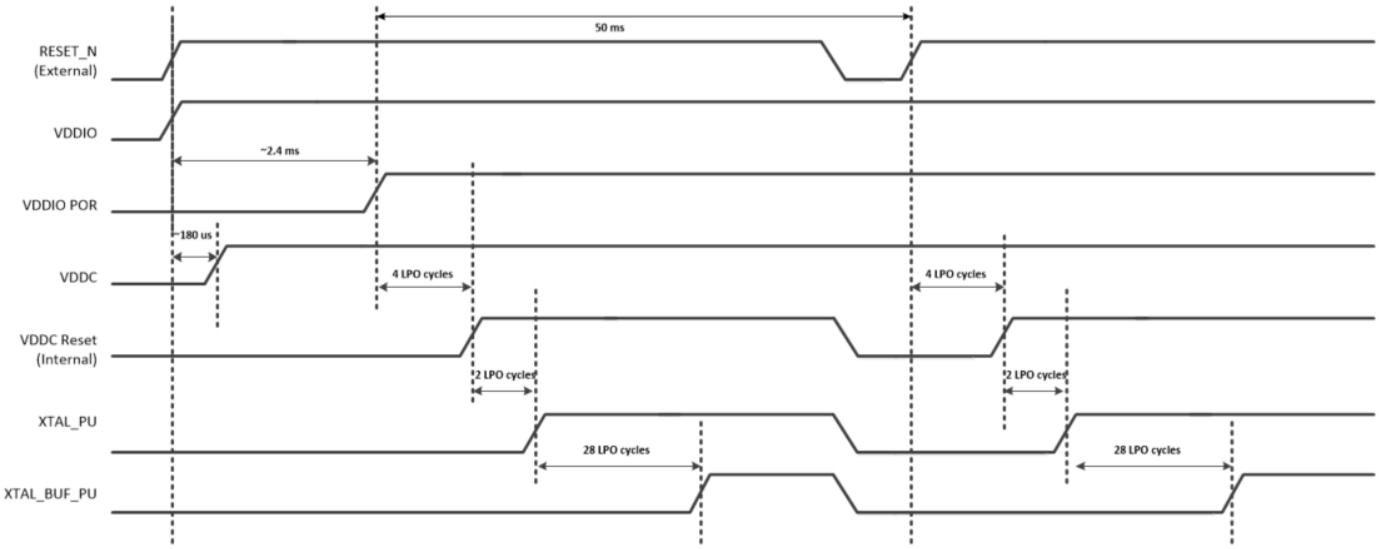
The CM4 also includes a single precision IEEE 754 compliant floating point unit (FPU).

The CM4 runs all the BT layers as well as application code. The ROM includes LM, HCI, L2CAP, GATT, as well as other stack layers freeing up the flash for application usage. A standard serial wire debug (SWD) interface provides debugging support.

External Reset

An external active-low reset signal, XRES, can be used to put the CYBT-423028-02 in the reset state. An external voltage detector reset IC with 50 ms delay is recommended on the XRES connection. The XRES must only be released after the VDDO supply voltage level has been stabilized for 50 ms.

Figure 11. Reset Timing



Peripheral and Communication Interfaces

I²C

The CYBT-423028-02 provides a 2-pin I²C compatible master interface to communicate with I²C compatible peripherals. The following transfer clock rates are supported are:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I²C-compatible speed)
- 1 MHz (Compatibility with high-speed I²C-compatible devices is not guaranteed)

SCL and SDA lines can be routed to any of the P0-P39 GPIOs allowing for flexible system configuration. When used as SCL/SDA the GPIOs go into open drain mode and require an external pull-up for proper operation. I²C block does not support multi master capability by either master or slave devices.

I²C1 is Master Only; I²C2 is Master/Slave. The Slave support is subject to driver support in WICED Studio.

HCI UART Interface

The CYBT-423028-02 includes a UART interface for factory programming as well as when operating as a BT HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 1.5 Mbps. Typical rates are 115200, 921600, 1500000 bps although intermediate speeds are also available. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command. The CYBT-423028-02 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%. The UART interface has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The CYBT-423028-02 can wake up the host as needed or allow the host to sleep via the HOST_WAKE signal (solder pad 2). signal allows the CYBT-423028-02 to optimize system power consumption by allowing a host device to remain in low power modes as long as possible. The HOST_WAKE signal can be enabled via a vendor specific command.

Peripheral UART Interface

The CYBT-423028-02 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYBT-423028-02 can map the peripheral UART to any GPIO. The Peripheral UART functionality is the same as the HCI UART, but with a 256-byte transmit and receive FIFO.

Serial Peripheral Interface

The CYBT-423028-02 has two independent SPI interfaces. Both interfaces support Single, Dual, and Quad mode SPI operations as well as MIPI DBI-C Interface.Either of the interface can be a master or a slave. SPI2 can support only 1 slave. SPI1 has a 1024 byte transmit and receive buffers which is shared with the host UART interface. SPI2 has a dedicated 256 byte transmit and receive buffers. To support more flexibility for user applications, the CYBT-423028-02 has optional I/O ports that can be configured individually and separately for each functional pin. SPI IO voltage depends on VDDO.

MIPI interface

There are three options in DBI type-C corresponding to 9-bit, 16-bit, and 8-bit modes. The CYBT-423028-02 plays the role of host, and only the 9-bit and 8-bit modes (option 1 and option 3 in DBI-C spec) are supported. In the 9-bit mode, the SCL, CS, MOSI, and MISO pins are used. In the 8-bit mode, an additional pin (DCX) is required. The DCX pin indicates if the current outgoing bit stream is a command or data byte.

32 kHz Crystal Oscillator

The CYBT-423028-02 uses the built-in Local Oscillator (LO) on the CYW20719 silicon device for 32kHz timing. The accuracy of the LO is +/- 500 ppm. The use of an external XTAL oscillator is optional. CYBT-423028-02 includes external XTAL oscillator connections for applications requiring higher timing accuracy. Figure 12 shows an external 32 kHz XTAL oscillator with external components and Table 9 lists the recommended external oscillator's characteristics. This oscillator input can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at similar frequency. The default component values are: R1 = 10 MΩ and C1 = C2 = ~6 pF. The values of C1 and C2 are used to fine-tune the oscillator.

Figure 12. 32 kHz Oscillator Block Diagram

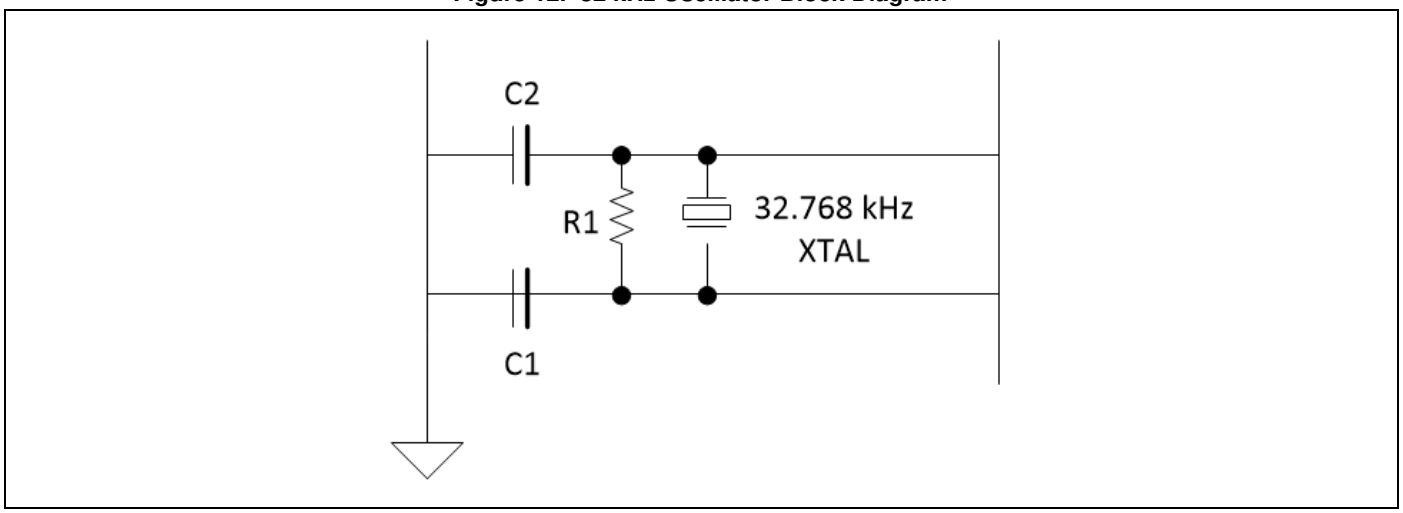


Table 9. XTAL Oscillator Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Crystal-dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	500	–	ms
XTAL drive level	P_{drv}	For crystal selection	–	–	0.5	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	–	–	2.2	pF
External AC Input Amplitude	V_{IN} (AC)	C_{couple} = 100 pF; R_{bias}= 10 Mohm	400	–	–	mVpp

ADC Port

The ADC is a Σ-Δ ADC core designed for audio (13 bits) and DC (10 bits) measurement. It operates at 12 MHz and has 11 solder pad connections that can act as input channels. The internal bandgap reference has ±5% accuracy without calibration. Calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

The following CYBT-423028-02 module solder pads can be used as ADC inputs:

- Pad 12: P33, ADC Input Channel 6
- Pad 15: P38, ADC Input Channel 1
- Pad 16: P34/P35/P36, ADC Input Channels 5/4/3 respectively; NOTE: only one ADC input on this solder pad can be active at a given time.
- Pad 17: P1, ADC Input Channel 28
- Pad 18: P0, ADC Input Channel 29
- Pad 19: P29, ADC Input Channel 10
- Pad 20: P13/P23/28, ADC Input Channels 22/12/11 respectively; NOTE: only one ADC input on this solder pad can be active at a given time.
- Pad 21: P10/P11, ADC Input Channels 25/24 respectively; NOTE: only one ADC input on this solder pad can be active at a given time.
- Pad 22: P17, ADC Input Channel 18
- Pad 25: P16, ADC Input Channel 19
- Pad 26: P15, ADC Input Channel 20

GPIO Ports

The CYBT-423028-02 has a maximum of 17 general-purpose I/Os (GPIOs). All GPIOs support the following:

- Programmable pull-up/down of approximately 45 KOhms.
- Input disable, allowing pins to be left floating or analog signals connected without risk of leakage.
- Source/sink 8 mA at 3.3V and 4 mA at 1.8V.
- P15 is Bonded to the same pin as XTALI_32K (Pad 26). If an External 32.768KHz crystal is not used, then this pin can be used as GPIO P15.
- P26/P28/P29 can sink/source 16 mA at 3.3V and 8 mA at 1.8V.

Most peripheral functions can be assigned to any GPIO. For details, refer to Table 5. For more details on Supermux configuration and control, refer to "Supermux Wizard for CYW20719" user guide.

The list below details the GPIOs that are available on the CYBT-423028-02 module:

- P0-P2, P4, P6, P7, P16, P17, P25, P26, P29, P33, and P38
- P10/P11 (Double bonded connection on the CYBT-423028-02 module, only one of two is available)
- P13/P23/P28 (Triple bonded connection on the CYBT-423028-02 module, only one of three is available)
- P15/XTALI_32K (Double bonded pin on the CYBT-423028-02 module, only one of two is available)
- P34/P35/P36 (Triple bonded pin on the CYBT-423028-02 module, only one of three is available)
- P19, P20 and P39 are reserved for system use. Please do not use those 3 GPIOs.

For GPIOs highlighted as double or triple bonded connections, only one of the connections can be used at a given time. When a certain GPIO is selected, the other GPIOs bonded to the same connection must be configured to input with output disable.

PWM

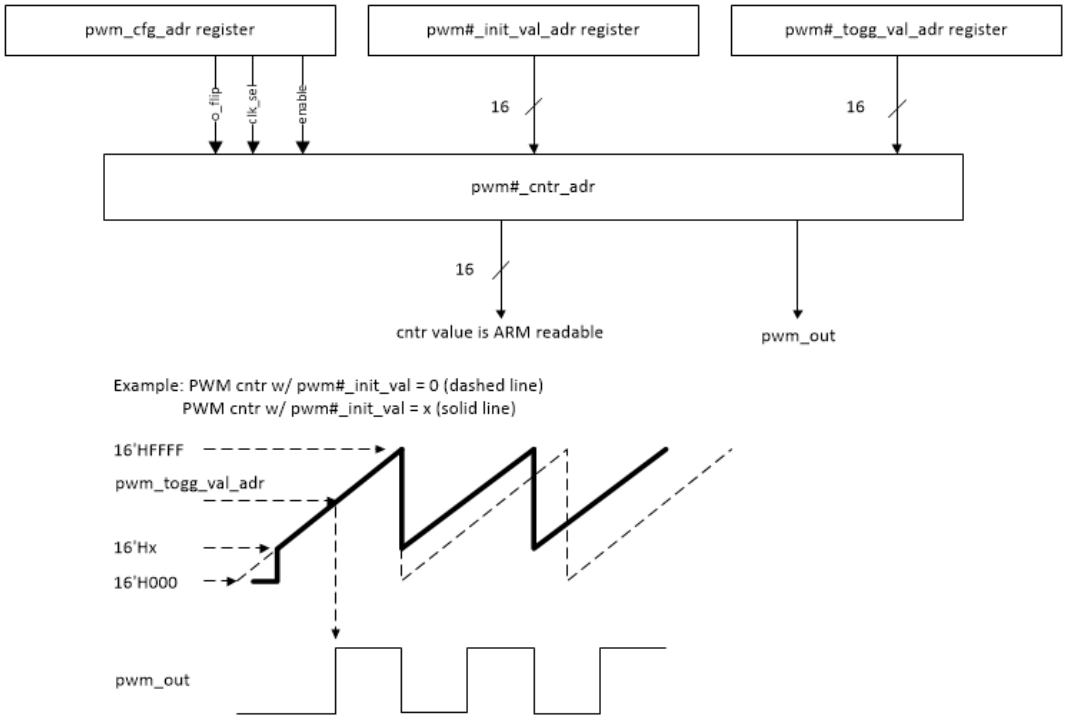
The CYBT-423028-02 has six internal PWMs, labeled PWM0-5. The PWM module consists of the following:

- Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0–5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

The application can access the PWM module through the FW driver.

Figure 13 shows the structure of one PWM channel.

Figure 13. PWM Block Diagram



PDM Microphone

The CYBT-423028-02 accepts a ΣΔ-based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The PDM input shares the filter path with the auxADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone takes in a 2.4 MHz clock generated by the CYBT-423028-02 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

Note: Subject to the driver support in WICED Studio.

I^2S Interface

The CYBT-423028-02 supports a single I^2S digital audio port. with both master and slave modes. The I^2S signals are:

- I^2S Clock: I^2S SCK
- I^2S Word Select: I^2S WS
- I^2S Data Out: I^2S DO
- I^2S Data In: I^2S DI

I^2S SCK and I^2S WS become outputs in master mode and inputs in slave mode, while I^2S DO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSN of the left-channel data is aligned with the MSB of the I^2S bus, per I^2S Specifications. The MSB of each data word is transmitted one bit clock cycle after the I^2S WS transition, synchronous with the falling edge of bit clock. Left Channel data is transmitted when I^2S WS is low, and right-channel data is transmitted when I^2S WS is high. Data bits sent by the CYBT-423028-02 are synchronized with the falling edge of I^2S SCK and should be sampled by the receiver on the rising edge of the I^2S SCK.

Note: The PCM interface shares HW with the I^2S interface and only one can be used at a given time.

PCM Interface

The CYBT-423028-02 includes a PCM interface that can connect to linear PCM codec devices in master or slave mode. In master mode, the CYBT-423028-02 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYBT-423028-02.The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Note: The PCM interface shares HW with the I^2S interface and only one can be used at a given time.

Slot Mapping

The CYBT-423028-02 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM Interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The CYBT-423028-02 supports both short- and long-frame synchronization in both master and slave modes. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCGM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The CYBT-423028-02 may be configured to generate and accept several different data formats. For conventional narrow band speech mode, the CYBT-423028-02 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

Security Engine

The CYBT-423028-02 includes a hardware security accelerator which greatly decreases the time required to perform typical security operations. Access to the hardware block is provided via a firmware interface (see firmware documentation for details).Thie security engine includes:

- Public key acceleration (PKA) cryptography
- AES-CTR/CBC-MAC/CCM acceleration
- SHA2 message hash and HMAC acceleration
- RSA encryption and decryption of modulus sizes up to 2048 bits
- Elliptic curve Diffie-Hellman in prime field GF(p)

Note: Security Engine is used only by the Bluetooth stack to reduce CPU overhead. It is not available for application use.

Random Number Generator

This hardware block is used for key generation for Bluetooth.

Note: Availability for use by the application is subject to the support in WICED Studio.

Note: The Random Number Generator block must be warmed up prior to use. A delay of 500 ms from cold boot is necessary prior to using the Random Number Generator.

Power Modes

The CYBT-423028-02 support the following HW power modes are supported:

- **Active mode** - Normal operating mode in which all peripherals are available and the CPU is active.
- **Idle mode** - In this mode, the CPU is in “Wait for Interrupt” (WFI) and the HCLK, which is the high frequency clock derived from the main crystal oscillator is running at a lower clock speed. Other clocks are active and the state of the entire chip is retained.
- **Sleep mode** - In this mode, CPU is in WFI and the HCLK is not running. The PMU determines if the other clocks can be turned off and does accordingly. State of the entire chip is retained, the internal LDOs run at a lower voltage (voltage is managed by the PMU), and SRAM is retained.
- **PDS mode** - This mode is an extension of the PMU Sleep wherein most of the peripherals such as UART and SPI are turned off. The entire memory is retained, and on wakeup the execution resumes from where it paused.
- **Shut Down Sleep (SDS)** - Everything is turned off except the IO Power Domain, RTC, and LPO. The device can come out of this mode either due to BT activity or by an external interrupt. Before going into this mode, the application can store some bytes of data into “Always On RAM” (AON). When the device comes out of this mode, the data from AON is restored. After waking from SDS, the application will start from the beginning (warmboot) and has to restore its state based on information stored in AON. In the SDS mode, a single BT task with no data activity, such as an ACL connection, BLE connection, or BLE advertisement can be performed.
- **HIDOFF (Timed-Wake) mode** - The device can enter this mode asynchronously, that is, the application can force the device into this mode at any time. IO Power Domain, RTC, and LPO are the only active blocks. A timer that runs off the LPO is used to wake the device up after a predetermined fixed time.
- **HIDOFF (External Interrupt-Waked) mode** - This mode is similar to Timed-Wake, but in HID-off mode even the LPO and RTC are turned off. So, the only wakeup source is an external interrupt.

Transition between power modes is handled by the on-chip firmware with host/application involvement. Please see Firmware Section for details.

Firmware

The CYBT-423028-02 ROM firmware runs on a real time operating system and handles the programming and configuration of all on-chip hardware functions as well as the BT/LE baseband, LM, HCI, GATT, ATT, L2CAP and SDP layers. The ROM also includes drivers for on-chip peripherals as well as handling on-chip power management functions including transitions between different power modes.

The CYBT-423028-02 is fully supported by the Cypress WICED Studio platform. WICED releases provide latest ROM patches, drivers, and sample applications allowing customized applications using the CYBT-423028-02 to be built quickly and efficiently.

Please refer to WICED Technical Brief and CYBT-423028-02 Product Guide for details on the firmware architecture, driver documentation, power modes and how to write applications/profiles using the CYBT-423028-02.