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# IBIS5 1.3 Megapixel CMOS Image Sensor

## Features

- 1280 × 1024 active pixels
- 6.7 μm × 6.7 μm square pixels
- 2/3" optical format
- Global and rolling shutter
- Master clock: 40 MHz
- 27 fps (1280 × 1024) and 106 fps (640 × 480)
- On-chip 10-bit ADCs
- Serial peripheral interface (SPI)
- Windowing (ROI)
- Sub-sampling: 1:2 mode
- Supply voltage
  - Analog: 3.0 V to 4.5 V
  - Digital: 3.3 V
  - I/O: 3.3 V
- Power consumption: 200 mW
- 0 °C to +65 °C operating temperature range
- 84-pin LCC package

## Applications

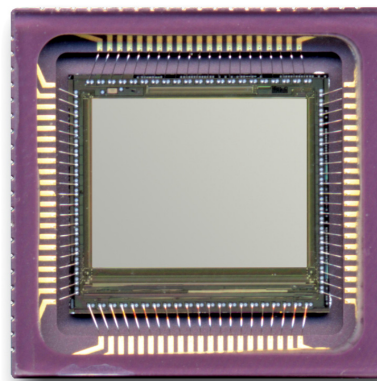
- Machine vision
- Inspection
- Robotics
- Traffic monitoring

## Description

The IBIS5-B-1300 is a solid state CMOS image sensor that integrates the functionality of complete analog image acquisition, digitizer, and digital signal processing system on a single chip. This 1.3-mega pixel (1280 × 1024) CMOS active pixel sensor dedicated to industrial vision applications features both rolling and snapshot (or global) shutter. Full frame readout time is 36 ms (max. 27.5 fps), and readout speed are boosted by windowed region of interest (ROI) readout. Another feature includes the double and multiples slope functionality to capture high dynamic range scenes. The sensor is available in a monochrome version or Bayer (RGB) patterned color filter array.

User programmable row and column start/stop positions allow windowing down to a 2×1 pixel window for digital zoom. Sub sampling or viewfinder mode reduces resolution while maintaining the constant field of view and an increased frame rate. An on-chip analog signal pipeline processes the analog video output of the pixel array. Double sampling (DS) eliminates the fixed pattern noise. The programmable gain and offset amplifier maps the signal swing to the ADC input range. A 10-bit ADC converts the analog data to a 10-bit digital word stream. The sensor uses a 3-wire serial peripheral interface (SPI), or a 16-bit parallel interface. It operates with a 3.3 V power supply and requires only one master clock for operation up to 40 MHz. It is housed in an 84-pin ceramic LCC package.

**Figure 1. IBIS5-B-1300 Photo**



## Ordering Information

See [Ordering Code Information](#) on page 33 for more information.

Marketing Part Number	Description	Package
CYII5SM1300AB-QDC	Mono with glass	84-pin LCC
CYII5SM1300AB-QWC	Mono without glass	
CYII5SC1300AB-QDC	Color with glass	
CYII5FM1300AB-QDC	Mono with thicker epi with glass	

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## Specifications

### Key Specifications

**Table 1. General Specifications**

Parameter	Specifications
Active pixels	1280 (H) × 1024 (V)
Pixel size	6.7 μm × 6.7μm
Master Clock	40 MHz
Shutter type	Global and rolling shutter
Frame rate	27 fps at full resolution
Windowing (ROI)	Randomly programmable ROI read out. Implemented as scanning of lines or columns from an uploaded position
ADC resolution	10-bit, on-chip
Extended dynamic range	Global shutter: Up to 4 slopes Rolling shutter: Double slope
Power dissipation	200 mW

**Table 2. Electro Optical Specifications**

Parameter	Specifications
Sensitivity	8.4 V/lux.s at 650 nm
Full Well Charge	62500 e <sup>-</sup>
Temporal Noise	2.5 LSB10
Parasitic light sensitivity	3%
Dark noise	21e <sup>-</sup>
Signal to Noise Ratio	64 dB
Fixed pattern noise (FPN)	4.5 LSB10
Dark signal	5.5 LSB10/sec at 30 °C

**Table 3. Recommended Operating Ratings<sup>[2]</sup>**

Symbol	Description	Min	Max	Units
T <sub>J</sub> <sup>[2]</sup>	Operating temperature range	0	65	°C
T <sub>S</sub> <sup>[1]</sup>	Storage temperature range	20	40	°C
	Storage humidity range	30	60	%RH

**Table 4. Absolute Maximum Ratings<sup>[1]</sup>**

Symbol	Description	Min	Max	Units
ABS (3.0-V to 3.3-V supply group)	ABS rating for 3.0 V and 3.3 V supply group	-0.5	4.3	V
ABS (4.5-V supply group)	ABS rating for 4.5 V supply group	-0.5	5.5	V
T <sub>S</sub> <sup>[1]</sup>	ABS storage temperature range	0	150	°C
	ABS storage humidity range	5	90	%RH
Electrostatic discharge (ESD) <sup>[3]</sup>	Human Body Model (HBM)	See Note 4		V
	Charged Device Model (CDM)			
LU <sup>[3]</sup>	Latch-up	See Note 5		mA

**Notes**

1. Absolute maximum ratings are limits beyond which damage may occur. Long term exposure toward the maximum storage temperature accelerates color filter degradation.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. Cypress recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625-A. Refer to Application Note [AN52561](#).
4. The IBIS5-B-1300 complies with JESD22-A114 HBM Class 0 and JESD22-C101 Class I. It is recommended that extreme care be taken while handling these devices to avoid damages due to ESD event. Refer to Application Note [AN52561](#).
5. The IBIS5-B-1300 does not have latch-up protection.

**Electrical Specifications**
*Recommended Operating Conditions*
**Table 5. Recommended Operating Conditions**

Parameter	Description	Typical Currents	Peak Currents	Min	Typ	Max	Unit
VDDH	Voltage on HOLD switches.	0.047 mA	100 mA	+3.3	+4.5	+4.5	V
VDDR_LEFT	Highest reset voltage.	0.050 mA	100 mA	+3.3	+4.5	+4.5	V
VDDC	Pixel core voltage.	0.052 mA	100 mA	+2.5	+3.0	+3.3	V
VDDA	Analog supply voltage of the image core.	19.265 mA	N/A	+3.0	+3.3	+3.6	V
VDDD	Digital supply voltage of the image core.	5.265 mA	N/A	+3.0	+3.3	+3.6	V
IDDA_ADC	Analog supply of ADC	34.5 mA	N/A	N/A	N/A	N/A	mA
IDDD_ADC	Digital supply of ADC	10.5 mA	N/A	N/A	N/A	N/A	mA
T <sub>A</sub>	Commercial operating temperature.	N/A	N/A	0	30	65	°C

All parameters are characterized for DC conditions after thermal equilibrium is established.

Always tie unused inputs to an appropriate logic level, for example, either VDD or GND.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, take normal precautions to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.

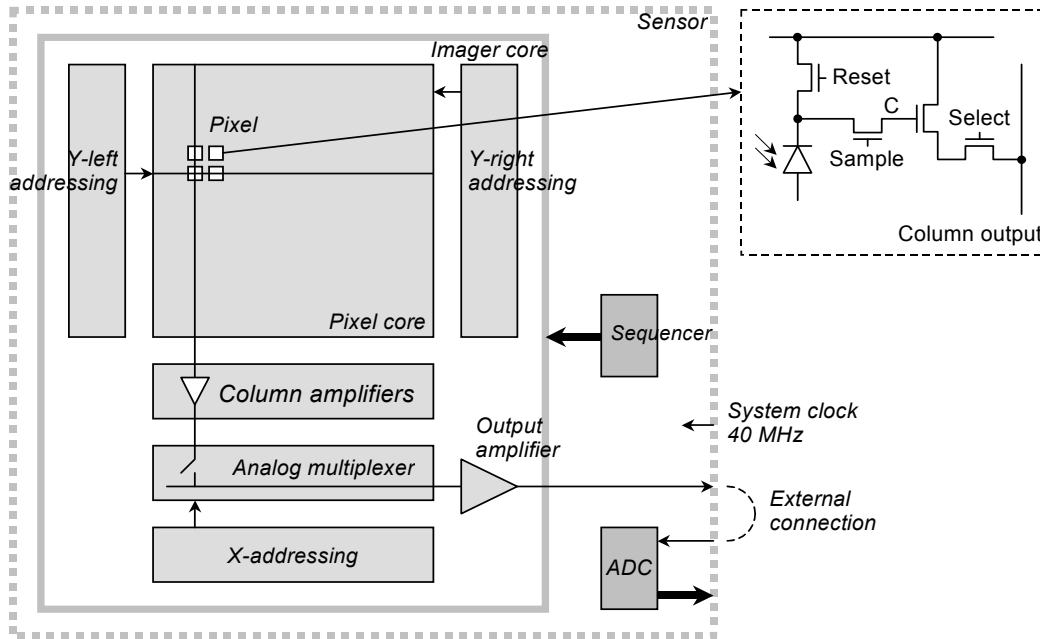
*DC Electrical Characteristics*
**Table 6. DC Electrical Characteristics**

Parameter	Characteristic	Condition	Min	Max	Unit
V <sub>IH</sub>	Input high voltage		2.1	–	V
V <sub>IL</sub>	Input low voltage		–	0.6	V
I <sub>IN</sub>	Input leakage current	V <sub>IN</sub> = VDD or GND	–10	+10	μA
V <sub>OH</sub>	Output high voltage	VDD = min; I <sub>OH</sub> = –100 μA	2.2	–	V
V <sub>OL</sub>	Output low voltage	VDD = min; I <sub>OH</sub> = 100 μA		0.5	V
I <sub>DD</sub>	Maximum operating current	System clock <= 40 MHz	40	60	mA

## Architecture and Operation

This section presents detailed information about the most important sensor blocks

**Figure 2. Block Diagram of IBIS5-B-1300 Image Sensor**



### Floor Plan

Figure 2 shows the architecture of the IBIS5-B-1300 image sensor. It consists basically of a pixel array, one X- and two Y-addressing registers for the readout in X- and Y-direction, column amplifiers that correct for the fixed pattern noise, an analog multiplexer, and an analog output amplifier.

Use the left Y-addressing register for readout operation. Use the right Y-addressing register for reset of pixel rows. In multiple slope synchronous shutter mode, the right Y-addressing register resets the whole pixel core with a lowered reset voltage. In rolling

curtain shutter mode, use the right Y-addressing register for the reset pointer in single and double slope operation to reset one pixel row.

The on-chip sequencer generates most of the signals for the image core. Some basic signals (such as start/stop integration, line and frame sync signals) are generated externally.

A 10-bit ADC is implemented on chip but electrically isolated from the image core. You must route the analog pixel output to the analog ADC input on the outside.

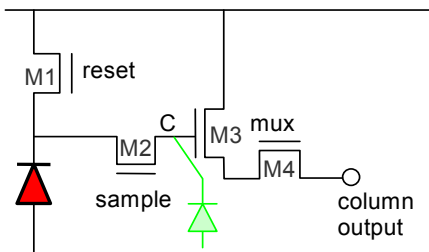
**Pixel**

A description of the pixel architecture and the color filter array follows.

**Architecture**

The pixel architecture used in the IBIS5-B-1300 is a 4-transistor pixel as shown in Figure 3. Implement the pixel using the high fill factor technique as patented by Cypress (US patent No. 6,225,670 and others). The 4T-pixel features a snapshot shutter but can also emulate the 3T-pixel by continuously closing sampling switch M2. Using M2 as a global sample transistor for all pixels enables the snapshot shutter mode. Due to this pixel architecture, integration during read out is not possible in synchronous shutter mode.

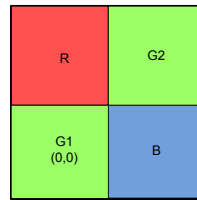
**Figure 3. 4T Pixel Architecture**



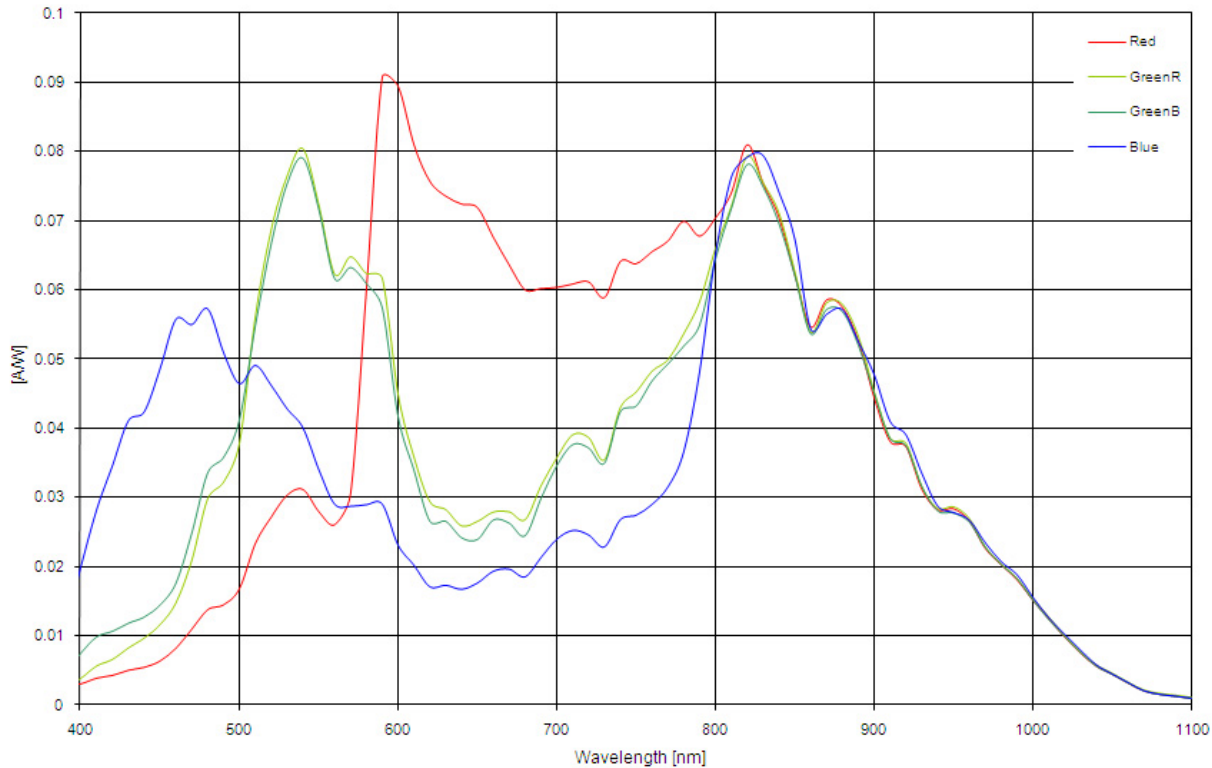
**Color Filter Array**

The IBIS5-B-1300 is also processed with a Bayer RGB color pattern. Pixel (0,0) is a green filter and is situated on a green-blue row. Green1 and Green2 have a slightly different spectral response due to cross talk from neighboring pixels. Green1 pixels are located on a blue-green row, green2 pixels are located on a green-red row. Figure 5 shows the response of the color filter array as function of the wavelength. Note that this response curve includes the optical cross talk of the pixels.

**Figure 4. Color Filter Arrangement of Pixels**



**Figure 5. Spectral Response for IBIS5-B-Color**



Spectral Response Curve

Figure 6. Spectral Response Curve

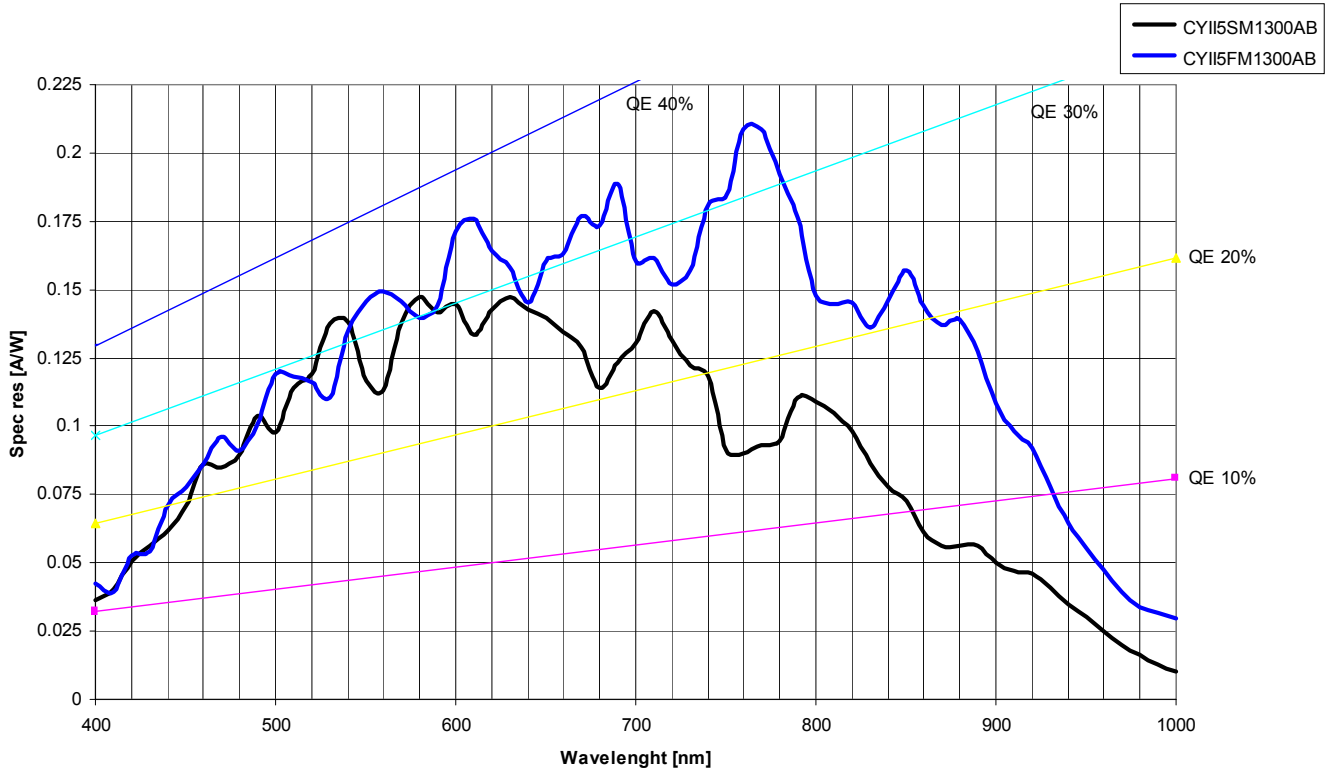


Figure 6 shows the spectral response characteristic for the IBIS5-B-1300 (CYII5SM1300AB) and the IBIS-5-BE-1300 (CYII5FM1300AB). The curve is measured directly on the pixels. It includes effects of non-sensitive areas in the pixel, for example, interconnection lines. The sensor is light sensitive between 400 and 1000 nm. The peak QE × FF is 30%, approximately around 650 nm. In view of a fill factor of 40%, the QE is thus close to 75% between 500 and 700 nm. The IBIS-5-BE-1300 has superior response in the NIR region (700-900 nm). For more information about the IBIS5-B-1300, refer to [IBIS5-BE-1300 \(CYII5FM1300AB\)](#) on page 8.



Electro-voltaic Response Curve

Figure 7. Electro-Voltaic Response Curve

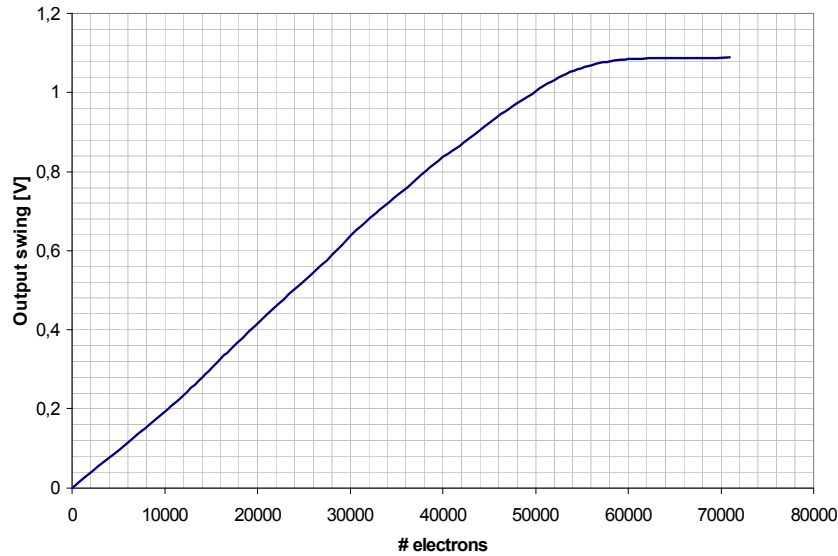


Figure 7 shows the pixel response curve in linear response mode. This curve is the relation between the electrons detected in the pixel and the output signal. The resulting voltage-electron curve is independent of any parameters (integration time, and others). The voltage to electrons conversion gain is 17.6  $\mu\text{V}/\text{electron}$ .

IBIS5-BE-1300 (CYII5FM1300AB)

The IBIS5-BE-1300 is processed on a thicker epitaxial Si layer featuring a superb sensitivity in the NIR (Near Infra Red) wavelengths (700–900 nm). The spectral response curves of the two IBIS5-B-1300 image sensors are shown in Figure 6 on page 7. As many machine vision applications use light sources in the NIR, the IBIS5-BE-1300 sensor has a significant sensitivity advantage in the NIR.

A drawback of the thicker epitaxial layer is a slight performance decrease in MTF (Modular Transfer Function or electrical pixel to pixel cross-talk) as indicated in Table 7.

Table 7. MTF Comparison

Direction	Wavelength	IBIS5-B-1300	IBIS5-BE-1300
Horizontal	600	0.58	0.37
Horizontal	700		0.18
Horizontal	800		0.16
Horizontal	900		0.07
Vertical	600	0.53	0.26
Vertical	700		0.16
Vertical	800		0.13
Vertical	900		0.11

The resulting image sharpness is hardly affected by this decreased MTF value. Both IBIS5-B-1300 versions are fully pin compatible and have identical timing and biasing

## Image Core Operation

### Image Core Operation and Signalling

Figure 8 is a functional representation of the image core without sub-sampling and column/row swapping circuits. Most of the signals involved are not available from the outside because they are generated by the X-sequencer and SS-sequencer blocks.

The integration of the pixels is controlled by internal signals such as reset, sample, and hold which are generated by the on-chip SS-sequencer that is controlled with the external signals SS\_START and SS\_STOP. Reading out the pixel array starts by applying a Y\_START together with a Y\_CLOCK signal; internally this is followed by a calibration sequence to calibrate the output amplifiers (during the row blanking time). Signals necessary to do this calibration are generated by the on-chip X-sequencer. This calibration sequence takes typically 3.5  $\mu$ s and is necessary to remove 'Fixed Pattern Noise' of the pixels and of the column amplifiers themselves by means of a double sampling technique. After the row blanking time, the pixels are fed to the output amplifier. The pixel rate is equal to the SYS\_CLOCK frequency.

### Image Core Supply Considerations

The image sensor has several supply voltages:

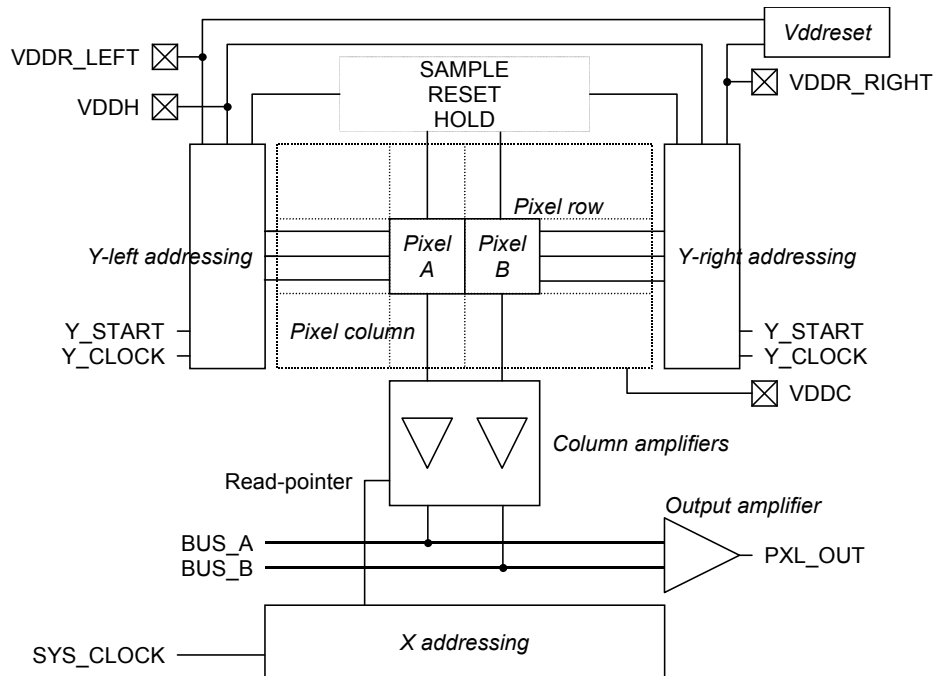
VDDH is the voltage that controls the sample switches. Do not apply a higher voltage than this to the chip.

The VDDR\_LEFT voltage is the highest (nominal) reset voltage of the pixel core.

The VDDR\_RIGHT voltage is generated from the VDDR\_LEFT voltage using a circuit that is programmed with the KNEEPOINT\_LSB/MSB bits in the sequencer register (see also [Pixel reset knee-point for multiple slope operation \(bits 8, 9, and 10\)](#) on page 17). You can disconnect the VDDR\_RIGHT pin from the circuit and apply an external voltage to supply the multiple slope reset voltage by setting the VDDR\_RIGHT\_EXT bit in the SEQUENCER register. When no external voltage is applied (recommended), connect the VDDR\_RIGHT pin to a capacitor (recommended value = 1 $\mu$ F). VDDC is the pixel core supply. VDDA is the image core and periphery analog supply. VDDD is the image core and periphery digital supply.

Note that the IBIS5-B-1300 image sensor has no on-chip power rejection circuitry. As a consequence all variations on the analog supply voltages can contribute to random variations (noise) on the analog pixel signal, which is seen as random noise in the image. During the camera design, take precautions to supply the sensor with very stable supply voltages to avoid this additional noise. The pixel array (VDDR\_LEFT, VDDH and VDDC) analog supplies are especially vulnerable to this.

Figure 8. Image Core



*Global Shutter Supply Considerations*

The recommended supply voltage settings listed in [Table 8](#) are used when the IBIS5-B-1300 sensor is in global shutter mode only.

**Table 8. Global Shutter Recommended Supply Settings**

Parameter	Description	Typ	Unit
VDDH	Voltage on HOLD switches.	+4.5	V
VDDR_LEFT	Highest reset voltage.	+4.5	V
VDDC	Pixel core voltage.	+3.3	V
VDDA	Analog supply voltage of the image core.	+3.3	V
VDDD	Digital supply voltage of the image core.	+3.3	V
GND_A	Analog ground.	0	V
GND_D	Digital ground.	0	V
GND_AB	Anti-blooming ground.	0	V

*Dual Shutter Supply Considerations*

If you analyze the supply settings listed in [Table 8](#), you can see some fixed column non-uniformities (FPN) when operating in rolling shutter mode. If a dual shutter mode (both rolling and global shutter) is required during operation, you must apply the

supply settings listed in [Table 9](#) to achieve the best possible image quality.

**Table 9. Dual Shutter Recommended Supply Settings**

Parameter	Description	Typ	Unit
VDDH	Voltage on HOLD switches.	+4.5	V
VDDR_LEFT	Highest reset voltage.	+4.5	V
VDDC	Pixel core voltage.	+3.0	V
VDDA	Analog supply voltage of the image core.	+3.3	V
VDDD	Digital supply voltage of the image core.	+3.3	V
GND_A	Analog ground.	0	V
GND_D	Digital ground.	0	V
GND_AB	Anti-blooming ground.	0	V

*Image Core Biasing Signals*

[Table 10](#) summarizes the biasing signals required to drive the IBIS5-B-1300. For optimization on speed and power dissipation of all internal blocks, several biasing resistors are needed.

Each biasing signal determines the operation of a corresponding module in the sense that it controls the speed and power dissipation. The tolerance on the DC-level of the bias levels can vary  $\pm 150$  mV due to process variations.

**Table 10. Overview of Bias Signals**

Signal	Comment	Related module	DC-Level
DEC_CMD	Connect to VDDA with R = 51 k $\Omega$ and decouple to GND_A with C = 100 nF.	Decoder stage.	1.0 V
DAC_VHIGH	Connect to VDDA with R = 0 $\Omega$ .	High level of DAC.	3.3 V
DAC_VLOW	Connect to GND_A with R = 0 $\Omega$ .	Low level of DAC.	0.0 V
AMP_CMD	Connect to VDDA with R = 51 k $\Omega$ and decouple to GND_A with C = 100 nF.	Output amplifier stage.	1.2 V
COL_CMD	Connect to VDDA with R = 51 k $\Omega$ and decouple to GND_A with C = 100 nF.	Columns amplifiers stage.	1.0 V
PC_CMD	Connect to VDDA with R = 22 k $\Omega$ and decouple to GND_A with C = 100 nF.	Pre-charge of column busses.	1.17 V
ADC_CMD	Connect to VDDA with R = 51 k $\Omega$ and decouple to GND_A with C = 100 nF.	Analog stage of ADC.	1.0 V
ADC_VHIGH	Connect to VDDA with R = 230 $\Omega$ and decouple to GND_A with C = 100 nF.	High level of ADC.	2.7 V
ADC_VLOW	Connect to GND_A with R = 410 $\Omega$ and decouple to GND_A with C = 100 nF.	Low level of ADC.	1.2 V

**X-Addressing**

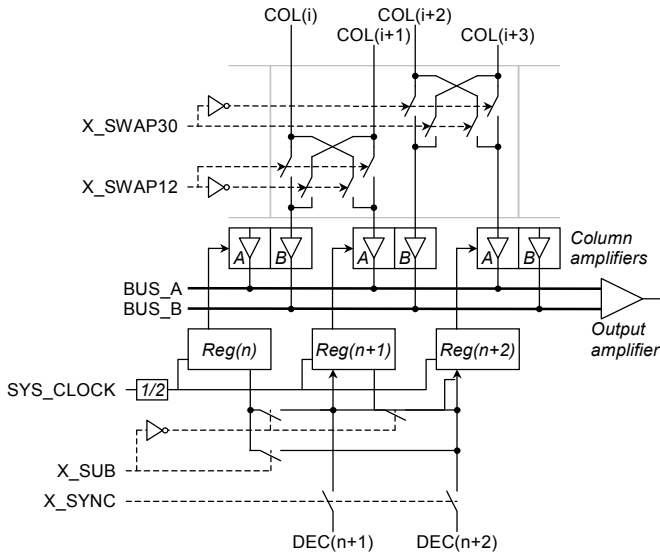
Because of the high pixel rate, the X-shift register selects two columns at a time for readout, so it runs at half the system clock speed. All even columns are connected to bus A; all odd columns to bus B. In the output amplifier, bus A and bus B are combined into one stream of pixel data at system clock speed.

At the end of the row blanking time, the X\_SYNC switch is closed while all other switches are open and the decoder output is fed to the register. The decoder loads a logical one in one of the registers and a logical zero in the rest. This defines the starting point of the window in the X direction. As soon as the X\_SYNC signal is released, the register starts shifting from the start position.

When no sub-sampling is required, X\_SUB is inactive. The pointer in the shift-register moves one bit at a time.

When sub-sampling is enabled, X\_SUB is activated. The shift register moves two bits at a time. Taking into account that every register selects two columns, hence two pixels sub-sampling results in the pattern 'XXOOXXOO' when eight pixels are considered. Suppose the columns are numbered from left to right starting with 0 (zero) and sub-sampling is enabled:

**Figure 9. Column Structure**

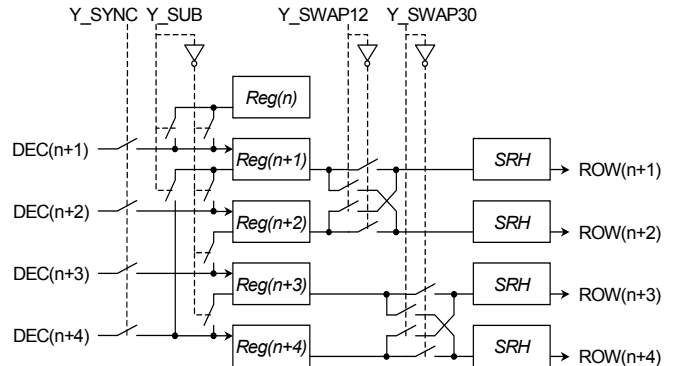


If columns 1 and 2, 5 and 6, 9 and 10 ... are swapped using the SWAP\_12 switches, a normal sub-sampling pattern of 'XOXOXOXO' is obtained.

If columns 3 and 4, 7 and 8, 11 and 12 ... are swapped using the SWAP\_30 switches, the pattern is 'OXOXOXOX'.

If both the SWAP\_12 and SWAP\_30 switches are closed, pattern 'OOXXOOXX' is obtained.

**Figure 10. Row Structure**



Because every register addresses two columns at a time, the addressable pixels range in sub-sample mode is from zero to half the maximum number of pixels in a row (only even values). For instance: 0, 2, 4, 6, 8... 638.

**Table 11. X-Sub-sampling Patterns**

X_SUB	X_SWAP12	X_SWAP30	Sub-Sample Pattern
0	0	0	XXXXXXXX
1	0	0	XXOOXXOO
1	1	0	XOXOXOXO
1	0	1	OXOXOXOX
1	1	1	OOXXOOXX

**Y-addressing**

For symmetry reasons, the sub-sampling modes in the Y-direction are the same as in X-direction.

**Table 12. Y-Sub-Sampling Patterns**

Y_SUB	Y_SWAP12	Y_SWAP30	Sub-Sample Pattern
0	0	0	XXXXXXXX
1	0	0	XXOOXXOO
1	1	0	XOXOXOXO
1	0	1	OXOXOXOX
1	1	1	OOXXOOXX

In normal mode, the pointer for the pixel row is shifted one at a time.

When sub-sampling is enabled, Y\_SYNC is activated. The Y-shift register shifts 2 succeeding bits and skips the 2 next bits. This results in pattern 'XXOOXXOO'.

Activating Y\_SWAP12 results in pattern 'XOXOXOXO'.

Activating Y\_SWAP30 results in pattern 'OXOXOXOX'.

Activating both Y\_SWAP12 and Y\_SWAP30 results in pattern 'OOXXOOXX'.

The addressable pixel range when Y-sub sampling is enabled is: 0-1, 4-5, 8-9, 12-13, ... 1020-1021

## Output Amplifier

### Architecture and Settings

The output amplifier stage is user programmable for gain and offset level. Gain is controlled by 4-bit wide word; offset by a 7-bit wide word. Gain settings are on an exponential scale. Offset is controlled by a 7-bit wide DAC, which selects the offset voltage between two reference voltages (DAC\_VHIGH and DAC\_VLOW) on a linear scale.

The amplifier is designed to match the specifications of the imager array output. This signal has a data rate of 40 MHz. The output impedance of the amplifier is 260 Ohms.

At unity gain and with a mid-range offset value, the amplifier outputs a signal in between 1.59 V (light) and 2.70 V (dark). This analog range must fit to the input range of the ADC, external or internal. The output swing in unity gain is approximately 1.11 V and it is maximum 1.78 V at the highest gain settings. So, the effective signal range is between 1.17 V and 2.95 V, depending on the gain and offset settings of the amplifier.

Figure 11. Output Structure

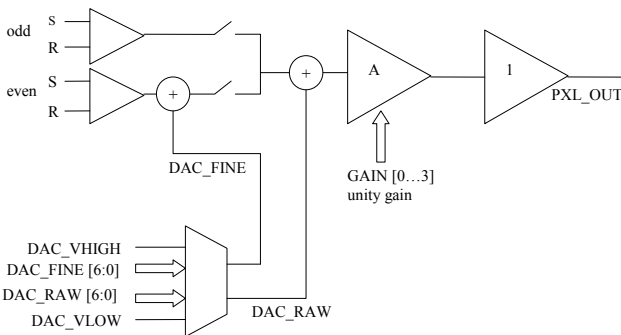


Figure 11 shows the architecture of the output amplifier. The odd and even column amplifiers sample both pixel and reset value to perform a double sampling FPN correction. You can adjust two different offsets using the on-chip DAC (7 bit): DAC\_FINE and DAC\_RAW. DAC\_FINE is used to tune the difference between odd and even columns; DAC\_RAW is used to add a common (both even and odd columns) to the FPN corrected pixel value. This pixel value is fed to the first amplifier stage which has an adjustable gain, controlled by a 4-bit word ('GAIN [0..3]').

After this, a unity feedback amplifier buffers the signal and the signal leaves the chip. This second amplifier stage determines the maximal readout speed, that is, the bandwidth and the slew rate of the output signal. The whole amplifier chain is designed for a data rate of 40 Mpix/s (at 20 pF).

The analog output of the IBIS5-B-1300 image sensor is not designed to drive very large loads on the PCB. Therefore, it is advised that the PXL\_OUT is connected to the ADC\_IN right below the sensor in the top layer with a thick track. It is better not to have vias on this trace. If there is a socket being used, then it is advised that we buffer the PXL\_OUT close to the sensor output pin and then take the signal to the ADC\_IN.

### Output Amplifier Gain Control

The output amplifier gain is controlled by a 4-bit word set in the AMPLIFIER register (see section Amplifier Register (6:0) on page 19). An overview of the gain settings is given in Table 13.

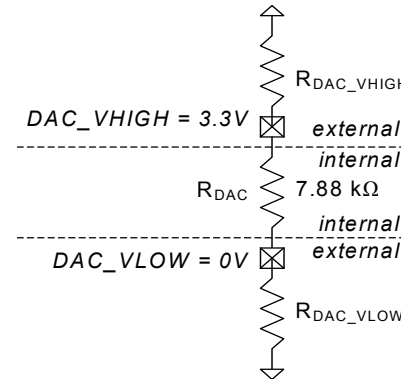
Table 13. Overview Gain Settings

Bits	DC Gain	Bits	DC Gain
0000	1.37	1000	6.25
0001	1.62	1001	7.89
0010	1.96	1010	9.21
0011	2.33	1011	11.00
0100	2.76	1100	11.37
0101	3.50	1101	11.84
0110	4.25	1110	12.32
0111	5.20	1111	12.42

### Setting of the DAC Reference Voltage

In the output amplifier, the offset is trimmed by loading registers DACRAW\_REG and DACFINE\_REG. DAC\_RAW is used to adjust the offset of the output amplifier and DAC\_FINE is used to tune the offset between the even and odd columns. These registers are inputs for two DACs (see Figure 12) that operate on the same resistor that is connected between pins DAC\_VHIGH and DAC\_VLOW. The range of the DAC is defined using a resistive division with  $R_{VHIGH}$ ,  $R_{DAC}$  and  $R_{VLOW}$ .

Figure 12. Internal and External ADC Connections



The internal resistor  $R_{DAC}$  has a value of approximately 7.88 kΩ. The recommend resistor values for both DAC\_VLOW and DAC\_VHIGH are 0 Ω.

### Analog-to-Digital Converter

The IBIS5-B-1300 has a 10-bit flash analog digital converter running nominally at 40 Msamples/s. The ADC is electrically separated from the image sensor. Tie the input of the ADC (ADC\_IN; pin 69) externally to the output (PXL\_OUT1; pin 28) of the output amplifier.

**Table 14. ADC Specifications**

Input range	1–3 V <sup>[6]</sup>
Quantization	10 bits
Nominal data rate	40 Msamples/s
DNL (linear conversion mode)	Typ. < 0.5 LSB
INL (linear conversion mode)	Typ. < 3 LSB
Input capacitance	< 20 pF
Power dissipation at 40 MHz	Typ. 45 mA × 3.3 V = 150 mW
Conversion law	Linear / Gamma-corrected

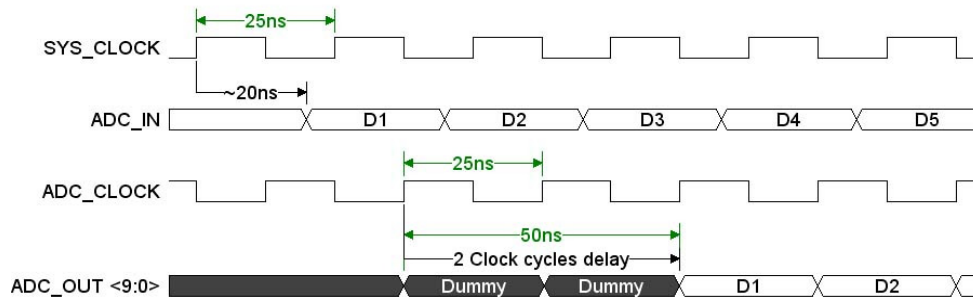
### ADC Timing

At the rising edge of SYS\_CLOCK, the next pixel is fed to the input of the output amplifier. Due to internal delays of the SYS\_CLOCK signal, it takes approximately 20 ns before the output amplifier outputs the analog value of the pixel, as shown in Figure 13.

The ADC converts the pixel data on the rising edge of the ADC\_CLOCK, but it takes two clock cycles before this pixel data is at the output of the ADC. Figure 13 shows this pipeline delay.

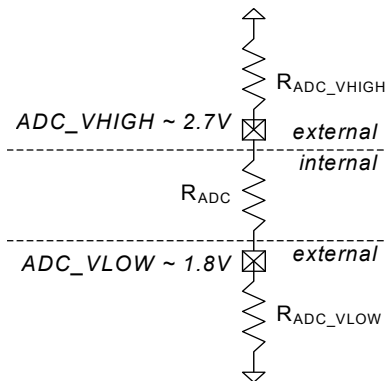
Due to these delays, it is advisable that a variable phase difference is foreseen between the ADC\_CLOCK and the SYS\_CLOCK to tune the optimal sample moment of the ADC.

**Figure 13. ADC Timing**



### Setting ADC Reference Voltages

**Figure 14. Internal and External ADC Connections**



The internal resistor  $R_{ADC}$  has a value of approximately 585  $\Omega$ . This results in the following values for the external resistors:

Resistor	Value ( $\Omega$ )
$R_{ADC\_VHIGH}$	360
$R_{ADC}$	585
$R_{ADC\_VLOW}$	1200

Note that the recommended ADC resistor values yield in a conversion of the full analog output swing at unity gain ( $V_{DARK\_ANALOG} < ADC\_VHIGH$  and  $V_{LIGHT\_ANALOG} > ADC\_VLOW$ ).

The values of the resistors depend on the value of  $R_{ADC}$ . To assure proper working of the ADC, make certain the voltage difference between  $ADC\_VLOW$  and  $ADC\_VHIGH$  is at least 1.0 V.

**Note**

6. The internal ADC range is typically 100 mV lower than the external applied  $ADC\_VHIGH$  and  $ADC\_VLOW$  voltages due to voltage drops over parasitic internal resistors in the ADC.

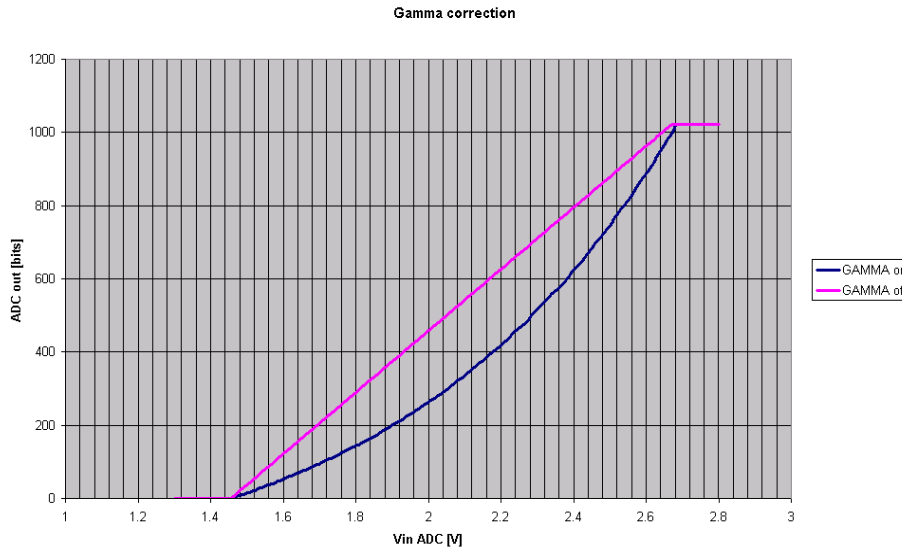
*Nonlinear and Linear Conversion Mode—'gamma' Correction*

Figure 15 shows the ADC transfer characteristic. The nonlinear (exponential) ADC conversion is intended for gamma-correction of the images. It increases contrast in dark areas and reduces contrast in bright areas. The non-linear transfer function is given by the following equation:

$$V_{in} = ADC\_VHIGH + (ADC\_VHIGH - ADC\_VLOW) * \frac{a*x + b*x^2}{a*1023 + b*1023^2}$$

where a = 5; b = 0.027; x = digital output code

**Figure 15. Linear and Nonlinear ADC Conversion Characteristics**



*Sensor Digital Outputs*

The digital outputs of the IBIS5-B-1300 sensor are not designed to drive large loads. Hence, the outputs cannot be used to directly drive cables or long traces on the PCB. If it is required to drive traces more than 5 inches long, it is advisable to use a buffer for all the digital signals given out by the sensor.

*Sensor Clock Inputs*

The ADC\_CLOCK and the SYS\_CLOCK of the sensor are typically 180 phase shifted from each other. However, depending on the board layout, it is possible that there may be a variation (increased phase shift of ADC\_CLOCK with respect to SYS\_CLOCK) in the phase shift between the clocks.

So, it is recommended that the phase shift between the clocks is maintained programmable.

*Clock Jitter Requirements:*

- Min low time: 11.00 ns
- Min high time: 11.00 ns
- max rise time: 5 ns
- max fall time: 5 ns
- Max Duty cycle: 47% to 53%
- Max period jitter: 150 ps

It is important that the clock is stable, reproducible and has low jitter. SYS\_CLOCK and ADC\_CLOCK are the most critical clocks, both clock interact in the readout path and influence the sensor performance.

*Black Calibration*

Due to slight variations in the chip fabrication process, the output analog voltage of the PGA is not perfectly matched to the input analog range of the ADC. As a result, a reduced dynamic range is compared when comparing sensors/cameras from different lots. This is especially true in the dark as it is possible that a part of the analog range gets clipped when it reaches the ADC.

For this reason, black calibration step is required. Because this is a fixed setting, and varies very slightly with temperature, the setting can be done at the factory itself.

While grabbing normal images, the settings can be loaded from an on-board memory.

In the IBIS5 image sensor, black calibration step also tries to match the output of the odd and even channels.

The steps for black calibration are -

1. Put the sensor in dark.
2. Change DAC\_RAW such that no pixel or least number of pixels (assuming there are defect pixels) have a zero ADC output value.
3. Change DAC\_FINE such that the average of the odd columns is almost same as the even columns.
4. Change DAC\_RAW again such that all pixels have a non-zero output, but are as close to zero as possible.
5. Repeat for different gains.

**Electronic Shutter Types**

The IBIS5-B-1300 has two different shutter types: a rolling (curtain) shutter and a snapshot (synchronous) shutter.

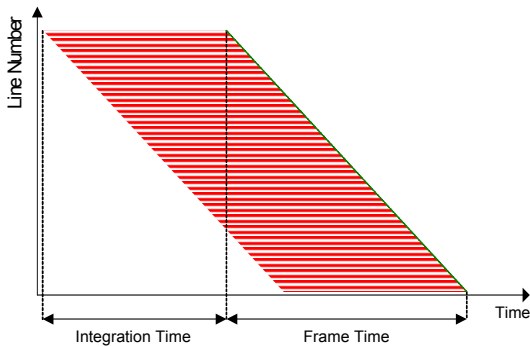
*Rolling (Curtain) Shutter*

The name is due to the fact that the effect is similar to a curtain shutter of a SLR film camera. Although it is an electronic operation, the shutter seems to slide over the image. A rolling shutter is easy and elegant to implement in a CMOS sensor. In the rolling shutter mode, there are two Y-shift registers. One of them points to the row that is currently being read out. The other shift register points to the row that is currently being reset. Both pointers are shifted by the same Y-clock and move over the focal plane. The integration time is set by the delay between both pointers.

Figure 16 graphically displays the relative shift of the integration times for different lines during the rolling shutter operation. Each line is read and reset in a sequential way. The integration time is the same for all lines, but is shifted in time. You can vary the integration time through the INT\_TIME register (in number of lines).

This indicates that all pixels are light sensitive at another period of time, and can cause some blurring if a fast moving object is captured.

**Figure 16. Rolling Shutter Operation**



When the sensor is set to rolling shutter mode, make certain to hold the input SS\_START and SS\_STOP low.

*Global Shutter*

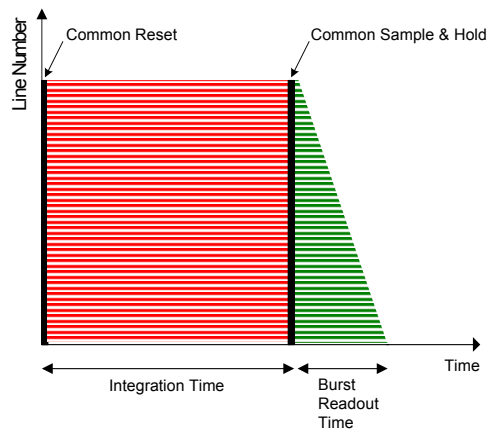
A synchronous (global, snapshot) shutter solves the inconvenience found in the rolling shutter. Light integration takes place on all pixels in parallel, although subsequent readout is sequential.

Figure 17 shows the integration and read out sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line

by line after integration. Note that the integration and read out cycle is carry-out in serial; that causes that no integration is possible during read out.

During synchronous shutter mode, the input pins SS\_START and SS\_STOP are used to start and stop the synchronous shutter.

**Figure 17. Global Shutter Operation**



**Sequencer**

Figure 8 on page 9 shows a number of control signals that are needed to operate the sensor in a particular sub-sampling mode with a certain integration time, output amplifier gain, and so on. Most of these signals are generated on-chip by the sequencer that uses only a few control signals. Make certain that these control signals are generated by the external system:

- SYS\_CLOCK (X-clock) defines the pixel rate
- Y\_START pulse indicates the start of a new frame read out
- Y\_CLOCK selects a new row and starts the row blanking sequence, including the synchronization and loading of the X-register
- SS\_START and SS\_STOP control the integration period in snapshot shutter mode.

The relative position of the pulses is determined by a number of data bits that are uploaded in internal registers through the serial or parallel interface.

*Internal Registers*

Table 15 shows a list of the internal registers with a short description. In the next section, the registers are explained in more detail. On power-on, all registers in the sensor are reset to zero. To start operating the sensor, first load all the registers using the parallel or serial-3-wire interface. The value to be loaded in each register on power-on is given in the table.



**Table 15. Internal Registers**

Register	Bit	Name	Description
0 (0000)	11:0	SEQUENCER register	Default value <11:0>: '000011000100'
	0	SHUTTER_TYPE	1 = rolling shutter 0 = synchronous shutter
	1	FRAME_CAL_MODE	0 = fast 1 = slow
	2	LINE_CAL_MODE	0 = fast 1 = slow
	3	CONT_CHARGE	1 = 'Continuous' precharge enabled
	4	GRAN_X_SEQ_LSB	Granularity of the X sequencer clock
	5	GRAN_X_SEQ_MSB	
	6	GRAN_SS_SEQ_LSB	Granularity of the SS sequencer clock
	7	GRAN_SS_SEQ_MSB	
	8	KNEEPOINT_LSB	Sets reset voltage for multiple slope operation
	9	KNEEPOINT_MSB	
	10	KNEEPOINT_ENABLE	1 = Enables multiple slope operation in synchronous shutter mode
11	VDDR_RIGHT_EXT	1 = Disables circuit that generates VDDR_RIGHT voltage; this allows the application of an external voltage	
1 (0001)	11:0	NROF_PIXELS	Number of pixels to count (maximum 1280/2) Default value <11:0>: '001001111111'
2 (0010)	11:0	NROF_LINES	Number of lines to count Default value <11:0>: '001111111111'
3 (0011)	11:0	INT_TIME	Integration time Default value <11:0>: '111111111111'
4 (0100)	10:0	X_REG	X start position (maximum 1280/2) Default value <10:0>: '00000000000'
5 (0101)	10:0	YL_REG	Y-left start position Default value <10:0>: '00000000000'
6 (0110)	10:0	YR_REG	Y-right start position Default value <10:0>: '00000000000'
7 (0111)	7:0	IMAGE CORE register	Default value <7:0>: '00000000'
	0	TEST_EVEN	Test even columns
	1	TEST_ODD	Test odd columns
	2	X_SUBSAMPLE	Enable sub-sampling in X-direction
	3	X_SWAP12	Swap columns 1-2, 5-6, ...
	4	X_SWAP30	Swap columns 3-4, 7-8, ...
	5	Y_SUBSAMPLE	Enable sub-sampling in Y-direction
	6	Y_SWAP12	Swap rows 1-2, 5-6, ...
7	Y_SWAP30	Swap rows 3-4, 7-8, ...	
8 (1000)	6:0	AMPLIFIER register	Default value <6:0>: '1010000'
	0	GAIN<0>	Output amplifier gain setting
	1	GAIN<1>	
	2	GAIN<2>	
	3	GAIN<3>	
	4	UNITY	1 = Amplifier in unity gain mode
	5	DUAL_OUT	1 = Activates second output
6	STANDBY	0 = Amplifier in standby mode	

**Table 15. Internal Registers** (continued)

Register	Bit	Name	Description
9 (1001)	6:0	DACRAW_REG	Amplifier DAC raw offset Default value <6:0>: '1000000'
10 (1010)	6:0	DACFINE_REG	Amplifier DAC fine offset Default value <6:0>: '1000000'
11 (1011)	2:0	ADC register	Default value <2:0>: '011'
	0	TRISTATE_OUT	0 = Output bus in tri-state
	1	GAMMA	0 = Gamma-correction on
	2	BIT_INV	1 = Bit inversion on output bus
12 (1100)		Reserved	
13 (1101)		Reserved	
14 (1110)		Reserved	
15 (1111)		Reserved	

**Detailed Description of Internal Registers**
**Sequencer register (7:0)**
**1. Shutter type (bit 0)**

The IBIS5-B-1300 image sensor has two shutter types:

0 = synchronous shutter

1 = rolling shutter

**2. Output amplifier calibration (bits 1 and 2)**

Bits FRAME\_CAL\_MODE and LINE\_CAL\_MODE define the calibration mode of the output amplifier.

During every row-blanking period, a calibration is done of the output amplifier. There are two calibration modes. The FAST mode (0) forces a calibration in one cycle but is not so accurate and suffers from KTC noise. The SLOW mode (1) only makes incremental adjustments and is noise free.

Approximately 200 or more 'slow' calibrations have the same effect as one 'fast' calibration. Different calibration modes are set at the beginning of the frame (FRAME\_CAL\_MODE bit) and for every subsequent line that is read (LINE\_CAL\_MODE bit). The Y\_START input defines the beginning of a frame, Y\_CLOCK defines the beginning of a new row.

**3. Continuous charge (bit 3)**

Some applications may require the use continuous charging of the pixel columns instead of a pre-charge on every line sample operation.

Setting bit CONT\_CHARGE to '1' activates this function. The resistor bit connected to pin PC\_CMD controls the current level on every pixel column.

**4. Internal clock granularities (bits 4, 5, 6 and 7)**

The system clock is divided several times on-chip. Half the system clock rate clocks the X-shift-register that controls the column/pixel readout. Odd and even pixel columns are switched to two separate buses. In the output amplifier, the pixel signals on the two buses are combined into one pixel stream at the same frequency as SYS\_CLOCK.

Use the bits GRAN\_SS\_SEQ\_MSB (bit 7) and GRAN\_SS\_SEQ\_LSB (bit 6) to program the clock that drives the 'snapshot' or synchronous shutter sequencer. This way the integration time in synchronous shutter mode is a multiple of 32, 64, 128, or 256 times the system clock period. To overcome global reset issues, use the longest SS granularity (bits 6 and 7 set to '1').

**Table 16. SS Sequencer Clock Granularities**

GRAN_SS_SEQ_MSB/ LSB	SS-Sequencer Clock	Integration Time Step <sup>[7]</sup>
00	32 × SYS_CLOCK	800 ns
01	64 × SYS_CLOCK	1.6 μs
10	128 × SYS_CLOCK	3.2 μs
11	256 × SYS_CLOCK	6.4 μs

The clock that drives the X-sequencer is a multiple of 4, 8, 16, or 32 times the system clock. Clocking the X-sequencer at a slower rate (longer row blanking time; pixel read out speed is always equal to the SYSTEM\_CLOCK) results in more signal swing for the same light conditions.

**Table 17. X Sequencer Clock Granularities**

GRAN_X_SEQ_MSB/ LSB	X-Sequencer Clock	Row Blanking Time <sup>[7]</sup>
00	4 × SYS_CLOCK	3.5 μs
01	8 × SYS_CLOCK	7 μs
10	16 × SYS_CLOCK	14 μs
11	32 × SYS_CLOCK	28 μs

**5. Pixel reset knee-point for multiple slope operation (bits 8, 9, and 10)**

In normal (single slope) mode the pixel reset is controlled from the left side of the image core using the voltage applied on pin VDDR\_LEFT as pixel reset voltage. In multiple slope operation, apply one or more variable pixel reset voltages.

**Note**

7. Using a SYS\_CLOCK of 40 MHz (25 ns period).

Bits KNEE\_POINT\_MSB and KNEE\_POINT\_LSB select the on chip-generated pixel reset voltage.

Bit KNEE\_POINT\_ENABLE set to '1' switches control to the right side of the image core so the pixel reset voltage (VDDR\_RIGHT), selected by bits KNEE\_POINT\_MSB/LSB, is used.

Use bit KNEE\_POINT\_ENABLE only for multiple slope operation in synchronous shutter mode. In rolling shutter mode, use only the bits KNEE\_POINT\_MSB/LSB to select the second knee-point in dual slope operation. The actual knee-point depends on VDDH, VDDR\_LEFT and VDDC applied to the sensor.

**Table 18. Multiple Slope Register Settings**

KNEE_POINT		Pixel Reset Voltage (V)VDDR_RIGHT	Knee-point (V)
MSB/LSB	ENABLE		
00	0 or 1	VDDR_LEFT	0
01	1	VDDR_LEFT – 0.76	+ 0.76
10	1	VDDR_LEFT – 1.52	+ 1.52
11	1	VDDR_LEFT – 2.28	+ 2.28

**6. External Pixel Reset Voltage for Multiple Slope (bit 11)**

Setting bit VDDR\_RIGHT\_EXT to '1' disables the circuit that generates the variable pixel reset voltage and uses the voltage externally applied to pin VDDR\_RIGHT as the double/multiple slope reset voltage.

Setting bit VDDR\_RIGHT\_EXT to '0' allows you to monitor the variable pixel reset voltage (used for multiple slope operation) on pin VDDR\_RIGHT.

**NROF\_PIXELS Register (11:0)**

After the internal x\_sync is generated (start of the pixel readout of a particular row), the PIXEL\_VALID signal goes high. The PIXEL\_VALID signal goes low when the pixel counter reaches the value loaded in the NROF\_PIXEL register. Due to the fact that two pixels are read at the same clock cycle, you must divide this number by 2 ( $NROF\_PIXELS = (width\ of\ ROI / 2) - 1$ ).

**ROF\_LINES Register (11:0)**

After the internal y1\_sync is generated (start of the frame readout with Y\_START), the line counter increases with each Y\_CLOCK pulse until it reaches the value loaded in the NROF\_LINES register and generates a LAST\_LINE pulse. It must be noted that

the value loaded in the register must be (Number of lines required - 1).

**INT\_TIME Register (11:0)**

Use the INT\_TIME register to set the integration time of the electronic shutter. The interpretation of the INT\_TIME depends on the chosen shutter type (rolling or synchronous).

■ **Global shutter**

After the SS\_START pulse is applied an internal counter counts the number of SS granulated clock cycles until it reaches the value loaded in the INT\_TIME register and generates a TIME\_OUT pulse. Use this TIME\_OUT pulse to generate the SS\_STOP pulse to stop the integration. When the INT\_TIME register is used, the maximum integration time is:

$$TINT\_MAX = 212 \times 256 \text{ (maximum granularity)} \times (40 \text{ MHz}) - 1 = 26.2 \text{ ms.}$$

You can increase this maximum time if you use an external counter to trigger SS\_STOP. Ten is the minimal value that you can load into the INT\_TIME register (see also [Internal clock granularities \(bits 4, 5, 6 and 7\)](#) on page 17).

■ **Rolling shutter**

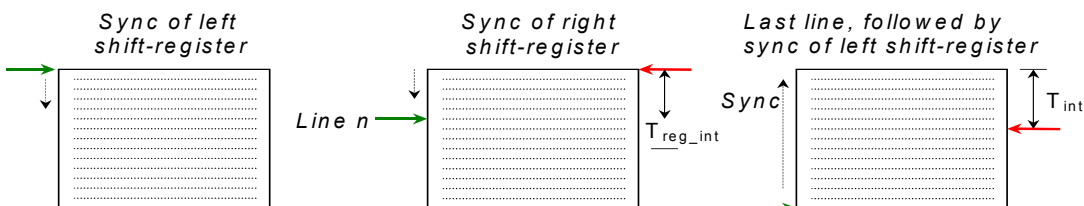
When the Y\_START pulse is applied (start of the frame read-out), the sequencer generates the y1\_sync pulse for the left Y-shift register (read out Y-shift register). This loads the left Y-shift register with the pointer loaded in YL\_REG register. At each Y\_CLOCK pulse, the pointer shifts to the next row and the integration time counter increases until it reaches the value loaded in the INT\_TIME register. At that moment, the sequencer generates the yr\_sync pulse for the right Y-shift register; it loads the right Y-shift register (reset Y-shift register) with the pointer loaded in YR\_REG register (see [Figure 18](#)). The integration time counter is reset when the sync for the left Y-shift register, y1\_sync is asserted. Both shift registers keep moving until the next sync is asserted, i.e., the y1\_sync for the left Y-shift register (generated by Y\_START) and the yr\_sync for the right Y-shift register (generated when the integration time counter reaches the INT\_TIME value).

$T_{reg\_int}$  Difference between the left and right pointer = value set in the INT\_TIME register (number of lines).

The actual integration time is given by  
 $T_{int}$  Integration time [# lines] = NROF\_LINES register – INT\_TIME register.

$T_{int}$  Integration time [# lines] = NROF\_LINES register – INT\_TIME register.

**Figure 18. Synchronization of Shift Registers in Rolling Shutter Mode**



**X\_REG Register (10:0)**

The X\_REG register determines the start position of the window in the X-direction. In this direction, there are 640 possible starting positions (two pixels are addressed at the same time in one clock cycle). If sub sampling is enabled, only the even pixels are set as starting position (for instance: 0, 2, 4, 6, 8... 638).

**YL\_REG (10:0) and YR\_REG (10:0)**

The YL\_REG and YR\_REG registers determine the start position of the window in the Y-direction. In this direction, there are 1024 possible starting positions. In rolling shutter mode the YL\_REG register sets the start position of the read (left) pointer and the YR\_REG sets the start position of the reset (right) pointer. For both shutter types YL\_REG is always equal to YR\_REG.

**Image Core Register (7:0)**

Bits 1:0 of the IMAGE\_CORE register define the test mode of the image core. Setting 00 is the default and normal operation mode. In case the bit is set to '1', the odd (bit 1) or even (bit 0) columns are tight to the reset level. If the internal ADC is used, bits 0 and 1 are used to create test pattern to test the sample moment of the ADC. If the ADC sample moment is not chosen correctly, the created test pattern is not black-white-black-etc. (IMAGE\_CORE register set at 1 or 2) or black-black-white-white-black-black (IMAGE\_CORE register set at 9) but grey shadings if the sensor is saturated.

Bits 7:2 of the IMAGE\_CORE register define the sub-sampling mode in the X-direction (bits 4:2) and in the Y-direction (bits 7:5). The sub-sampling modes and corresponding bit setting are given in Table 11 and Table 12 on page 11.

**Amplifier Register (6:0)**

1. GAIN (bits 3:0)

The gain bits determine the gain setting of the output amplifier. They are only effective if UNITY = 0. The gains and corresponding bit setting are given in Table 13 on page 12.

2. UNITY (bit 4)

In case UNITY = 1, the gain setting of GAIN is bypassed and the gain amplifier is put in unity feedback.

3. DUAL\_OUT (bit 5)

If DUAL\_OUT = 1, the two output amplifiers are active. If DUAL\_OUT = 0, the signals from the two buses are multiplexed to output PXL\_OUT1 which connects to ADC\_IN. The gain amplifier and output driver of the second path are put in standby.

4. STANDBY

If STANDBY = 0, the complete output amplifier is put in standby. For normal use, set STANDBY to '1'.

**DAC\_RAW Register (6:0) and DAC\_FINE (6:0) Register**

These registers determine the black reference level at the output of the output amplifier. Bit setting 111111 for the DAC\_RAW

register gives the highest offset voltage. Bit setting 000000 for the DAC\_RAW register gives the lowest offset voltage. Ideally, if the two output paths have no offset mismatch, the DAC\_FINE register is set to 1000000. Deviation from this value is used to compensate the internal mismatch (see Output Amplifier on page 12).

**ADC Register (2:0)**

1. TRISTATE\_OUT (bit 0)

In case TRISTATE = 0, the ADC\_D<9:0> outputs are in tri-state mode. TRISTATE = 1 for normal operation mode.

2. GAMMA (bit 1)

If GAMMA is set to '1', the ADC input to output conversion is linear; otherwise the conversion follows a 'gamma' law (more contrast in dark parts of the window, lower contrast in the bright parts).

3. BIT\_INV (bit 2)

If BIT\_INV = 1, 0000000000 is the conversion of the lowest possible input voltage, otherwise the bits are inverted.

**Data Interfaces**

Two different data interfaces are implemented. They are selected using pins IF\_MODE (pin 12) and SER\_MODE (pin 6).

**Table 19. Serial and Parallel Interface Selection**

IF_MODE	SER_MODE	Selected interface
1	X	Parallel
0	1	Serial 3 Wire

**Parallel Interface**

The parallel interface uses a 16-bit parallel input (P\_DATA (15:0)) to upload new register values. Asserting P\_WRITE loads the parallel data into the internal register of the IBIS5-B-1300 where it is decoded (see Figure 19). P\_DATA (15:12) address bits REG\_ADDR (3:0); P\_DATA (11:0) data bits REG\_DATA (11:0).

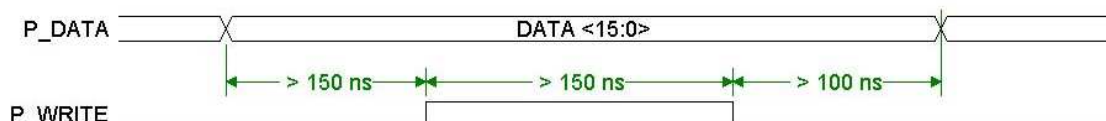
**Serial 3-Wire Interface**

The serial 3-wire interface (or serial-to-parallel Interface) uses a serial input to shift the data in the register buffer. When the complete data word is shifted into the register buffer the data word is loaded into the internal register where it is decoded (see Figure 19). S\_DATA (15:12) address bits REG\_ADDR (3:0); S\_DATA (11:0) data bits REG\_DATA (11:0). When S\_EN is asserted the parallel data is loaded into the internal registers of the IBIS5-B-1300. The maximum tested frequency of S\_DATA is 2.5 MHz.)

**Serial 2-Wire Interface**

The serial 2-wire interface is not operational in the IBIS5-B-1300 image sensor. Use the 3-wire SPI interface to load the sensor registers.

**Figure 19. Parallel Interface Timing**



## Timing Diagrams

### Frame Rate

The pixel rate for this sensor is high enough to support a frame rate of greater than 100 Hz for a window size of 640 × 480 pixels (VGA format). Considering a row blanking time of 3.5 μs (as baseline, see also [Internal clock granularities \(bits 4, 5, 6 and 7\)](#) on page 17), this requires a minimum pixel rate of nearly 40 MHz. The final bandwidth of the column amplifiers, output stage, and others is determined by external bias resistors. With a nominal pixel rate of 40 MHz, a full frame rate of a little more than 27 frames per second is obtained.

The frame period of the IBIS5-B-1300 sensor depends on the shutter type.

#### Rolling Shutter

=> Frame period = (Nr. Lines × (RBT + pixel period × Nr. Pixels)) with:

Nr. Lines      Number of lines read out each frame (Y)  
 Nr. Pixels     Number of pixels read out each line (X)  
 RBT            Row blanking time = 3.5 μs (typical)  
 Pixel period   1/40 MHz = 25 ns

**Example** Read out time of the full resolution at nominal speed (40-MHz pixel rate):

Frame period = (1024 × (3.5 μs + 25 ns × 1280)) = 36.4 ms = 27.5 fps

#### Global shutter

Frame period = Tint + Tread out  
 = Tint + (Nr. Lines × (RBT + pixel period × Nr. Pixels))

with: Tint      Integration (exposure) time  
 Nr. Lines      Number of lines read out each frame (Y)  
 Nr. Pixels      Number of pixels read out each line (X)  
 RBT            Row blanking time = 3.5 μs (typical)  
 Pixel period   1/40 MHz = 25 ns

**Example** Read out time of the full resolution at nominal speed (40 MHz pixel rate) with an integration time of 1 ms:

Frame period = 1 ms + (1024 × (3.5 μs + 25 ns × 1280)) = 37.4 ms = 26.8 fps

### Region-of-Interest (ROI) Read Out

Windowing is easily achieved by uploading the starting point of the X- and Y-shift registers in the sensor registers using the various interfaces. This downloaded starting point initiates the shift register in the X- and Y-direction triggered by the Y\_START (initiates the Y-shift register) and the Y\_CLK (initiates the X-shift register) pulse. The minimum step size for the x-address is two (only even start addresses are chosen) and one for the Y-address (every line is addressable). The frame rate increases almost linearly when fewer pixels are read out. [Table 20](#) gives an overview of the achievable frame rates (in rolling shutter mode) with various ROI dimensions.

**Table 20. Frame Rate vs. Resolution**

Image Resolution (X×Y)	Frame Rate [frames/s]	Frame ReadoutTime [ms]	Comment
1280 × 1024	27	36	Full resolution.
640 × 480	100	10	ROI read out.
100 × 100	1657	0.6	ROI read out.

### Timing Requirements

There are six control signals that operate the image sensor:

- SS\_START
- SS\_STOP
- Y\_CLOCK
- Y\_START
- X\_LOAD
- SYS\_CLOCK

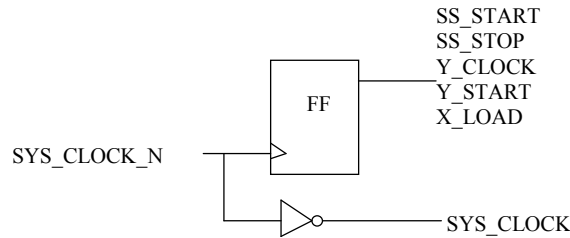
The external system generates these control signals with following time constraints to SYS\_CLOCK (rising edge = active edge):

T<sub>SETUP</sub> > 7.5 ns  
 T<sub>HOLD</sub> > 7.5 ns

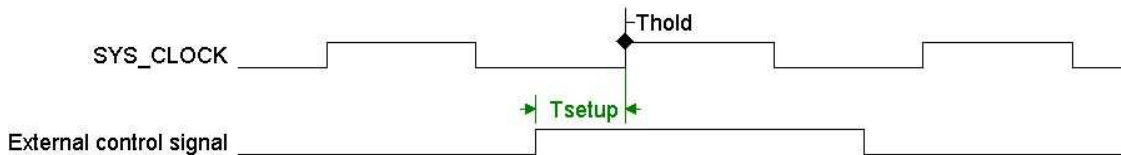
It is important that these signals are free of any glitches.

Figure 20 shows a recommended schematic for generating the basic signals and to avoid any timing problems.

**Figure 20. Recommended Schematic for Basic Signals**



**Figure 21. Relative Timing of 5-Sequencer Control Signal**



**Global Shutter: Single Slope Integration**

SS\_START and SS\_STOP must change on the falling edge of the SYS\_CLOCK ( $T_{setup}$  and  $T_{hold} > 7.5$  ns). Make certain that the pulse width of both signals is a minimum of 1 SYS\_CLOCK cycle. As long as SS\_START or SS\_STOP are asserted, the sequencer stays in a suspended state (see Figure 22).

$T_1$  - Time counted by the integration timer until the value of INT\_TIME register is reached. The integration timer is clocked by the granulated SS-sequencer clock.

$T_2$  - TIME\_OUT signal stays high for one granulated SS-sequencer clock period.

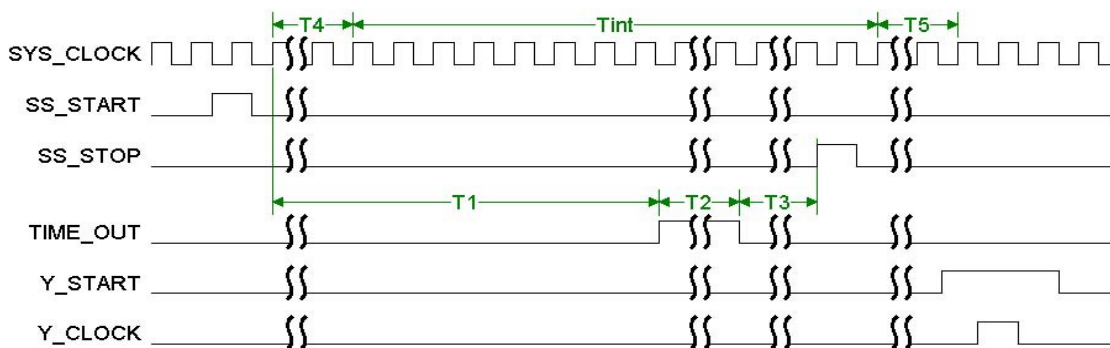
$T_3$  - There are no constraints for this time. Use the TIME\_OUT signal to trigger the SS\_STOP pin (or use an external counter to trigger SS\_STOP); you cannot tie both signals together.

$T_4$  - During this time, the SS-sequencer applies the control signals to reset the image core and start integration. This takes four granulated SS-sequencer clock periods. The integration time counter starts counting at the first rising edge after the falling edge of SS\_START.

$T_5$  - The SS-sequencer puts the image core in a readable state. It takes two granulated SS-sequencer clock periods.

$T_{int}$  - The 'real' integration or exposure time.

**Figure 22. Global Shutter: Single Slope Integration**



**Global Shutter: Pixel Readout**

*Basic Operation*

Y\_START and Y\_CLOCK must change on the falling edge of the SYS\_CLOCK (Tsetup and Thold > 7.5 ns). Make certain that the pulse width is a minimum of one clock cycle for Y\_CLOCK and three clock cycles for Y\_START. As long as Y\_CLOCK is applied, the sequencer stays in a suspended state. (See Figure 23)

T<sub>1</sub> - Row blanking time: During this period, the X-sequencer generates the control signals to sample the pixel signal and pixel reset levels (double sampling fpn-correction), and starts the readout of one line. The row blanking time depends on the granularity of the X-sequencer clock (see Table 21 on page 22).

T<sub>2</sub> - Pixels counted by pixel counter until the value of NROF\_PIXELS register is reached. PIXEL\_VALID goes high when the internal X\_SYNC signal is generated, in other words when the readout of the pixels is started. PIXEL\_VALID goes low

when the pixel counter reaches the value loaded in the NROF\_PIXELS register (after a complete row read out).

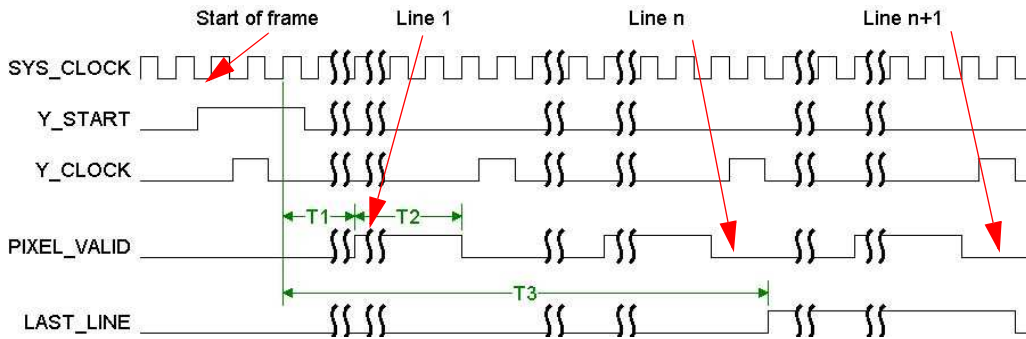
T<sub>3</sub> - LAST\_LINE goes high when the line counter reaches the value loaded in the NROF\_LINES register and stays high for one line period (until the next falling edge of Y-CLOCK).

On Y\_START the left Y-shift-register of the image core is loaded with the YL-pointer that is loaded in to register YL\_REG.

*Advanced Operation:*

It was observed during characterization of the IBIS5-B-1300 image sensor that there are column non-uniformities in the image in synchronous shutter mode, when the Y-readout pointer is still selecting a line during the global reset for the next frame. To avoid this problem, an advanced timing has been generated for the synchronous shutter mode. See question 12 in AN6004, Frequently Asked Questions about the IBIS5 Device for more information. The application note discusses the cause and corrective action for this problem.

**Figure 23. Global Shutter: Pixel Read Out**



*Pixel Output*

The pixel signal at the PXL\_OUT1 output becomes valid after five SYS\_CLOCK cycles when the internal X\_SYNC (start of PIXEL\_VALID output or external X\_LOAD pulse) pulse is asserted (see Figure 24).

T<sub>1</sub> - Row blanking time (see Table 21).

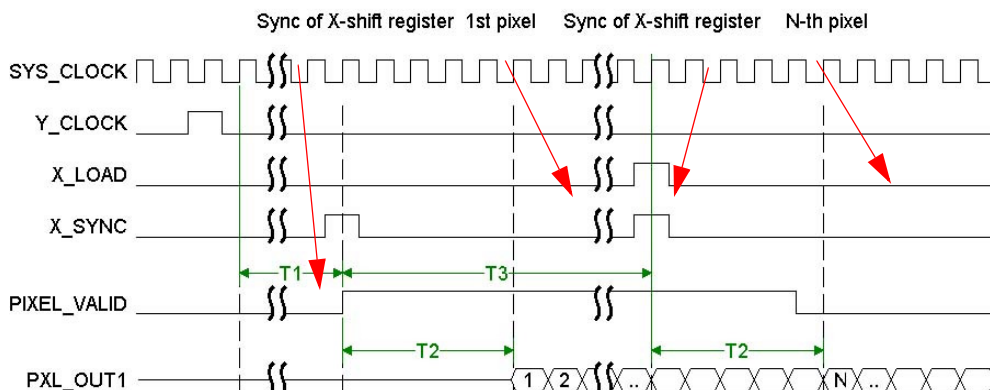
T<sub>2</sub> - 5 SYS\_CLOCK cycles.

T<sub>3</sub> - Time for new X-pointer position upload in X\_REG register (see Windowing in X-Direction on page 24 for more details).

**Table 21. Row Blanking Time as Function of X-Sequencer Granularity**

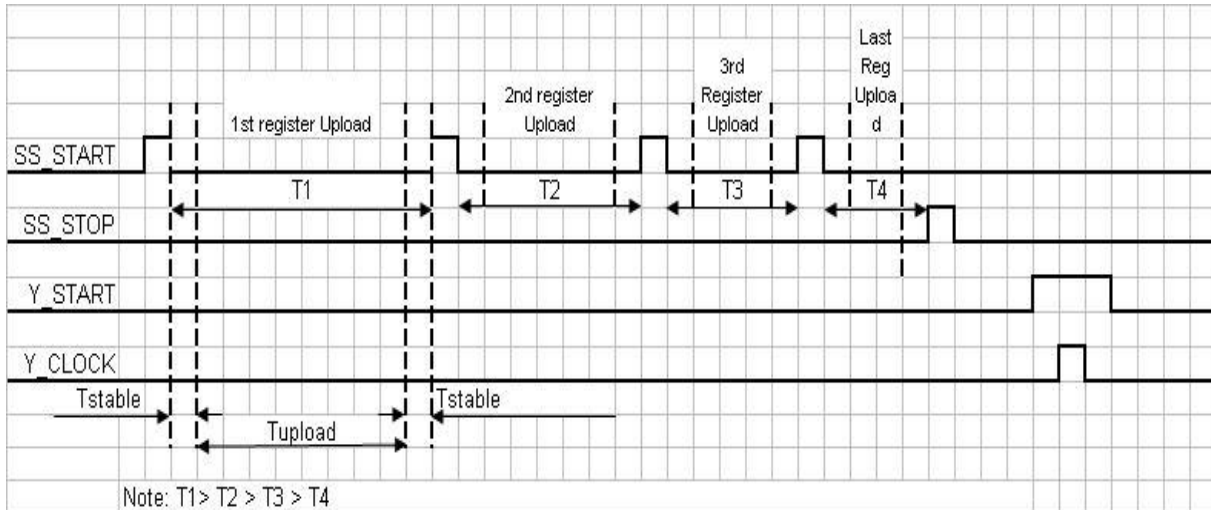
Granularity N <sub>GRAN</sub>	T <sub>1</sub> (μs) = 35 × N <sub>GRAN</sub> × T <sub>SYS_CLOCK</sub>	GRAN_X_SEQ MSB/LSB
× 4	140 × T <sub>SYS_CLOCK</sub> = 3.5	00
× 8	280 × T <sub>SYS_CLOCK</sub> = 7.0	01
× 16	560 × T <sub>SYS_CLOCK</sub> = 14.0	10
× 32	1120 × T <sub>SYS_CLOCK</sub> = 28.0	11

**Figure 24. Pixel Output**



Global Shutter: Multiple Slope Integration

Figure 25. Multiple Slope Integration



Use up to four different pixel reset voltages during multiple slope operation in synchronous shutter mode. This is done by uploading new values to register bits KNEEPOINT\_MSB/LSB/ENABLE before a new SS\_START pulse is applied.

Set bit KNEEPOINT\_ENABLE high to do a pixel reset with a lower voltage.

Set bits KNEEPOINT\_MSB/LSB/ENABLE back to '0' before the SS\_STOP pulse is applied. Every time an SS\_START pulse is applied, the integration time counter is reset.

The TIME\_OUT signal cannot be used in multi-slope operation to determine the location of the next SS\_START or SS\_STOP pulse. External counters must be used for generating these signals.

Table 22. Multiple Slope Register Settings

	Kneepoint	
	MSB/LSB	Enable
Initial Setup	00	0
1st Register Upload	01	1
2nd Register Upload	10	1
3th Register Upload	11	1
4th Register Upload	00	0

Upload the register after time  $T_{stable}$ , otherwise, the change affects the SS-sequencer resulting in a bad pixel reset.  $T_{stable}$  depends on the granularity of the SS-sequencer clock (see Table 23).

Table 23.  $T_{stable}$  for Different Granularity Settings

Granularity $N_{GRAN}$	$T_{stable} (\mu s) = 5 \times N_{GRAN} \times T_{SYS\_CLOCK}$	GRAN_SS_SEQ MSB/LSB
$\times 32$	$160 \times T_{SYS\_CLOCK} = 4$	00
$\times 64$	$320 \times T_{SYS\_CLOCK} = 8$	01
$\times 128$	$640 \times T_{SYS\_CLOCK} = 16$	10
$\times 256$	$1280 \times T_{SYS\_CLOCK} = 32$	11

$T_{upload}$  depends on the interface mode used to upload the registers.

Table 24.  $T_{upload}$  for Different Interface Modes

Interface Mode	$T_{upload} (\mu s)$
Parallel	1
Serial 3-wire	8



### Rolling Shutter Operation

The integration of the light in the image sensor is done during readout of the other lines.

The only difference with synchronous shutter is that the TIME\_OUT pin is used to indicate when the Y\_SYNC pulse for the right Y-shift-register (reset Y-shift register) is generated. This loads the right Y-shift-register with the pointer loaded in register YR\_REG. The Y\_SYNC pulse for the left Y-shift register (read Y-shift register) is generated with Y\_START.

The INT\_TIME register defines how many lines to count before the Y\_SYNC of the right Y-shift-register is generated, hence defining the integration time. See also [INT\\_TIME Register \(11:0\)](#) on page 18 for a detailed description of the rolling shutter operation.

$T_{int}$  Integration time [# lines] = register(NROF\_LINES) – register(INT\_TIME)

**Note** For normal operation the values of the YL\_REG and YR\_REG registers are equal.

### Windowing in X-Direction

An X\_LOAD pulse overrides the internal X\_SYNC signal, loading a new X-pointer (stored in the X\_REG register) into the X-shift-register.

The X\_LOAD pulse must appear on the falling edge of SYS\_CLOCK and remain high for two SYS\_CLOCK cycles overlapping two rising edges of SYS\_CLOCK. The new X-pointer is loaded on one of the two rising edges of SYS\_CLOCK.

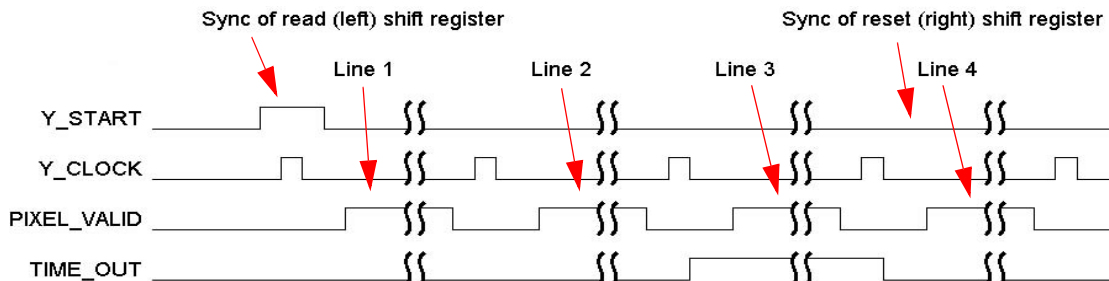
The available time to upload the register is  $T_{load}$ ; it is defined from the previous register load to the rising edge of X\_LOAD. It depends on the settling time of the register and the X-decoder.

**Table 25.  $T_{load}$  for Different Interfaces**

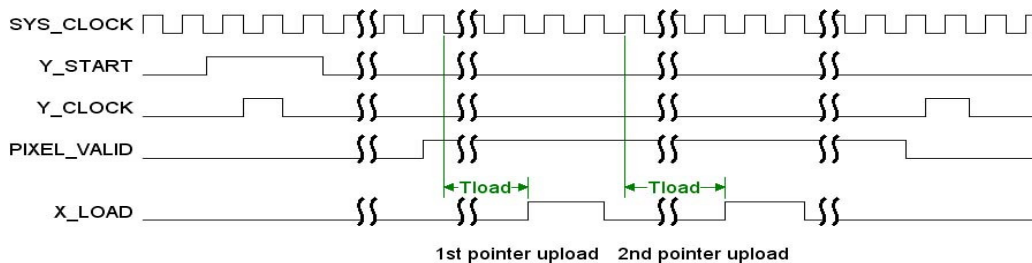
Interface Mode	$T_{load}$ ( $\mu$ s)
Parallel interface	1 (about 40 SYS_CLOCK cycles)
Serial 3 Wire	16 (at 2.5 MHz data rate)

The actual time to load the register itself depends on the interface mode that is used. The parallel interface is the fastest.

**Figure 26. Rolling Shutter Operation**



**Figure 27. Windowing in X-Direction**



**Windowing in Y-Direction**

Reapply the Y\_START pulse after loading a new Y-pointer value into the YL\_REG and YR\_REG registers to load a new Y-pointer into the Y-shift-register.

Every time a Y\_START pulse appears, a frame calibration of the output amplifier occurs.

**Initialization (Startup Behavior)**

To avoid any high current consumption at startup, apply the SYS\_CLOCK signal as soon as possible after or even before power on of the image sensor. After power on, apply SYS\_RESET for a minimum of five SYS\_CLOCK periods to ensure a proper reset of the on-chip sequencer and timing circuitry. All internal registers are set to '0' after SYS\_RESET is applied.

Because all the IBIS5-B-1300 control signals are active high, apply a low level (before SYS\_RESET occurs) to these pins at start up to avoid latch up.

Figure 28. Windowing in Y-Direction

