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# CYP15G0201DXB

# Dual-channel HOTLink II™ Transceiver

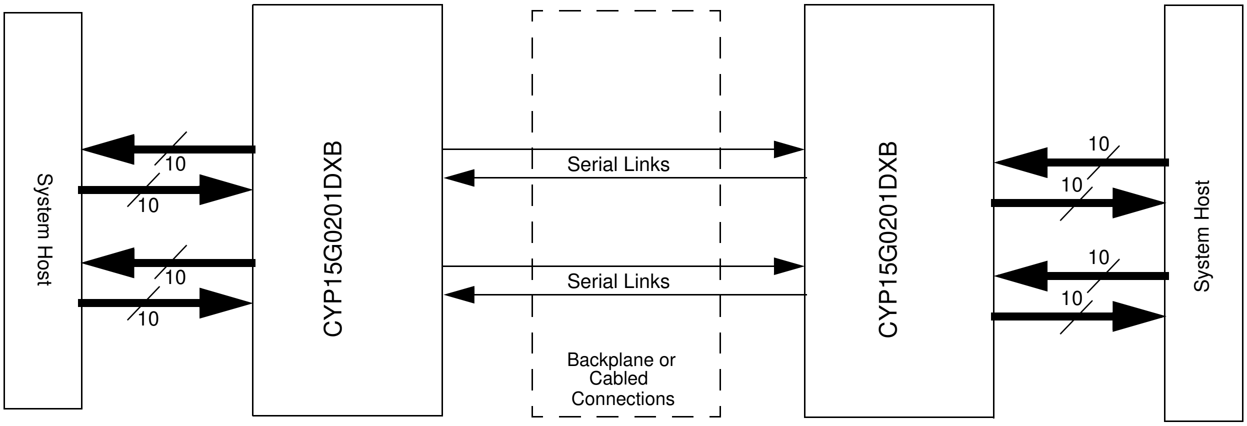
## Features

- Second-generation HOTLink® technology
  - ❐ Compliant to multiple standards
    - ESCON, DVB-ASI, Fibre Channel, and Gigabit Ethernet (IEEE 802.3z)
    - CPRI™ compliant
    - 8B/10B encoded or 10-bit unencoded data
- Dual-channel transceiver operates from 195- to 1500-MBd serial data rate
  - ❐ Aggregate throughput of 6 Gbps
- Selectable parity check/generate
- Selectable dual-channel bonding option
  - ❐ One 16-bit channels
- Skew alignment support for multiple bytes of offset
- Selectable I/O clocking options
- MultiFrame™ receive framer
  - ❐ Bit and byte alignment
  - ❐ Comma or full K28.5 detect
  - ❐ Single- or multi-byte framer for byte alignment
  - ❐ Low-latency option
- Synchronous LVTTL parallel interface
- Internal phase-locked loops (PLLs) with no external PLL components
- Optional phase-align buffer in transmit path
- Optional elasticity buffer in receive path
- Dual differential positive ECL (PECL) compatible serial inputs per channel
  - ❐ Internal DC-restoration
- Dual differential PECL-compatible serial outputs per channel
  - ❐ Source matched for 50-Ω transmission lines
  - ❐ No external bias resistors required
  - ❐ Signaling-rate controlled edge-rates
- Compatible with
  - ❐ Fiber optic modules
  - ❐ Copper cables
  - ❐ Circuit board traces
- JTAG boundary scan
- Built-in self-test (BIST) for at-speed link testing
- Per-channel link quality indicator
  - ❐ Analog signal detect
  - ❐ Digital signal detect
- Low power 1.8 W at 3.3-V typical
- Single 3.3 V supply
- 196-ball BGA
- Pb-free package
- 0.25-µm BiCMOS technology

## Functional Description

The CYP15G0201DXB dual-channel HOTLink II™ transceiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 195- to 1500-MBd per serial link.

**Figure 1. HOTLink II™ System Connections**



The CYP15G0201DXB operates from 195 to 1500 MBd.

The two channels may be combined to allow transport of wide buses across significant distances with minimal concern for offsets in clock phase or link delay. Each transmit channel accepts parallel characters in an input register, encodes each character for transport, and converts it to serial data. Each receive channel accepts serial data and converts it to parallel data, decodes the data into characters, and presents these characters to an Output Register. Figure 1 on page 1 illustrates typical connections between independent host systems and corresponding CYP15G0201DXB parts. As a second-generation HOTLink device, the CYP15G0201DXB extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data, command, and BIST) with other HOTLink devices.

The transmit (TX) section of the CYP15G0201DXB Dual HOTLink II consists of two byte-wide channels that can be operated independently or bonded to form wider buses. Each channel can accept either 8-bit data characters or pre-encoded 10-bit transmission characters. Data characters are passed from the Transmit Input Register to an embedded 8B/10B Encoder to improve their serial transmission characteristics. These encoded characters are then serialized and output from dual Positive ECL (PECL) compatible differential transmission-line drivers at a bit-rate of either 10 or 20 times the input reference clock.

The receive (RX) section of the CYP15G0201DXB Dual HOTLink II consists of two byte-wide channels that can be operated independently or synchronously bonded for greater bandwidth. Each channel accepts a serial bit-stream from one of two PECL-compatible differential line receivers and, using a completely integrated PLL clock synchronizer, recovers the timing information necessary for data reconstruction. Each recovered bit-stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are then written to an internal Elasticity Buffer, and presented to the destination host system. The integrated 8B/10B encoder/decoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface.

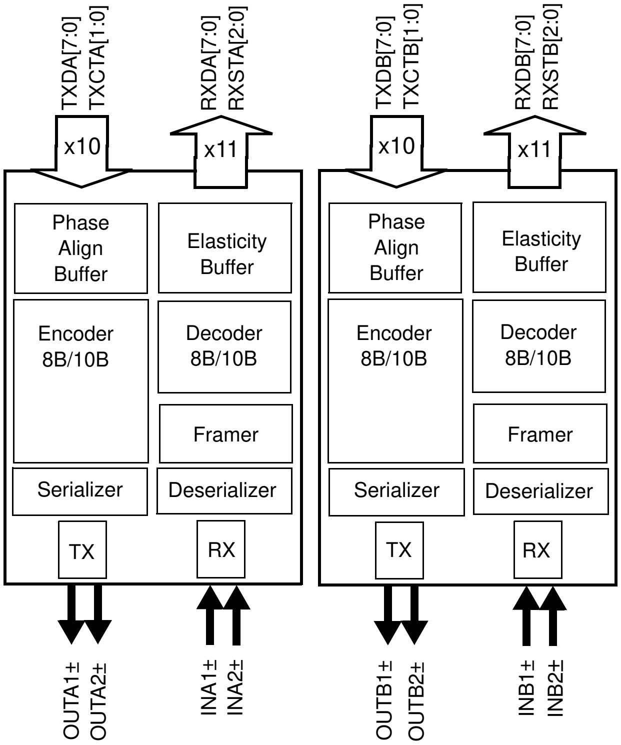
For those systems using buses wider than a single byte, the two independent receive paths can be bonded together to allow synchronous delivery of data across a two-byte-wide (16-bit) path.

The parallel I/O interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. In addition to clocking the transmit path interfaces from one of multiple sources, the receive interface may be configured to present data relative to a recovered clock or to a local reference clock.

Each transmit and receive channel contains independent BIST pattern generators and checkers. This BIST hardware allows at-speed testing of the high-speed serial data paths in each transmit and receive section, and across the interconnecting links.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting backplanes on switches, routers, base-stations, servers and video transmission systems.

## Transceiver Logic Block Diagram



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## Pin Configuration

Top View [1]

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $V_{CC}$ | INA2+ | OUTA2– | $V_{CC}$ | INA1+ | OUTA1– | $V_{CC}$ | $V_{CC}$ | INB2+ | OUTB2– | $V_{CC}$ | INB1+ | OUTB1– | $V_{CC}$ |
| **B** | TDO | INA2– | OUTA2+ | $V_{CC}$ | INA1– | OUTA1+ | NC | NC | INB2– | OUTB2+ | $V_{CC}$ | INB1– | OUTB1+ | BOE[3] |
| **C** | NC | RFEN | $V_{CC}$ | LPEN | RXLE | RXRATE | **GND** | **GND** | SPDSEL | PARCTL | RFMODE | $V_{CC}$ | SDASEL | BOE[2] |
| **D** | $V_{CC}$ | $V_{CC}$ | NC | TXRATE | RXMODE [1] | RXMODE [0] | **GND** | **GND** | TCLK | TDI | INSELB | INSELA | $V_{CC}$ | $V_{CC}$ |
| **E** | BISTLE | FRAM CHAR | TXMODE [1] | TXMODE [0] | BOE[0] | BOE[1] | **GND** | **GND** | TXOPB | TXPERB | TXCKSEL | RXCKSEL | $\overline{\text{TRSTZ}}$ | TMS |
| **F** | DECMODE | OELE | RXCLKC+ | RXSTA[2] | RXSTA[1] | **GND** | **GND** | **GND** | **GND** | TXDB[4] | TXDB[3] | TXDB[2] | TXDB[1] | TXDB[0] |
| **G** | $V_{CC}$ | NC | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | NC | $V_{CC}$ |
| **H** | $V_{CC}$ | NC | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | NC | $V_{CC}$ |
| **J** | RXSTA[0] | RXOPA | RXDA[0] | RXDA[1] | RXDA[2] | **GND** | **GND** | **GND** | **GND** | TXCTB[0] | TXCTB[1] | TXDB[7] | TXDB[6] | TXDB[5] |
| **K** | RXDA[3] | RXDA[4] | RXDA[5] | RXDA[6] | TXDA[4] | TXCLKA | **GND** | **GND** | NC | RXOPB | RXCLKB+ | RXCLKB- | $\overline{\text{LFIB}}$ | TXCLKB |
| **L** | $V_{CC}$ | $V_{CC}$ | RXDA[7] | $\overline{\text{LFIA}}$ | TXDA[3] | TXOPA | **GND** | **GND** | SCSEL | RXSTB[2] | RXSTB[1] | RXDB[7] | $V_{CC}$ | $V_{CC}$ |
| **M** | RXCLKA- | TXCTA[1] | $V_{CC}$ | NC | TXDA[2] | TXPERA | **GND** | **GND** | $\overline{\text{TXRST}}$ | NC | RXSTB[0] | $V_{CC}$ | RXDB[5] | RXDB[6] |
| **N** | RXCLKA+ | TXCTA[0] | TXDA[6] | $V_{CC}$ | TXDA[1] | NC | NC | NC | REFCLK- | TXCLKO+ | $V_{CC}$ | RXDB[2] | RXDB[3] | RXDB[4] |
| **P** | $V_{CC}$ | TXDA[7] | TXDA[5] | $V_{CC}$ | TXDA[0] | NC | $V_{CC}$ | $V_{CC}$ | REFCLK+ | TXCLKO- | $V_{CC}$ | RXDB[1] | RXDB[0] | $V_{CC}$ |

**Note**

1. NC = Do not connect.

## Pin Configuration

Bottom View[1]

| 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | OUTB1– | INB1+ | $V_{CC}$ | OUTB2– | INB2+ | $V_{CC}$ | $V_{CC}$ | OUTA1– | INA1+ | $V_{CC}$ | OUTA2– | INA2+ | $V_{CC}$ | **A** |
| BOE[3] | OUTB1+ | INB1– | $V_{CC}$ | OUTB2+ | INB2– | NC | NC | OUTA1+ | INA1– | $V_{CC}$ | OUTA2+ | INA2– | TDO | **B** |
| BOE[2] | SDASEL | $V_{CC}$ | RFMODE | PARCTL | SPDSEL | **GND** | **GND** | RXRATE | RXLE | LPEN | $V_{CC}$ | RFEN | NC | **C** |
| $V_{CC}$ | $V_{CC}$ | INSELA | INSELB | TDI | TCLK | **GND** | **GND** | RXMODE[0] | RXMODE[1] | TXRATE | NC | $V_{CC}$ | $V_{CC}$ | **D** |
| TMS | $\overline{TRSTZ}$ | RXCKSEL | TXCKSEL | TXPERB | TXOPB | **GND** | **GND** | BOE[1] | BOE[0] | TXMODE[0] | TXMODE[1] | FRAMCHAR | BISTLE | **E** |
| TXDB[0] | TXDB[1] | TXDB[2] | TXDB[3] | TXDB[4] | **GND** | **GND** | **GND** | **GND** | RXSTA[1] | RXSTA[2] | RXCLKC+ | OELE | DECMODE | **F** |
| $V_{CC}$ | NC | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | NC | $V_{CC}$ | **G** |
| $V_{CC}$ | NC | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | **GND** | NC | $V_{CC}$ | **H** |
| TXDB[5] | TXDB[6] | TXDB[7] | TXCTB[1] | TXCTB[0] | **GND** | **GND** | **GND** | **GND** | RXDA[2] | RXDA[1] | RXDA[0] | RXOPA | RXSTA[0] | **J** |
| TXCLKB | $\overline{LFIB}$ | RXCLKB- | RXCLKB+ | RXOPB | NC | **GND** | **GND** | TXCLKA | TXDA[4] | RXDA[6] | RXDA[5] | RXDA[4] | RXDA[3] | **K** |
| $V_{CC}$ | $V_{CC}$ | RXDB[7] | RXSTB[1] | RXSTB[2] | SCSEL | **GND** | **GND** | TXOPA | TXDA[3] | $\overline{LFIA}$ | RXDA[7] | $V_{CC}$ | $V_{CC}$ | **L** |
| RXDB[6] | RXDB[5] | $V_{CC}$ | RXSTB[0] | NC | $\overline{TXRST}$ | **GND** | **GND** | TXPERA | TXDA[2] | NC | $V_{CC}$ | TXCTA[1] | RXCLKA- | **M** |
| RXDB[4] | RXDB[3] | RXDB[2] | $V_{CC}$ | TXCLKO+ | REFCLK- | NC | NC | NC | TXDA[1] | $V_{CC}$ | TXDA[6] | TXCTA[0] | RXCLKA+ | **N** |
| $V_{CC}$ | RXDB[0] | RXDB[1] | $V_{CC}$ | TXCLKO- | REFCLK+ | $V_{CC}$ | $V_{CC}$ | NC | TXDA[0] | $V_{CC}$ | TXDA[5] | TXDA[7] | $V_{CC}$ | **P** |

## Pin Descriptions

CYP15G0201DXB Dual HOTLink II Transceiver

| Pin Name | I/O Characteristics | Signal Description |
|---|---|---|
| **Transmit Path Data Signals** | | |
| TXPERA<br>TXPERB | LVTTL Output, changes relative to REFCLK↑ [2] | **Transmit Path Parity Error**. Active HIGH. Asserted (HIGH) if parity checking is enabled and a parity error is detected at the Encoder. This output is HIGH for one transmit character clock period to indicate detection of a parity error in the character presented to the Encoder.<br>If a parity error is detected, the character in error is replaced with a C0.7 character to force a corresponding bad-character detection at the remote end of the link. This replacement takes place regardless of the encoded/non-encoded state of the interface.<br>When BIST is enabled for the specific transmit channel, BIST progress is presented on these outputs. Once every 511 character times (plus a 16-character Word Sync Sequence when the receive channels are clocked by a common clock, that is, RXCKSEL = LOW or HIGH), the associated TXPERx signal pulses HIGH for one transmit-character clock period (if RXCKSEL = MID) or seventeen transmit- character clock periods (if RXCKSEL = LOW or HIGH) to indicate a complete pass through the BIST sequence. For RXCKSEL = LOW or HIGH, if TXMODE[1:0] = LL, then no Word Sync Sequence is sent in BIST, and TXPERx pulses HIGH for one transmit-character clock period.<br>These outputs also provide indication of a transmit Phase-Align Buffer underflow or overflow. When the transmit Phase-Align Buffers are enabled (TXCKSEL ≠ LOW, or TXCKSEL = LOW and TXRATE = HIGH), if an underflow or overflow condition is detected, TXPERx for the channel in error is asserted and remains asserted until either an atomic word sync sequence is transmitted or $\overline{\text{TXRST}}$ is sampled LOW to re-center the transmit phase-align buffers. |
| TXCTA[1:0]<br>TXCTB[1:0] | LVTTL Input, synchronous, sampled by the selected TXCLKx↑ or REFCLK↑ [2] | **Transmit Control**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL, and are passed to the Encoder or Transmit Shifter. They identify how the associated TXDx[7:0] characters are interpreted. When the Encoder is bypassed, these inputs are interpreted as data bits. When the Encoder is enabled, these inputs determine if the TXDx[7:0] character is encoded as Data, a Special Character code, or replaced with other Special Character codes. See Table 1 on page 13 for details. |
| TXDA[7:0]<br>TXDB[7:0] | LVTTL Input, synchronous, sampled by the selected TXCLKx↑ or REFCLK↑ [2] | **Transmit Data Inputs**. These inputs are captured on the rising edge of the transmit interface clock (selected by TXCKSEL) and passed to the Encoder or Transmit Shifter.<br>When the Encoder is enabled (TXMODE[1:0] ≠ LL), TXDx[7:0] specify the specific data or command character to be sent.<br>When the Encoder is bypassed, these inputs are interpreted as data bits of the 10-bit input character. See Table 1 on page 13 for details. |
| $\overline{\text{TXRST}}$ | LVTTL Input, asynchronous, internal pull-up, REFCLK↑ [2] | **Transmit Clock Phase Reset**. **Transmit Clock Phase Reset**. Active LOW. When sampled LOW, the transmit Phase-align Buffers are allowed to adjust their data-transfer timing (relative to the selected input clock) to allow clean transfer of data from the Input Register to the Encoder or Transmit Shifter. When $\overline{\text{TXRST}}$ is sampled HIGH, the internal phase relationship between the associated TXCLKx and the internal character-rate clock is fixed and the device operates normally.<br>When configured for half-rate REFCLK sampling of the transmit character stream (TXCKSEL = LOW and TXRATE = HIGH), assertion of $\overline{\text{TXRST}}$ is only used to clear Phase-align buffer faults caused by highly asymmetric REFCLK periods or REFCLKs with excessive cycle-to-cycle jitter. During this alignment period, one or more characters may be added to or lost from all the associated transmit paths as the transmit Phase-align Buffers are adjusted. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive rising edges of REFCLK to ensure the reset operation is initiated correctly on all channels. This input is ignored when both TXCKSEL and TXRATE are LOW, since the phase align buffer is bypassed. In all other configurations, $\overline{\text{TXRST}}$ should be asserted during device initialization to ensure proper operation of the Phase-align buffer. $\overline{\text{TXRST}}$ should be asserted after presence of a valid TXCLKx and after allowing enough time for the TXPLL to lock to the reference clock (as specified by parameter $t_{TXLOCK}$). |

**Note**

2. When REFCLK is configured for half-rate operation (TXRATE = HIGH), these inputs are sampled (or the outputs change) relative to both the rising and falling edges of REFCLK.

## Pin Descriptions (continued)

CYP15G0201DXB Dual HOTLink II Transceiver

| Pin Name | I/O Characteristics | Signal Description |
|---|---|---|
| SCSEL | LVTTL Input, synchronous, internal pull-down, sampled by TXCLKA↑ or REFCLK↑ [2] | **Special Character Select**. Used in some transmit modes along with TXCTx[1:0] to encode special characters or to initiate a Word Sync Sequence. When the transmit paths are configured for independent inputs clocks (TXCKSEL = MID), SCSEL is captured relative to TXCLKA↑. |
| TXOPA<br>TXOPB | LVTTL Input, synchronous, internal pull-up, sampled by the respective TXCLKx↑ or REFCLK↑ [2] | **Transmit Path Odd Parity**. When parity checking is enabled (PARCTL ≠ LOW), the parity captured at these inputs is XORed with the data on the associated transmit data TXDx bus to verify the integrity of the captured character. |
| **Transmit Path Clock and Clock Control** | | |
| TXCKSEL | 3-Level Select[3] Static Control Input | **Transmit Clock Select**. Selects the clock source, used to write data into the Transmit Input Register, of the transmit channel(s).<br>When LOW, both Input Registers are clocked by REFCLK↑ [2]. When MID, TXCLKx↑ is used as the Input Register clock for TXDx[7:0] and TXCTx[1:0]. When HIGH, TXCLKA↑ is used to clock data into the Input Register of each channel.<br>When TXCKSEL = MID or HIGH (TXCLKx or TXCLKA selected to clock input register), configuring TXRATE = HIGH (Half-rate REFCLK) is an invalid mode of operation. |
| TXRATE | LVTTL Input, Static Control input, internal pull-down | **Transmit PLL Clock Rate Select**. When TXRATE = HIGH, the Transmit PLL multiplies REFCLK by 20 to generate the serial symbol-rate clock. When TXRATE = LOW, the transmit PLL multiplies REFCLK by 10 to generate the serial symbol-rate clock. See Table 10 on page 19 for a list of operating serial rates.<br>When REFCLK is selected to clock the receive parallel interfaces (RXCKSEL = LOW), the TXRATE input also determines if the clocks on the RXCLKA± and RXCLKC± outputs are full or half-rate. When TXRATE = HIGH (REFCLK is half-rate), the RXCLKA± and RXCLKC± output clocks are also half-rate clocks and follow the frequency and duty cycle of the REFCLK input. When TXRATE = LOW (REFCLK is full-rate), the RXCLKA± and RXCLKC± output clocks are full-rate clocks and follow the frequency and duty cycle of the REFCLK input.<br>When TXCKSEL = MID or HIGH (TXCLKx or TXCLKA selected to clock input register), configuring TXRATE = HIGH (Half-rate REFCLK) is an invalid mode of operation. |
| TXCLKO± | LVTTL Output | **Transmit Clock Output**. This true and complement output clock is synthesized by the transmit PLL and operates synchronous to the internal transmit character clock. It operates at either the same frequency as REFCLK (when TXRATE = LOW), or at twice the frequency of REFCLK (when TXRATE = HIGH). This output clock has no direct phase relationship to REFCLK. |
| TXCLKA<br>TXCLKB | LVTTL Clock Input, internal pull-down | **Transmit Path Input Clocks**. These clocks must be frequency-coherent to TXCLKO±, but may be offset in phase. The internal operating phase of each input clock (relative to REFLCK or TXCLKO±) is adjusted when TXRST = LOW and locked when TXRST = HIGH. |
| **Transmit Path Mode Control** | | |
| TXMODE[1:0] | 3-Level Select[3] Static Control inputs | **Transmit Operating Mode**. These inputs are interpreted to select one of nine operating modes of the transmit path. See Table 3 on page 15 for a list of operating modes. |

---

**Note**

[3] 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to $V_{SS}$ (ground). The HIGH level is usually implemented by direct connection to $V_{CC}$ (power). When not connected or allowed to float, a 3-Level select input self-biases to the MID level.

## Pin Descriptions (continued)

CYP15G0201DXB Dual HOTLink II Transceiver

| Pin Name | I/O Characteristics | Signal Description |
|---|---|---|
| **Receive Path Data Signals** | | |
| RXDA[7:0]<br>RXDB[7:0] | LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [2] input | **Parallel Data Output**. These outputs change following the rising edge of the selected receive interface clock.<br>When the Decoder is enabled (DECMODE = HIGH or MID), these outputs represent either received data or special characters. The status of the received data is represented by the values of RXSTx[2:0]. When the Decoder is bypassed (DECMODE = LOW), RXDx[7:0] become the higher order bits of the 10-bit received character. See Table 16 on page 25 for details. |
| RXSTA[2:0]<br>RXSTB[2:0] | LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [2] input | **Parallel Status Output**. These outputs change following the rising edge of the selected receive interface clock.<br>When the Decoder is bypassed (DECMODE = LOW), RXSTx[1:0] become the two low-order bits of the 10-bit received character, while RXSTx[2] = HIGH indicates the presence of a Comma character in the Output Register. See Table 16 on page 25 for details.<br>When the Decoder is enabled (DECMODE = HIGH or MID), RXSTx[2:0] provide status of the received signal. See Table 18 on page 27, Table 19 and Table 20 on page 30 for a list of Receive Character status. |
| RXOPA<br>RXOPB | 3-state, LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [2] input | **Receive Path Odd Parity**. When parity generation is enabled (PARCTL ≠ LOW), the parity output at these pins is valid for the data on the associated RXDx bus bits. When parity generation is disabled (PARCTL = LOW) these output drivers are disabled (High-Z). |
| **Receive Path Clock and Clock Control** | | |
| RXRATE | LVTTL Input<br>Static Control Input, internal pull-down | **Receive Clock Rate Select**. When LOW, the RXCLKx± recovered clock outputs are complementary clocks operating at the recovered character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–. When HIGH, the RXCLKx± recovered clock outputs are complementary clocks operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–.<br>When REFCLK± is selected to clock the output registers (RXCKSELx = LOW), RXRATEx is not interpreted. The RXCLKA± and RXCLKC± output clocks follow the frequency and duty cycle of REFCLK±. |
| RXCLKA±<br>RXCLKB± | Three-state, LVTTL Output clock or Static control input | **Receive Character Clock Output or Clock Select Input**. When configured such that all output data paths are clocked by the recovered clock (RXCKSEL = MID), these true and complement clocks are the receive interface clocks which are used to control timing of output data (RXDx[7:0], RXSTx[2:0] and RXOPx). These clocks are output continuously at either the dual-character rate (1/20th the serial symbol-rate) or character rate (1/10th the serial symbol-rate) of the data being received, as selected by RXRATE.<br>When configured such that all output data paths are clocked by REFCLK instead of a recovered clock (RXCKSEL = LOW), the RXCLKA± and RXCLKC+ output drivers present a buffered and delayed form of REFCLK. RXCLKA± and RXCLKC+ are buffered forms of REFCLK that are slightly different in phase. This phase difference allows the user to select the optimal setup/hold timing for their specific interface.<br>When RXCKSEL = HIGH and dual-channel bonding is enabled, one of the recovered clocks from channels A or B is selected to present bonded data from channels A and B. RXCLKA± output the recovered clock from either receive channel A or receive channel B as selected by RXCLKB+ to clock the bonded output data from channels A and B. See Table 14 on page 24 for details.<br>When RXCKSEL = LOW and dual-channel bonding is enabled, REFCLK is selected to present bonded data from channels A and B. RXCLKA± and RXCLKC+ output drivers present a buffered and delayed form of REFCLK. The master channel for bonding is selected by RXCLKB+ (which acts as an input in this mode) to clock the bonded output data from channels A and B. See Table 14 on page 24 for details. |

## Pin Descriptions (continued)

CYP15G0201DXB Dual HOTLink II Transceiver

| Pin Name | I/O Characteristics | Signal Description |
|---|---|---|
| RXCKSEL | 3-Level Select[3]<br>Static Control Input | **Receive Clock Mode**. Selects the receive clock-source used to transfer data to the output registers.<br>When LOW, both Output Registers are clocked by REFCLK. RXCLKB± outputs are disabled (High-Z), and RXCLKA± and RXCLKC+ present buffered and delayed forms of REFCLK.<br>When MID, each RXCLKx± output follows the recovered clock for the respective channel, as selected by RXRATE. When the 8B/10B Decoder and Elasticity Buffer are bypassed (DECMODE = LOW), RXCKSEL must be MID.<br>When HIGH, and channel bonding is enabled in dual-channel mode (RX modes 2 and 3), RXCLKA± outputs the recovered clock from either receive channel A or receive channel B as selected by RXCLKB+. These output clocks may operate at the character-rate or half the character-rate as selected by RXRATE. |
| DECMODE | 3-Level Select[3]<br>Static Control Input | **Decoder Mode Select**. This input selects the behavior of the Decoder block.<br>When LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. When the Decoder is bypassed, RXCKSEL must be MID.<br>When MID, the Decoder is enabled and the Cypress decoder table for Special Code characters is used. When HIGH, the Decoder is enabled and the alternate Decoder table for Special Code characters is used. See Table 25 on page 47 for a list of the Special Codes supported in both encoded modes. |
| RXMODE[1:0] | 3-Level Select[3]<br>Static Control Inputs | **Receive Operating Mode**. These inputs are interpreted to select one of nine operating modes of the receive path. See Table 13 on page 23 for details. |
| RFEN | LVTTL input,<br>asynchronous,<br>internal pull-down | **Reframe Enable for All Channels**. Active HIGH. When HIGH, the framers in both channels are enabled to frame per the presently enabled framing mode and selected framing character. |
| RFMODE | 3-Level Select[3]<br>Static Control Input | **Reframe Mode Select**. Used to control the type of character framing used to adjust the character boundaries (based on detection of one or more framing characters in the received serial bit stream). This signal operates in conjunction with the presently enabled channel bonding mode, and the type of framing character selected.<br>When LOW, the low-latency framer is selected. This frames on each occurrence of the selected framing character(s) in the received data stream. This mode of framing stretches the recovered clock for one or multiple cycles to align that clock with the recovered data.<br>When MID, the Cypress-mode multi-byte parallel framer is selected. This requires a pair of the selected framing character(s), on identical 10-bit boundaries, within a span of 50 bits, before the character boundaries are adjusted. The recovered character clock remains in the same phasing regardless of character offset.<br>When HIGH, the alternate mode multi-byte parallel framer is selected. This requires detection of the selected framing character(s) of the allowed disparities in the received serial bit stream, on identical 10-bit boundaries, on four directly adjacent characters. The recovered character clock remains in the same phasing regardless of character offset. |
| FRAMCHAR | 3-Level Select[3]<br>Static Control Input | **Framing Character Select**. Used to control the character or portion of a character used for character framing of the received data streams.<br>When MID, the framer looks for both positive and negative disparity versions of the 8-bit Comma character. When HIGH, the framer looks for both positive and negative disparity versions of the K28.5 character. Configuring FRAMCHAR to LOW is reserved for component test. |

## Pin Descriptions (continued)

CYP15G0201DXB Dual HOTLink II Transceiver

| Pin Name | I/O Characteristics | Signal Description |
|---|---|---|
| **Device Control Signals** | | |
| PARCTL | 3-Level Select[3] Static Control Input | **Parity Check/Generate Control**. Used to control the different parity check and generate functions.<br>When LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z). When MID, and the Encoder/Decoder are enabled (TXMODE[1] ≠ LOW, DECMODE ≠ LOW), TXDx[7:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[7:0] outputs and presented on RXOPx. When the Encoder and Decoder are disabled (TXMODE[1] = LOW, DECMODE = LOW), the TXDx[7:0] and TXCTx[1:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[7:0] and RXSTx[1:0] outputs and presented on RXOPx. When HIGH, parity checking and generation are enabled. The TXDx[7:0] and TXCTx[1:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[7:0] and RXSTx[2:0] outputs and presented on RXOPx. |
| REFCLK± | Differential LVPECL or single-ended LVTTL input clock | **Reference Clock**. This clock input is used as the timing reference for the transmit and receive PLLs. This input clock may also be selected to clock the transmit and receive parallel interfaces. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLK input, and leave the alternate REFCLK input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs. When TXCKSEL = LOW, REFCLK is also used as the clock for the parallel transmit data (input) interface. When RXCKSEL = LOW, the Elasticity Buffer is enabled and REFCLK is used as the clock for the parallel receive data (output) interface.<br>If the Elasticity Buffer is used, then the framing characters are inserted or deleted to/from the data stream to compensate frequency differences between the reference clock and recovered clock. When addition happens, a K28.5 is appended immediately after a framing character is detected in the elasticity buffer. When deletion happens, a framing character is removed from the datastream when detected in the elasticity buffer. |
| RXCLKC+ | 3-state LVTTL Output | **Delayed REFCLK+ when RXCKSEL = LOW**. Delayed form of REFCLK+, used for transfer of recovered data to a host system. This output is only enabled when the receive parallel interface is configured to present data relative to REFCLK (RXCKSEL = LOW). |
| SPDSEL | 3-Level Select[3], static control input | **Serial Rate Select**. This input specifies the operating bit-rate range of both transmit and receive PLLs. LOW = 195 to 400 MBd, MID = 400 to 800 MBd, HIGH = 800 to 1500 MBd (800–1540 MBd for CYW15G0201DXB). When SPDSEL is LOW, setting TXRATE = HIGH (Half-rate Reference Clock) is invalid. |
| $\overline{\text{TRSTZ}}$ | LVTTL Input, internal pull-up | **Device Reset**. Active LOW. Initializes all state machines and counters in the device.<br>When sampled LOW by the rising edge of REFLCK, this input resets the internal state machines and sets the Elasticity Buffer pointers to a nominal offset. When the reset is removed ($\overline{\text{TRSTZ}}$ sampled HIGH by REFCLK↑), the status and data outputs become deterministic in less than 16 REFCLK cycles.<br>The BISTLE, OELE, and RXLE latches are reset by $\overline{\text{TRSTZ}}$.<br>If the Elasticity Buffer or the Phase Align Buffer are used, $\overline{\text{TRSTZ}}$ should be applied after power-up to initialize the internal pointers into these memory arrays. |
| **Analog I/O and Control** | | |
| OUTA1±<br>OUTB1± | CML Differential Output | **Primary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3 V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules. |
| OUTA2±<br>OUTB2± | CML Differential Output | **Secondary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3 V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules. |
| INA1±<br>INB1± | LVPECL Differential Input | **Primary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The INx1± serial streams are passed to the receiver Clock and Data Recovery (CDR) circuits to extract the data content when INSELx = HIGH. |

## Pin Descriptions (continued)

CYP15G0201DXB Dual HOTLink II Transceiver

| Pin Name | I/O Characteristics | Signal Description |
|---|---|---|
| INA2±<br>INB2± | LVPECL Differential Input | **Secondary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The INx2± serial streams are passed to the receiver Clock and Data Recovery (CDR) circuits to extract the data content when INSELx = LOW. |
| INSELA<br>INSELB | LVTTL Input, asynchronous | **Receive Input Selector**. Determines which external serial bit stream is passed to the receiver Clock and Data Recovery circuit. When HIGH, the INx1± input is selected. When LOW, the INx2± input is selected. |
| SDASEL | 3-Level Select[3], static configuration input | **Signal Detect Amplitude Level Select**. Allows selection of one of three predefined amplitude trip points for a valid signal indication, as listed in Table 11 on page 20. |
| LPEN | LVTTL Input, asynchronous, internal pull-down | **All-Port Loop-Back-Enable**. Active HIGH. When asserted (HIGH), the transmit serial data from each channel is internally routed to the associated receiver Clock and Data Recovery (CDR) circuit. All serial drivers are forced to differential logic “1”. All serial data inputs are ignored. |
| OELE | LVTTL Input, asynchronous, internal pull-up | **Serial Driver Output Enable Latch Enable**. Active HIGH. When OELE = HIGH, the signals on the BOE[3:0] inputs directly control the OUTxy± differential drivers. When the BOE[x] input is HIGH, the associated OUTxy± differential driver is enabled. When the BOE[x] input is LOW, the associated OUTxy± differential driver is powered down. When OELE returns LOW, the last values present on BOE[3:0] are captured in the internal Output Enable Latch. The specific mapping of BOE[3:0] signals to transmit output enables is listed in Table 9 on page 18.<br>If the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable all outputs. |
| RXLE | LVTTL Input, asynchronous, internal pull-up | **Receive Channel Power-Control Latch Enable**. Active HIGH. When RXLE = HIGH, the signals on the BOE[3:0] inputs directly control the power enables for the receive PLLs and analog logic. When the BOE[3:0] input is HIGH, the associated receive channel A and receive channel B PLL and analog logic are active. When the BOE[3:0] input is LOW, the associated receive channel A and receive channel B PLL and analog logic are placed in a non-functional power saving mode. When RXLE returns LOW, the last values present on BOE[3:0] are captured in the internal RX PLL Enable Latch. The specific mapping of BOE[3:0] signals to the associated receive channel enables is listed in Table 9 on page 18. When the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable both receive channels. |
| BISTLE | LVTTL Input, asynchronous, internal pull-up | **Transmit and Receive BIST Latch Enable**. Active HIGH. When BISTLE = HIGH, the signals on the BOE[3:0] inputs directly control the transmit and receive BIST enables. When the BOE[x] input is LOW, the associated transmit or receive channel is configured to generate or compare the BIST sequence. When the BOE[x] input is HIGH, the associated transmit or receive channel is configured for normal data transmission or reception. When BISTLE returns LOW, the last values present on BOE[3:0] are captured in the internal BIST Enable Latch. The specific mapping of BOE[3:0] signals to transmit and receive BIST enables is listed in Table 9 on page 18. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable BIST on all transmit and receive channels. |
| BOE[3:0] | LVTTL Input, asynchronous, internal pull-up | **BIST, Serial Output, and Receive Channel Enables**. These inputs are passed to and through the Output Enable Latch when OELE = HIGH, and captured in this latch when OELE returns LOW. These inputs are passed to and through the BIST Enable Latch when BISTLE = HIGH, and captured in this latch when BISTLE returns LOW. These inputs are passed to and through the Receive Channel Enable Latch when RXLE = HIGH, and captured in this latch when RXLE returns LOW. |
| $\overline{\text{LFIA}}$<br>$\overline{\text{LFIB}}$ | LVTTL Output, Asynchronous | **Link Fault Indication Output**. Active LOW. $\overline{\text{LFIx}}$ is the logical OR of four internal conditions:<br>1. Received serial data frequency outside expected range.<br>2. Analog amplitude below expected levels.<br>3. Transition density lower than expected.<br>4. Receive Channel disabled. |

## Pin Descriptions (continued)

CYP15G0201DXB Dual HOTLink II Transceiver

| Pin Name | I/O Characteristics | Signal Description |
|---|---|---|
| **JTAG Interface** | | |
| TMS | LVTTL Input, internal pull-up | **Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained HIGH for >5 TCLK cycles, the JTAG test controller is reset. The TAP controller is also reset automatically upon application of power to the device. |
| TCLK | LVTTL Input, internal pull-down | **JTAG Test Clock**. |
| TDO | 3-State<br>LVTTL Output | **Test Data Out**. JTAG data output buffer which is High-Z while JTAG test mode is not selected. |
| TDI | LVTTL Input, internal pull-up | **Test Data In**. JTAG data input port. |
| **Power** | | |
| $V_{CC}$ | | +3.3 V power. |
| GND | | Signal and Power Ground for all internal circuits. |

## CYP15G0201DXB HOTLink II Operation

The CYP15G0201DXB is a highly configurable device designed to support reliable transfer of large quantities of data, using high-speed serial links, from one or multiple sources to one or multiple destinations. This device supports two single-byte or single-character channels that may be combined to support transfer of wider buses.

### CYP15G0201DXB Transmit Data Path

*Operating Modes*

The transmit path of the CYP15G0201DXB supports two character-wide data paths. These data paths are used in multiple operating modes as controlled by the TXMODE[1:0] inputs.

*Input Register*

The bits in the input register for each channel support different assignments, based on if the character is unencoded, encoded with two control bits, or encoded with three control bits. These assignments are shown in Table 1.

Each input register captures a minimum of eight data bits and two control bits on each input clock cycle. When the Encoder is bypassed, the TXCTx[1:0] control bits are part of the pre-encoded 10-bit character.

When the encoder is enabled (TXMODE[1] ≠ LOW), the TXCTx[1:0] bits are interpreted along with the associated TXDx[7:0] character to generate the specific 10-bit transmission character. When TXMODE[0] ≠ HIGH, an additional special character select (SCSEL) input is also captured and interpreted. This SCSEL input is used to modify the encoding of the associated characters. When the transmit input registers are clocked by a common clock (TXCLKA↑ or REFCLK↑), this SCSEL input can be changed on a clock-by-clock basis and affects both channels. When operated with a separate input clock on each transmit channel, this SCSEL input is sampled synchronous to TXCLKA↑. While the value on SCSEL still affects both channels, it is interpreted when the character containing it is read from the transmit phase-align buffer (where both paths are internally clocked synchronously).

**Table 1. Input Register Bit Assignments**[4]

| Signal Name | Unencoded | Encoded | |
|---|---|---|---|
| | | **2-bit Control** | **3-bit Control** |
| TXDx[0] (LSB) | DINx[0] | TXDx[0] | TXDx[0] |
| TXDx[1] | DINx[1] | TXDx[1] | TXDx[1] |
| TXDx[2] | DINx[2] | TXDx[2] | TXDx[2] |
| TXDx[3] | DINx[3] | TXDx[3] | TXDx[3] |
| TXDx[4] | DINx[4] | TXDx[4] | TXDx[4] |
| TXDx[5] | DINx[5] | TXDx[5] | TXDx[5] |
| TXDx[6] | DINx[6] | TXDx[6] | TXDx[6] |
| TXDx[7] | DINx[7] | TXDx[7] | TXDx[7] |
| TXCTx[0] | DINx[8] | TXCTx[0] | TXCTx[0] |
| TXCTx[1] (MSB) | DINx[9] | TXCTx[1] | TXCTx[1] |
| SCSEL | N/A | N/A | SCSEL |

*Phase-Align Buffer*

Data from the input registers is passed either to the encoder or to the associated phase-align buffer. When the transmit paths are operated synchronous to REFCLK↑ (TXCKSEL = LOW and TXRATE = LOW), the phase-align buffers are bypassed and data is passed directly to the parity check and Encoder blocks to reduce latency.

When an Input-Register clock with an uncontrolled phase relationship to REFCLK is selected (TXCKSEL ≠ LOW) or if data is captured on both edges of REFCLK (TXRATE = HIGH), the phase-align buffers are enabled. These buffers are used to absorb clock phase differences between the presently selected input clock and the internal character clock.

Initialization of these phase-align buffers takes place when the TXRST input is sampled by two consecutive rising edges of REFCLK. When TXRST is returned HIGH, the present input clock phase relative to REFCLK↑ is set. TXRST is an asynchronous input, but is sampled internally to synchronize it to the internal transmit path state machines.

After set, the input clocks are allowed to skew in time up to half a character period in either direction relative to REFCLK↑; that is, ±180°. This time shift allows the delay paths of the character clocks (relative to REFLCK↑) to change due to operating voltage and temperature, while not affecting the design operation.

If the phase offset, between the initialized location of the input clock and REFCLK↑, exceeds the skew handling capabilities of the phase-align buffer, an error is reported on the associated TXPERx output. This output indicates a continuous error until the phase-align buffer is reset. While the error remains active, the transmitter for the associated channel outputs a continuous C0.7 character to indicate to the remote receiver that an error condition is present in the link.

In specific transmit modes, it is also possible to reset the phase-align buffers individually and with minimal disruption of the serial data stream. When the transmit interface is configured for generation of atomic word sync sequences (TXMODE[1] = MID) and a phase-align buffer error is present, the transmission of a word sync sequence recenters the phase align buffer and clears the error condition.[5]

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**Notes**

4. The TXOPx inputs are also captured in the associated Input Register, but their interpretation is under the separate control of PARCTL.
5. One or more K28.5 characters may be added or lost from the data stream during this reset operation. When used with non-Cypress devices that require a complete 16-character word sync sequence for proper receive elasticity buffer alignment, it is recommend that the sequence be followed by a second word sync sequence to ensure proper operation.

*Parity Support*

In addition to the ten data and control bits that are captured at each transmit input register, a TXOPx input is also available on each channel. This allows the CYP15G0201DXB to support ODD parity checking for each channel. This parity checking is available for all operating modes (including encoder bypass). The specific mode of parity checking is controlled by the PARCTL input, and operates per Table 2.

**Table 2. Input Register Bits Checked for Parity**[6]

| Signal Name | Transmit Parity Check Mode (PARCTL) | | | |
|---|---|---|---|---|
| | LOW | MID | | HIGH |
| | | TXMODE[1] = LOW | TXMODE[1] ≠ LOW | |
| TXDx[0] | | X[7] | X | X |
| TXDx[1] | | X | X | X |
| TXDx[2] | | X | X | X |
| TXDx[3] | | X | X | X |
| TXDx[4] | | X | X | X |
| TXDx[5] | | X | X | X |
| TXDx[6] | | X | X | X |
| TXDx[7] | | X | X | X |
| TXCTx[0] | | X | | X |
| TXCTx[1] | | X | | X |
| TXOPx | | X | X | X |

When PARCTL is MID (open) and the encoders are enabled (TXMODE[1] ≠ L), only the TXDx[7:0] data bits are checked for ODD parity along with the associated TXOPx bit. When PARCTL = HIGH with the Encoder enabled (or MID with the encoder bypassed), the TXDx[7:0] and TXCTx[1:0] inputs are checked for ODD parity along with the associated TXOPx bit. When PARCTL = LOW, parity checking is disabled.

When parity checking and the encoder are both enabled (TXMODE[1] ≠ LOW), the detection of a parity error causes a C0.7 character of proper disparity to be passed to the transmit shifter. When the encoder is bypassed (TXMODE[1] = LOW), detection of a parity error causes a positive disparity version of a C0.7 transmission character to be passed to the transmit shifter.

*Encoder*

The character, received from the input register or phase-align buffer and parity check logic, is then passed to the encoder logic. this block interprets each character and any associated control bits, and outputs a 10-bit transmission character.

Depending on the configured operating mode, the generated transmission character may be,

- The 10-bit pre-encoded character accepted in the input register
- The 10-bit equivalent of the 8-bit data character accepted in the input register
- The 10-bit equivalent of the 8-bit special character code accepted in the Input Register
- The 10-bit equivalent of the C0.7 SVS character if parity checking was enabled and a parity error was detected
- The 10-bit equivalent of the C0.7 SVS character if a Phase-Align Buffer overflow or underflow error is present
- A character that is part of the 511-character BIST sequence
- A K28.5 character generated as an individual character or as part of the 16-character Word Sync Sequence.

The selection of the specific characters generated is controlled by the TXMODE[1:0], SCSEL, TXCTx[1:0], and TXDx[7:0] inputs for each character.

*Data Encoding*

Raw data, as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee

- A minimum transition density (to allow the serial receive PLL to extract a clock from the data stream)
- A DC-balance in the signaling (to prevent baseline wander)
- Run-length limits in the serial data (to limit the bandwidth requirements of the serial link)
- The remote receiver a way of determining the correct character boundaries (framing)

When the encoder is enabled (TXMODE[1] ≠ LOW), the characters to be transmitted are converted from data or special character codes to 10-bit transmission characters (as selected by their respective TXCTX[1:0] and SCSEL inputs), using an integrated 8B/10B encoder. When directed to encode that is, the character as a special character code, it is encoded using the special character encoding rules listed in Table 25 on page 47. When directed to encode the character as a data character, it is encoded using the data character encoding rules in Table 24 on page 43.

The 8B/10B Encoder is standards compliant with ANSI/NCITS ASC X3.230-1994 (Fibre Channel), IEEE 802.3z (Gigabit Ethernet), the IBM® ESCON® and FICON® channels, and Digital Video Broadcast DVB-ASI standards for data transport.

Many of the Special Character codes listed in Table 25 on page 47 may be generated by more than one input character. The CYP15G0201DXB is designed to support two independent (but non-overlapping) Special Character code tables. This allows the CYP15G0201DXB to operate in mixed environments with other CYP15G0201DXBs using the enhanced Cypress command code set, and the reduced command sets of other non-Cypress devices. Even when used in an environment that normally uses non-Cypress Special Character codes, the selective use of Cypress command codes can permit operation where running disparity and error handling must be managed.

Following conversion of each input character from eight bits to a 10-bit transmission character, it is passed to the Transmit Shifter and is shifted out LSB first, as required by ANSI and IEEE standards for 8B/10B coded serial data streams.

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**Notes**

6. Transmit path parity errors are reported on the associated TXPERx output.
7. Bits marked as X are XORed together. Result must be a logic-1 for parity to be valid.

## Transmit Modes

The operating mode of the transmit path is set through the TXMODE[1:0] inputs. These 3-level select inputs allow one of nine transmit modes to be selected. The transmit modes are listed in Table 3.

The encoded modes (TX Modes 3 through 8) support multiple encoding tables. These encoding tables vary by the specific combinations of SCSEL, TXCTx[1], and TXCTx[0] that are used to control the generation of data and control characters. These multiple encoding forms allow maximum flexibility in interfacing to legacy applications, while also supporting numerous extensions in capabilities.

**Table 3. Transmit Operating Modes**

| TX Mode | | Operating Mode | | |
|---|---|---|---|---|
| **Mode Number** | **TXMODE [1:0]** | **Word Sync Sequence Support** | **SCSEL Control** | **TXCTx Function** |
| 0 | LL | None | None | Encoder Bypass |
| 1 | LM | None | None | Reserved for test |
| 2 | LH | None | None | Reserved for test |
| 3 | ML | Atomic | Special character | Encoder Control |
| 4 | MM | Atomic | Word Sync | Encoder Control |
| 5 | MH | Atomic | None | Encoder Control |
| 6 | HL | Interruptible | Special character | Encoder Control |
| 7 | HM | Interruptible | Word sync | Encoder Control |
| 8 | HH | Interruptible | None | Encoder Control |

### *TX Mode 0—Encoder Bypass*

When the Encoder is bypassed, the character captured in the TXDx[7:0] and TXCTx[1:0] inputs is passed directly to the Transmit Shifter without modification. If parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected, the 10-bit character is replaced with the 1001111000 pattern (+C0.7 character).

With the Encoder bypassed, the TXCTx[1:0] inputs are considered part of the data character and do not perform a control function that would otherwise modify the interpretation of the TXDx[7:0] bits. The bit usage and mapping of these control bits when the Encoder is bypassed is shown in Table 4.

**Table 4. Encoder Bypass Mode (TXMODE[1:0] = LL)**

| Signal Name | Bus Weight | 10B Name |
|---|---|---|
| TXDx[0] (LSb)[8] | $2^0$ | a |
| TXDx[1] | $2^1$ | b |
| TXDx[2] | $2^2$ | c |
| TXDx[3] | $2^3$ | d |
| TXDx[4] | $2^4$ | e |
| TXDx[5] | $2^5$ | i |
| TXDx[6] | $2^6$ | f |
| TXDx[7] | $2^7$ | g |
| TXCTx[0] | $2^8$ | h |
| TXCTx[1] (MSb) | $2^9$ | j |

### *TX Modes 1 and 2—Factory Test Modes*

In Encoder Bypass the SCSEL input is ignored. All clocking modes interpret the data the same, with no internal linking between channels.

These modes enable specific factory test configurations. They are not considered normal operating modes of the device. Entry or configuration into these test modes do not damage the device.

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**Note**

[8] LSb is shifted out first.

### *TX Mode 3—Atomic Word Sync and SCSEL Control of Special Codes*

When configured in TX Mode 3, the SCSEL input is captured along with the associated TXCTx[1:0] data control inputs. These bits combine to control the interpretation of the TXDx[7:0] bits and the characters generated by them. These bits are interpreted as listed in Table 5.

**Table 5. TX Modes 3 and 6 Encoding**

| SCSEL | TXCTx[1] | TXCTx[0] | Characters Generated |
|---|---|---|---|
| X | X | 0 | Encoded data character |
| 0 | 0 | 1 | K28.5 fill character |
| 1 | 0 | 1 | Special character code |
| X | 1 | 1 | 16-character word sync sequence |

When TXCKSEL = MID, both transmit channels capture data into their Input Registers using independent TXCLKx clocks. The SCSEL input is sampled only by TXCLKA↑. When the character (accepted in the Channel-A Input Register) has passed through the Phase-Align Buffer and any selected parity validation, the level captured on SCSEL is passed to the Encoder of Channel-B during this same cycle.

To avoid the possible ambiguities that may arise due to the uncontrolled arrival of SCSEL relative to the characters in the alternate channel, SCSEL is often used as a static control input.

### *Word Sync Sequence*

When TXCTx[1:0] = 11, a 16-character sequence of K28.5 characters, known as a word sync sequence, is generated on the associated channel. This sequence of K28.5 characters may start with either a positive or negative disparity K28.5 (as determined by the current running disparity and the 8B/10B coding rules). The disparity of the second and third K28.5 characters in this sequence are reversed from what normal 8B/10B coding rules would generate. The remaining K28.5 characters in the sequence follow all 8B/10B coding rules. The disparity of the generated K28.5 characters in this sequence would follow a pattern of either + + − − + − + − + − + − + − + − or − − + + − + − + − + − + − + − +.

When TXMODE[1] = MID (open, TX modes 3, 4, and 5), the generation of this character sequence is an atomic (non-interruptible) operation. After it has been successfully started, it cannot be stopped until all 16 characters have been generated. The content of the associated Input Register(s) is ignored for the duration of this 16-character sequence.

At the end of this sequence, if the TXCTx[1:0] = 11 condition is sampled again, the sequence restarts and remains uninterruptible for the following 15 character clocks.

If parity checking is enabled, the character used to start the Word Sync Sequence must also have correct ODD parity. After the sequence is started, parity is not checked on the following 15 characters in the Word Sync Sequence.

When TXMODE[1] = HIGH (TX modes 6, 7, and 8), the generation of the word sync sequence becomes an interruptible operation. In TX Mode 6, this sequence is started as soon as the TXCTx[1:0] = 11 condition is detected on a channel. In order for the sequence to continue on that channel, the TXCTx[1:0] inputs must be sampled as 00 for the remaining 15 characters of the sequence.

If at any time a sample period exists where TXCTx[1:0] ≠ 00, the word sync sequence is terminated, and a character representing the associated data and control bits is generated by the Encoder. This resets the word sync sequence state machine such that it starts at the beginning of the sequence at the next occurrence of TXCTx[1:0] = 11.

When parity checking is enabled and TXMODE[1] = HIGH, all characters (including those in the middle of a word sync sequence) must have correct parity. The detection of a character with incorrect parity during a word sync sequence (regardless of the state of TXCTx[1:0]) interrupts that sequence and forces the generation of a C0.7 SVS character. Any interruption of the Word Sync Sequence causes the sequence to terminate.

When TXCKSEL = LOW, the Input Registers for both transmit channels are clocked by REFCLK[2]. When TXCKSEL = HIGH, the Input Registers for both transmit channels are clocked with TXCLKA↑. In these clock modes both sets of TXCTx[1:0] inputs operate synchronous to the SCSEL input.[9]

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**Note**

9. When operated in any condition where receive channels are bonded together, TXCKSEL must be either LOW or HIGH (not MID) to ensure that associated characters are transmitted in the same character cycle.

*TX Mode 4—Atomic Word Sync and SCSEL Control of Word Sync Sequence Generation*

When configured in TX Mode 4, the SCSEL input is captured along with the associated TXCTx[1:0] data control inputs. These bits combine to control the interpretation of the TXDx[7:0] bits and the characters generated by them. These bits are interpreted as listed in Table 6.

**Table 6. TX Modes 4 and 7 Encoding**

| SCSEL | TXCTx[1] | TXCTx[0] | Characters Generated |
|---|---|---|---|
| X | X | 0 | Encoded data character |
| 0 | 0 | 1 | K28.5 fill character |
| 0 | 1 | 1 | Special character code |
| 1 | X | 1 | 16-character Word Sync Sequence |

When TXCKSEL = MID, both transmit channels operate independently. The SCSEL input is sampled only by TXCLKA↑. When the character accepted in the Channel-A input register has passed any selected validation and is ready to be passed to the encoder, the level captured on SCSEL is passed to the Encoder of Channel-B during this same cycle.

Changing the state of SCSEL changes the relationship of the characters on the alternate channel. SCSEL should either be used as a static configuration input or changed only when the state of TXCTx[1:0] on the alternate channel are such that SCSEL is ignored during the change.

TX Mode 4 also supports an atomic word sync sequence. Unlike TX Mode 3, this sequence is started when both SCSEL and TXCTx[0] are sampled HIGH. With the exception of the combination of control bits used to initiate the sequence, the generation and operation of this word sync sequence is the same as that documented for TX Mode 3.

*TX Mode 5—Atomic Word Sync, No SCSEL*

When configured in TX Mode 5, the SCSEL signal is not used. In addition to the standard character encodings, both with and without atomic word sync sequence generation, two additional encoding mappings are controlled by the channel bonding selection made through the RXMODE[1:0] inputs.

For non-bonded operation, the TXCTx[1:0] inputs for each channel control the characters generated by that channel. The specific characters generated by these bits are listed in Table 7 on page 17.

**Table 7. TX Modes 5 and 8 Encoding, Non-Bonded (RXMODE[1] = LOW)**

| SCSEL | TXCTx[1] | TXCTx[0] | Characters Generated |
|---|---|---|---|
| X | 0 | 0 | Encoded data character |
| X | 0 | 1 | K28.5 fill character |
| X | 1 | 0 | Special character code |
| X | 1 | 1 | 16-character Word Sync Sequence |

TX Mode 5 also has the capability of generating an atomic Word Sync Sequence. For the sequence to be started, the TXCTx[1:0] inputs must both be sampled HIGH. With the exception of the combination of control bits used to initiate the sequence, the generation and operation of this Word Sync Sequence is the same as that documented for TX Mode 3.

Two additional encoding maps are provided for use when receive channel bonding is enabled. When dual-channel bonding is enabled (RXMODE[1] = HIGH), the CYP15G0201DXB is configured such that channels A and B are bonded together to form a two-character-wide path.

When operated in this two-channel bonded mode, the TXCTA[0] and TXCTB[0] inputs control the interpretation of the data on both the A and B channels. The characters on each half of these bonded channels are controlled by the associated TXCTx[1] bit. The specific characters generated by these control bit combinations are listed in Table 8.

**Table 8. TX Modes 5 and 8, Dual-channel Bonded (RXMODE[1] = HIGH)**

| SCSEL | TXCTA[1] | TXCTA[0] | TXCTB[1] | TXCTB[0] | Characters Generated |
|---|---|---|---|---|---|
| X | 0 | 0 | X | 0 | Encoded data character on channel A |
| X | 0 | 1 | X | 0 | K28.5 fill character on channel A |
| X | 1 | 0 | X | 0 | Special character code on channel A |
| X | 1 | 1 | X | 0 | 16-character word sync on channel A |
| X | X | 0 | 0 | 0 | Encoded data character on channel B |
| X | X | 1 | 0 | 0 | K28.5 fill character on channel B |
| X | X | 0 | 1 | 0 | Special character code on channel B |
| X | X | 1 | 1 | 0 | 16-character word sync on channel B |
| X | X | X | X | 1 | 16-character word sync on channels A and B |

Note especially that any time TXCTB[0] is sampled HIGH, both channels A and B start generating an Atomic Word Sync Sequence, regardless of the state of any of the other bits in the A or B Input Registers (with the exception of any enabled parity checking).

### Transmit BIST

Each transmit channel contains an internal pattern generator that can be used to validate both device and link operation. These generators are enabled by the associated BOE[x] signals listed in Table 9 on page 18 (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated transmit channel becomes a signature pattern generator by logically converting to a linear feedback shift register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached receiver(s). If the receive channels are configured for common clock operation (RXCKSEL ≠ MID) and Encoder is enabled (TXMODE[1] ≠ LOW) each pass is preceded by a 16-character Word Sync Sequence to allow Elasticity Buffer alignment and management of clock- frequency variations.

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator in the associated transmit channel (or the BIST checker in the associated receive channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH to open the latch. A device reset, (TRSTZ sampled LOW) presets the BIST Enable Latch to disable BIST on all channels. All data and data-control information present at the associated TXDx[7:0] and TXCTx[1:0] inputs are ignored when BIST is active on that channel.

### Serial Output Drivers

The serial interface output drivers use high-performance differential current mode logic (CML) to provide a source-matched driver for the transmission lines. These drivers accept data from the transmit shifters. these outputs have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

When configured for local loopback (LPEN = HIGH), all enabled Serial Drivers are configured to drive a static differential logic-1.

Each serial driver can be enabled or disabled separately through the BOE[3:0] inputs, as controlled by the OELE latch-enable signal. When OELE is HIGH, the signals present on the BOE[3:0] inputs are passed through the Serial Output Enable Latch to control the serial output drivers. The BOE[3:0] input associated with a specific OUTxy± driver is listed in Table 9.

**Table 9. Output Enable, BIST, and Receive Channel Enable Signal Map**

| BOE Input | Output Controlled (OELE) | BIST Channel Enable (BISTLE) | Receive PLL Channel Enable (RXLE) |
|---|---|---|---|
| BOE[3] | OUTB2± | Transmit B | X |
| BOE[2] | OUTB1± | Receive B | Receive B |
| BOE[1] | OUTA2± | Transmit A | X |
| BOE[0] | OUTA1± | Receive A | Receive A |

When OELE is HIGH and BOE[x] is HIGH, the associated serial driver is enabled. When OELE is HIGH and BOE[x] is LOW, the associated driver is disabled and internally powered down. If both outputs for a channel are in this disabled state, the associated internal logic for that channel is also powered down. When OELE returns LOW, the values present on the BOE[3:0] inputs are latched in the Output Enable Latch, and remain there until OELE returns HIGH to enable the latch. A device reset (TRSTZ sampled LOW) clears this latch and disables all output drivers.

**Note**. When all transmit channels are disabled (that is, both outputs disabled in all channels) and a channel is re-enabled, the data on the Serial Drivers may not meet all timing specifications for up to 200 µs.

### Transmit PLL Clock Multiplier

The transmit PLL clock multiplier accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiplies that clock by 10 or 20 (as selected by TXRATE) to generate a bit-rate clock for use by the Transmit Shifter. It also provides a character-rate clock used by the transmit paths.

The clock multiplier PLL can accept a REFCLK input between 10 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYP15G0201DXB clock multiplier (controlled by TXRATE) and by the level on the SPDSEL input.

SPDSEL is a 3-level select[10] (ternary) input that selects one of three operating ranges for the serial data outputs and inputs. The operating serial signaling-rate and allowable range of REFCLK frequencies are listed in Table 10.

**Table 10. Operating Speed Settings**

| SPDSEL | TXRATE | REFCLK Frequency (MHz) | Signaling Rate (MBd) |
|---|---|---|---|
| LOW | 1 | Reserved | 195–400 |
| | 0 | 19.5–40 | |
| MID (Open) | 1 | 20–40 | 400–800 |
| | 0 | 40–80 | |
| HIGH | 1 | 40–75 | 800–1500 |
| | 0 | 80–150 | |

When TXRATE = HIGH (Half-rate REFCLK), TXCKSEL = HIGH or MID (TXCLKx or TXCLKA selected to clock input register) is an invalid mode of operation.

The REFCLK± input is a differential input with each input internally biased to 1.4 V. If the REFCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point.

When both the REFCLK+ and REFCLK– inputs are connected, the clock source must be a differential clock. This can be either a differential LVPECL clock that is DC-or AC-coupled, or a differential LVTTL or LVCMOS clock.

By connecting the REFCLK– input to an external voltage source or resistive voltage divider, it is possible to adjust the reference point of the REFCLK+ input for alternate logic levels. When doing so it is necessary to ensure that the 0 V differential crossing point remains within the parametric range supported by the input.

## CYP15G0201DXB Receive Data Path

### Serial Line Receivers

Two differential line receivers, INx1± and INx2±, are available on each channel for accepting serial data streams. The active serial line receiver on a channel is selected using the associated INSELx input. The serial line receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least $VI_{DIFF} \geq 100$ mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3 V powered fiber-optic interface modules (any ECL/PECL logic family, not limited to 100 K PECL) or AC-coupled to +5 V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

The local loopback input (LPEN) allows the serial transmit data outputs to be routed internally back to the clock and data recovery circuit associated with each channel. When configured for local loopback, all transmit serial driver outputs are forced to output a differential logic-1. This prevents local diagnostic patterns from being broadcast to attached remote receivers.

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**Note**

10. 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to $V_{SS}$ (ground). The HIGH level is usually implemented by direct connection to $V_{CC}$ (power). When not connected or allowed to float, a 3-level select input self-biases to the MID level.

## Signal Detect/Link Fault

Each selected line receiver (that is, that routed to the clock and data recovery PLL) is simultaneously monitored for

- Analog amplitude above limit specified by SDASEL
- Transition density greater than specified limit
- Range controller reports the received data stream within normal frequency range (±1500 ppm)[11]
- Receive channel enabled

All of these conditions must be valid for the signal detect block to indicate a valid signal is present. This status is presented on the link fault indicator (LFIx) output associated with each receive channel, which changes synchronous to the selected receive interface clock.

**Table 11. Analog Amplitude Detect Valid Signal Levels**[12]

| SDASEL | Typical signal with peak amplitudes above |
|---|---|
| LOW | 140 mV p-p differential |
| MID (Open) | 280 mV p-p differential |
| HIGH | 420 mV p-p differential |

### *Analog Amplitude*

While the majority of these signal monitors are based on fixed constants, the analog amplitude level detection is adjustable to allow operation with highly attenuated signals, or in high-noise environments. This adjustment is made through the SDASEL signal, a 3-level select[13] input, which sets the trip point for the detection of a valid signal at one of three levels, as listed in Table 11. This control input effects the analog monitors for all receive channels.

The analog signal detect monitors are active for the line receiver, selected by the associated INSELx input. When configured for local loopback (LPEN = HIGH), no line receivers are selected, and the LFIx output for each channel reports only the receive VCO frequency out-of-range and transition density status of the associated transmit signal. When local loopback is active, the analog signal detect monitors are disabled.

### *Transition Density*

The transition detection logic checks for the absence of any transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received on a channel (within the referenced period), the transition detection logic for that channel asserts LFIx. The LFIx output remains asserted until at least one transition is detected in each of three adjacent received characters.

### *Range Controls*

The clock/data recovery (CDR) circuit includes logic to monitor the frequency of the phase-locked loop (PLL) voltage controlled oscillator (VCO) used to sample the incoming data stream. This logic ensures that the VCO operates at, or near the rate of the incoming data stream for two primary cases:

- when the incoming data stream resumes after a time in which it has been “missing”
- when the incoming data stream is outside the acceptable frequency range

To perform this function, the frequency of the VCO is periodically sampled and compared to the frequency of the REFCLK input. If the VCO is running at a frequency beyond ±1500 ppm[11] as defined by the reference clock frequency, it is periodically forced to the correct frequency (as defined by REFCLK, SPDSEL, and TXRATE) and then released in an attempt to lock to the input data stream. The sampling and relock period of the Range Control is calculated as follows: RANGE CONTROL SAMPLING PERIOD = (REFCLKPERIOD) × (16000).

During the time that the range control forces the PLL VCO to run at REFCLK×10 (or REFCLK×20 when TXRATE = HIGH) rate, the LFIx output is asserted LOW. While the PLL is attempting to re-lock to the incoming data stream, LFIx may be either HIGH or LOW (depending on other factors such as transition density and amplitude detection) and the recovered byte clock (RXCLKx) may run at an incorrect rate (depending on the quality or existence of the input serial data stream). After a valid serial data stream is applied, it may take up to one RANGE CONTROL SAMPLING PERIOD before the PLL locks to the input data stream, after which LFIx should be HIGH.

### *Receive Channel Enabled*

The CYP15G0201DXB contains two receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the BOE[3:0] inputs, as controlled by the RXLE latch-enable signal. When RXLE is HIGH, the signals present on the BOE[3:0] inputs are passed through the receive channel enable latch to control the PLLs and logic of the associated receive channel. The BOE[3:0] input associated with a specific receive channel is listed in Table 9.

When RXLE = HIGH and BOE[x] = HIGH, the associated receive channel is enabled to receive and decode a serial stream. When RXLE = HIGH and BOE[x] = LOW, the associated receive channel is disabled and internally configured for minimum power dissipation. If a single channel of a bonded-pair is disabled, the other receive channels may not bind correctly. If the disabled channel is selected as the master channel for insert/delete functions, or recovered clock select, these functions do not work correctly. Any disabled channel indicates an asserted LFIx output. When RXLE returns LOW, the values present on the BOE[3:0] inputs are latched in the receive channel enable latch, and remain there until RXLE returns HIGH to opened the latch again.[14]

**Notes**

11. REFCLK has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±1500 ppm (±0.15%) of the remote transmitter’s PLL reference (REFCLK) frequency. Although transmitting to a HOTLink II receiver necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500 ppm, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard. For example, to be IEEE 802.3z Gigabit Ethernet compliant, the frequency stability of the crystal needs to be within ±100 PPM.
12. The peak amplitudes listed in this table are for typical waveforms that have generally 3–4 transitions for every ten bits. In a worse case environment the signals may have a sign-wave appearance (highest transition density with repeating 0101...). Signal peak amplitudes levels within this environment type could increase the values in the table by approximately 100 mV.
13. 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to $V_{SS}$ (ground). The HIGH level is usually implemented by direct connection to $V_{CC}$ (power). When not connected or allowed to float, a 3-Level select input self-biases to the MID level.
14. When a disabled receive channel is re-enabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 10 ms.

## Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate CDR block within each receive channel. The clock extraction function is performed by high-performance embedded PLLs that track the frequency of the transitions in the incoming bit streams and align the phase of their internal bit-rate clocks to the transitions in the selected serial data streams.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit rate ÷ 20) reference clock from the REFCLK input. This REFCLK input is used to

- Ensure that the VCO (within each CDR) is operating at the correct frequency (rather than some harmonic of the bit rate)
- Improve PLL acquisition time
- And to limit unlocked frequency excursions of the CDR VCO when no data is present at the selected Serial Line Receiver. Regardless of the type of signal present, the CDR attempts to recover a data stream from it. If the frequency of the recovered data stream is outside the limits set by the range control monitors, the CDR switches to track REFCLK instead of the data stream. After the CDR output (RXCLKx) frequency returns back close to REFCLK frequency, the CDR input is switched back to the input data stream to check its frequency. In case no data is present at the input this switching behavior may result in brief RXCLKx frequency excursions from REFCLK. However, the validity of the input data stream is indicated by the LFIx output. The frequency of REFCLK is required to be within ±1500 ppm[11] of the frequency of the clock that drives the REFCLK input of the *remote* transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the $\overline{\text{LFIx}}$ output can be used to select an alternate data stream. When an LFIx indication is detected, external logic can toggle selection of the associated INx1± and INx2± inputs through the associated INSELx input. When a port switch takes place, it is necessary for the receive PLL for that channel to reacquire the new serial stream and frame to the incoming character boundaries. If channel bonding is also enabled, a channel alignment event is also required before the output data may be considered usable.

## Deserializer/Framer

Each CDR circuit extracts bits from the associated serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream looking for one or more Comma or K28.5 characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

### *Framing Character*

The CYP15G0201DXB allows selection of two combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input.

The specific bit combinations of these framing characters are listed in Table 12. When the specific bit combination of the selected framing character is detected by the framer, the boundaries of the characters present in the received data stream are known.

**Table 12. Framing Character Selector**

| FRAMCHAR | Bits Detected in Framer | |
|---|---|---|
| | **Character Name** | **Bits Detected** |
| LOW | Reserved for test | |
| MID (Open) | Comma+<br>Comma– | 00111110XX [15]<br>or 11000001XX |
| HIGH | –K28.5<br>+K28.5 | 0011111010 or<br>1100000101 |

### *Framer*

The framer on each channel operates in one of three different modes, as selected by the RFMODE input. In addition, the framer itself may be enabled or disabled through the RFEN input. When RFEN = LOW, the framers in both receive paths are disabled, and no combination of bits in a received data stream alters the character boundaries. When RFEN = HIGH, the framer selected by RFMODE is enabled on both channels.

When RFMODE = LOW, the low-latency framer is selected. This framer operates by stretching the recovered character clock until it aligns with the received character boundaries. In this mode the framer starts its alignment process on the first detection of the selected framing character. To reduce the impact on external circuits that make use of a recovered clock, the clock period is not stretched by more than two bit-periods in any one clock cycle. When operated in with a character-rate output clock (RXRATE = LOW), the output of properly framed characters may be delayed by up to nine character-clock cycles from the detection of the selected framing character. When operated with a half-character-rate output clock (RXRATE = HIGH), the output of properly framed characters may be delayed by up to 14 character-clock cycles from the detection of the selected framing character.[16]

When RFMODE is MID (open) the Cypress-mode multi-byte framer is selected. The required detection of multiple framing characters makes the associated link much more robust to incorrect framing due to aliased SYNC characters in the data stream. In this mode, the framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock does not contain any significant phase changes or hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other external circuits or components using PLL-based clock distribution elements. In this framing mode the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

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**Notes**

[15] The standard definition of a Comma contains only seven bits. However, since all valid Comma characters within the 8B/10B character set also have the 8th bit as an inversion of the 7th bit, the compare pattern is extended to a full eight bits to reduce the possibility of a framing error.

[16] When Receive BIST is enabled on a channel, the Low-latency Framer must not be enabled. The BIST sequence contains an aliased K28.5 framing character, which causes the Receiver to update its character boundaries incorrectly.

When RFMODE = HIGH, the alternate-mode multi-byte framer is enabled. Like the Cypress-mode multi-byte framer, multiple framing characters must be detected before the character boundary is adjusted. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, on identical 10-bit boundaries, before character framing is adjusted. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock.

Framing for all channels is enabled when RFEN = HIGH. If RFEN = LOW, the framer for each channel is disabled. When the framers are disabled, no changes are made to the recovered character boundaries on any channel, regardless of the presence of framing characters in the data stream.

## 8B/10B Decoder Block

The decoder logic block performs three primary functions:

- Decoding the received transmission characters back into data and special character codes,
- Comparing generated BIST patterns with received characters to permit at-speed link and device testing,
- Generation of ODD parity on the decoded characters.

### *8B/10B Decoder*

The framed parallel output of each deserializer shifter is passed to the 8B/10B decoder where, if the decoder is enabled (DECMODE ≠ LOW), it is transformed from a 10-bit transmission character back to the original data and special character codes. This block uses the 8B/10B Decoder patterns in Table 24 on page 43 and Table 25 on page 47 of this datasheet. Valid data characters are indicated by a 000b bit-combination on the associated RXSTx[2:0] status bits, and special character codes are indicated by a 001b bit-combination on these same status outputs. Framing characters, invalid patterns, disparity errors, and synchronization status are presented as alternate combinations of these status bits.

The 8B/10B decoder operates in two normal modes, and can also be bypassed. The operating mode for the Decoder is controlled by the DECMODE input.

When DECMODE = LOW, the decoder is bypassed and raw 10-bit characters are passed to the output register. In this mode, channel bonding is not possible, the receive Elasticity Buffers are bypassed, and RXCKSEL must be MID. This clock mode generates separate RXCLKx± outputs for each receive channel.

When DECMODE = MID (or open), the 10-bit transmission characters are decoded using Table 24 on page 43 and Table 25 on page 47. Received Special Code characters are decoded using the Cypress column of Table 25 on page 47.

When DECMODE = HIGH, the 10-bit transmission characters are decoded usingTable 24 on page 43 and Table 25 on page 47. received special code characters are decoded using the Alternate column of Table 25 on page 47.

In all settings where the decoder is enabled, the receive paths may be operated as separate channels or bonded to form dual-channel buses.

## Receive BIST Operation

The receiver interfaces contain internal pattern generators that can be used to validate both device and link operation. These generators are enabled by the associated BOE[x] signals listed in Table 9 on page 18 (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated receive channel becomes a signature pattern generator and checker by logically converting to a linear feedback shift register (LFSR). This LFSR generates a 511-character sequence that includes all data and special character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached transmitter(s). If the receive channels are configured for common clock operation (RXCKSEL ≠ MID) each pass is preceded by a 16-character word sync sequence. When synchronized with the received data stream, the associated Receiver checks each character in the decoder with each character generate by the LFSR and indicates compare errors and BIST status at the RXSTx[2:0] bits of the output register. Refer Table 20 on page 30 for details.

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator/checker in the associated receive channel (or the BIST generator in the associated transmit channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST enable latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH. All captured signals in the BIST Enable Latch are set HIGH (that is, BIST is disabled) following a device reset ($\overline{\text{TRSTZ}}$ is sampled LOW).

When BIST is first recognized as being enabled in the Receiver, the LFSR is preset to the BIST-loop start-code of D0.0 This code D0.0 is sent only once per BIST loop. The status of the BIST progress and any character mismatches is presented on the RXSTx[2:0] status outputs.

Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXSTx[2:0] indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress. These same status values are presented when the decoder is bypassed and BIST is enabled on a receive channel.

The specific status reported by the BIST state machine are listed in Table 18 on page 27. These same codes are reported on the receive status outputs regardless of the state of DECMODE.

The specific patterns checked by each receiver are described in detail in the Cypress application note entitled “HOTLink built-in self-test.” The sequence compared by the CYP15G0201DXB when RXCKSEL = MID is identical to that in the CY7B933 and CY7C924DX, allowing interoperable systems to be built when used at compatible serial signaling rates.

If the number of invalid characters received ever exceeds the number of valid characters by 16, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

When the receive paths are configured for common clock operation (RXCKSEL ≠ MID) each pass must be preceded by a 16-character Word Sync Sequence to allow output buffer alignment and management of clock frequency variations.

This is automatically generated by the transmitter when its local RXCKSEL ≠ MID and encoder is enabled.

The BIST state machine requires the characters to be correctly framed for it to detect the BIST sequence. If the Low Latency framer is enabled (RFMODE = LOW), the framer misaligns to an aliased SYNC character within the BIST sequence. If the alternate multi-byte framer is enabled (RFMODE = HIGH) and the Receiver outputs are clocked relative to a recovered clock, it is generally necessary to frame the receiver before BIST is enabled. If the receive outputs are clocked relative to REFCLK (RXCKSEL = LOW), the transmitter precedes every 511 character BIST sequence with a 16-character Word Sync Sequence.

### Receive Elasticity Buffer

Each receive channel contains an elasticity buffer that is designed to support multiple clocking modes. These buffers allow data to be read using an elasticity buffer read-clock that is asynchronous in both frequency and phase from the elasticity buffer write clock, or to use a read clock that is frequency coherent but with uncontrolled phase relative to the elasticity buffer write clock.

Each elasticity buffer is a minimum of 10 characters deep, and supports a 12-bit-wide data path. It is capable of supporting a decoded character, three status bits, and a parity bit for each character present in the buffer. The write clock for these buffers is always the recovered clock for the associated read channel.

The read clock for the elasticity buffers may come from one of three selectable sources. It may be a,

- Character-rate REFCLK
- Recovered clock from the same receive channel
- Recovered clock from an alternate receive channel

These elasticity buffers are also used to align the output data streams when both channels are bonded together. More details on how the elasticity buffer is used for independent channel modes and channel bonded modes is discussed in the next section. The elasticity buffers are bypassed whenever the decoders are bypassed (DECMODE = LOW). When the decoders and elasticity buffers are bypassed, RXCKSELx must be set to MID.

### Receive Modes

The operating mode of the receive path is set through the RXMODE[1:0] inputs. The ‘Reserved for test’ settings (RXMODE0=M) is not allowed, even if the receiver is not being used. A[1:0] settings are ignored as long as they are not test modes. It stops normal function of the device. When the decoder is disabled, the RX MODE. These modes determine the type (if any) of channel bonding and status reporting. The different receive modes are listed in Table 13. When RXMODE[1] = MID or RXMODE[0] = MID the resulting modes are reserved for test.

**Table 13. Receive Operating Modes**

| RX Mode | | Operating Mode | |
|---|---|---|---|
| **Mode Number** | **RXMODE [1:0]** | **Channel Bonding** | **RXSTx Status Reporting** |
| 0 | LL | Independent | Status A |
| 1 | LH | Independent | Status B |
| 2 | HL | Dual | Status A |
| 3 | HH | Dual | Status B |

*Independent Channel Modes*

In independent channel modes (RX Modes 0 and 1, where RXMODE[1] = LOW), both receive paths may be clocked in any clock mode selected by RXCKSEL.

When RXCKSEL = LOW, both channels are clocked by REFCLK. RXCLKB± output is disabled (High-Z), and the RXCLKA± and RXCLKC+ outputs presents buffered and delayed forms of REFCLK. In this mode, the receive elasticity buffers are enabled. For REFCLK clocking, the elasticity buffers must be able to insert K28.5 characters and delete framing characters as appropriate.

The insertion of a K28.5 or deletion of a framing character can occur at any time on any channel, however, the actual timing on these insertions and deletions is controlled in part by the how the transmitter sends its data. Insertion of a K28.5 character can only occur when the receiver has a framing character in the elasticity buffer. Likewise, to delete a framing character, one must also be in the elasticity buffer. To prevent a receive buffer overflow or underflow on a receive channel, a minimum density of framing characters must be present in the received data streams.

When RXCKSEL = MID (or open), each received channel output register is clocked by the recovered clock for that channel. Since no characters may be added or deleted, the receiver elasticity buffer is bypassed.

When RXCKSEL = HIGH, all channels are clocked by the selected recovered clock. This selected clock is always output on RXCLKA±. In this mode the receive elasticity buffers are enabled. When data is output using a recovered clock (RXCKSEL = HIGH), receive channels are not allowed to insert and delete characters, except as necessary for elasticity buffer alignment.

When the elasticity buffer is used, prior to delivery of valid data, a word sync sequence (or at least four framing characters) must be received to center the elasticity buffers. The elasticity buffer may also be centered by a device reset operation initiated through the TRSTZ input, however, following such an event the CYP15G0201DXB normally requires a framing event before it correctly decodes the characters. When RXCKSEL = HIGH, since the Elasticity buffer is not allowed to insert or delete framing characters, the transmit clocks on all received channels must all be from a common source.

*Dual-channel Bonded Modes*

In dual-channel bonded modes (RX Modes 2 and 3, where RXMODE[1] = HIGH), the associated receive channel pair Output Registers must be clocked by a common clock. This mode does not operate when RXCKSEL = MID.

Proper operation in this mode requires that the associated transmit data streams are clocked from a common reference with no long-term character slippage between the bonded channels. In dual-channel mode this means that channels A and B must be clocked from a common reference.

Prior to the reception of valid data, a word sync sequence (or that portion of one necessary to align the receive buffers) must be received on the bonded channels (within the allowable inter-channel skew window) to allow the receive elasticity buffers to be centered. While normal characters may be output prior to this alignment event, they are not necessarily aligned within the same word boundaries as when they were transmitted.

When RXCKSEL = LOW, both receive channels are clocked by REFCLK. RXCLKB± outputs are disabled (High-Z), and the RXCLKA± and RXCLKC+ outputs present buffered and delayed forms of REFCLK. In this mode, the receive Elasticity Buffers are enabled. For REFCLK clocking, the elasticity buffers must be able to insert K28.5 characters and delete framing characters as appropriate. While these insertions and deletions can take place at any time, they must occur at the same time on both channels that are bonded together. This is necessary to keep the data in the bonded channel-pair properly aligned. This insert and delete process is controlled by the master channel selected by the RXCLKB+ input as listed in Table 14.

When RXCKSEL = HIGH, the A and B channels are clocked by the selected recovered clock, as shown in Table 14. The output clock for the channel A/B bonded-pair is output continuously on RXCLKA±. The clock source for this output is selected from the recovered clock for channel A or channel B using the RXCLKB+ input.

**Table 14. Dual-Channel Bonded Recovered Clock Select and Master Channel Select**

| RXCLKB+ | Clock Source |
|---|---|
| | RXCLKA± |
| 0 | RXCLKA |
| 1 | RXCLKB |

When data is output using a recovered clock (RXCKSEL = HIGH), receive channels are not allowed to insert and delete characters, except as necessary for elasticity buffer alignment.

## Power Control

The CYP15G0201DXB supports user control of the powered-up or down state of each transmit and receive channel. The receive channels are controlled by the RXLE signal and values present on the BOE [3:0] bus. The transmit channels are controlled by the OELE signal and the values present on the BOE[3:0] bus. Powering down unused channels saves power and reduces system heat generation. Controlling system power dissipation improves the system performance.

*Receive Channels*

When RXLE = HIGH, the signals on the BOE[3:0] inputs directly control the power enables for the receive PLLs and analog circuits. When a BOE[3:0] input is HIGH, the associated receive channel [A and B] PLL and analog logic are active. When a BOE[3:0] input is LOW, the associated receive channel [A and B] PLL and analog logic are powered down. When RXLE returns LOW, the last values present on the BOE[3:0] inputs are captured. The specific BOE[3:0] input signal associated with a receive channel is listed in Table 9 on page 18.

Any disabled receive channel indicates a constant $\overline{\text{LFIx}}$ output.

When a disable receive channel is re-enabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 10 ms.

*Transmit Channels*

When OELE is HIGH, the signals on the BOE[3:0] inputs directly control the power enables for the serial drivers. When BOE[3:0] input is HIGH, the associated serial driver is enabled. When BOE[3:0] input is LOW, the associated Serial Driver is disabled and powered down. If both serial drivers of a channel are disabled, the internal logic for that channel is powered down. When OELE returns LOW, the value present on the BOE[3:0] inputs are latched in the output enable latch.

*Device Reset State*

When the CYP15G0201DXB is reset by the assertion of $\overline{\text{TRSTZ}}$, the transmit enable and receive enable latches are both cleared, and the BIST enable latch is preset. In this state, all transmit and receive channels are disabled, and BIST is disabled on all channels.

Following a device reset, it is necessary to enable the transmit and receive channels used for normal operation. This can be done by sequencing the appropriate values on the BOE[3:0] inputs while the OELE and RXLE signals are raised and lowered. For systems that do not require dynamic control of power, or want the device to power-up in a fixed configuration, it is also possible to strap the RXLE and OELE control signals HIGH to permanently enable their associated latches. Connection of the associated BOE[3:0] signals HIGH, enables the respective transmit and receive channels as soon as the TRSTZ signal is deasserted.

## Output Bus

Each receive channel presents a 12-signal output bus consisting of,

- an 8-bit data bus
- a 3-bit status bus
- a parity bit.

The signals present on this output bus are modified by the present operating mode of the CYP15G0201DXB as selected by DECMODE. The bits are assigned per Table 15.

**Table 15. Output Register Bit Assignments**[17]

| Signal Name | DECMODE = LOW | DECMODE = MID or HIGH |
|---|---|---|
| RXSTx[2] (LSb) | COMDETx | RXSTx[2] |
| RXSTx[1] | DOUTx[0] | RXSTx[1] |
| RXSTx[0] | DOUTx[1] | RXSTx[0] |
| RXDx[0] | DOUTx[2] | RXDx[0] |
| RXDx[1] | DOUTx[3] | RXDx[1] |
| RXDx[2] | DOUTx[4] | RXDx[2] |
| RXDx[3] | DOUTx[5] | RXDx[3] |
| RXDx[4] | DOUTx[6] | RXDx[4] |
| RXDx[5] | DOUTx[7] | RXDx[5] |
| RXDx[6] | DOUTx[8] | RXDx[6] |
| RXDx[7] (MSb) | DOUTx[9] | RXDx[7] |

When the 8B/10B decoder is bypassed (DECMODE = LOW), the framed 10-bit and a single status bit are presented at the receiver output register. The status output indicates if the character in the output register is one of the selected framing characters. The bit usage and mapping of the external signals to the raw 10B transmission character is shown in Table 16.

**Table 16. Decoder Bypass Mode (DECMODE = LOW)**

| Signal Name | Bus Weight | 10B Name |
|---|---|---|
| RXSTx[2] (LSb) | COMDETx | |
| RXSTx[1] | $2^0$ | a |
| RXSTx[0] | $2^1$ | b |
| RXDx[0] | $2^2$ | c |
| RXDx[1] | $2^3$ | d |
| RXDx[2] | $2^4$ | e |
| RXDx[3] | $2^5$ | i |
| RXDx[4] | $2^6$ | f |
| RXDx[5] | $2^7$ | g |
| RXDx[6] | $2^8$ | h |
| RXDx[7] (MSb) | $2^9$ | j |

The COMDETx status outputs operate the same regardless of the bit combination selected for character framing by the FRAMCHAR input. They are HIGH when the character in the Output Register contains the selected framing character at the proper character boundary, and LOW for all other bit combinations.

When the low-latency framer and half-rate receive port clocking are also enabled (RFMODE = LOW, RXRATE = HIGH, and RXCKSEL ≠ LOW), the framer stretches the recovered clock to the nearest 20-bit boundary such that the rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

When the Cypress or Alternate Mode Framer is enabled and half-rate receive port clocking is also enabled (RFMODE ≠ LOW and RXRATE = HIGH), the output clock is not modified when framing is detected, but a single pipeline stage may be added or subtracted from the data stream by the framer logic such that the rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

This adjustment only occurs when the framer is enabled (RFEN = HIGH). When the framer is disabled, the clock boundaries are not adjusted, and COMDETx may be asserted during the rising edge of RXCLKx– (if an odd number of characters were received following the initial framing).

## Parity Generation

In addition to the eleven data and status bits that are presented by each channel, an RXOPx parity output is also available on each channel. This allows the CYP15G0201DXB to support ODD parity generation for each channel. To handle a wide range of system environments, the CYP15G0201DXB supports multiple different forms of parity generation including no parity. When the decoders are enabled (DECMODE ≠ LOW), parity can be generated on

- the RXDx[7:0] character
- the RXDx[7:0] character and RXSTx[2:0] status.

When the decoders are bypassed (DECMODE = LOW), parity can be generated on

- the RXDx[7:0] and RXSTx[1:0] bits
- the RXDx[7:0] and RXSTx[2:0] bits.

These modes differ in the number bits which are included in the parity calculation. For all cases, only ODD parity is provided which ensures that at least one bit of the data bus is always a logic-1. Those bits covered by parity generation are listed in Table 17 on page 26.

Parity generation is enabled through the 3-level select PARCTL input. When PARCTL = LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z).

When PARCTL = MID (open) and the decoders are enabled (DECMODE ≠ LOW), ODD parity is generated for the received and decoded character in the RXDx[7:0] signals and is presented on the associated RXOPx output.

When PARCTL = MID (open) and the decoders are bypassed (DECMODE = LOW), ODD parity is generated for the received and decoded character in the RXDx[7:0] and RXSTx[1:0] bit positions.

When PARCTL = HIGH, ODD parity is generated for the RXDx[7:0] and the associated RXSTx[2:0] status bits.

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**Note**

[17] The RXOPx outputs are also driven from the associated Output Register, but their interpretation is under the separate control of PARCTL.