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PRELIMINARY

CYP15G0401TB

Quad HOTLink II™ Transmitter

Features

- **Quad transmitter for 195 to 1500 MBaud serial signaling rate**
  - **— Aggregate throughput of 6 GBits/second**
- **Second-generation HOTLink® technology**
- **Compliant to multiple standards**
  - **— ESCON, DVB-ASI, Fibre Channel and Gigabit Ethernet (IEEE802.3z)**
  - **— 8B/10B encoded or 10-bit unencoded data**
- **Selectable parity check**
- **Selectable input clocking options**
- **Synchronous LVTTL parallel interface**
- **Optional Phase Align Buffer in Transmit Path**
- **Internal phase-locked loop (PLL) with no external PLL components**
- **Dual differential PECL-compatible serial outputs per channel**
  - **— Source matched for 50Ω transmission lines**
  - **— No external bias resistors required**
  - **— Signaling-rate controlled edge-rates**
- **Compatible with**
  - **— fiber-optic modules**
  - **— copper cables**
  - **— circuit board traces**
- **JTAG boundary scan**
- **Built-In Self-Test (BIST) for at-speed link testing**
- **Low power 1.9W @ 3.3V typical**
- **Single 3.3V supply**
- **256-ball thermally enhanced BGA**
- **Pb free package option available**
- **0.25µ BiCMOS technology**

Functional Description

The CYP15G0401TB Quad HOTLink II™ Transmitter is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 195-to-1500 MBaud per serial link.

Each transmitter accepts parallel characters in an Input Register, encodes each character for transport, and converts it to serial data. *Figure 1* illustrates typical connections between independent host systems and corresponding CYP15G0401TB and CYP15G0401RB parts.

As a second-generation HOTLink device, the CYP15G0401TB extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data, command, and BIST) with other HOTLink devices. The transmitters (TX) of the CYP15G0401TB Quad HOTLink II consist of four byte-wide channels. Each channel can accept either eight-bit data characters or pre-encoded 10-bit transmission characters. Data characters are passed from the Transmit Input Register to an embedded 8B/10B Encoder to improve their serial transmission characteristics. These encoded characters are then serialized and output from dual Positive ECL (PECL)-compatible differential trans-mission-line drivers at a bit-rate of either 10- or 20-times the input reference clock. The integrated 8B/10B Encoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface.

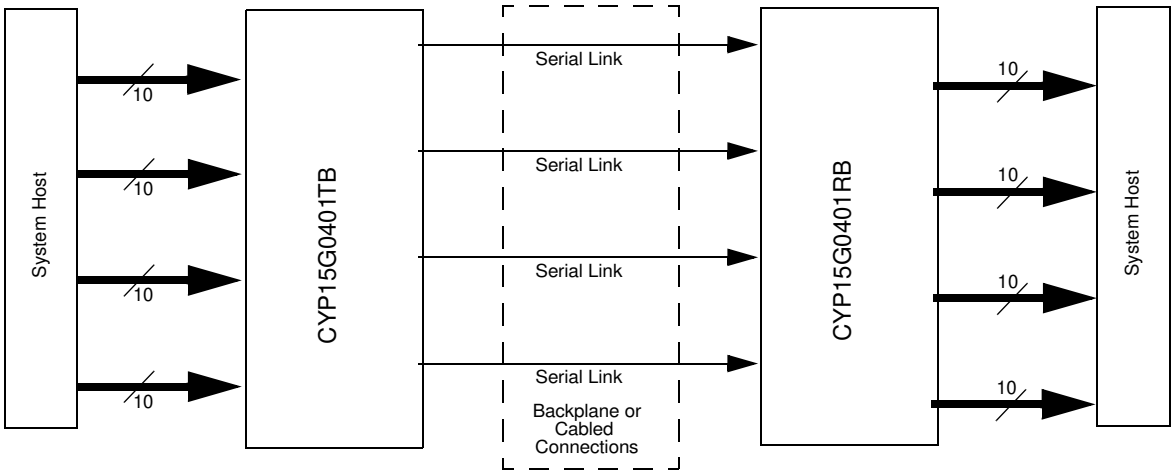


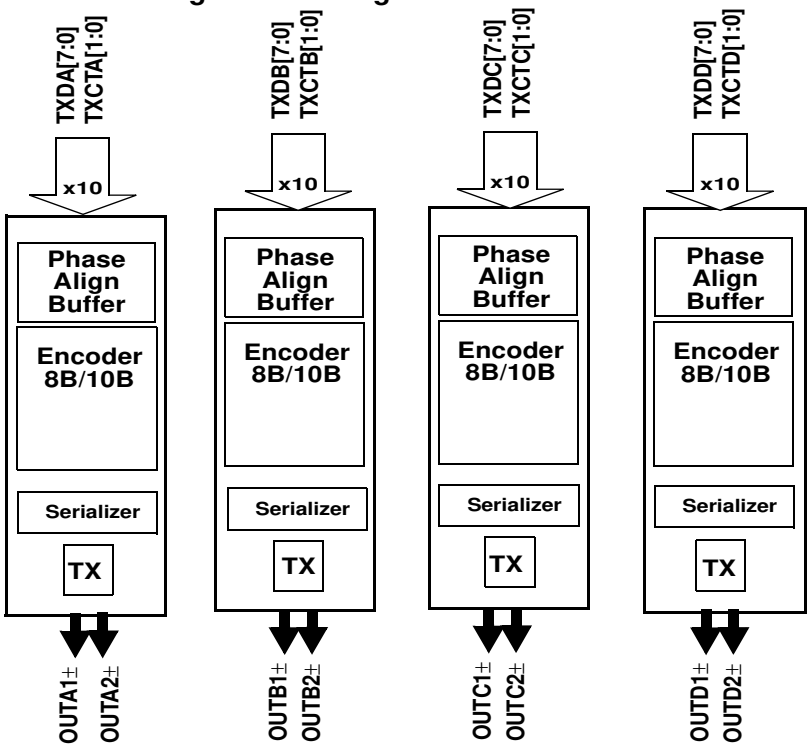
Figure 1. HOTLink II System Connections

The parallel input interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture.

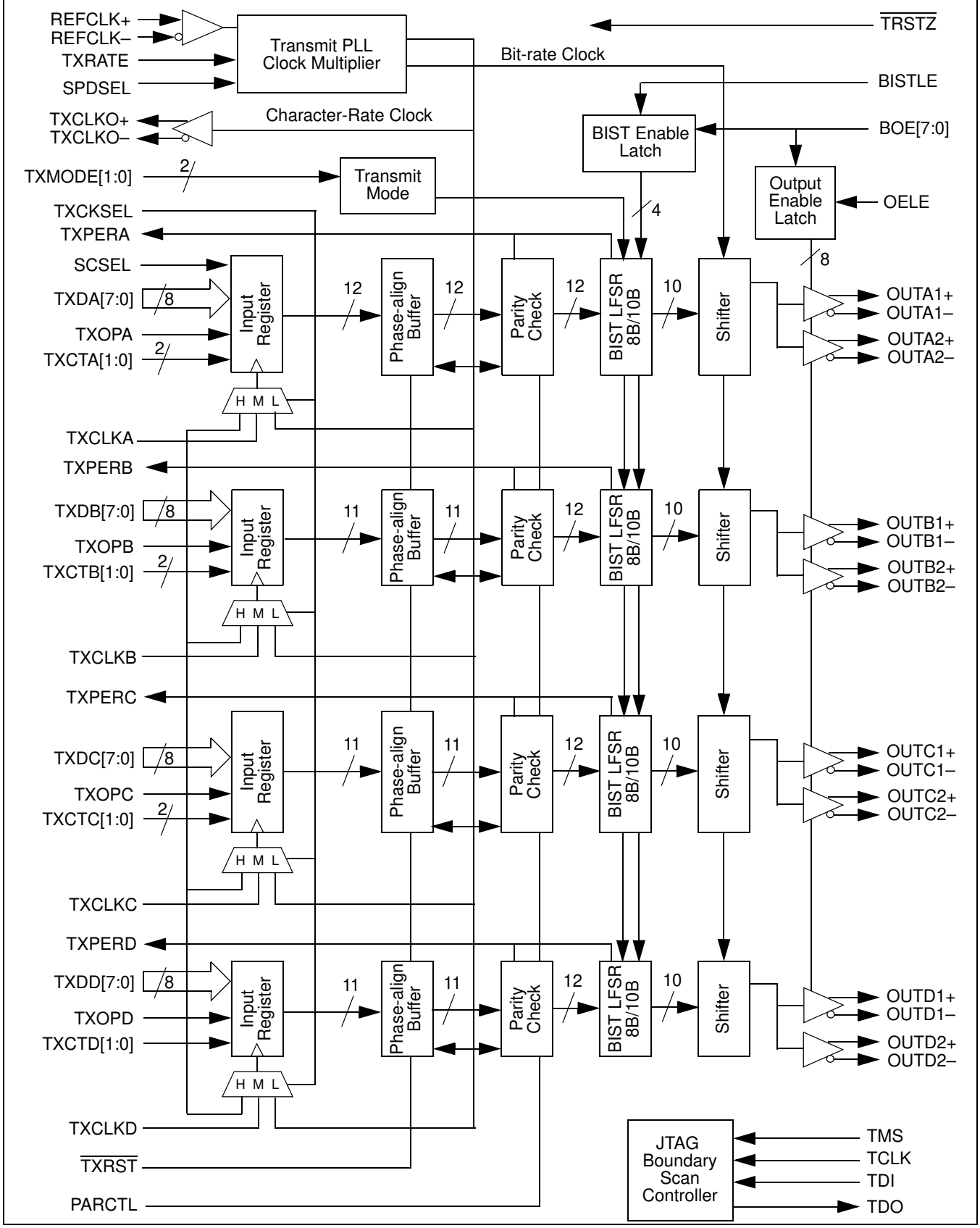
Each transmitter contains an independent BIST pattern generator. This BIST hardware allows at-speed testing of the high-speed serial data paths in each transmit section, and across the interconnecting links.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting backplanes on switches, routers, servers and video transmission systems.

CYP15G0401TB Transmitter Logic Block Diagram



Transmit Path Block Diagram



Pin Configuration (Top View)[1]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	N/C	OUT C1-	N/C	OUT C2-	V_{CC}	N/C	OUT D1-	GND	GND	OUT D2-	GND	OUT A1-	GND	N/C	OUT A2-	V_{CC}	N/C	OUT B1-	N/C	OUT B2-
B	V_{CC}	OUT C1+	V_{CC}	OUT C2+	V_{CC}	V_{CC}	OUT D1+	GND	N/C	OUT D2+	N/C	OUT A1+	GND	GND	OUT A2+	V_{CC}	V_{CC}	OUT B1+	GND	OUT B2+
C	TDI	TMS	V_{CC}	V_{CC}	V_{CC}	PAR CTL	N/C	GND	BOE[7]	BOE[5]	BOE[3]	BOE[1]	GND	TX MODE [0]	GND	V_{CC}	TX RATE	GND	GND	TDO
D	TCLK	$\overline{\text{TRSTZ}}$	V_{CC}	V_{CC}	V_{CC}	V_{CC}	SPD SEL	GND	BOE[6]	BOE[4]	BOE[2]	BOE[0]	GND	TX MODE [1]	GND	V_{CC}	V_{CC}	GND	N/C	N/C
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	TXPERC	TXOPC	TXDC [0]	N/C													BISTLE	N/C	N/C	N/C
G	TXDC [7]	TXCKSEL	TXDC [4]	TXDC [1]													GND	OELE	N/C	N/C
H	GND	GND	GND	GND													GND	GND	GND	GND
J	TXCTC [1]	TXDC [5]	TXDC [2]	TXDC [3]													N/C	N/C	N/C	N/C
K	N/C	N/C	TXCTC [0]	N/C													N/C	N/C	N/C	N/C
L	N/C	N/C	TXCLKC	TXDC [6]													N/C	N/C	N/C	TXDB [6]
M	N/C	N/C	N/C	N/C													TXCTB [1]	TXCTB [0]	TXDB [7]	TXCLKB
N	GND	GND	GND	GND													GND	GND	GND	GND
P	N/C	N/C	N/C	N/C													TXDB [5]	TXDB [4]	TXDB [3]	TXDB [2]
R	N/C	N/C	TXPERD	TXOPD													TXDB [1]	TXDB [0]	TXOPB	TXPERB
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	TXDD [0]	TXDD [1]	TXDD [2]	TXCTD [1]	V_{CC}	N/C	N/C	GND	N/C	N/C	REF CLK-	TXDA [1]	GND	TXDA [4]	TXCTA [0]	V_{CC}	N/C	N/C	N/C	N/C
V	TXDD [3]	TXDD [4]	TXCTD [0]	N/C	V_{CC}	N/C	N/C	GND	N/C	N/C	REF CLK+	N/C	GND	TXDA [3]	TXDA [7]	V_{CC}	N/C	N/C	N/C	N/C
W	TXDD [5]	TXDD [7]	N/C	N/C	V_{CC}	N/C	N/C	GND	TXCLKO-	$\overline{\text{TXRST}}$	TXOPA	SCSEL	GND	TXDA [2]	TXDA [6]	V_{CC}	N/C	N/C	N/C	N/C
Y	TXDD [6]	TXCLKD	N/C	N/C	V_{CC}	N/C	N/C	GND	TXCLKO+	N/C	TXCLKA	TXPERA	GND	TXDA [0]	TXDA [5]	V_{CC}	TXCTA [1]	N/C	N/C	N/C

Note:
1. N/C = Do Not Connect

Pin Configuration (Bottom View)[1]

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
OUT B2-	N/C	OUT B1-	N/C	V_{CC}	OUT A2-	N/C	GND	OUT A1-	GND	OUT D2-	GND	GND	OUT D1-	N/C	V_{CC}	OUT C2-	N/C	OUT C1-	N/C	A
OUT B2+	GND	OUT B1+	V_{CC}	V_{CC}	OUT A2+	GND	GND	OUT A1+	N/C	OUT D2+	N/C	GND	OUT D1+	V_{CC}	V_{CC}	OUT C2+	V_{CC}	OUT C1+	V_{CC}	B
TDO	GND	GND	TX RATE	V_{CC}	GND	TX MODE [0]	GND	BOE[1]	BOE[3]	BOE[5]	BOE[7]	GND	N/C	PAR CTL	V_{CC}	V_{CC}	V_{CC}	TMS	TDI	C
N/C	N/C	GND	V_{CC}	V_{CC}	GND	TX MODE [1]	GND	BOE[0]	BOE[2]	BOE[4]	BOE[6]	GND	SPD SEL	V_{CC}	V_{CC}	V_{CC}	V_{CC}	$\overline{\text{TRSTZ}}$	TCLK	D
V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}	E
N/C	N/C	N/C	BISTLE													N/C	TXDC [0]	TXOP C	TXPER C	F
N/C	N/C	OELE	GND													TXDC [1]	TXDC [4]	TXCK SEL	TXDC [7]	G
GND	GND	GND	GND													GND	GND	GND	GND	H
N/C	N/C	N/C	N/C													TXDC [3]	TXDC [2]	TXDC [5]	TXCTC [1]	J
N/C	N/C	N/C	N/C													N/C	TXCTC [0]	N/C	N/C	K
TXDB [6]	N/C	N/C	N/C													TXDC [6]	TXCLK C	N/C	N/C	L
TXCLK B	TXDB [7]	TXCTB [0]	TXCTB [1]													N/C	N/C	N/C	N/C	M
GND	GND	GND	GND													GND	GND	GND	GND	N
TXDB [2]	TXDB [3]	TXDB [4]	TXDB [5]													N/C	N/C	N/C	N/C	P
TXPER B	TXOP B	TXDB [0]	TXDB [1]													TXOP D	TXPER D	N/C	N/C	R
V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}	T
N/C	N/C	N/C	N/C	V_{CC}	TXCTA [0]	TXDA [4]	GND	TXDA [1]	REF CLK-	N/C	N/C	GND	N/C	N/C	V_{CC}	TXCTD [1]	TXDD [2]	TXDD [1]	TXDD [0]	U
N/C	N/C	N/C	N/C	V_{CC}	TXDA [7]	TXDA [3]	GND	N/C	REF CLK+	N/C	N/C	GND	N/C	N/C	V_{CC}	N/C	TXCTD [0]	TXDD [4]	TXDD [3]	V
N/C	N/C	N/C	N/C	V_{CC}	TXDA [6]	TXDA [2]	GND	SCSEL	TXOP A	$\overline{\text{TXRST}}$	TXCLK O-	GND	N/C	N/C	V_{CC}	N/C	N/C	TXDD [7]	TXDD [5]	W
N/C	N/C	N/C	TXCTA [1]	V_{CC}	TXDA [5]	TXDA [0]	GND	TXPER A	TXCLK A	N/C	TXCLK O+	GND	N/C	N/C	V_{CC}	N/C	N/C	TXCLK D	TXDD [6]	Y

Pin Descriptions

CYP15G0401TB Quad HOTLink II Transmitter

Pin Name	I/O Characteristics	Signal Description
Transmit Path Data Signals		
TXPERA TXPERB TXPERC TXPERD	LVTTL Output, changes relative to REFCLK↑ [2]	**Transmit Path Parity Error**. Active HIGH. Asserted (HIGH) if parity checking is enabled and a parity error is detected at the Encoder. This output is HIGH for one transmit character clock period to indicate detection of a parity error in the character presented to the Encoder. If a parity error is detected, the character in error is replaced with a C0.7 character to force a corresponding bad-character detection at the remote end of the link. This replacement takes place regardless of the encoded/non-encoded state of the interface. When BIST is enabled for the specific transmit channel, BIST progress is presented on these outputs. Once every 511 character times, the associated TXPERx signal will pulse HIGH for one transmit-character clock period to indicate a complete pass through the BIST sequence. Therefore, in this case TXPERx signal will pulse HIGH for one transmit-character clock period. These outputs also provide indication of a transmit Phase-align Buffer underflow or overflow. When the transmit Phase-align Buffers are enabled (TXCKSEL ≠ LOW, or TXCKSEL = LOW and TXRATE = HIGH), if an underflow or overflow condition is detected, TXPERx for the channel in error is asserted and remains asserted until either an atomic Word Sync Sequence is transmitted or $\overline{\text{TXRST}}$ is sampled LOW to re-center the transmit Phase-align Buffers.
TXCTA[1:0] TXCTB[1:0] TXCTC[1:0] TXCTD[1:0]	LVTTL Input, synchronous, sampled by the selected TXCLKx↑ or REFCLK↑ [2]	**Transmit Control**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL, and are passed to the Encoder or Transmit Shifter. They identify how the associated TXDx[7:0] characters are interpreted. When the Encoder is bypassed, these inputs are interpreted as data bits of 10-bit input character. When the Encoder is enabled, these inputs determine if the TXDx[7:0] character is encoded as Data, a Special Character code, a K28.5 fill character or a Word Sync Sequence. See *Table 1* for details.
TXDA[7:0] TXDB[7:0] TXDC[7:0] TXDD[7:0]	LVTTL Input, synchronous, sampled by the selected TXCLKx↑ or REFCLK↑ [2]	**Transmit Data Inputs**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL and passed to the Encoder or Transmit Shifter. When the Encoder is enabled (TXMODE[1:0] ≠ LOW), TXDx[7:0] specify the specific data or command character to be sent. When the Encoder is bypassed, these inputs are interpreted as data bits of the 10-bit input character. See *Table 1* for details.
TXOPA TXOPB TXOPC TXOPD	LVTTL Input, synchronous, internal pull-up, sampled by the respective TXCLKx↑ or REFCLK↑ [2]	**Transmit Path Odd Parity**. When parity checking is enabled (PARCTL ≠ LOW), the parity captured at these inputs is XORed with the data on the associated TXDx bus (and sometimes TXCT[1:0]) to verify the integrity of the captured character. See *Table 2* for details.
SCSEL	LVTTL Input, synchronous, internal pull-down, sampled by TXCLKA↑ or REFCLK↑ [2]	**Special Character Select**. Used in some transmit modes along with TXCTx[1:0] to encode special characters or to initiate a Word Sync Sequence. When the transmit paths are configured for independent input clocks (TXCKSEL = MID), SCSEL is captured relative to TXCLKA↑.

Note:
2. When REFCLK is configured for half-rate operation (TXRATE = HIGH), these inputs are sampled (or the outputs change) relative to both the rising and falling edges of REFCLK.

Pin Descriptions (continued)

CYP15G0401TB Quad HOTLink II Transmitter

Pin Name	I/O Characteristics	Signal Description
$\overline{\text{TXRST}}$	LVTTL Input, asynchronous, internal pull-up, sampled by REFCLK↑ [2]	**Transmit Clock Phase Reset**. Active LOW. When sampled LOW, the transmit Phase-align Buffers are allowed to adjust their data-transfer timing (relative to the selected input clock) to allow clean transfer of data from the Input Register to the Encoder or Transmit Shifter. When $\overline{\text{TXRST}}$ is sampled HIGH, the internal phase relationship between the associated TXCLKx and the internal character-rate clock is fixed and the device operates normally. When configured for half-rate REFCLK sampling of the transmit character stream (TXCKSEL = LOW and TXRATE = HIGH), assertion of $\overline{\text{TXRST}}$ is only used to clear Phase-align buffer faults caused by highly asymmetric REFCLK periods or REFCLKs with excessive cycle-to-cycle jitter. During this alignment period, one or more characters may be added to or lost from all the associated transmit paths as the transmit Phase-align Buffers are adjusted. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive rising edges REFCLK to ensure the reset operation is initiated correctly on all channels. This input is ignored when both TXCKSEL and TXRATE are LOW, since the phase align buffer is bypassed. In all other configurations, $\overline{\text{TXRST}}$ should be asserted during device initialization to ensure proper operation of the Phase-align buffer. $\overline{\text{TXRST}}$ should be asserted after the presence of a valid TXCLKx and after allowing enough time for the TXPLL to lock to the reference clock (as specified by parameter t_{TXLOCK}).
Transmit Path Clock and Clock Control		
TXCKSEL	Three-level Select [3], static control input	**Transmit Clock Select**. Selects the clock source, used to write data into the transmit Input Register of the transmit channel(s). When LOW, REFCLK↑ [2] is used as the Input Register clock for TXDx[7:0] and TXCTx[1:0] of all channels. When MID, TXCLKx↑ is used as the Input Register clock for TXDx[7:0] and TXCTx[1:0]. When HIGH, TXCLKA↑ is used as the Input Register clock for TXDx[7:0] and TXCTx[1:0] of all channels.
TXCLKO±	LVTTL Output	**Transmit Clock Output**. This true and complement output clock is synthesized by the transmit PLL and is synchronous to the internal transmit character clock. It has the same frequency as REFCLK (when TXRATE = LOW), or twice the frequency of REFCLK (when TXRATE = HIGH). This output clock has no direct phase relationship to REFCLK.
TXRATE	LVTTL Input, static control input, internal pull-down	**Transmit PLL Clock Rate Select**. When TXRATE = HIGH, the Transmit PLL multiplies REFCLK by 20 to generate the serial bit-rate clock. When TXRATE = LOW, the transmit PLL multiples REFCLK by 10 to generate the serial bit-rate clock. See *Table 9* for a list of operating serial rates. When TXCKSEL = MID or HIGH (TXCLKx or TXCLKA selected to clock input register), configuring TXRATE = HIGH (Half-rate REFCLK) is an invalid mode of operation.
TXCLKA TXCLKB TXCLKC TXCLKD	LVTTL Clock Input, internal pull-down	**Transmit Path Input Clocks**. These clocks must be frequency-coherent to TXCLKO±, but may be offset in phase. The internal operating phase of each input clock (relative to REFLCK or TXCLKO±) is adjusted when $\overline{\text{TXRST}}$ = LOW and locked when $\overline{\text{TXRST}}$ = HIGH.
Transmit Path Mode Control		
TXMODE[1:0]	Three-level Select [3] static control inputs	**Transmit Operating Mode**. These inputs are interpreted to select one of nine operating modes of the transmit path. See *Table 3* for a list of operating modes.

Note:

3. Three-level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC}. When not connected or allowed to float, a Three-level select input will self-bias to the MID level.

Pin Descriptions (continued)

CYP15G0401TB Quad HOTLink II Transmitter

Pin Name	I/O Characteristics	Signal Description
Device Control Signals		
PARCTL	Three-level Select [3], static control input	**Parity Check Control**. Used to control the different parity check functions. When LOW, parity check is disabled. When MID, and the 8B/10B Encoder is enabled (TXMODE[1] ≠ LOW), TXDx[7:0] inputs are checked (along with TXOPx) for valid ODD parity. When the Encoder is disabled (TXMODE[1] = LOW), theTXDx[7:0] and TXCTx[1:0] inputs are checked (along with TXOPx) for valid ODD parity. When HIGH, parity check is enabled. The TXDx[7:0] and TXCTx[1:0] inputs are checked (along with TXOPx) for valid ODD parity. See *Table 2* for details.
SPDSEL	Three-level Select [3] static control input	**Serial Rate Select**. This input specifies the operating bit-rate range of the transmit PLLs. LOW = 195–400 MBd, MID = 400–800 MBd, HIGH = 800–1500 MBd. When SPDSEL is LOW, setting TXRATE = HIGH (Half-rate Reference Clock) is invalid.
$\overline{\text{TRSTZ}}$	LVTTL Input, internal pull-up	**Device Reset**. Active LOW. Initializes all state machines and counters in the device. When sampled LOW by the rising edge of REFCLK↑, this input resets the internal state machines. When the reset is removed ($\overline{\text{TRSTZ}}$ sampled HIGH by REFCLK↑), the status and data outputs will become deterministic in less than 16 REFCLK cycles. The BISTLE and OELE latches are reset by $\overline{\text{TRSTZ}}$. If the Phase-align Buffer is used, $\overline{\text{TRSTZ}}$ should be applied after power up to initialize the internal pointers into these memory arrays.
REFCLK±	Differential LVPECL or single-ended LVTTL Input Clock	**Reference Clock**. This clock input is used as the timing reference for the transmit PLL. This input clock may also be selected to clock the transmit parallel interfaces. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLK input, and leave the alternate REFCLK input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs. When TXCKSEL = LOW, REFCLK is also used as the clock for the parallel transmit data (input) interface.
Analog I/O and Control		
OUTA1± OUTB1± OUTC1± OUTD1±	CML Differential Output	**Primary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules.
OUTA2± OUTB2± OUTC2± OUTD2±	CML Differential Output	**Secondary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules.
OELE	LVTTL Input, asynchronous, internal pull-up	**Serial Driver Output Enable Latch Enable**. Active HIGH. When OELE = HIGH, the signals on the BOE[7:0] inputs directly control the OUTxy± differential drivers. When the BOE[x] input is HIGH, the associated OUTxy± differential driver is enabled. When the BOE[x] input is LOW, the associated OUTxy± differential driver is powered down. The specific mapping of BOE[7:0] signals to transmit output enables is listed in *Table 8*. When OELE returns LOW, the last values present on BOE[7:0] are captured in the internal Output Enable Latch. If the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable all outputs.
BISTLE	LVTTL Input, asynchronous, internal pull-up	**Transmit BIST Latch Enable**. Active HIGH. When BISTLE = HIGH, the signals on the BOE[7:0] inputs directly control the transmit BIST enables. When the BOE[x] input is LOW, the associated transmit channel is configured to generate the BIST sequence. When the BOE[x] input is HIGH, the associated transmit channel is configured for normal data transmission. The specific mapping of BOE[7:0] signals to transmit BIST enables is listed in *Table 8*. When BISTLE returns LOW, the last values present on BOE[7:0] are captured in the internal BIST Enable Latch. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable BIST on all transmit channels.

Pin Descriptions (continued)

CYP15G0401TB Quad HOTLink II Transmitter

Pin Name	I/O Characteristics	Signal Description
BOE[7:0]	LVTTL Input, asynchronous, internal pull-up	**BIST and Serial Output, and Enables**. These inputs are passed to and through the Output Enable Latch when OELE is HIGH, and captured in this latch when OELE returns LOW. These inputs are passed to and through the BIST Enable Latch when BISTLE is HIGH, and captured in this latch when BISTLE returns LOW.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset. The TAP controller is also reset automatically upon application of power to the device.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**
TDO	Three-state LVTTL Output	**Test Data Out**. JTAG data output buffer which is High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
Power		
V_{CC}		**+3.3V Power**
GND		**Signal and power ground for all internal circuits**.

CYP15G0401TB HOTLink II Operation

The CYP15G0401TB is a highly configurable device designed to support reliable transfer of large quantities of data, using high-speed serial links, from one source to one or multiple destinations. This device supports four single-byte or single-character channels.

CYP15G0401TB Transmit Data Path

Operating Modes

The transmit path of the CYP15G0401TB supports four character-wide data paths. These data paths are used in multiple operating modes as controlled by the TXMODE[1:0] inputs.

Input Register

The bits in the Input Register for each channel support different assignments, based on if the character is unencoded, encoded with two control bits, or encoded with three control bits. These assignments are shown in *Table 1*. Each Input Register captures a minimum of eight data bits and two control bits on each input clock cycle. When the Encoder is bypassed, the TXCTx[1:0] control bits, are part of the preencoded 10-bit character.

When the Encoder is enabled (TXMODE[1] ≠ LOW), the TXCTx[1:0] bits are interpreted along with the associated TXDx[7:0] character to generate the specific 10-bit transmission character. When TXMODE[0] ≠ HIGH, an additional special character select (SCSEL) input is also captured and interpreted. This SCSEL input is used to modify the encoding of the associated characters. When the transmit Input Registers are clocked by a common clock (TXCLKA↑ or REFCLK↑), this SCSEL input can be changed on a clock-by-clock basis and affects all four channels.

When operated with a separate input clock on each transmit channel, this SCSEL input is sampled synchronous to TXCLKA↑. While the value on SCSEL still affects all channels, it is interpreted when the character containing it is read from the transmit Phase-align Buffer (where all four paths are internally clocked synchronously).

Table 1. Input Register Bit Assignments [4]

Signal Name	Unencoded	Encoded	
		2-bit Control	3-bit Control
TXDx[0] (LSB)	DINx[0]	TXDx[0]	TXDx[0]
TXDx[1]	DINx[1]	TXDx[1]	TXDx[1]
TXDx[2]	DINx[2]	TXDx[2]	TXDx[2]
TXDx[3]	DINx[3]	TXDx[3]	TXDx[3]
TXDx[4]	DINx[4]	TXDx[4]	TXDx[4]
TXDx[5]	DINx[5]	TXDx[5]	TXDx[5]
TXDx[6]	DINx[6]	TXDx[6]	TXDx[6]
TXDx[7]	DINx[7]	TXDx[7]	TXDx[7]
TXCTx[0]	DINx[8]	TXCTx[0]	TXCTx[0]
TXCTx[1] (MSB)	DINx[9]	TXCTx[1]	TXCTx[1]
SCSEL	N/A	N/A	SCSEL

Phase-align Buffer

Data from the Input Registers are passed either to the Encoder or to the associated Phase-align Buffer. When the transmit paths are operated synchronous to REFCLK↑ (TXCKSEL = LOW and TXRATE = LOW), the Phase-align Buffers are bypassed and data is passed directly to the Parity Check and Encoder blocks to reduce latency.

When an Input-Register clock with an uncontrolled phase relationship to REFCLK is selected (TXCKSEL ≠ LOW) or if data is captured on both edges of REFCLK (TXRATE = HIGH), the Phase-align Buffers are enabled. These buffers are used

to absorb clock phase differences between the presently selected input clock and the internal character clock.

Initialization of the Phase-align Buffers takes place when the TXRST input is sampled LOW by two consecutive rising edges of REFCLK. When TXRST is returned HIGH, the present input clock phase relative to REFCLK is set. TXRST is an asynchronous input, but is sampled internally to synchronize it to the internal transmit path state machines.

Once set, the input clocks are allowed to skew in time up to half a character period in either direction relative to REFCLK; i.e., ±180°. This time shift allows the delay paths of the character clocks (relative to REFCLK) to change due to operating voltage and temperature, while not affecting the design operation.

If the phase offset, between the initialized location of the input clock and REFCLK↑, exceeds the skew handling capabilities of the Phase-align Buffer, an error is reported on the associated TXPERx output. This output indicates a continuous error until the Phase-align Buffer is reset. While the error remains active, the transmitter for the associated channel will output a continuous C0.7 character to indicate to the remote receiver that an error condition is present in the link.

In specific transmit modes, it is also possible to reset the Phase-align Buffers individually and with minimal disruption of the serial data stream. When the transmit interface is configured for generation of atomic Word Sync Sequences (TXMODE[1] = MID) and a Phase-align Buffer error is present, the transmission of a Word Sync Sequence will re-center the Phase-align Buffer and clear the error condition.[5]

Parity Support

In addition to the ten data and control bits that are captured at each transmit Input Register, a TXOPx input is also available on each channel. This allows the CYP15G0401TB to support ODD parity checking for each channel. Parity checking is available for all operating modes (including Encoder Bypass). The specific mode of parity checking is controlled by the PARCTL input, and operates per *Table 2*.

When PARCTL is MID (open) and the Encoders are enabled (TXMODE[1] ≠ LOW), only the TXDx[7:0] data bits are checked for ODD parity along with the associated TXOPx bit. When PARCTL = HIGH with the Encoder enabled (or MID with the Encoder bypassed), the TXDx[7:0] and TXCTx[1:0] inputs are checked for ODD parity along with the associated TXOPx bit. When PARCTL = LOW, parity checking is disabled.

When parity checking and the Encoder are both enabled (TXMODE[1] ≠ LOW), the detection of a parity error causes a C0.7 character of proper disparity to be passed to the Transmit Shifter. When the Encoder is bypassed (TXMODE[1] = LOW, LOW), detection of a parity error causes a positive disparity version of a C0.7 transmission character to be passed to the Transmit Shifter.

Encoder

The character, received from the Input Register or Phase-align Buffer and Parity Check Logic, is then passed to the Encoder logic. This block interprets each character and any associated control bits, and outputs a 10-bit transmission character.

Table 2. Input Register Bits Checked for Parity [6]

Signal Name	Transmit Parity Check Mode (PARCTL)			
	LOW	MID		HIGH
		TXMODE[1] = LOW	TXMODE[1] ≠ LOW	
TXDx[0]		X [7]	X	X
TXDx[1]		X	X	X
TXDx[2]		X	X	X
TXDx[3]		X	X	X
TXDx[4]		X	X	X
TXDx[5]		X	X	X
TXDx[6]		X	X	X
TXDx[7]		X	X	X
TXCTx[0]		X		X
TXCTx[1]		X		X
TXOPx		X	X	X

Depending on the configured operating mode, the generated transmission character may be

- the 10-bit pre-encoded character accepted in the Input Register
- the 10-bit equivalent of the eight-bit Data character accepted in the Input Register
- the 10-bit equivalent of the eight-bit Special Character code accepted in the Input Register
- the 10-bit equivalent of the C0.7 SVS character if parity checking was enabled and a parity error was detected
- the 10-bit equivalent of the C0.7 SVS character if a Phase-align Buffer overflow or underflow error is present
- a character that is part of the 511-character BIST sequence
- a K28.5 character generated as an individual character or as part of the 16-character Word Sync Sequence.

The selection of the specific characters generated are controlled by the TXMODE[1:0], SCSEL, TXCTx[1:0], and TXDx[7:0] inputs for each character.

Data Encoding

Raw data, as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee

- a minimum transition density (to allow the remote serial receive PLL to extract a clock from the data stream).
- a DC-balance in the signaling (to prevent baseline wander).
- run-length limits in the serial data (to limit the bandwidth requirements of the serial link).

Notes:

4. The TXOPx inputs are also captured in the associated Input Register, but their interpretation is under the separate control of PARCTL.
5. One or more K28.5 characters may be added or lost from the data stream during this reset operation. When used with non-Cypress devices that require a complete 16-character Word Sync Sequence for proper Receive Elasticity Buffer alignment, it is recommend that the sequence be followed by a second Word Sync Sequence to ensure proper operation.
6. Transmit path parity errors are reported on the associated TXPERx output.
7. Bits marked as X are XORed together. Result must be a logic-1 for parity to be valid.

- the remote receiver a way of determining the correct character boundaries (framing).

When the Encoder is enabled (TXMODE[1] ≠ LOW), the characters to be transmitted are converted from Data or Special Character codes to 10-bit transmission characters (as selected by their respective TXCTx[1:0] and SCSEL inputs), using an integrated 8B/10B Encoder. When directed to encode the character as a Special Character code, it is encoded using the Special Character encoding rules listed in *Table 14*. When directed to encode the character as a Data character, it is encoded using the Data Character encoding rules in *Table 13*.

The 8B/10B Encoder is standards compliant with ANSI/NCITS ASC X3.230-1994 (Fibre Channel), IEEE 802.3z (Gigabit Ethernet), the IBM® ESCON® and FICON™ channels, Digital Video Broadcast (DVB-ASI), and ATM Forum standards for data transport.

Many of the Special Character codes listed in *Table 14* may be generated by more than one input character. The CYP15G0401TB is designed to support two independent (but non-overlapping) Special Character code tables. This allows the CYP15G0401TB to operate in mixed environments with other Cypress HOTLink devices using the enhanced Cypress command code set, and the reduced command sets of other non-Cypress devices. Even when used in an environment that normally uses non-Cypress Special Character codes, the selective use of Cypress command codes can permit operation where running disparity and error handling must be managed.

Following conversion of each input character from eight bits to a 10-bit transmission character, it is passed to the Transmit Shifter and is shifted out LSB first, as required by ANSI and IEEE standards for 8B/10B coded serial data streams.

Transmit Modes

The operating mode of the transmit path is set through the TXMODE[1:0] inputs. These static three-level select inputs allow one of nine transmit modes to be selected. The transmit modes are listed in *Table 3*

Table 3. Transmit Operating Modes

TX Mode		Operating Mode		
Mode Number	TXMODE [1:0]	Word Sync Sequence Support	SCSEL Control	TXCTx Function
0	LL	None	None	Encoder Bypass
1	LM	None	None	Reserved for test
2	LH	None	None	Reserved for test
3	ML	Atomic	Special Character	Encoder Control
4	MM	Atomic	Word Sync	Encoder Control
5	MH	Atomic	None	Encoder Control
6	HL	Interruptible	Special Character	Encoder Control
7	HM	Interruptible	Word Sync	Encoder Control
8	HH	Interruptible	None	Encoder Control

Note:
8. LSB is shifted out first.

The encoded modes (TX Modes 3 through 8) support multiple encoding tables. These encoding tables vary by the specific combinations of SCSEL, TXCTx[1], and TXCTx[0] that are used to control the generation of data and control characters. These multiple encoding forms allow maximum flexibility in interfacing to legacy applications, while also supporting numerous extensions in capabilities.

TX Mode 0—Encoder Bypass

When the Encoder is bypassed, the character captured from the TXDx[7:0] and TXCTx[1:0] inputs is passed directly to the Transmit Shifter without modification. If parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected, the 10-bit character is replaced with the 1001111000 pattern (+C0.7 character).

With the Encoder bypassed, the TXCTx[1:0] inputs are considered part of the data character and do not perform a control function that would otherwise modify the interpretation of the TXDx[7:0] bits. The bit usage and mapping of these control bits when the Encoder is bypassed is shown in *Table 4*.

In Encoder Bypass mode, the SCSEL input is ignored. All clocking modes interpret the data the same, with no internal linking between channels.

Table 4. Encoder Bypass Mode (TXMODE[1:0] = LL)

Signal Name	Bus Weight	10Bit Name
TXDx[0] (LSB)[8]	2^0	a
TXDx[1]	2^1	b
TXDx[2]	2^2	c
TXDx[3]	2^3	d
TXDx[4]	2^4	e
TXDx[5]	2^5	i
TXDx[6]	2^6	f
TXDx[7]	2^7	g
TXCTx[0]	2^8	h
TXCTx[1] (MSB)	2^9	j

TX Modes 1 and 2—Factory Test Modes

These modes enable specific factory test configurations. They are not considered normal operating modes of the device. Entry or configuration of the device into these modes will not damage the device.

TX Mode 3— Word Sync and SCSEL Control of Special Codes

When configured in TX Mode 3, the SCSEL input is captured along with the associated TXCTx[1:0] data control inputs. These bits combine to control the interpretation of the TXDx[7:0] bits and the characters generated by them. These bits are interpreted as listed in *Table 5*.

When TXCKSEL = MID, all transmit channels capture data into their Input Registers using independent TXCLKx clocks. In this mode, the SCSEL input is sampled only by TXCLKA↑. When the character (accepted in the Channel-A Input Register) has passed through the Phase-align Buffer and any selected parity validation, the level captured on SCSEL is passed to the Encoder of the remaining channels during this same cycle.

Table 5. TX Modes 3 and 6 Encoding

SCSEL	TXCTx[1]	TXCTx[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
1	0	1	Special character code
X	1	1	16-character Word Sync Sequence

To avoid the possible ambiguities that may arise due to the uncontrolled arrival of SCSEL relative to the characters in the alternate channels, SCSEL is often used as static control input.

Word Sync Sequence

When TXCTx[1:0] = 11, a 16-character sequence of K28.5 characters, known as a Word Sync Sequence, is generated on the associated channel. This sequence of K28.5 characters may start with either a positive or negative disparity K28.5 (as determined by the current running disparity and the 8B/10B coding rules). The disparity of the second and third K28.5 characters in this sequence are reversed from what normal 8B/10B coding rules would generate. The remaining K28.5 characters in the sequence follow all 8B/10B coding rules. The disparity of the generated K28.5 characters in this sequence follow a pattern of either ++−−+−+−+−+−+− or −−++−+−+−+−+−+.

When TXMODE[1] = MID (open, TX modes 3, 4, and 5), the generation of this character sequence is an atomic (non-interruptible) operation. Once it has been successfully started, it cannot be stopped until all sixteen characters have been generated. The content of the associated Input Registers is ignored for the duration of this 16-character sequence. At the end of this sequence, if the TXCTx[1:0] = 11 condition is sampled again, the sequence restarts and remains uninterruptible for the following fifteen character clocks.

If parity checking is enabled, the character used to start the Word Sync Sequence must also have correct ODD parity. Once the sequence is started, parity is not checked on the following fifteen characters in the Word Sync Sequence.

When TXMODE[1] = HIGH (TX modes 6, 7, and 8), the generation of the Word Sync Sequence becomes an interruptible operation. In TX Mode 6, this sequence is started as soon as the TXCTx[1:0] = 11 condition is detected on a channel. In order for the sequence to continue on that channel, the TXCTx[1:0] inputs must be sampled as 00 for the remaining fifteen characters of the sequence.

If at any time a sample period exists where TXCTx[1:0] ≠ 00, the Word Sync Sequence is terminated, and a character representing the associated data and control bits is generated by the Encoder. This resets the Word Sync Sequence state machine such that it will start at the beginning of the sequence at the next occurrence of TXCTx[1:0] = 11.

When parity checking is enabled and TXMODE[1] = HIGH, all characters (including those in the middle of a Word Sync Sequence) must have correct parity. The detection of a character with incorrect parity during a Word Sync Sequence will interrupt that sequence and force generation of a C0.7 SVS character. Any interruption of the Word Sync Sequence causes the sequence to terminate.

When TXCKSEL = LOW, the Input Registers for all four transmit channels are clocked by REFCLK.[2] When TXCKSEL = HIGH, the Input Registers for all four transmit channels are clocked with TXCLKA↑. In these clock modes all four sets of TXCTx[1:0] inputs operate synchronous to the SCSEL input.

TX Mode 4—Atomic Word Sync and SCSEL Control of Word Sync Sequence Generation

When configured in TX Mode 4, the SCSEL input is captured along with the associated TXCTx[1:0] data control inputs. These bits combine to control the interpretation of the TXDx[7:0] bits and the characters generated by them. These bits are interpreted as listed in *Table 6*.

When TXCKSEL = MID, all transmit channels operate independently. In this mode, the SCSEL input is sampled only by TXCLKA↑. When the character accepted in the Channel-A Input Register has passed any selected validation and is ready to be passed to the Encoder, the level captured on SCSEL is passed to the Encoders of the remaining channels during this same cycle.

Table 6. TX Modes 4 and 7 Encoding

SCSEL	TXCTx[1]	TXCTx[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
0	1	1	Special character code
1	X	1	16-character Word Sync Sequence

Changing the state of SCSEL will change the relationship of the characters to other channels. SCSEL should either be used as a static configuration input, or changed only when the state of TXCTx[1:0] on the alternate channels are such that SCSEL is ignored during the change.

TX Mode 4 also supports an Word Sync Sequence. Unlike TX Mode 3, this sequence starts when SCSEL and TXCTx[0] are both high. With the exception of the combination of control bits used to initiate the sequence, the generation and operation of this Word Sync Sequence is the same as for TX Mode 3.

TX Mode 5—Atomic Word Sync generation without SCSEL.

When configured in TX Mode 5, the SCSEL signal is not used. The TXCTx[1:0] inputs for each channel control the characters generated by that channel. The specific characters generated by these bits are listed in *Table 7*.

TX Mode 5 also has the capability of generating an atomic Word Sync Sequence. For the sequence to be started, the TXCTx[1:0] inputs must both be sampled HIGH. The generation and operation of this Word Sync Sequence is the same as TX Mode 3.

Transmit BIST

Each transmit channel contains an internal pattern generator that can be used to validate both device and link operation.

Table 7. TX Modes 5 and 8 Encoding

SCSEL	TXCTx[1]	TXCTx[0]	Characters Generated
X	0	0	Encoded data character
X	0	1	K28.5 fill character
X	1	0	Special character code
X	1	1	16-character Word Sync Sequence

These generators are enabled by the associated BOE[x] signals listed in *Table 8* (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to identical LFSR in the attached remote Receiver(s), the CYP15G0401RB for example. To enable BIST for serial link testing, ensure that the remote HOTLink receivers are using the recovered clock from the associated receive CDR PLL to clock the receive parallel interface (for example RXCKSEL = MID for the CYP15G0401RB device).

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator in the associated transmit channel. When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH to open the latch. A device reset (TRSTZ sampled LOW), presets the BIST Enable Latch to disable BIST on all channels.

All data and data-control information present at the associated TXDx[7:0] and TXCTx[1:0] inputs are ignored when BIST is active on that channel.

Serial Output Drivers

The serial interface Output Drivers use high-performance differential CML (Current Mode Logic) to provide source-matched drivers for the transmission lines. These Serial Drivers accept data from the Transmit Shifters. These outputs have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines. To achieve OBSAI RP3 compliancy, the serial output drivers must be AC-coupled to the transmission medium.

Each Serial Driver can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the OELE latch-enable signal. When OELE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Serial Output Enable Latch to control the Serial Driver. The BOE[7:0] input associated with a specific OUTxy± driver is listed in *Table 8*. When OELE is HIGH and BOE[x] is HIGH, the associated Serial Driver is enabled. When OELE is HIGH and BOE[x] is LOW, the associated Serial Driver is disabled and internally powered down. If both Serial Drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch, and remain there until OELE returns HIGH to enable the latch. A device reset (TRSTZ sampled LOW) clears this latch and disables all Serial Drivers.

Table 8. Output Enable and BIST Enable Signal Map

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)
BOE[7]	OUTD2±	Transmit D
BOE[6]	OUTD1±	X
BOE[5]	OUTC2±	Transmit C
BOE[4]	OUTC1±	X
BOE[3]	OUTB2±	Transmit B
BOE[2]	OUTB1±	X
BOE[1]	OUTA2±	Transmit A
BOE[0]	OUTA1±	X

NOTE: When all transmit channels are disabled (i.e., both outputs disabled in all channels) and a channel is re-enabled, the data on the Serial Drivers may not meet all timing specifications for up to 200 µs.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiples that clock by 10 or 20 (as selected by TXRATE) to generate a bit-rate clock for use by the Transmit Shifter. It also provides a character-rate clock used by the transmit paths.

This clock multiplier PLL can accept a REFCLK input between 20 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYP15G0401TB clock multiplier (controlled by TXRATE) and by the level on the SPDSEL input.

When TXRATE = HIGH (Half-rate REFCLK), TXCKSEL = HIGH or MID (TXCLKx or TXCLKA selected to clock input register) is an invalid mode of operation.

SPDSEL is a static three-level select [3] (ternary) input that selects one of three operating ranges for the serial data outputs and inputs. The operating serial signaling-rate and allowable range of REFCLK frequencies are listed in *Table 9*.

Table 9. Operating Speed Settings

SPDSEL	TXRATE	REFCLK Frequency (MHz)	Signaling Rate (MBaud)
LOW	1	reserved	195–400
	0	19.5–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

The REFCLK± input is a differential input with each input internally biased to 1.4V. If the REFCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, REFCLK– can be left floating and the input signal is recognized when it passes through the internally biased reference point.

When both the REFCLK+ and REFCLK– inputs are connected, the clock source must be a differential clock. This can be either a differential LVPECL clock that is DC- or AC-coupled, or a differential LVTTL or LVCMOS clock.

By connecting the REFCLK– input to an external voltage source or resistive voltage divider, it is possible to adjust the reference point of the REFCLK+ input for alternate logic levels. When doing so, it is necessary to ensure that the input differential crossing point remains within the parametric range supported by the input.

Power Control

The CYP15G0401TB supports user control of the powered up or down state of each transmit channel. The transmit channels are controlled by the OELE signal and the values present on the BOE[7:0] bus. Powering down unused channels will save power and reduce system heat generation. Controlling system power dissipation will improve the system performance.

Transmit Channels

When OELE is HIGH, the signals on the BOE[7:0] inputs directly control the power enables for the Serial Drivers. When a BOE[x] input is HIGH, the associated Serial Driver is enabled. When a BOE[x] input is LOW, the associated Serial Driver is disabled and powered down. If both Serial Drivers of a channel are disabled, the internal logic for that transmit channel is powered down. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch.

Device Reset State

When the CYP15G0401TB is reset by assertion of $\overline{\text{TRSTZ}}$, the Transmit Enable Latches are cleared, and the BIST Enable Latch is preset. In this state, all transmit channels are disabled, and BIST is disabled on all channels.

Following a device reset, it is necessary to enable the transmit channels used for normal operation. This can be done by sequencing the appropriate values on the BOE[7:0] inputs while the OELE signal is raised and lowered. For systems that do not require dynamic control of power, or want the device to power up in a fixed configuration, it is also possible to strap the OELE control signal HIGH to permanently enable its associated latches. Connection of the associated BOE[7:0] signals to a stable HIGH will then enable the respective transmit channels as soon as the $\overline{\text{TRSTZ}}$ signal is deasserted.

JTAG Support

The CYP15G0401TB contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, only boundary scan is supported. This capability is present only on the LVTTL inputs, LVTTL outputs and the REFCLK± clock input. The high-speed serial inputs and outputs are not part of the JTAG test chain.

JTAG ID

The JTAG device ID for the CYP15G0401TB is ‘1C800069’x.

Three-level Select Inputs

Each Three-level select input reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11, respectively.

Maximum Ratings

(Above which the useful life may be impaired. User guidelines only, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +3.8V

DC Voltage Applied to LVTTL Outputs in High-Z State .....–0.5V to V_{CC} + 0.5V

Output Current into LVTTL Outputs (LOW).....60 mA

DC Input Voltage.....–0.5V to V_{CC} + 0.5V

Static Discharge Voltage.....> 2000 V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Power-up Requirements

The CYP15G0401TB requires one power-supply. The Voltage on any input or I/O pin cannot exceed the power pin during power-up

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ±5%
Industrial	–40°C to +85°C	+3.3V ±5%

CYP15G0401TB DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL-compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = –4 mA, V_{CC} = Min.	2.4	V_{CC}	V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{CC} = Min.	0	0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[9]	–20	–100	mA
I_{OZL}	High-Z Output Leakage Current		–20	20	µA
LVTTL-compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK Input, V_{IN} = V_{CC}		1.5	mA
		Other Inputs, V_{IN} = V_{CC}		+40	µA
I_{ILT}	Input LOW Current	REFCLK Input, V_{IN} = 0.0V		–1.5	mA
		Other Inputs, V_{IN} = 0.0V		–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: REFCLK±					
V_{DIFF}[10]	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.2	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		0.0	$V_{CC/2}$	V
V_{COMREF}[11]	Common Mode Range		1.0	V_{CC} – 1.2V	V
Three-level Inputs					
V_{IHH}	Three-level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}		200	µA
I_{IMM}	Input MID current	V_{IN} = V_{CC}/2	–50	50	µA
I_{ILL}	Input LOW current	V_{IN} = GND		–200	µA
Differential CML Serial Outputs: OUTA1±, OUTA2±, OUTB1±, OUTB2±, OUTC1±, OUTC2±, OUTD1±, OUTD2±					
V_{OHC}	Output HIGH Voltage (V_{CC} referenced)	100Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
		150Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V

Notes:

9. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
10. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
11. The common mode range defines the allowable range of REFCLK+ and REFCLK– when REFCLK+ = REFCLK–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

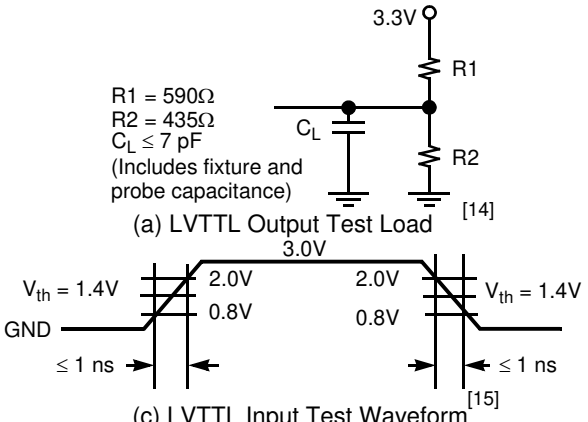
CYP15G0401TB DC Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OLC}	Output LOW Voltage (V_{CC} referenced)	100Ω differential load	V_{CC} – 1.4	V_{CC} – 0.7	V
		150Ω differential load	V_{CC} – 1.4	V_{CC} – 0.7	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100Ω differential load	450	900	mV
		150Ω differential load	560	1000	mV

Power Supply

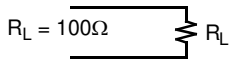
Parameter	Description	Test Conditions	Typ.[12]	Max.[13]	Unit
I_{CC}	Power Supply Current REFCLK = Max.	Commercial	610	770	mA
		Industrial		820	mA
I_{CC}	Power Supply Current REFCLK = 125 MHz	Commercial	590	750	mA
		Industrial		800	mA

Test Loads and Waveforms



(a) LVTTL Output Test Load [14]

(c) LVTTL Input Test Waveform [15]



(b) CML Output Test Load [14]

CYP15G0401TB AC Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
CYP15G0401TB Transmitter LVTTL Switching Characteristics Over the Operating Range				
f_{TS}	TXCLKx Clock Frequency	19.5	150	MHz
t_{TXCLK}	TXCLKx Period	6.66	51.28	ns
t_{TXCLKH}[16]	TXCLKx HIGH Time	2.2		ns
t_{TXCLKL}[16]	TXCLKx LOW Time	2.2		ns
t_{TXCLKR}[16, 17, 18]	TXCLKx Rise Time	0.2	1.7	ns
t_{TXCLKF}[16, 17, 18]	TXCLKx Fall Time	0.2	1.7	ns
t_{TXDS}	Transmit Data Set-Up Time to TXCLKx↑ (TXCKSEL ≠ LOW)	1.7		ns
t_{TXDH}	Transmit Data Hold Time from TXCLKx↑ (TXCKSEL ≠ LOW)	0.8		ns
f_{TOS}	TXCLKO Clock Frequency = 1x or 2x REFCLK Frequency	20	150	MHz
t_{TXCLKO}	TXCLKO Period	6.66	51.28	ns

Notes:

12. Maximum I_{CC} is measured with V_{CC} = MAX, with all TX channels and Serial Line Drivers enabled, sending a continuous alternating 01 pattern to the associated remote receive channel, and outputs unloaded.
13. Typical I_{CC} is measured under similar conditions except with V_{CC} = 3.3V, T_A = 25°C, with all TX channels enabled and one Serial Line Driver per transmit channel sending a continuous alternating 01 pattern to the associated remote receive channel. The redundant outputs on each channel are powered down and the parallel outputs are unloaded.
14. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only. 5-pF differential load reflects tester capacitance, and is recommended at low data rates only.
15. The LVTTL switching threshold is 1.4V. All timing references are made relative to the point where the signal edges crosses the threshold voltage.
16. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
17. The ratio of rise time to falling time must not vary by greater than 2:1.
18. For a given operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.

CYP15G0401TB AC Characteristics Over the Operating Range (continued)

Parameter	Description	Min.	Max.	Unit
$t_{TXCLKOD+}$	TXCLKO+ Duty Cycle with 60% HIGH time	–1.0	+0.5	ns
$t_{TXCLKOD–}$	TXCLKO– Duty Cycle with 40% HIGH time	–0.5	+1.0	ns

CYP15G0401TB REFCLK Switching Characteristics Over the Operating Range				
f_{REF} [19]	REFCLK Clock Frequency	19.5	150	MHz
t_{REFCLK}	REFCLK Period	6.66	51.28	ns
t_{REFH}	REFCLK HIGH Time (TXRATE = HIGH)	5.9		ns
	REFCLK HIGH Time (TXRATE = LOW)	2.9 [16]		ns
t_{REFL}	REFCLK LOW Time (TXRATE = HIGH)	5.9		ns
	REFCLK LOW Time (TXRATE = LOW)	2.9 [16]		ns
t_{REFD} [20]	REFCLK Duty Cycle	30	70	%
t_{REFR} [16, 17, 18]	REFCLK Rise Time (20% – 80%)		2	ns
t_{REFF} [16, 17, 18]	REFCLK Fall Time (20% – 80%)		2	ns
t_{TREFDS}	Transmit Data Setup Time to REFCLK (TXCKSEL = LOW)	1.7		ns
t_{TREFDH}	Transmit Data Hold Time from REFCLK (TXCKSEL = LOW)	0.8		ns

CYP15G0401TB Transmit Serial Outputs and TX PLL Characteristics Over the Operating Range					
Parameter	**Description**	**Condition**	**Min.**	**Max.**	**Unit**
t_B	Bit Time		5100	649	ps
t_{RISE} [16]	CML Output Rise Time 20% – 80% (CML Test Load)	SPDSEL = HIGH	60	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	180	1000	ps
t_{FALL} [16]	CML Output Fall Time 80% – 20% (CML Test Load)	SPDSEL = HIGH	60	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	180	1000	ps
t_{DJ} [16, 21, 23]	Deterministic Jitter (peak-peak)	IEEE 802.3z[24]		25	ps
t_{RJ} [16, 22, 23]	Random Jitter (σ)	IEEE 802.3z[24]		11	ps
t_{TXLOCK}	Transmit PLL lock to REFCLK			200	us

Capacitance [16]

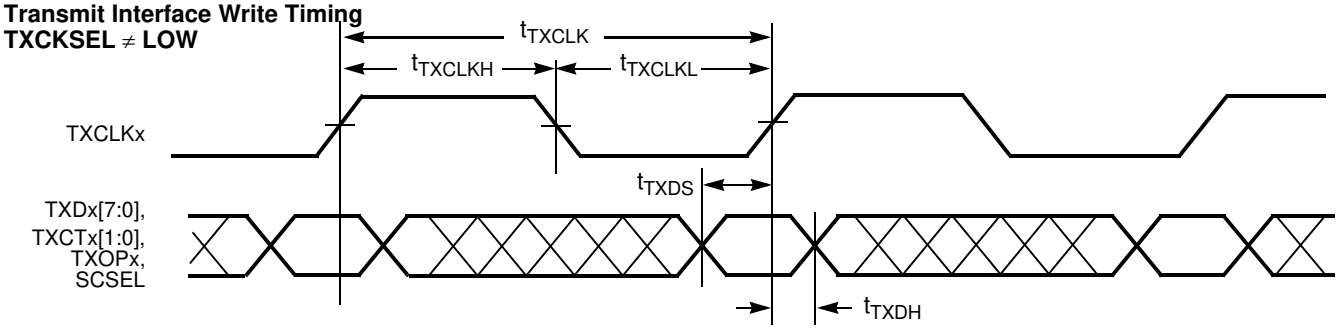
Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	7	pF
C_{INPECL}	PECL input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	4	pF

Notes:

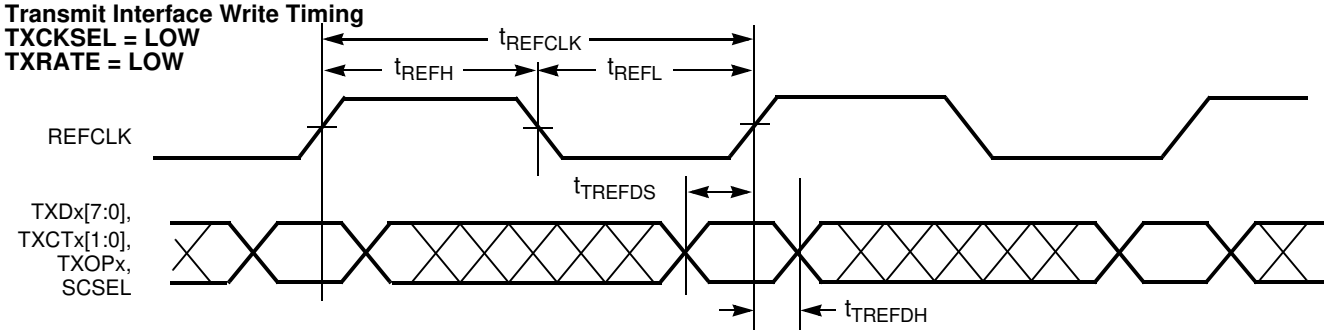
19. While transmitting to a remote HOTLink II receiver the frequency difference between the transmitter and receiver reference clocks must be within ±1500-PPM. While transmitting to an unknown remote receiver compliant to a particular standard, the stability of the crystal needs to be within the limits specified by the appropriate standard. For example, to be IEEE 802.3z Gigabit Ethernet compliant, the frequency stability of the crystal needs to be within ±100 PPM.
20. The duty cycle specification is a simultaneous condition with the t_{REFH} and t_{REFL} parameters. This means that at faster character rates the REFCLK duty cycle cannot be as large as 30% – 70%.
21. While sending continuous K28.5s, outputs loaded to a balanced 100Ω load, measured at the cross point of differential outputs, over the operating range.
22. While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.
23. Total jitter is calculated at an assumed BER of 1E –12. Hence: total jitter (t_J) = (t_{RJ} * 14) + t_{DJ}.
24. Also meets all Jitter Generation requirements as specified by OBSAI RP3, CPRI, ESCON, FICON, Fibre Channel and DVB-ASI.

CYP15G0401TB HOTLink II Transmitter Switching Waveforms

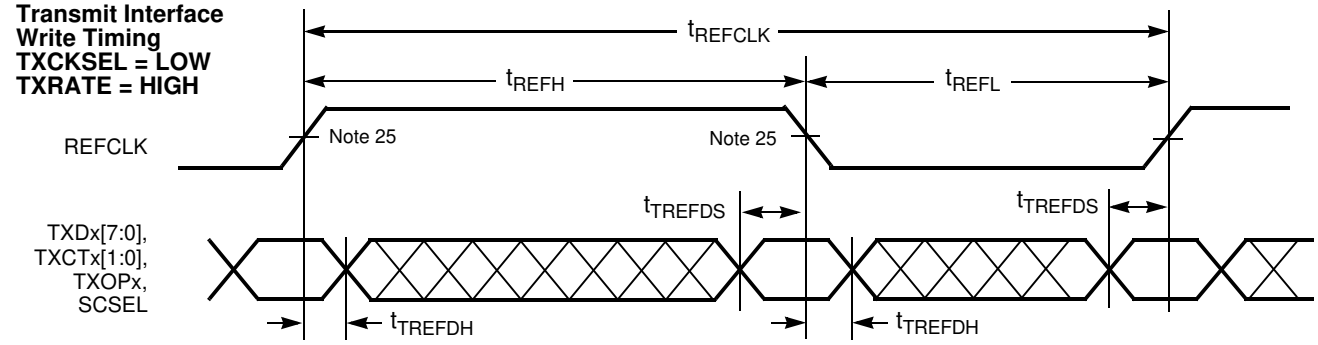
Transmit Interface Write Timing
TXCKSEL ≠ LOW



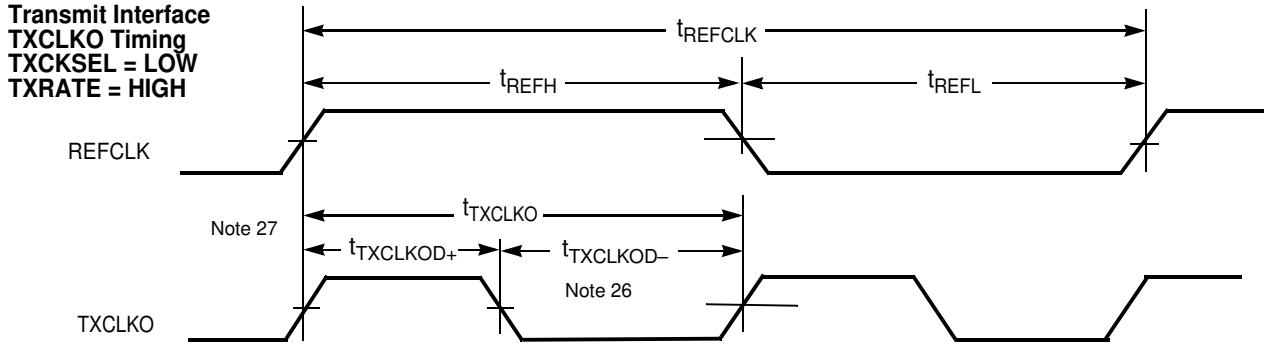
Transmit Interface Write Timing
TXCKSEL = LOW
TXRATE = LOW



Transmit Interface Write Timing
TXCKSEL = LOW
TXRATE = HIGH



Transmit Interface TXCLKO Timing
TXCKSEL = LOW
TXRATE = HIGH



Notes:
25. When REFCLK is configured for half-rate operation (TXRATE = HIGH) and data is captured using REFCLK instead of a TXCLKx clock (TXCKSEL = LOW), data is captured using both the rising and falling edges of REFCLK.
26. The TXCLKO output is at twice the rate of REFCLK when TXRATE = HIGH and same rate as REFCLK when TXRATE = LOW. TXCLKO does not follow the duty cycle of REFCLK.
27. The rising edge of TXCLKO output has no direct phase relationship to the REFCLK input.

CYP15G0401TB HOTLink II Transmitter Switching Waveforms (continued)

Transmit Interface
TXCLKO Timing
TXCKSEL = LOW
TXRATE = LOW

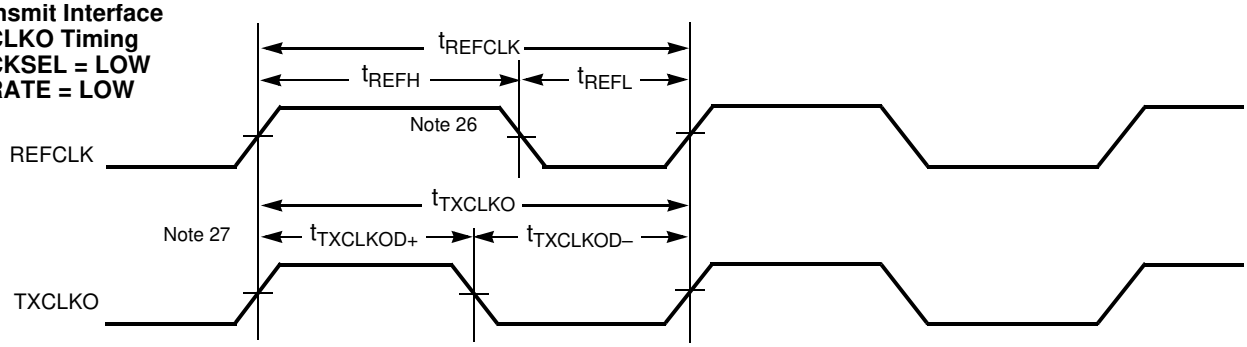


Table 10.Package Coordinate Signal Allocation

Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type
A01	N/C	NO CONNECT	C04	VCC	POWER	E19	VCC	POWER
A02	OUTC1–	CML OUT	C05	VCC	POWER	E20	VCC	POWER
A03	N/C	NO CONNECT	C06	PARCTL	3-LEVEL SEL	F01	TXPERC	LVTTL OUT
A04	OUTC2–	CML OUT	C07	N/C	NO CONNECT	F02	TXOPC	LVTTL IN PU
A05	VCC	POWER	C08	GND	GROUND	F03	TXDC[0]	LVTTL IN
A06	N/C	NO CONNECT	C09	BOE[7]	LVTTL IN PU	F04	N/C	NO CONNECT
A07	OUTD1–	CML OUT	C10	BOE[5]	LVTTL IN PU	F17	BISTLE	LVTTL IN PU
A08	GND	GROUND	C11	BOE[3]	LVTTL IN PU	F18	N/C	NO CONNECT
A09	GND	GROUND	C12	BOE[1]	LVTTL IN PU	F19	N/C	NO CONNECT
A10	OUTD2–	CML OUT	C13	GND	GROUND	F20	N/C	NO CONNECT
A11	GND	GROUND	C14	TXMODE[0]	3-LEVEL SEL	G01	TXDC[7]	LVTTL IN
A12	OUTA1–	CML OUT	C15	GND	GROUND	G02	TXCKSEL	3-LEVEL SEL
A13	GND	GROUND	C16	VCC	POWER	G03	TXDC[4]	LVTTL IN
A14	N/C	NO CONNECT	C17	TXRATE	LVTTL IN PD	G04	TXDC[1]	LVTTL IN
A15	OUTA2–	CML OUT	C18	GND	GROUND	G17	GND	GROUND
A16	VCC	POWER	C19	GND	GROUND	G18	OELE	LVTTL IN PU
A17	N/C	NO CONNECT	C20	TDO	LVTTL 3-S OUT	G19	N/C	NO CONNECT
A18	OUTB1–	CML OUT	D01	TCLK	LVTTL IN PD	G20	N/C	NO CONNECT
A19	N/C	NO CONNECT	D02	$\overline{\text{TRSTZ}}$	LVTTL IN PU	H01	GND	GROUND
A20	OUTB2–	CML OUT	D03	VCC	POWER	H02	GND	GROUND
B01	VCC	POWER	D04	VCC	POWER	H03	GND	GROUND
B02	OUTC1+	CML OUT	D05	VCC	POWER	H04	GND	GROUND
B03	VCC	POWER	D06	VCC	POWER	H17	GND	GROUND
B04	OUTC2+	CML OUT	D07	SPDSEL	3-LEVEL SEL	H18	GND	GROUND
B05	VCC	POWER	D08	GND	GROUND	H19	GND	GROUND
B06	VCC	POWER	D09	BOE[6]	LVTTL IN PU	H20	GND	GROUND
B07	OUTD1+	CML OUT	D10	BOE[4]	LVTTL IN PU	J01	TXCTC[1]	LVTTL IN
B08	GND	GROUND	D11	BOE[2]	LVTTL IN PU	J02	TXDC[5]	LVTTL IN
B09	N/C	NO CONNECT	D12	BOE[0]	LVTTL IN PU	J03	TXDC[2]	LVTTL IN
B10	OUTD2+	CML OUT	D13	GND	GROUND	J04	TXDC[3]	LVTTL IN
B11	N/C	NO CONNECT	D14	TXMODE[1]	3-LEVEL SEL	J17	N/C	NO CONNECT
B12	OUTA1+	CML OUT	D15	GND	GROUND	J18	N/C	NO CONNECT
B13	GND	GROUND	D16	VCC	POWER	J19	N/C	NO CONNECT
B14	GND	GROUND	D17	VCC	POWER	J20	N/C	NO CONNECT
B15	OUTA2+	CML OUT	D18	GND	GROUND	K01	N/C	NO CONNECT
B16	VCC	POWER	D19	N/C	NO CONNECT	K02	N/C	NO CONNECT
B17	VCC	POWER	D20	N/C	NO CONNECT	K03	TXCTC[0]	LVTTL IN
B18	OUTB1+	CML OUT	E01	VCC	POWER	K04	N/C	NO CONNECT
B19	GND	GROUND	E02	VCC	POWER	K17	N/C	NO CONNECT
B20	OUTB2+	CML OUT	E03	VCC	POWER	K18	N/C	NO CONNECT
C01	TDI	LVTTL IN PU	E04	VCC	POWER	K19	N/C	NO CONNECT
C02	TMS	LVTTL IN PU	E17	VCC	POWER	K20	N/C	NO CONNECT
C03	VCC	POWER	E18	VCC	POWER	L01	N/C	NO CONNECT

Table 10.Package Coordinate Signal Allocation (continued)

Ball ID	Signal Name	Signal Type
L02	N/C	NO CONNECT
L03	TXCLKC	LVTTL IN PD
L04	TXDC[6]	LVTTL IN
L17	N/C	NO CONNECT
L18	N/C	NO CONNECT
L19	N/C	NO CONNECT
L20	TXDB[6]	LVTTL IN
M01	N/C	NO CONNECT
M02	N/C	NO CONNECT
M03	N/C	NO CONNECT
M04	N/C	NO CONNECT
M17	TXCTB[1]	LVTTL IN
M18	TXCTB[0]	LVTTL IN
M19	TXDB[7]	LVTTL IN
M20	TXCLKB	LVTTL IN PD
N01	GND	GROUND
N02	GND	GROUND
N03	GND	GROUND
N04	GND	GROUND
N17	GND	GROUND
N18	GND	GROUND
N19	GND	GROUND
N20	GND	GROUND
P01	N/C	NO CONNECT
P02	N/C	NO CONNECT
P03	N/C	NO CONNECT
P04	N/C	NO CONNECT
P17	TXDB[5]	LVTTL IN
P18	TXDB[4]	LVTTL IN
P19	TXDB[3]	LVTTL IN
P20	TXDB[2]	LVTTL IN
R01	N/C	NO CONNECT
R02	N/C	NO CONNECT
R03	TXPERD	LVTTL OUT
R04	TXOPD	LVTTL IN PU
R17	TXDB[1]	LVTTL IN
R18	TXDB[0]	LVTTL IN
R19	TXOPB	LVTTL IN PU
R20	TXPERB	LVTTL OUT
T01	VCC	POWER
T02	VCC	POWER
T03	VCC	POWER
T04	VCC	POWER
T17	VCC	POWER
T18	VCC	POWER
T19	VCC	POWER
T20	VCC	POWER
U01	TXDD[0]	LVTTL IN
U02	TXDD[1]	LVTTL IN
U03	TXDD[2]	LVTTL IN
U04	TXCTD[1]	LVTTL IN
U05	VCC	POWER
U06	N/C	NO CONNECT
U07	N/C	NO CONNECT
U08	GND	GROUND
U09	N/C	NO CONNECT
U10	N/C	NO CONNECT
U11	REFCLK–	PECL IN
U12	TXDA[1]	LVTTL IN
U13	GND	GROUND
U14	TXDA[4]	LVTTL IN
U15	TXCTA[0]	LVTTL IN
U16	VCC	POWER
U17	N/C	NO CONNECT
U18	N/C	NO CONNECT
U19	N/C	NO CONNECT
U20	N/C	NO CONNECT
V01	TXDD[3]	LVTTL IN
V02	TXDD[4]	LVTTL IN
V03	TXCTD[0]	LVTTL IN
V04	N/C	NO CONNECT
V05	VCC	POWER
V06	N/C	NO CONNECT
V07	N/C	NO CONNECT
V08	GND	GROUND
V09	N/C	NO CONNECT
V10	N/C	NO CONNECT
V11	REFCLK+	PECL IN
V12	N/C	NO CONNECT
V13	GND	GROUND
V14	TXDA[3]	LVTTL IN
V15	TXDA[7]	LVTTL IN
V16	VCC	POWER
V17	N/C	NO CONNECT
V18	N/C	NO CONNECT
V19	N/C	NO CONNECT
V20	N/C	NO CONNECT
W01	TXDD[5]	LVTTL IN
W02	TXDD[7]	LVTTL IN
W03	N/C	NO CONNECT
W04	N/C	NO CONNECT
W05	VCC	POWER
W06	N/C	NO CONNECT
W07	N/C	NO CONNECT
W08	GND	GROUND
W09	TXCLKO–	LVTTL OUT
W10	$\overline{\text{TXRST}}$	LVTTL IN PU
W11	TXOPA	LVTTL IN PU
W12	SCSEL	LVTTL IN PD
W13	GND	GROUND
W14	TXDA[2]	LVTTL IN
W15	TXDA[6]	LVTTL IN
W16	VCC	POWER
W17	N/C	NO CONNECT
W18	N/C	NO CONNECT
W19	N/C	NO CONNECT
W20	N/C	NO CONNECT
Y01	TXDD[6]	LVTTL IN
Y02	TXCLKD	LVTTL IN
Y03	N/C	NO CONNECT
Y04	N/C	NO CONNECT
Y05	VCC	POWER
Y06	N/C	NO CONNECT
Y07	N/C	NO CONNECT
Y08	GND	GROUND
Y09	TXCLKO+	LVTTL OUT
Y10	N/C	NO CONNECT
Y11	TXCLKA	LVTTL IN PD
Y12	TXPERA	LVTTL OUT
Y13	GND	GROUND
Y14	TXDA[0]	LVTTL IN
Y15	TXDA[5]	LVTTL IN
Y16	VCC	POWER
Y17	TXCTA[1]	LVTTL IN
Y18	N/C	NO CONNECT
Y19	N/C	NO CONNECT
Y20	N/C	NO CONNECT

X3.230 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data characters are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 eight-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard contain a distinct and easily recognizable bit pattern that assists the receiver in achieving character alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an eight-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the eight-bit byte for the raw eight-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown below.

```
FC-2 bit designation—   7  6  5  4  3  2 1  0
HOTLink D/Q designation—7  6  5  4  3  2 1  0
8B/10B bit designation— H  G  F  E  D  C B  A
```

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character.

```
FC-2  45H
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation, note that the order of bits has been reversed):

```
Data Byte Name  D5.2
      Bits: ABCDE FGH
            10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
      Bits: abcdei fghj
            101001 0101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D, and SC/D = LOW) or a Special Character (c is set to K, and SC/D = HIGH). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7). This definition of the 10-bit Transmission Code is based on the following references.

A.X. Widmer and P.A. Franaszek. “A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code” IBM Journal of Research and Development, 27, No. 5: 440-451 (September, 1983).

U.S. Patent 4,486,739. Peter A. Franaszek and Albert X. Widmer. “Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code” (December 4, 1984).

Fibre Channel Physical and Signaling Interface (ANS X3.230-1994 ANSI FC-PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22-7202).

8B/10B Transmission Code

The following information describes how the tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within any higher-level constructs specified by a standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit “a” is transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order.

Note that bit i is transmitted between bit e and bit f, rather than in alphabetical order.

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters and checking the validity of received Transmission Characters. In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two Transmission Characters. The two columns correspond to the current value of the running disparity. Running disparity is a binary parameter with either a negative (–) or positive (+) value.

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Trans-

mitter calculates a new value for its running disparity based on the contents of the transmitted character. Special Character codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3.230.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver decides whether the Transmission Character is valid or invalid according to the following rules and tables and calculates a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity are used to calculate the new running-disparity value for Transmission Characters that have been transmitted and received.

Running disparity for a Transmission Character is calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other sub-block. Running disparity at the beginning of the six-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the four-bit sub-block is the running disparity at the end of the six-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the four-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the six-bit sub-block if the six-bit sub-block is 000111, and it is positive at the end of the four-bit sub-block if the four-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the six-bit sub-block if the six-bit sub-block is 111000, and it is negative at the end of the six-bit sub-block if the four-bit sub-block is 1100.
3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate entry in *Table 13* for the Valid Data byte or *Table 14* for Special Character byte identify which Transmission Character is to be generated. The current value of the Transmitter's running disparity is used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity is calculated. This new value is used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. *Table 11*shows naming notations and examples of valid transmission characters.

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity is searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the associated Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's validity, the received Transmission Character is used to calculate a new value of running disparity. The new value is used as the Receiver's current running disparity for the next received Transmission Character.

Table 11.Valid Transmission Characters

Data			
	D_{IN} or Q_{OUT}		
Byte Name	765	43210	Hex Value
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
. .	. .	. .	. .
D5.2	010	00101	45
. .	. .	. .	. .
D30.7	111	11110	FE
D31.7	111	11111	FF

Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. *Table 11* shows an example of this behavior.

Table 12.Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

Table 13.Valid Data Characters (TXCTx[0] = 0)

Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj
D0.0	000 00000	100111 0100	011000 1011
D1.0	000 00001	011101 0100	100010 1011
D2.0	000 00010	101101 0100	010010 1011
D3.0	000 00011	110001 1011	110001 0100
D4.0	000 00100	110101 0100	001010 1011
D5.0	000 00101	101001 1011	101001 0100
D6.0	000 00110	011001 1011	011001 0100
D7.0	000 00111	111000 1011	000111 0100
D8.0	000 01000	111001 0100	000110 1011
D9.0	000 01001	100101 1011	100101 0100
D10.0	000 01010	010101 1011	010101 0100
D11.0	000 01011	110100 1011	110100 0100
D12.0	000 01100	001101 1011	001101 0100
D13.0	000 01101	101100 1011	101100 0100
D14.0	000 01110	011100 1011	011100 0100
D15.0	000 01111	010111 0100	101000 1011
D16.0	000 10000	011011 0100	100100 1011
D17.0	000 10001	100011 1011	100011 0100
D18.0	000 10010	010011 1011	010011 0100
D19.0	000 10011	110010 1011	110010 0100
D20.0	000 10100	001011 1011	001011 0100
D21.0	000 10101	101010 1011	101010 0100
D22.0	000 10110	011010 1011	011010 0100
D23.0	000 10111	111010 0100	000101 1011
D24.0	000 11000	110011 0100	001100 1011
D25.0	000 11001	100110 1011	100110 0100
D26.0	000 11010	010110 1011	010110 0100
D27.0	000 11011	110110 0100	001001 1011
D28.0	000 11100	001110 1011	001110 0100
D29.0	000 11101	101110 0100	010001 1011
D30.0	000 11110	011110 0100	100001 1011
D31.0	000 11111	101011 0100	010100 1011

Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj
D0.1	001 00000	100111 1001	011000 1001
D1.1	001 00001	011101 1001	100010 1001
D2.1	001 00010	101101 1001	010010 1001
D3.1	001 00011	110001 1001	110001 1001
D4.1	001 00100	110101 1001	001010 1001
D5.1	001 00101	101001 1001	101001 1001
D6.1	001 00110	011001 1001	011001 1001
D7.1	001 00111	111000 1001	000111 1001
D8.1	001 01000	111001 1001	000110 1001
D9.1	001 01001	100101 1001	100101 1001
D10.1	001 01010	010101 1001	010101 1001
D11.1	001 01011	110100 1001	110100 1001
D12.1	001 01100	001101 1001	001101 1001
D13.1	001 01101	101100 1001	101100 1001
D14.1	001 01110	011100 1001	011100 1001
D15.1	001 01111	010111 1001	101000 1001
D16.1	001 10000	011011 1001	100100 1001
D17.1	001 10001	100011 1001	100011 1001
D18.1	001 10010	010011 1001	010011 1001
D19.1	001 10011	110010 1001	110010 1001
D20.1	001 10100	001011 1001	001011 1001
D21.1	001 10101	101010 1001	101010 1001
D22.1	001 10110	011010 1001	011010 1001
D23.1	001 10111	111010 1001	000101 1001
D24.1	001 11000	110011 1001	001100 1001
D25.1	001 11001	100110 1001	100110 1001
D26.1	001 11010	010110 1001	010110 1001
D27.1	001 11011	110110 1001	001001 1001
D28.1	001 11100	001110 1001	001110 1001
D29.1	001 11101	101110 1001	010001 1001
D30.1	001 11110	011110 1001	100001 1001
D31.1	001 11111	101011 1001	010100 1001

Table 13.Valid Data Characters (TXCTx[0] = 0) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010