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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



General Description

EZ-PD™ CCG3 is a highly integrated USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG3 provides a complete USB Type-C and USB-Power Delivery port control solution for notebooks, dongles, monitors, docking stations and power adapters. CCG3 uses Cypress's proprietary M0S8 technology with a 32-bit, 48-MHz ARM® Cortex®-M0 processor with 128-KB flash, 8-KB SRAM, 20 GPIOs, full-speed USB device controller, a Crypto engine for authentication, a 20V-tolerant regulator, and a pair of FETs to switch a 5V (VCONN) supply, which powers cables. CCG3 also integrates two pairs of gate drivers to control external VBUS FETs and system level ESD protection. CCG3 is available in 40-QFN, 32-QFN, and 42-WLCSP packages.

Features

Type-C and USB-PD Support

- Integrated USB Power Delivery 3.0 support
- Integrated USB-PD BMC transceiver
- Integrated VCONN FETs
- Configurable resistors R_A , R_P and R_D
- Dead Battery Detection support
- Integrated fast role swap and extended data messaging
- Supports one USB Type-C port
- Integrated Hardware based overcurrent protection (OCP) and overvoltage protection (OVP)

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU
- 128-KB Flash
- 8-KB SRAM

Integrated Digital Blocks

- Hardware Crypto block enables Authentication
- Full-Speed USB Device Controller supporting Billboard Device Class
- Integrated timers and counters to meet response times required by the USB-PD protocol
- Four run-time reconfigurable serial communication blocks (SCBs) with reconfigurable I²C, SPI, or UART functionality

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Power

- 2.7 V to 21.5 V operation
- 2x Integrated dual-output gate drivers for external VBUS FET switch control
- Independent supply voltage pin for GPIO that allows 1.71 V to 5.5 V signaling on the I/Os
- Reset: 30 μ A, Deep Sleep: 30 μ A, Sleep: 3.5 mA

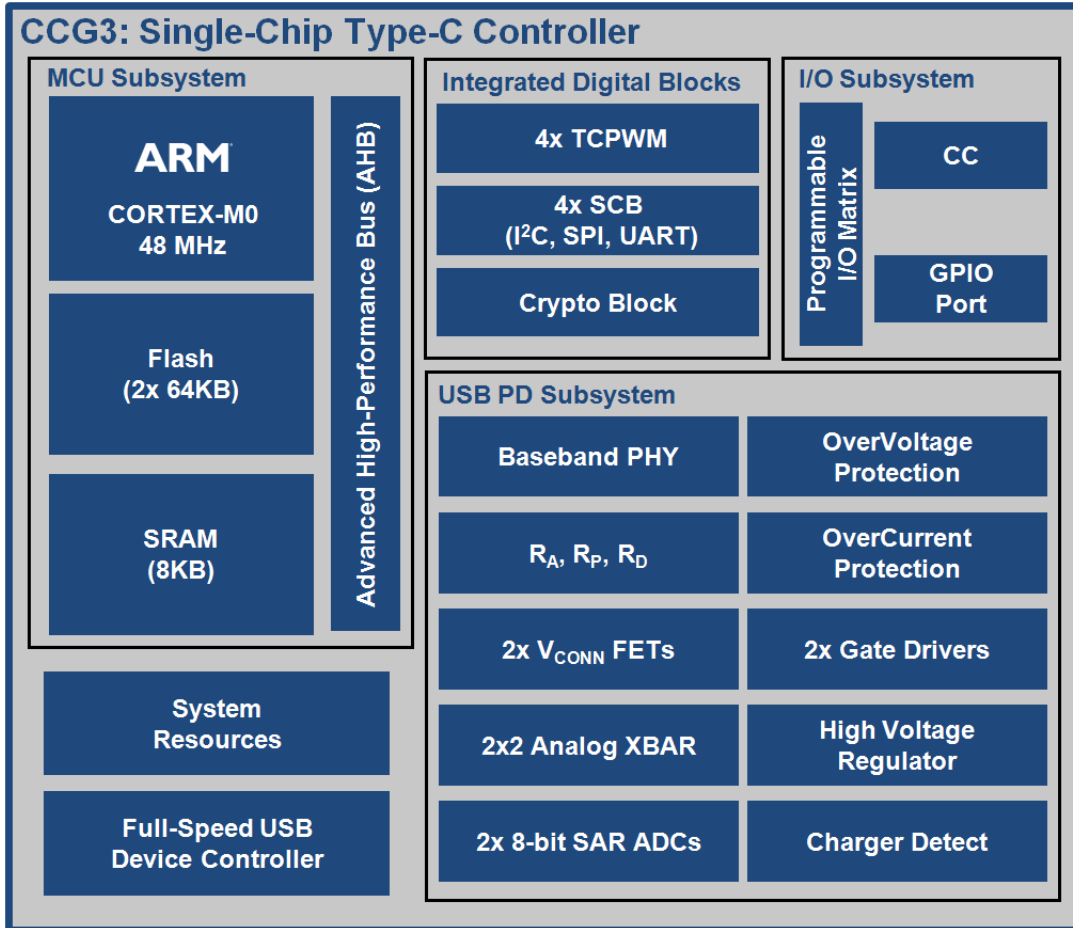
System-Level ESD Protection

- On CC, SBU, DPLUS, DMINUS and VBUS pins
- ± 8 -kV Contact Discharge and ± 15 -kV Air Gap Discharge based on IEC61000-4-2 level 4C

Packages

- 40-pin QFN, 32-pin QFN, and 42-ball CSP for Notebooks/Accessories
- Supports industrial temperature range (-40 °C to $+105$ °C)

Logic Block Diagram

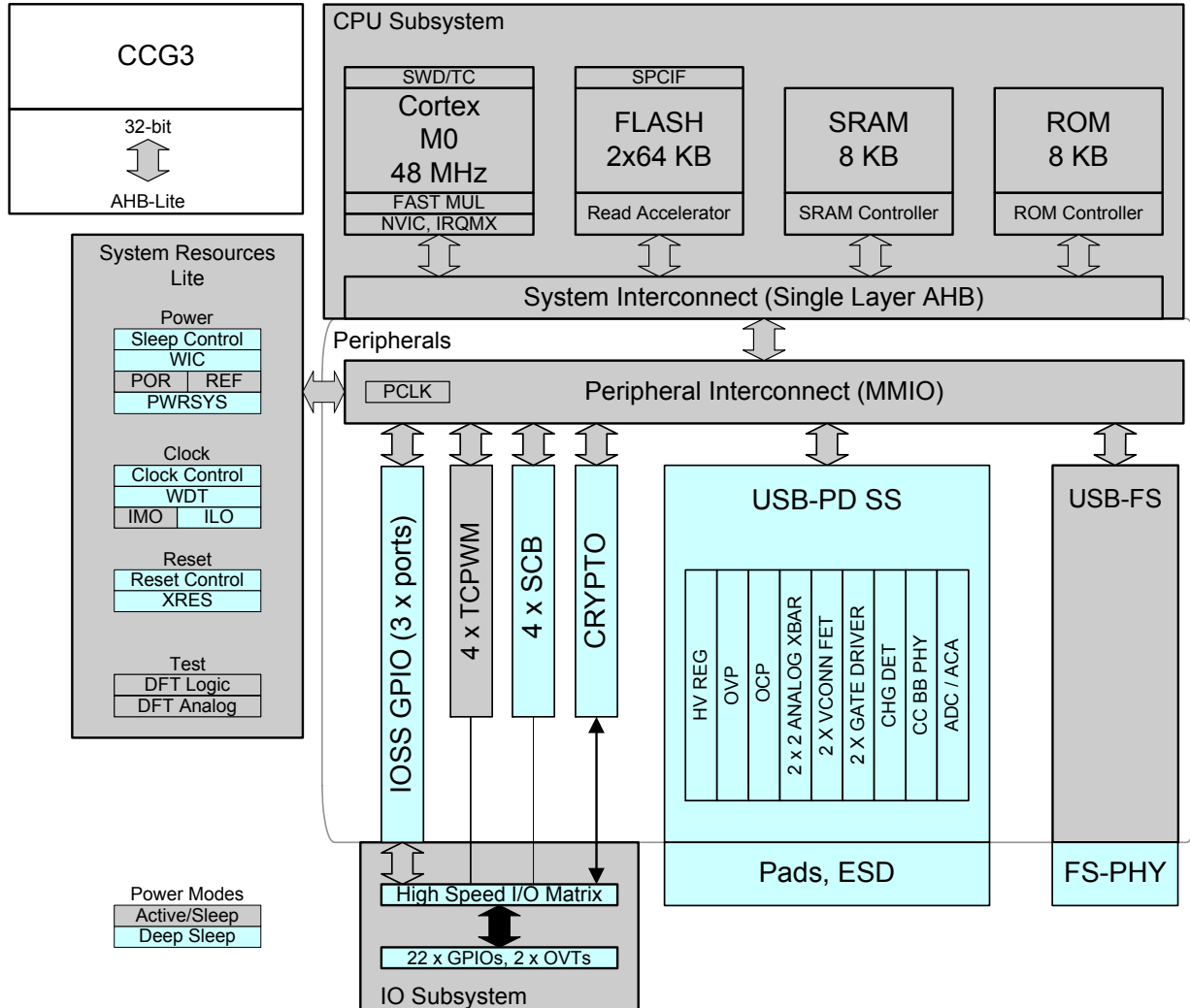


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EZ-PD CCG3 Block Diagram

Figure 1. EZ-PD CCG3 Block Diagram^[1]



Note

1. See [Acronyms](#) section for more details.

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG3 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for EZ-PD CCG3 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG3 device has a flash module with two banks of 64 KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

A supervisory ROM that contains boot and configuration routines is provided.

Crypto Block

CCG3 integrates a crypto block for hardware assisted authentication of firmware images. It also supports field upgradeability of firmware in a trusted ecosystem. The CCG3 Crypto block provides cryptography functionality. It includes hardware acceleration blocks for AES (Advanced Encryption Standard) block cipher, SHA-1 (Secure Hash Algorithm) and SHA-2 hash, Cyclic Redundancy Check (CRC) and pseudo random number generation.

Integrated Billboard Device

CCG3 integrates a complete full speed USB 2.0 device controller capable of functioning as a Billboard class device. The USB 2.0 device controller can also support other device classes.

USB-PD Subsystem (USBPD SS)

The USB-PD sub-system contains all of the blocks related to USB Type-C and Power Delivery. The sub-system is comprised of the following:

- BMC PHY: USB-PD Transceiver with Fast Role Swap (FRS) transmit and detect
- VCONN power FETs for the CC lines
- VCONN Ra Termination and Leakers
- Analog Cross-Bar to switch between the SBU1/SBU2 and AUX_P/AUX_N pins
- Programmable Pull-up and Pull-down termination on the AUX_P/AUX_N pins
- HPD Processor
- VBUS_C Regulator (20V LDO)
- Power Switch between VSYS supply and VBUS_C Regulator output
- VBUS_C Over-Voltage (OV) and Under-Voltage (UV) Detectors
- Current Sense Amplifier (CSA) for over current detection
- Gate Drivers for VBUS_P and VBUS_C external Power FETs
- VBUS_C discharge switch
- USB2.0 Full-Speed (FS) PHY with integrated 5.0V to 3.3V regulator
- Charger Detection / Emulation for USB BC1.2 and other proprietary protocols
- 2 instances of 8-bit SAR ADCs
- 8kV IEC ESD Protection on the following pins: VBUS_C, CC1, CC2, SBU1, SBU2, DP, DM

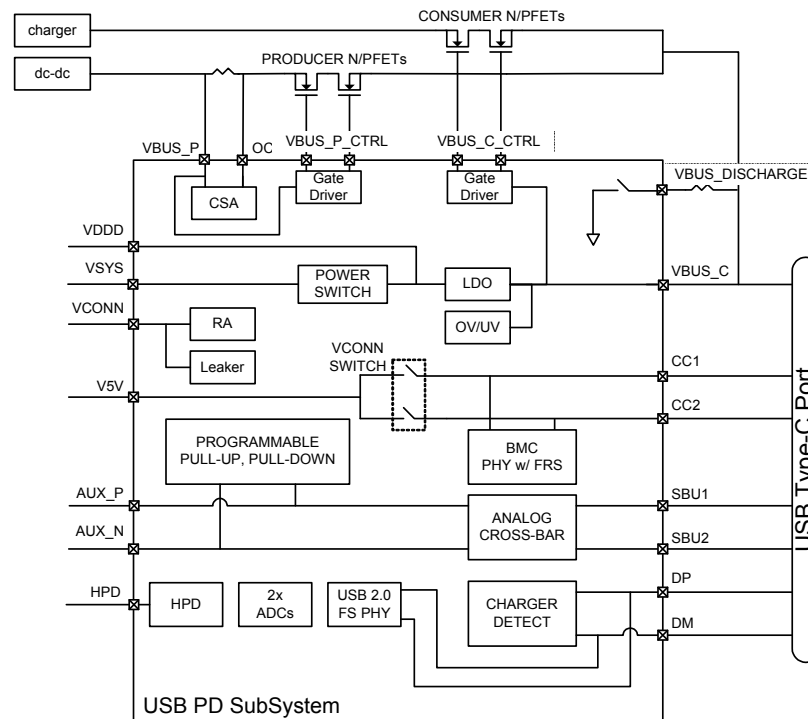
The EZ-PD™ CCG3 USB-PD subsystem interfaces to the pins of a USB Type-C connector. It includes a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as integrating the 1.2V analog front end. This subsystem integrates the required terminations to identify the role of the CCG3 device, including Rp and Rd for UFP/DFP roles and Ra for EMCA/VCONN powered accessories. The programmable VCONN leakers are included in order to discharge VCONN capacitance during a disconnect event. It also integrates power FETs for supplying VCONN power to the CC1/CC2 pins from the V5V pin. The Analog Cross-Bar allows for connecting either of the SBU1/SBU2 pins to either of the AUX_P/AUX_N pins to support DisplayPort sideband signaling. The integrated HPD processor can be used to control or monitor the HPD signal of a DisplayPort source or sink.

The OV/UV (Over-Voltage/Under-Voltage) block monitors the VBUS_C supply for programmable over-voltage and under-voltage conditions. The CSA amplifies the voltage across an external sense resistor, which is proportional to the current being drawn from the external DC-DC VBUS supply converter. The CSA output can either be measured with an ADC or configured to detect an over-current condition. The VBUS_P and VBUS_C gate drivers control the gates of external power FETs for the VBUS_C and VBUS_P supplies. The gate drivers can be configured to support both P and N type external power FETs. The gate drivers are configured by default for nFET devices. In applications using pFETs, the gate drivers must be appropriately configured. The OV/UV and CSA blocks can generate interrupts to automatically turn off the power FETs for the programmed over-voltage and over-current conditions. The VBUS_C

discharge switch allows for discharging the VBUS_C line through an external resistor.

The USB-PD sub-system also contains two 8-bit Successive Approximation Register (SAR) ADCs for analog to digital conversions. Each ADC includes an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage and an internal voltage proportional to the absolute temperature. Each GPIO pin can be connected to the global Analog Multiplex Busses through a switch, which allows either ADC to sample the pin voltage. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDD or VDDIO supply values.

Figure 2. USB-PD Subsystem



Full-Speed USB Subsystem

The FSUSB subsystem contains a full speed USB device controller as described in the [Integrated Billboard Device](#) section.

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG3 has four SCBs, which can be configured to implement an I²C, SPI, or UART interface. The hardware I²C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I²C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I²C that creates a mailbox address range in the memory of EZ-PD CCG3 and effectively reduce I²C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I²C peripherals are compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual ([UM10204](#)).

The I²C bus I/Os are implemented with GPIO in open-drain modes.

The I²C port on SCB 1-3 blocks of EZ-PD CCG3 are not completely compliant with the I²C specification in the following aspects:

- The GPIO cells for SCB 1's I²C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG3 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality.

GPIO

EZ-PD CCG3 has up to 20 GPIOs (these GPIOs can be configured for GPIOs, SCB, SBU, and Aux signals) and SWD pins, which can also be used as GPIOs. The I²C pins from SCB 0 are overvoltage-tolerant.

The GPIO block implements the following:

- Seven drive strength modes:
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Power Systems Overview

Figure 3 shows an overview of the power system requirement for CCG3. CCG3 shall be able to operate from two possible external supply sources VBUS (4.0 V–21.5 V) or VSYS (2.7 V–5.5 V). The VBUS supply is regulated inside the chip with a low-dropout regulator (LDO) down to 3.3 V level. The chip’s internal VDDD rail is intelligently switched between the output of the VBUS regulator and unregulated VSYS. The switched supply, VDDD is either used directly inside some analog blocks or further regulated down to VCCD which powers majority of the core using

regulators. Besides Reset mode, CCG3 has three different power modes: Active, Sleep and Deep Sleep, transitions between which are managed by the Power System. A separate power domain VDDIO is provided for the GPIOs. The VDDD and VCCD pins, both the output of regulators are brought out for connecting a 1-μF capacitor for the regulator stability only. These pins are not supported as power supplies. When CCG3 is powered from VSYS that is greater than 3.3 V, the dedicated USB regulator allows USB operation.

Figure 3. EZ-PD CCG3 Power System Block Diagram

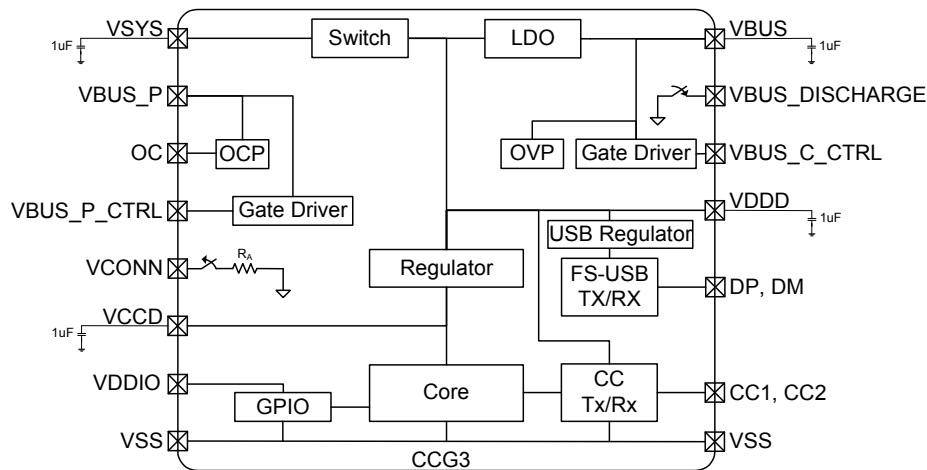


Table 1. CCG3 Power Modes

Mode	Description
RESET	Power is Valid and XRES is not asserted. An internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is Valid and CPU is executing instructions.
SLEEP	Power is Valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.

Pinouts

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN and 40-QFN Devices

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
A5	N/A	1	VBUS_P_CTRL1	VBUS Gate Driver Control 1 for Producer Switch
A6	1	2	VBUS_P_CTRL0	VBUS Gate Driver Control 0 for Producer Switch
B6	2	3	CC2	USB PD connector detect/Configuration Channel 2
C5	N/A	N/A	CC2	USB PD connector detect/Configuration Channel 2
D4	3	4	V5V	5.0V – 5.5V supply for VCONN FETs
C6	4	5	CC1	USB PD connector detect/Configuration Channel 1
D6	N/A	N/A	CC1	USB PD connector detect/Configuration Channel 1
E6	N/A	6	VCONN	VCONN Input - provides Ra termination for cable applications
F6	5	7	P1.0	GPIO/UART_2_TX / SPI_2_MISO
D5	N/A	8	P1.1	GPIO/UART_2_RX / SPI_2_SEL
E5	6	9	P1.2	GPIO/UART_0_RX/ UART_3_CTS/ SPI_3_MOSI/ I2C_3_SCL / HPD
G6	7	10	P1.3	GPIO/UART_0_TX/ UART_3_RTS/ SPI_3_CLK/ I2C_3_SDA
E4	N/A	11	AUX_P / P1.6	DisplayPort AUX_P signal / GPIO / UART_1_TX / SPI_1_MISO
F5	8	12	SBU1 / P1.4	USB Type-C SBU1 signal / GPIO / UART_3_TX/ SPI_3_MISO/ SWD_1_CLK
G5	9	13	SBU2 / P1.5	USB Type-C SBU2 signal / GPIO / UART_3_RX/ SPI_3_SEL/ SWD_1_DAT
G4	N/A	14	AUX_N / P1.7	DisplayPort AUX_N signal / GPIO / UART_1_RX / SPI_1_SEL
F4	10	15	P2.0	GPIO / UART_1_CTS / SPI_1_CLK/ I2C_1_SCL / SWD_0_DAT
G3	11	16	P2.1	GPIO / UART_1_RTS / SPI_1_MOSI/ I2C_1_SDA / SWD_0_CLK
G2	13	17	VDDD	VDDD Supply Input / Output (2.7 V–5.5 V)
F3	14	18	VDDIO	1.71 V–5.5 V supply for I/Os. This supply also powers the global analog multiplex buses.
F2	15	19	VCCD	1.8V regulator output for filter capacitor
G1	16	20	VSYS	System Power Supply (2.7 V–5.5 V)
F1	17	21	DPLUS	USB 2.0 DP
E1	18	22	DMINUS	USB 2.0 DM
E2	19	23	P2.4	GPIO
D3	20	24	P2.5	GPIO / UART_0_TX/ SPI_0_MOSI
D2	N/A	25	P2.6	GPIO / UART_0_RX/ SPI_0_CLK
D1	21	26	XRES	External Reset Input. Internally pulled-up to VDDIO.
C3	22	27	P0.0	I2C_0_SDA / GPIO_OVT / UART_0_CTS / SPI_0_SEL/ TCPWM0
C2	23	28	P0.1	I2C_0_SCL / GPIO_OVT / UART_0_RTS / SPI_0_MISO/ TCPWM1

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN and 40-QFN Devices (continued)

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
C1	N/A	29	VBUS_C_CTRL1	VBUS Gate Driver Control 1 for Consumer Switch
C4	24	30	VBUS_C_CTRL0	VBUS Gate Driver Control 0 for Consumer Switch
B1	25	31	VBUS	VBUS Input
A1	26	32	VBUS_DISCHARGE	VBUS Discharge Control output
E3	12, 27	33	VSS	Ground Supply (GND)
	EPAD	EPAD	VSS	
A2	28	34	P3.2	GPIO / TCPWM0
B2	N/A	35	P3.3	GPIO / TCPWM1
B3	29	36	P3.4	GPIO / UART_2_CTS / SPI_2_MOSI / I2C_2_SDA / TCPWM2
A3	30	37	P3.5	GPIO / UART_2_RTS / SPI_2_CLK / I2C_2_SCL / TCPWM3
B4	N/A	38	P3.6	GPIO
A4	31	39	OC	Over-current Sensor Input
B5	32	40	VBUS_P	VBUS Producer Input

Figure 4. Pinout of 40-QFN Package (Top View)

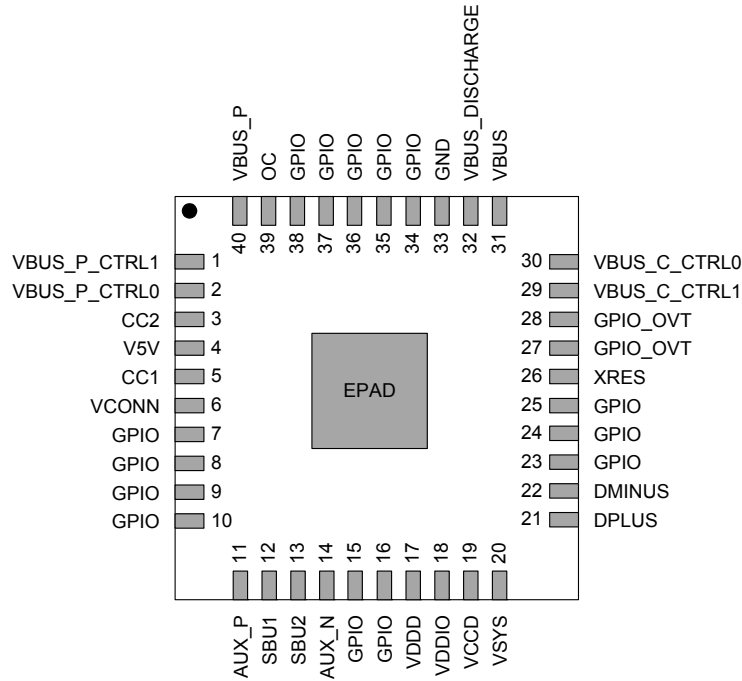


Figure 5. Pinout of 32-QFN Package (Top View)

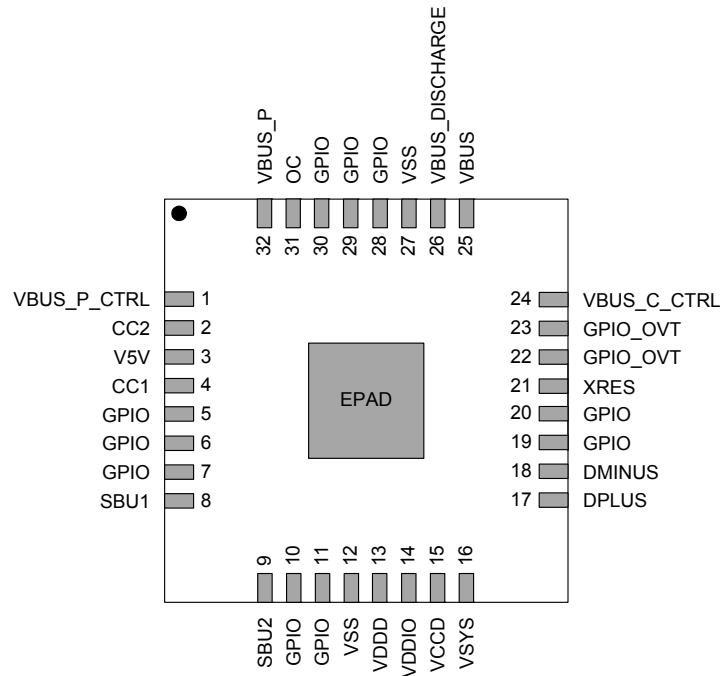
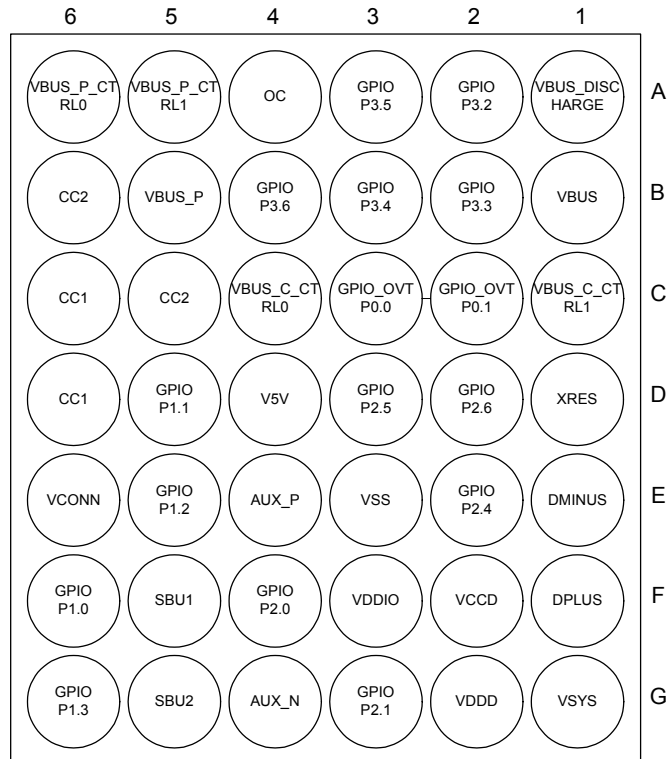


Figure 6. Pinout of 42-WLCSP Bottom (Balls Up) View



Available Firmware and Software Tools

EZ-PD Configuration Utility

The EZ-PD Configuration Utility is a GUI-based Microsoft Windows application developed by Cypress to guide a CCGx user through the process of configuring and programming the chip. The utility allows users to:

1. Select and configure the parameters they want to modify
2. Program the resulting configuration onto the target CCGx device.

The utility works with the Cypress supplied CCG1, CCG2, CCG3, and CCG4 kits, which host the CCGx controllers along with a USB interface. This version of the EZ-PD Configuration Utility supports configuration and firmware update operations on CCGx controllers implementing EMCA and Display Dongle applications. Support for other applications, such as Power Adapters and Notebook port controllers, will be provided in later versions of the utility.

You can download the EZ-PD Configuration Utility and its associated documentation at the following link:

<http://www.cypress.com/documentation/software-and-drivers/ez-pd-configuration-utility>

CCG3 Programming and Bootloading

There are two ways to program application firmware into a CCG3 device:

1. Programming the device flash over SWD Interface
2. Application firmware update over specific interfaces (CC, USB, I²C)

Generally, the CCG3 devices are programmed over SWD interface only during development or during the manufacturing process of the end product. Once the end product is manufactured, the CCG3 device's application firmware can be updated via the appropriate bootloader interface.

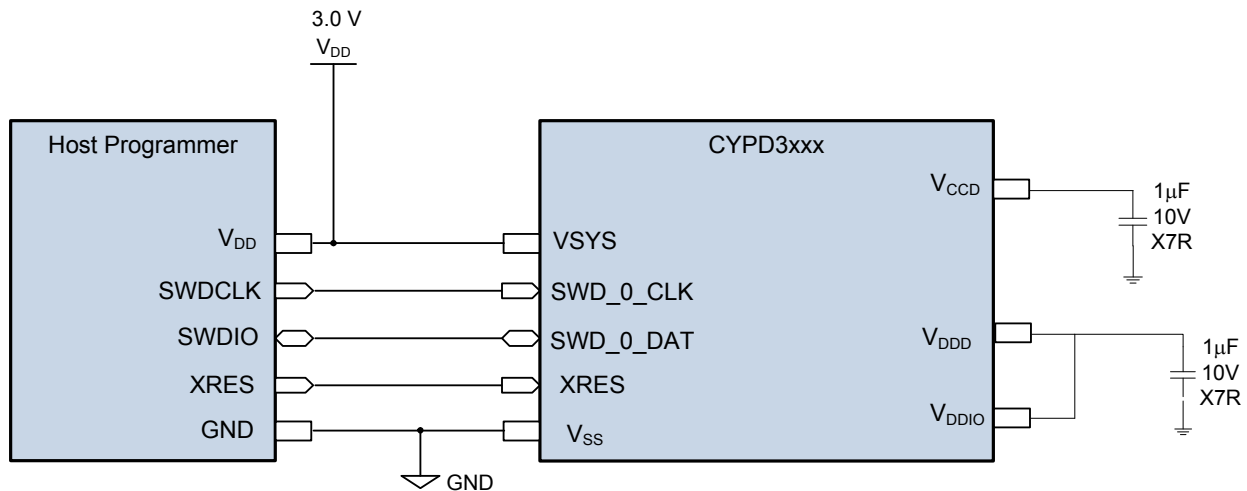
Programming the Device Flash over SWD Interface

CCG3 family of devices can be programmed using the SWD interface. Cypress provides a programming kit ([CY8CKIT-002 MiniProg3 Kit](#)) called MiniProg3 which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in [PSoC Creator Software](#). Click [here](#) for more information on how to use the MiniProg3 programmer. There are many third party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in [Figure 7](#), the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VSYS pin of CCG3 device. If the CCG3 device is powered using an on-board power supply, it can be programmed using the “Reset Programming” option. For more details, refer to the [CYPD3XXX Programming Specifications](#).

The CYPD3105 device for Thunderbolt cable applications is pre-programmed with a micro-bootloader that allows users to program the flash using the alternate SWD pins (SBU1 for SWD_1_CLK and SBU2 for SWD_1_DAT) that can be connected to the SBU interface of a Type-C connector. Note that this interface can be used to program the flash only once. Subsequent re-programming of this device can be done through the primary SWD interface (SWD_0_CLK and SWD_0_DAT pins). Irrespective of which SWD interface is used for programming the device, once the device is programmed with the hex file provided by Cypress for thunderbolt cable application, subsequent updates to the application firmware can be done over the CC line. Refer to [Application Firmware Update over Specific Interfaces \(I²C, CC, USB\)](#) for more details.

Figure 7. Connecting the Programmer to CYPD3xxx Device



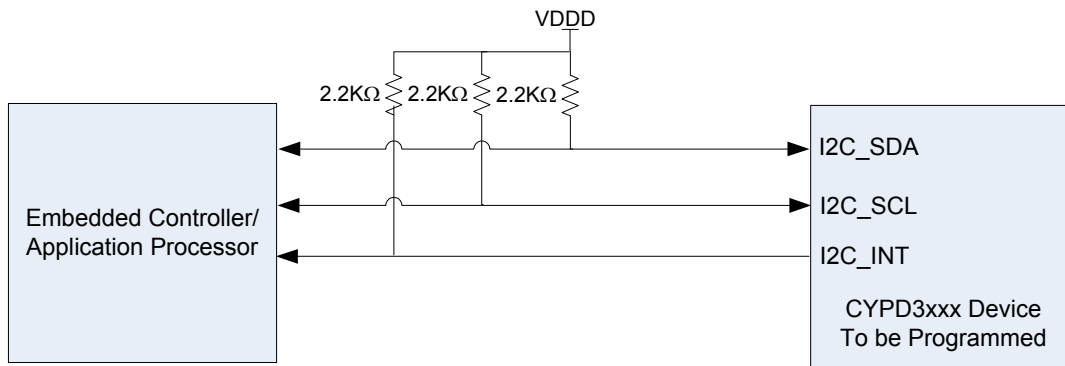
Application Firmware Update over Specific Interfaces (I²C, CC, USB)

The application firmware can be updated over three different interfaces depending on the default firmware programmed into the CCG3 device. Refer to [Table 38](#) for more details on default firmware that various part numbers of the CCG3 family of devices are pre-programmed with (Note that some of the devices have bootloader only and some have bootloader plus application firmware). The application firmware provided by Cypress for all CCG3 applications have dual images. This allows fail-safe update of the alternate image while executing from the current image. For more information, refer to the [EZ-PD Configuration Utility User Manual](#).

Application Firmware Update over I²C Interface

This method primarily applies to CYPD3122, CYPD3125 and CYPD3126 devices of the CCG3 family. In these applications, the CCG3 device interfaces to an on-board application processor or an embedded controller over I²C interface. Refer to [Figure 8](#) for more details. Cypress provides pseudo-code for the host processor for updating the CCG3 device firmware.

Figure 8. Application Firmware Update over I²C Interface

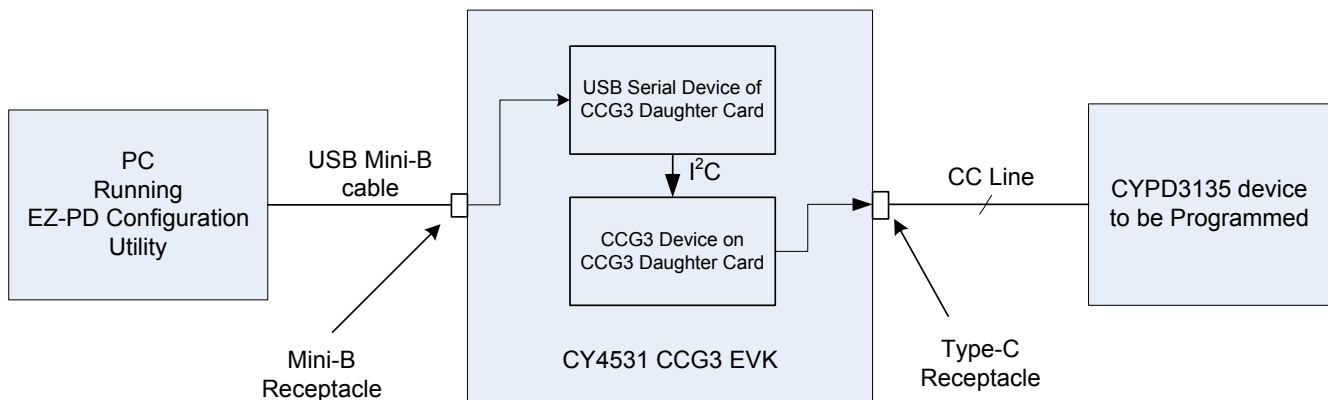


Application Firmware Update over CC Line

This method primarily applies to CYPD3135 device of the CCG3 family. In these applications, the CY4531 CCG3 EVK can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The

CY4531 CCG3 EVK is connected to the system containing CCG3 device on one end and a Windows PC running the EZ-PDTM Configuration Utility as shown in Figure 9 on the other end to program the CCG3 device.

Figure 9. Application Firmware Update over CC Line



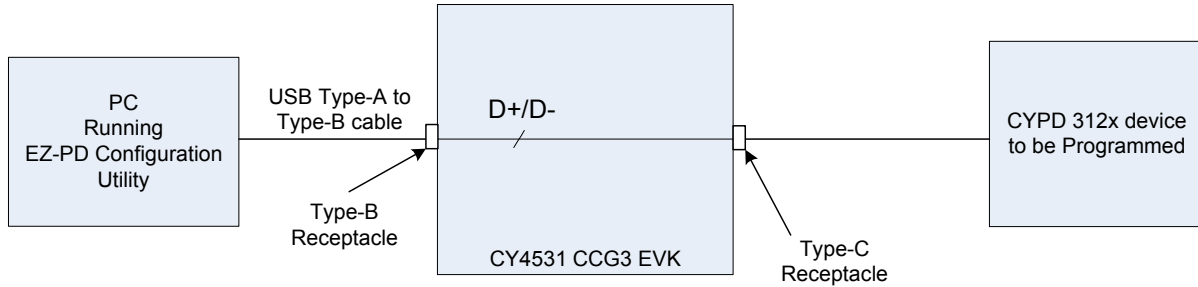
Application Firmware Update over USB

This method primarily applies to the CYPD3120 and CYPD3121 devices of the CCG3 family. In these applications, the firmware update can be performed over the D+/D- lines (USB2.0) using various possible options as shown in Figure 10. Option 1 is to have a Windows PC running EZ-PD™ Configuration Utility connected to the device to be programmed via the CY4531

CCG3 EVK. This setup can be avoided using option 2, where the user has a Type-A to Type-C cable. This option requires that the system contain the CCG3 device to be programmed to have a Type-C receptacle. The other option (Option 3) is to have a Windows PC with a native Type-C connector as shown in Figure 10.

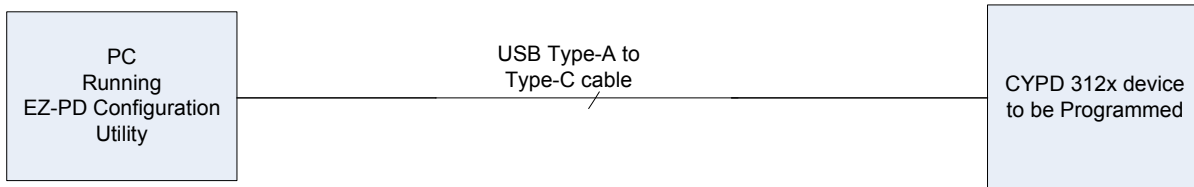
Figure 10. Application Firmware Update over USB

Option 1



OR

Option 2



OR

Option 3



Applications

Figure 11 illustrates the application diagram of a power adapter using a CCG3 device. In this application, CCG3 is used as DFP (power provider) only. The maximum power profile that can be supported by power adapters is up to 20 V, 100 W using 40-pin QFN CCG3 devices. CCG3 has the ability to drive both types of FETs and the state of GPIO P1.0 (floating or grounded) indicates the type of FET (N-MOS or P-MOS FET) being used in the power provider path.

CCG3 integrates all termination resistors and uses GPIOs (VSEL0 and VSEL1) to indicate the negotiated power profile. If required, the power profile can also be selected using CCG3 serial interfaces (I²C, SPI) or PWM. The VBUS voltage on the Type-C port is monitored using internal circuits to detect under-voltage and overvoltage conditions. To ensure quick discharge of VBUS when the power adapter cable is detached, a discharge path is provided with a resistor connected to the VBUS_DISCHARGE pin of the CCG3 device.

Overcurrent protection is enabled by sensing the current through the 10-mΩ sense resistor using the “OC” and “VBUS_P” pins of the CCG3 device. The VBUS provider through the Type-C connector can be turned on or off using the provider path FETs. The power provider FETs are controlled by high-voltage gate driver outputs (VBUS_P_CTRL0 and VBUS_P_CTRL1 pins of CCG3 device). The CCG3 device is also capable of supporting proprietary charging protocols over the DP and DM lines of the Type-C receptacle. By providing a 5-V source at the V5V pin of the CCG3 device, the device becomes capable of delivering the VCONN supply over either the CC1 or CC2 pins of the Type-C connector.

Figure 11. Power Adapter Application Diagram (40-QFN Device)

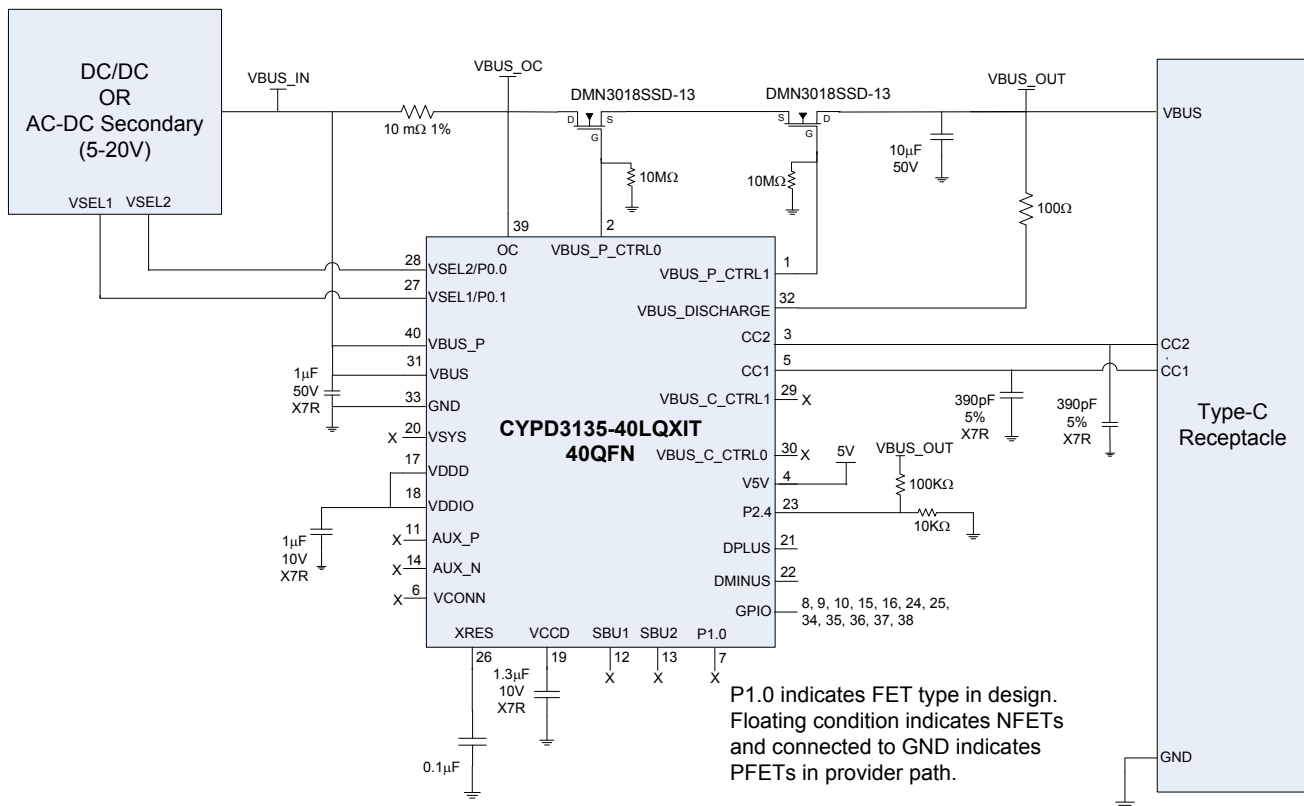


Figure 12 illustrates a power bank application diagram using a CCG3 device. In this application, the Type-C receptacle is used for providing as well as consuming power. The consumer path will be active when the battery is charged using a Type-C power source that is connected to the Type-C receptacle in Figure 12. The provider path will be active when the power bank is used for providing power to a sink device connected to the Type-C receptacle. Additionally, a Type-A receptacle can also be provided for providing power to the sinks that have a legacy USB interface.

The CCG3 device negotiates power contracts between the power bank and the sink/source device connected to the Type-C receptacle. The CCG3 device also controls and drives the provider and consumer path FETs and can monitor overcurrent and overvoltage conditions on the Type-C VBUS line.

Figure 12. Power Bank Application Diagram (40-QFN Device)

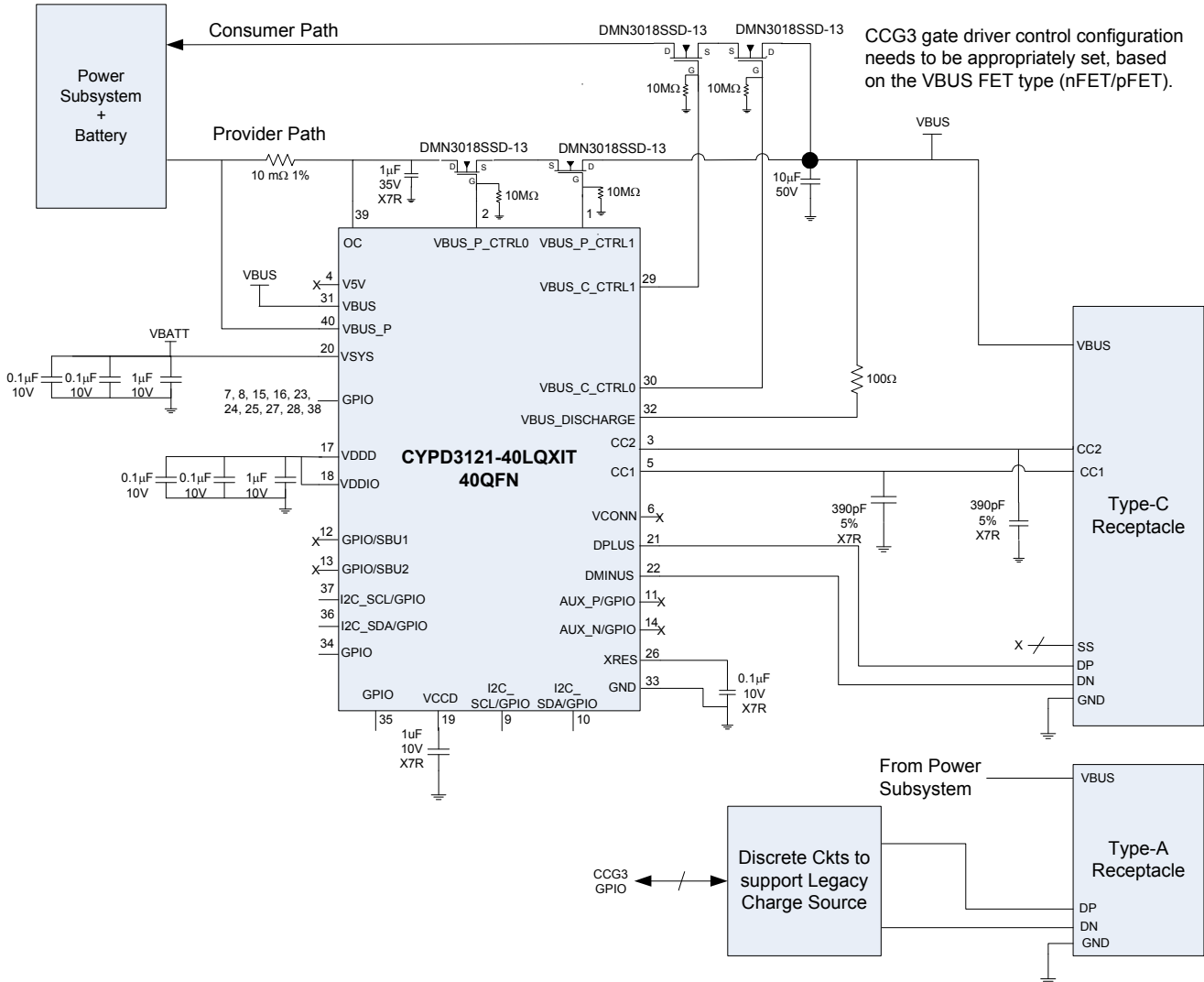


Figure 13 illustrates a USB Type-C to DisplayPort (4-lane) adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has a DisplayPort interface.

The application meets the requirements described in Section 4.2 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0 (Scenarios 2a and 2b USB Type-C to DisplayPort Cables).

Figure 13. USB Type-C to DisplayPort Adapter Application Diagram

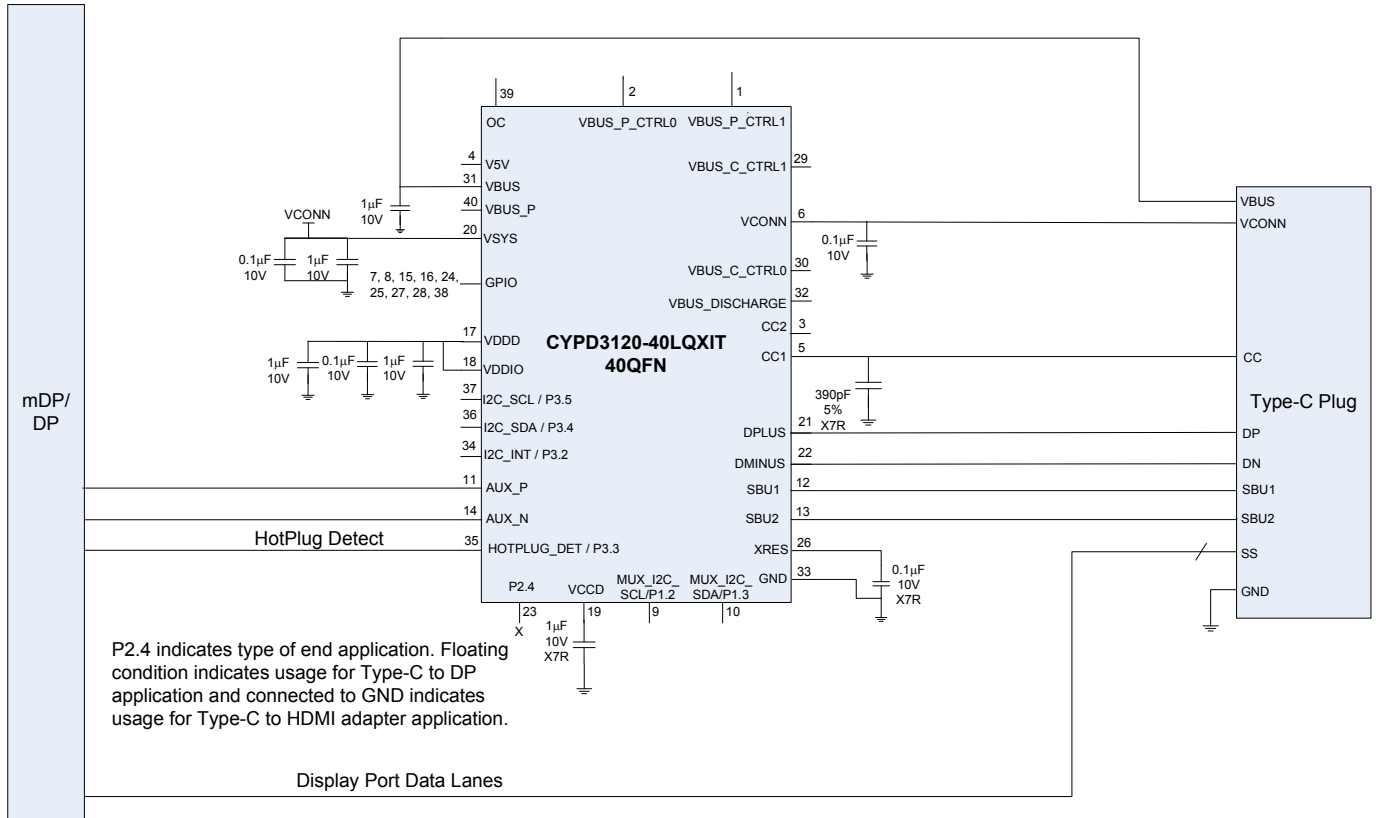


Figure 14 illustrates a USB Type-C to HDMI adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has HDMI interface. It enables users of any Notebook that implements USB-Type C to connect to other display types.

This application meets the requirements described in Section 4.3 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0. This application supports display output at a resolution of up to 4K Ultra HD (3840x2160) at 60 Hz.

Figure 14. USB Type-C to HDMI Adapter Application

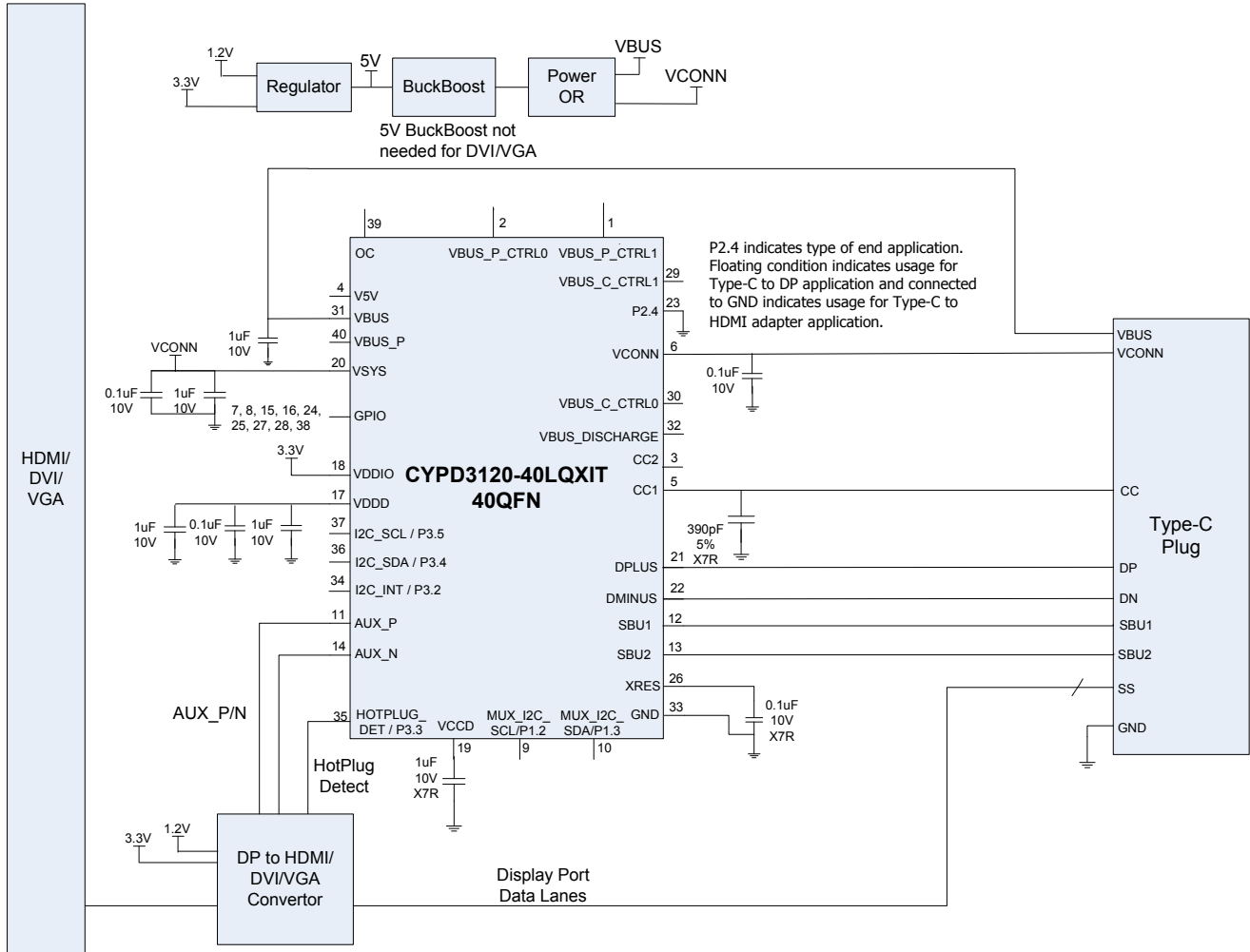


Figure 15 illustrates a Notebook DRP application diagram using a CCG3 device. The Type-C port can be used as a power provider or a power consumer. The CCG3 device communicates with the embedded controller (EC) over I²C. It also controls the Data Mux to route the HighSpeed signals either to the USB

chipset (during normal mode) or the DisplayPort Chipset (during Alternate Mode). The SBU, SuperSpeed, and HighSpeed lines are routed directly from the Display Mux of the notebook to the Type-C receptacle.

Figure 15. DRP Application Diagram

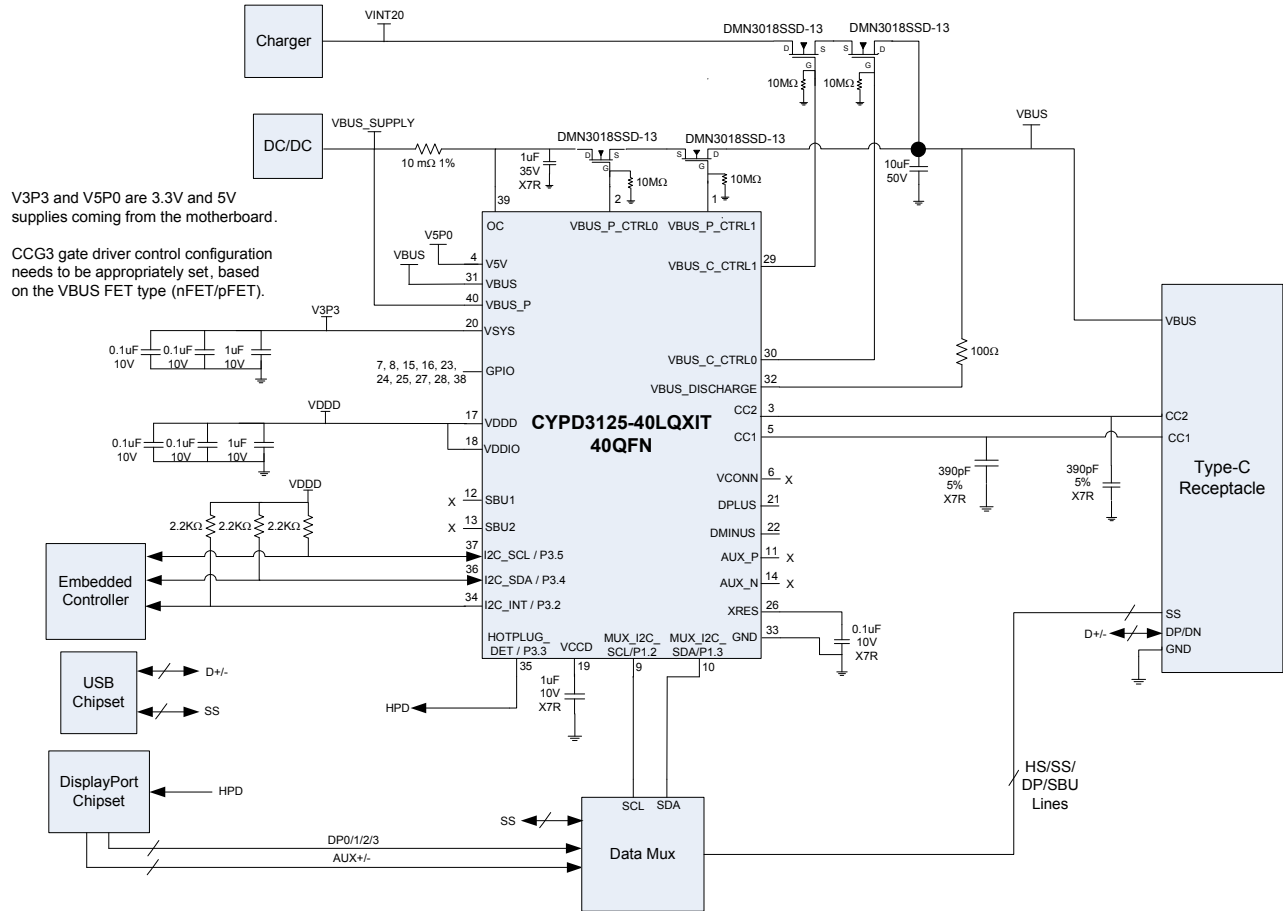
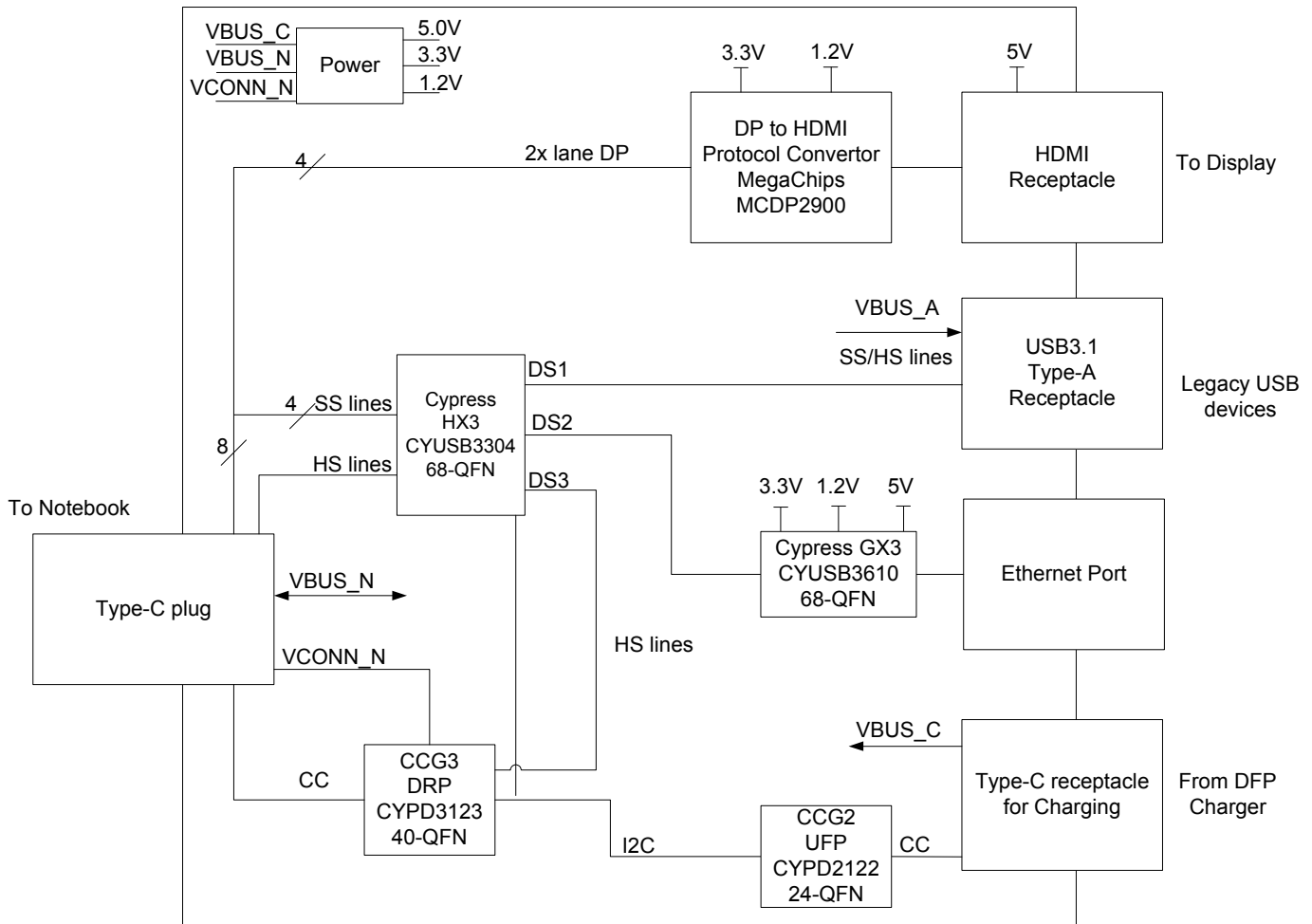


Figure 16 illustrates a CCG3 device based Charge-through Dongle application block diagram. This Charge-through dongle application also implements Cypress's USB SuperSpeed Hub controller HX3 (CYUSB3304-68LTXI) available in 68-QFN package, Low-power single chip USB 3.0 to Gigabit Ethernet Bridge Controller GX3 (CYUSB3610-68LTXC) available in 68-QFN package and the CCG2 (CYPD2122-24LQXI) which acts as an Upstream Facing Port (UFP) and sinks power when connected to USB Type-C chargers.

This application enables connectivity between a USB Type-C Notebook and HDMI Display, legacy USB device and Gigabit Ethernet while also connecting a USB Type-C charging cable. The Charge-Through Dongle solution allows simultaneous HDMI display, Superspeed data transfers, Ethernet connection and charging of a USB Type-C Notebook. Charge-Through Dongle is also widely known as Multiport Adapter. More details including the schematic of the CCG3 device based Charge-through Dongle reference design can be found [here](#).

Figure 16. Charge-through Dongle Application Block Diagram (40-QFN Device)



Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V _{SYS_MAX}	Digital supply relative to V _{SS}	-0.5	-	6	V	Absolute max
V _{5V}	Max supply voltage relative to V _{SS}	-	-	6	V	
V _{BUS_MAX_ON}	Max supply voltage relative to V _{SS} , V _{BUS} regulator enabled	-	-	26	V	
V _{BUS_MAX_OFF}	Max supply voltage relative to V _{SS} , V _{BUS} regulator enabled 100% of the time	-	-	24.5	V	
	Max supply voltage relative to V _{SS} , V _{BUS} regulator enabled 25% of the time	-	-	26	V	
V _{DDIO_MAX}	Max supply voltage relative to V _{SS}	-	-	6	V	
V _{GPIO_ABS}	GPIO voltage	-0.5	-	V _{DDIO} + 0.5	V	
V _{GPIO_OVT_ABS}	OVT GPIO voltage	-0.5	-	6	V	
I _{GPIO_ABS}	Maximum current per GPIO	-25	-	25	mA	
V _{CONN_MAX}	Max voltage relative to V _{SS}	-	-	6	V	
V _{CC_ABS}	Max voltage on CC1 and CC2 pins	-	-	6	V	
I _{GPIO_INJECTION}	GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS}	-0.5	-	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	-	-	V	-
ESD_CDM	Electrostatic discharge charged device model	500	-	-	V	-
LU	Pin current for latch-up	-100	-	100	mA	Tested at 125 °C
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	-	-	V	Contact discharge on CC1, CC2, V _{BUS} , DPLUS, DMINUS, SBU1 and SBU2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	-	-	V	Air discharge for CC1, CC2, V _{BUS} , DPLUS, DMINUS, SBU1 and SBU2 pins

Device-Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ and $T_J \leq 120\text{ }^{\circ}\text{C}$, except where noted.

Table 4. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	VSYS	–	2.7	–	5.5	V	UFP Mode.
SID.PWR#1_A	VSYS	–	3	–	5.5	V	DFP/DRP or Gate Driver Modes
SID.PWR#23	VCONN	Power Supply Input Voltage	2.7	–	5.5	V	–
SID.PWR#13	VDDIO	IO Supply Voltage	1.71	–	5.5 ^[2]	V	$2.7\text{V} < V_{DDD} < 5.5\text{V}$
SID.PWR#13_A	VDDIO	IO Supply Voltage for ADC operation	2.7	–	5.5	V	$2.7\text{V} < V_{DDD} < 5.5\text{V}$
SID.PWR24	VCCD	Output Voltage for core Logic	–	1.8	–	V	–
SID.PWR#4	IDD	Supply current	–	25	–	mA	From VSYS or VBUS VBUS = 5V, $T_A = 25\text{ }^{\circ}\text{C}$ / VSYS = 5 V, $T_A = 25\text{ }^{\circ}\text{C}$ FS USB, CC IO in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, CPU at 24 MHz.
SID.PWR#1_B	VSYS	Power supply for USB operation	4.5	–	5.5	V	USB configured, USB Regulator enabled
SID.PWR#1_C	VSYS	Power supply for USB operation	3.15	–	3.45	V	USB configured, USB Regulator disabled
SID.PWR#1_D	VSYS	Power supply for charger detect/emulation operation	3.15	–	5.5	V	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ T_A
SID.PWR#27	VBUS	Power supply input voltage	3.5	–	21.5	V	FS USB disabled. Total current consumption from VBUS <15 mA.
SID.PWR#28	VBUS	Power supply input voltage for USB operation	4.5	–	21.5	V	FS USB configured, USB Regulator disabled
SID.PWR#30	VBUS_P	Power supply input voltage	4.00	–	21.5	V	
SID.PWR#15	C _{efc}	External regulator voltage bypass for VCCD	1	1.3	1.6	μF	X5R ceramic or better
SID.PWR#16	C _{exc}	Power supply decoupling capacitor for VSYS	0.8	1	–	μF	X5R ceramic or better
Sleep Mode. VSYS = 2.7 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and T_A = 25 °C.							
SID25A	I _{DD20A}	CC, I ² C, WDT wakeup on. IMO at 48 MHz.	–	3.5	–	mA	VSYS = 3.3 V, $T_A = 25\text{ }^{\circ}\text{C}$, All blocks except CPU are on, CC IO on, USB in Suspend Mode, no I/O sourcing current
Deep Sleep Mode							
SID_DS	I _{DD_DS}	VSYS = 3.0 to 3.6 V. CC Attach, I ² C, WDT Wakeup on.	–	30	–	μA	Power Source = VSYS, DFP Mode, Type-C Not Attached. CC Attach, I ² C and WDT enabled for Wakeup.
XRES Current							
SID307	I _{DD_XR}	Supply current while XRES asserted. This does not include current drawn due to the XRES internal pull-up resistor.	–	30	–	μA	Power Source = VSYS = 3.3 V, Type-C device not attached, $T_A = 25\text{ }^{\circ}\text{C}$

Note

2. If VDDIO > VDDD, GPIO P2.4 cannot be used. It must be left unconnected. See Table 2 for pin numbers.

Table 5. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F _{CPU}	CPU input frequency	DC	–	48	MHz	All VDDD
SID.PWR#20	T _{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#21	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	–	–	35	µs	–
SID.XRES#5	T _{XRES}	External reset pulse width	5	–	–	µs	All VDDIO
SYS.FES#1	T _{PWR_RDY}	Power-up to “Ready to accept I ² C/CC command”	–	5	25	ms	–

I/O

Table 6. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V _{IH_CMOS}	Input voltage HIGH threshold	0.7 × VDDIO	–	–	V	CMOS input
SID.GIO#38	V _{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × VDDIO	V	CMOS input
SID.GIO#39	V _{IH_VDDIO2.7-}	LVTTL input, VDDIO < 2.7 V	0.7 × VDDIO	–	–	V	–
SID.GIO#40	V _{IL_VDDIO2.7-}	LVTTL input, VDDIO < 2.7 V	–	–	0.3 × VDDIO	V	–
SID.GIO#41	V _{IH_VDDIO2.7+}	LVTTL input, VDDIO ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	V _{IL_VDDIO2.7+}	LVTTL input, VDDIO ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V _{OH_3V}	Output voltage HIGH level	VDDIO – 0.6	–	–	V	I _{OH} = 4 mA at 3V VDDIO
SID.GIO#34	V _{OH_1.8V}	Output voltage HIGH level	VDDIO – 0.5	–	–	V	I _{OH} = 1 mA at 1.8V VDDIO
SID.GIO#35	V _{OL_1.8V}	Output voltage LOW level	–	–	0.6	V	I _{OL} = 4 mA at 1.8V VDDIO
SID.GIO#36	V _{OL_3V}	Output voltage LOW level	–	–	0.6	V	I _{OL} = 4 mA at 3V VDDIO for SBU and AUX pins
SID.GIO#5	R _{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T _A , all VDDIO
SID.GIO#6	R _{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T _A , all VDDIO
SID.GIO#16	I _{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T _A , all VDDIO. Guaranteed by characterization.
SID.GIO#17	C _{PIN}	Max pin capacitance	–	3.0	7	pF	All VDDIO, all packages, all I/Os except SBU and AUX. Guaranteed by characterization.
SID.GIO#17A	C _{PIN_SBU}	Max pin capacitance	–	16	18	pF	All VDDIO, all packages, SBU pins only. Guaranteed by characterization.
SID.GIO#17B	C _{PIN_AUX}	Max pin capacitance	–	12	14	pF	All VDDIO, all packages, AUX pins only. Guaranteed by characterization.
SID.GIO#43	V _{HYSTTL}	Input hysteresis, LVTTL VDDIO > 2.7 V	15	40	–	mV	Guaranteed by characterization
SID.GIO#44	V _{HYSCMOS}	Input hysteresis CMOS	0.05 × VDDIO	–	–	mV	VDDIO < 4.5 V. Guaranteed by characterization.
SID69	I _{DIODE}	Current through protection diode to VDDIO/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I _{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by characterization