Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

EZ-PD™ CCG4

USB Type-C Port Controller

General Description

EZ-PD™ CCG4 is a dual USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG4 provides a complete dual USB Type-C and USB-Power Delivery port control solution for notebooks, power adapters and docking stations. It can also be used in dual role and downstream facing port applications. EZ-PD CCG4 uses Cypress's proprietary M0S8 technology with a 32-bit, 48-MHz ARM® Cortex®-M0 processor with 128 KB flash and integrates two complete Type-C Transceivers including the Type-C termination resistors R_P and R_D.

Applications

- Notebooks
- Power adapters
- Docking stations

Features

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU
- 128-KB Flash
- 8-KB SRAM

Integrated Digital Blocks

- Up to four integrated timers and counters to meet response times required by the USB-PD protocol
- Four run-time serial communication blocks (SCBs) with reconfigurable I^2C, SPI, or UART functionality

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Type-C and USB-PD Support

- Integrated USB Power Delivery 3.0 support
- Two integrated USB-PD BMC transceivers
- Integrated UFP[1] (R_D) and current sources for DFP[2] (R_P) on both Type-C ports
- Integrated dead battery termination for DRP (Power Source/Sink) applications
- Supports two USB Type-C ports
- Integrated VCONN FETs to power EMCA cables
- Integrated fast role swap and extended data messaging

Low-Power Operation

- 2.7-V to 5.5-V operation
- Independent supply voltage pin for GPIO that allows 1.71-V to 5.5-V signaling on the I/Os
- Reset: 1.0 µA, Deep Sleep: 2.5 µA, Sleep: 2.5 mA

System-Level ESD on CC Pins

- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C

Hot Swappable I/Os

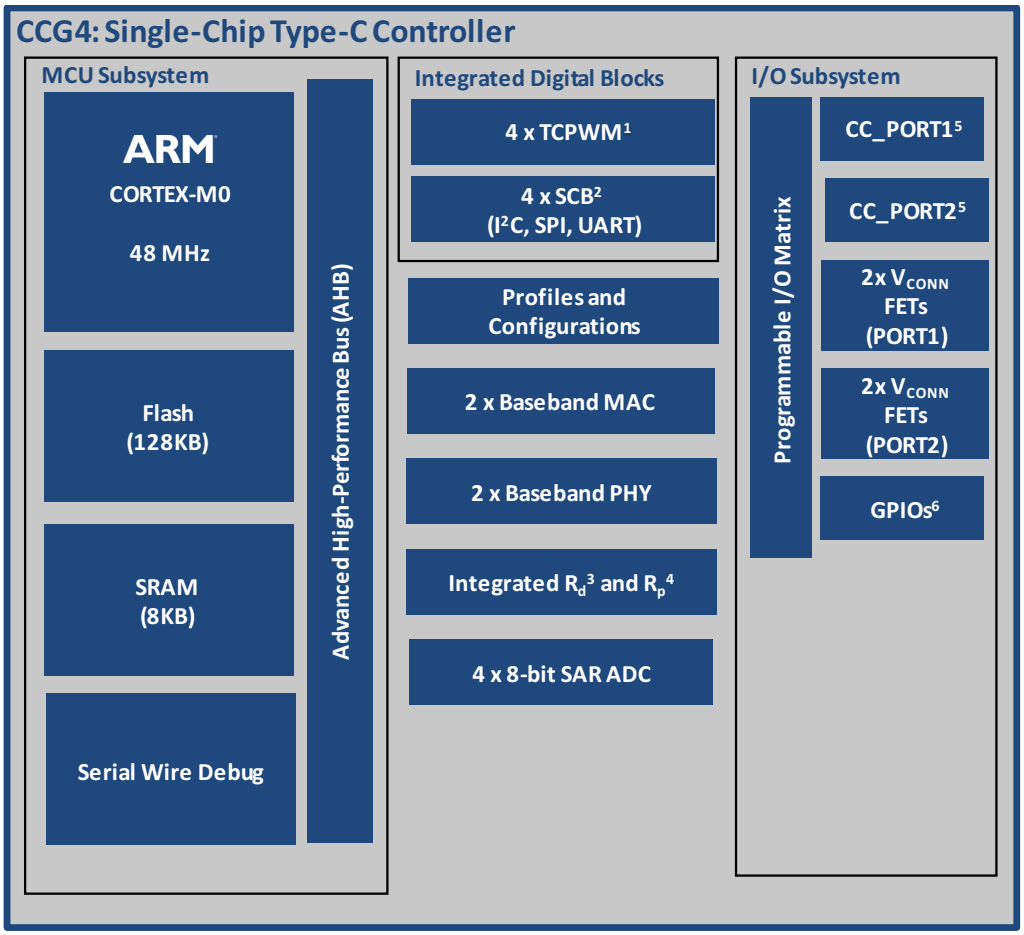
- Port 1 I^2C pins and CC1, CC2 pins are hot-swappable

Packages

- 6.0 mm × 6.0 mm, 0.6 mm, 40-pin QFN
- Supports industrial temperature range (–40 °C to +85 °C)

Notes
1. UFP refers to Power Sink.
2. DFP refers to Power Source.

Logic Block Diagram



1. Timer, counter, pulse width modulation block
2. Serial communication block configurable as UART, SPI, or I^2C
3. Termination resistor denoting a UFP
4. Current Sources to indicate a DFP
5. Configuration Channel
6. General purpose input/output

Available Firmware and Software Tools

EZ-PD Configuration Utility

The EZ-PD Configuration Utility is a GUI-based Microsoft Windows application developed by Cypress to guide a CCGx user through the process of configuring and programming the chip. The utility allows users to:

1. Select and configure the parameters they want to modify
2. Program the resulting configuration onto the target CCGx device.

The utility works with the Cypress supplied CCG1, CCG2, CCG3, and CCG4 kits, which host the CCGx controllers along with a USB interface. This version of the EZ-PD Configuration Utility supports configuration and firmware update operations on CCGx controllers implementing EMCA and Display Dongle applications. Support for other applications, such as Power Adapters and Notebook port controllers, will be provided in later versions of the utility.

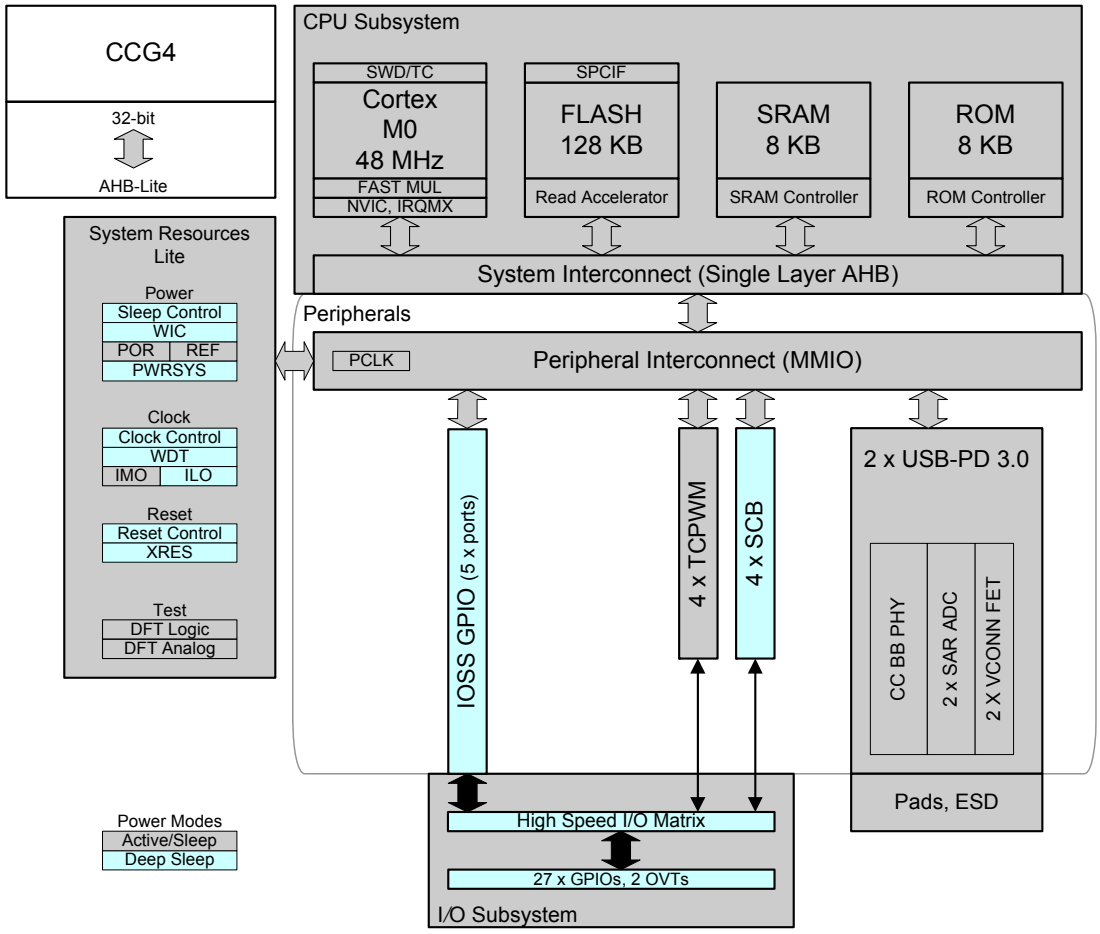
You can download the EZ-PD Configuration Utility and its associated documentation at the following link:

http://www.cypress.com/documentation/software-and-drivers/ez-pd-configuration-utility

Contents

Functional Overview **6**
CPU and Memory Subsystem 6
USB-PD Subsystem (SS) 6
System Resources 7
Peripherals 7
GPIO 8
Pinouts **9**
Power **14**
Application Diagrams **15**
Electrical Specifications **17**
Absolute Maximum Ratings 17
Device-Level Specifications 17
Digital Peripherals 20
Memory 21
System Resources 21
Ordering Information **24**
Ordering Code Definitions 24
Packaging **25**
Acronyms **26**
Document Conventions **27**
Units of Measure 27
References and Links To Applications Collaterals 28
Document History Page **29**
Sales, Solutions, and Legal Information **30**
Worldwide Sales and Design Support 30
Products 30
PSoC® Solutions 30
Cypress Developer Community 30
Technical Support 30

Figure 1. EZ-PD CCG4 Block Diagram



Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG4 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a nonmaskable interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG4 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG4 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait-states (WS) access time at 48 MHz and with 0-WS access time at 16 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

EZ-PD CCG4 has two USB-PD subsystems consisting of USB Type-C baseband transceivers and physical-layer logic. These transceivers perform the BMC and the 4b/5b encoding and decoding functions as well as the 1.2-V analog front end. This subsystem integrates the required termination resistors to identify the role of the EZ-PD CCG4 solution. R_D is used to identify EZ-PD CCG4 as a UFP in a DRP application. When configured as a DFP, integrated current sources perform the role of R_P or pull-up resistors. These current sources can be programmed to indicate the complete range of current capacity on VBUS defined in the USB Type-C spec. EZ-PD CCG4 responds to all USB-PD communication.

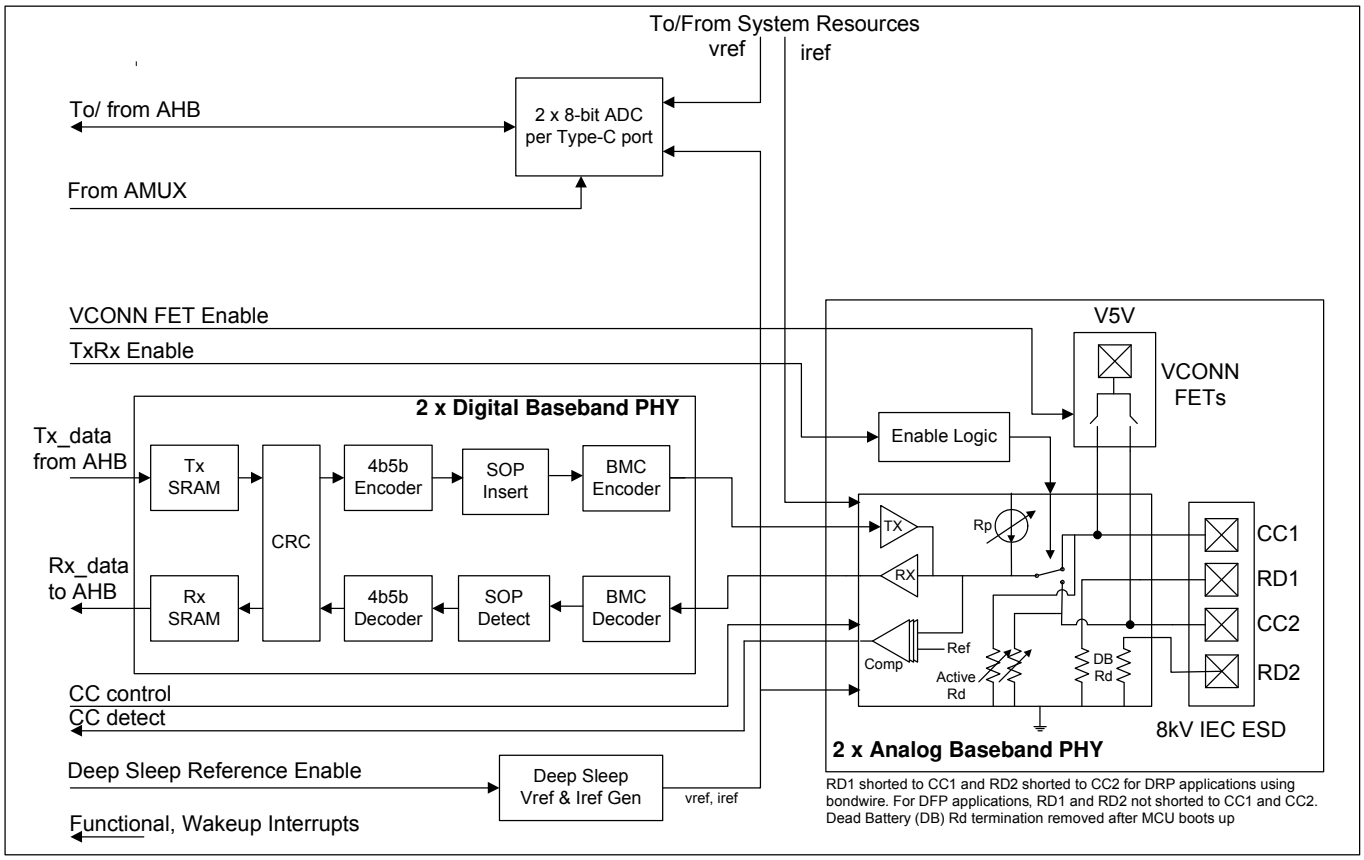
The USB-PD sub-system contains two 8-bit SAR (successive approximation register) ADCs for analog to digital conversions. The ADCs include an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses an internal bandgap voltage and an internal voltage proportional to the absolute temperature. All GPIO inputs can be connected to the global analog multiplex busses through a switch at each GPIO that can enable that GPIO to be connected to the mux bus for ADC use. The CC1 and CC2 pins of both Type-C ports are not available to connect to the mux busses.

To support the latest USB-PD 3.0 specification, CCG4 has implemented the fast role swap feature. Fast Role Swap enables externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed. For more details, refer to Section 6.3.17 (FR_Swap Message) in the USB-PD 3.0 specification.

CCG4 is designed to be fully interoperable with revision 3.0 of the USB Power Delivery specification as well as revision 2.0 of the USB Power Delivery specification.

CCG4 supports Extended Messages containing data of up to 260 bytes. The Extended Messages will be larger than expected by the USB-PD 2.0 hardware. To accommodate Revision 2.0 based systems, a Chunking mechanism is implemented such that Messages are limited to Revision 2.0 sizes unless it is discovered that both systems support the longer Message lengths.

Figure 2. USB-PD Subsystem



System Resources

Power System

The power system is described in detail in the section "Power" on page 14. It provides the assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). EZ-PD CCG4 can operate from three different power sources over the range of 2.7 to 5.5 V and has three different power modes, transitions between which are managed by the power system. EZ-PD CCG4 provides Sleep and Deep Sleep low-power modes.

Clock System

The clock system for EZ-PD CCG4 consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO).

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG4 has four SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as a master or a slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD CCG4 and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 2, SCB 3 and SCB 4 blocks of EZ-PD CCG4 are not completely compliant with the I^2C spec in the following:

- The GPIO cells for SCB 2 to SCB 4 I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG4 has up to four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

GPIO

EZ-PD CCG4 has 30 GPIOs that includes the I^2C and SWD pins, which can also be used as GPIOs. The I^2C pins from only SCB 1 are overvoltage-tolerant. The number of available GPIOs vary with the part numbers. The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Pinouts

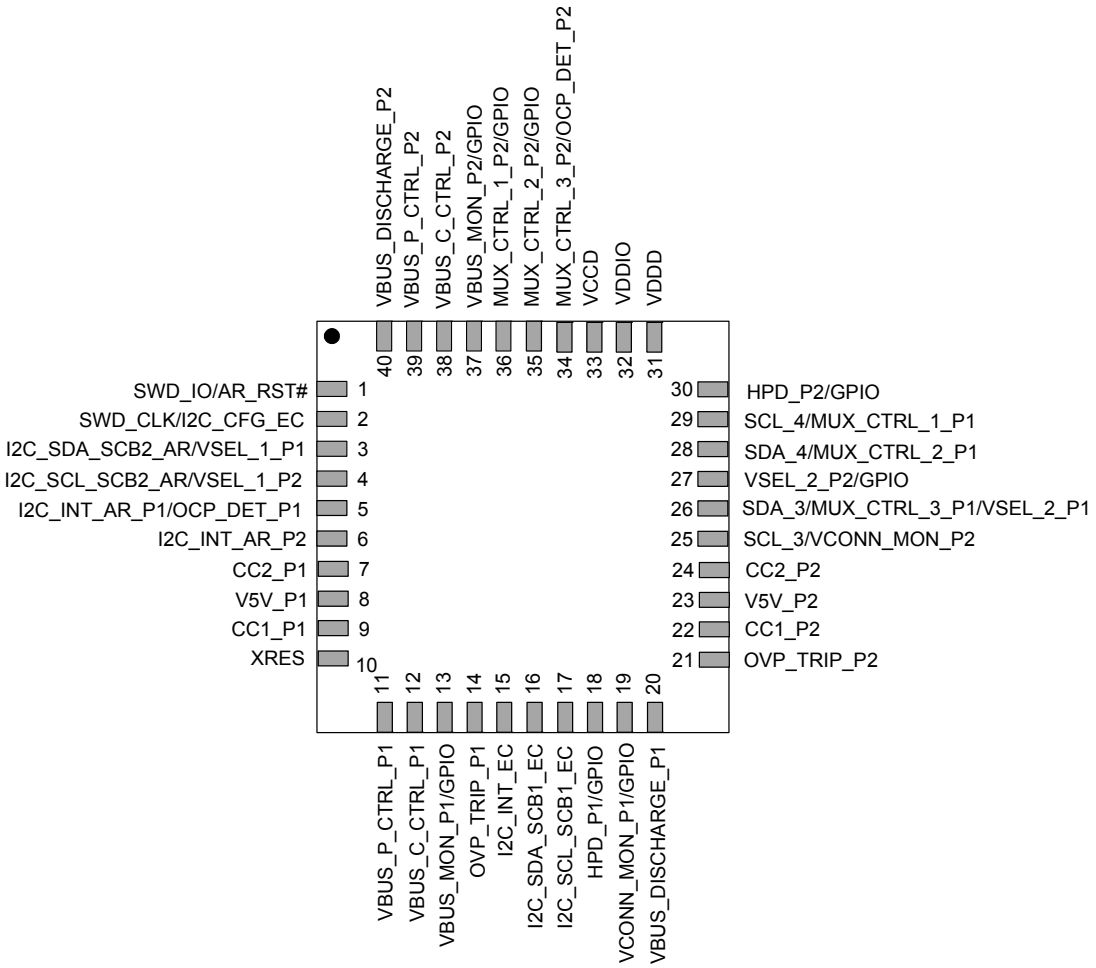
Table 1. Pinout for CYPD4225-40LQXIT

Group	Pin Name	Pin Number	Description
USB Type-C Port 1	CC1_P1	9	USB PD connector detect/Configuration Channel 1
	CC2_P1	7	USB PD connector detect/Configuration Channel 2
USB Type-C Port 2	CC1_P2	22	USB PD connector detect/Configuration Channel 1
	CC2_P2	24	USB PD connector detect/Configuration Channel 2
VBUS Control	VBUS_P_CTRL_P1	11	Full rail control I/O for enabling/disabling Provider load FET of USB Type-C port 1
	VBUS_C_CTRL_P1	12	Full rail control I/O for enabling/disabling Consumer load FET of USB Type-C port 1/SCB1 (see Table 3 through Table 6 on page 12)
	VBUS_P_CTRL_P2	39	Full rail control I/O for enabling/disabling Provider load FET of USB Type-C port 2
	VBUS_C_CTRL_P2	38	Full rail control I/O for enabling/disabling Consumer load FET of USB Type-C port 2
	VBUS_DISCHARGE_P1	20	I/O used for discharging VBUS line during voltage change
	VBUS_DISCHARGE_P2	40	I/O used for discharging VBUS line during voltage change
VCONN Control	VCONN_MON_P1/GPIO	19	VCONN_MON_P1 (Monitor VCONN for UVP condition on port 1)/GPIO
	SCL_3/VCONN_MON_P2	25	SCB3 (see Table 3 through Table 6) or VCONN_MON_P2(Monitor VCONN for UVP condition on port 2)
Overvoltage Protection (OVP)	OVP_TRIP_P1	14	VBUS overvoltage output indicator for port 1 (active LOW)
	OVP_TRIP_P2	21	VBUS overvoltage output indicator for port 2 (active LOW)
GPIOs and Serial Interfaces	VBUS_MON_P1/GPIO	13	VBUS_MON_P1 (VBUS overvoltage protection monitoring signal)/GPIO
	HPD_P1/GPIO	18	HPD_P1 (Hot Plug Detect I/O for port 1)/GPIO
	HPD_P2/GPIO	30	HPD_P2 (Hot Plug Detect I/O for port 2)/GPIO
	MUX_CTRL_3_P2/OCP_DET_P2	34	MUX_CTRL_3_P2 (Mux control for port 2) or VBUS Overcurrent Protection Input for port 2 (active LOW)
	GPIO/MUX_CTRL_2_P2	35	MUX_CTRL_2_P2 (Mux control for port 2)/SCB4 (see Table 3 through Table 6)
	GPIO/MUX_CTRL_1_P2	36	MUX_CTRL_1_P2 (Mux control for port 2)/SCB4 (see Table 3 through Table 6)
	VBUS_MON_P2	37	VBUS_MON_P2(VBUS overvoltage protection monitoring signal)
	VSEL_2_P2/GPIO	27	VSEL_2_P2(Voltage selection control for VBUS on port 2)/GPIO
	I2C_SCL_SCB1_EC	17	SCB1/SCB4 (see Table 3 through Table 6)
	I2C_SDA_SCB1_EC	16	SCB1/SCB3 (see Table 3 through Table 6)
	I2C_INT_EC	15	I2C Interrupt line
	I2C_SCL_SCB2_AR/VSEL_1_P2	4	SCB2 (see Table 3 through Table 6) or VSEL_1_P2 (Voltage selection control for VBUS on port 2)
	I2C_SDA_SCB2_AR/VSEL_1_P1	3	SCB1/SCB2 (see Table 3 through Table 6) or VSEL_1_P1 (Voltage selection control for VBUS on port 1)
	I2C_INT_AR_P1/OCP_DET_P1	5	I2C interrupt line or VBUS Overcurrent Protection Input for port 1 (active LOW)
	I2C_INT_AR_P2	6	I2C interrupt line/SCB1/SCB2 (see Table 3 through Table 6)
	SDA_3/MUX_CTRL_3_P1/VSEL_2_P1	26	SCB3 (see Table 3 through Table 6) or MUX_CTRL_3_P1 (Mux control for port 1) or VSEL_2_P1 (Voltage selection control for VBUS on port 1)
	SCL_4/MUX_CTRL_1_P1	29	SCB4 (see Table 3 through Table 6)/MUX_CTRL_1_P1 (Mux control for port 1)

Table 1. Pinout for CYPD4225-40LQXIT *(continued)*

Group	Pin Name	Pin Number	Description
GPIOs and Serial Interfaces	SDA_4/MUX_CTRL_2_P1	28	SCB4 (see Table 3 through Table 6)/MUX_CTRL_2_P1 (Mux control for port 1)
	SWD_IO/AR_RST#	1	SWD_IO (serial wire debug I/O)/SCB1. See Table 3 through Table 6.
	SWD_CLK/I2C_CFG_EC	2	SWD Clock/I2C_CFG_EC
Reset	XRES[3]	10	Reset input (active LOW)
Power	V5V_P1	8	2.7-V to 5.5-V supply for VCONN FET of Type-C port 1
	V5V_P2	23	2.7-V to 5.5-V supply for VCONN FET of Type-C port 2
	VDDIO	32	1.71-V to 5.5-V supply for I/Os
	VCCD	33	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	VDDD	31	VDDD supply input/output (2.7 V to 5.5 V)
	VSS	EPAD	Ground supply

Figure 3. 40-Pin QFN Pin Map (Top View) for CYPD4225-40LQXIT



Note
3. This is firmware configurable GPIO. By default, this pin is floating. Firmware can add pull-up/pull-down and enable/disable I/O buffers.

Table 2. Pinout for CYPD4125-40LQXIT

Group	Pin Name	Pin Number	Description
USB Type-C Port 1	CC1_P1	9	USB PD connector detect/Configuration Channel 1
	CC2_P1	7	USB PD connector detect/Configuration Channel 2
VBUS Control	VBUS_P_CTRL_P1	11	Full rail control I/O for enabling/disabling. Provider load FET of USB Type-C port 1.
	VBUS_C_CTRL_P1	12	Full rail control I/O for enabling/disabling. Consumer load FET of USB Type-C port 1/SCB1 (see Table 3 through Table 6 on page 12).
	VBUS_DISCHARGE_P1	20	I/O used for discharging VBUS line during voltage change
VCONN Control	VCONN_MON_P1/GPIO	19	VCONN_MON_P1 (Monitor VCONN for OVP condition on port 1)/GPIO
Overvoltage Protection (OVP)	OVP_TRIP_P1	14	VBUS overvoltage output indicator for port 1 (active LOW)
GPIOs and Serial Interfaces	GPIO	27	SCB3 (see Table 3 through Table 6)/GPIO
	VBUS_MON_P1/GPIO	13	VBUS_MON_P1 (VBUS overvoltage protection monitoring signal)/GPIO
	HPD_P1/GPIO	18	HPD_P1 (Hot Plug Detect I/O for port 1)/GPIO
	GPIO	21	GPIO
	GPIO	30	
	GPIO	34	
	GPIO	35	GPIO/SCB4 (see Table 3 through Table 6)
	GPIO	36	
	GPIO	37	GPIO
	GPIO	38	
	GPIO	39	
	GPIO	40	
	I2C_SCL_SCB1_EC	17	SCB1/SCB4 (see Table 3 through Table 6)
	I2C_SDA_SCB1_EC	16	SCB1/SCB3 (see Table 3 through Table 6)
	I2C_INT_EC	15	I2C interrupt line
	I2C_SCL_SCB2_AR	4	SCB2 (see Table 3 through Table 6)
	I2C_SDA_SCB2_AR/VSEL_1_P1	3	SCB1 or SCB2 (see Table 3 through Table 6) or voltage selection control for VBUS on port 2
	I2C_INT_AR_P1/OCP_DET_P1	5	I2C interrupt line or VBUS Overcurrent Protection Input for port 1 (Active LOW)
	GPIO	6	GPIO/SCB1/SCB2 (see Table 3 through Table 6)
	SCL_3/GPIO	25	GPIO/SCB3 (see Table 3 through Table 6)
	SDA_3/MUX_CTRL_3_P1/VSEL_2_P1	26	SCB3 (see Table 3 through Table 6) or MUX_CTRL_3_P1 (Mux control for port 1), or Voltage selection control for VBUS on port 1
	SCL_4/MUX_CTRL_1_P1	29	SCB3 (see Table 3 through Table 6) or MUX_CTRL_1_P1 (Mux control for port 1)
	SDA_4/MUX_CTRL_2_P1	28	SCB4 (see Table 3 through Table 6) or MUX_CTRL_2_P1 (Mux control for port 1)
	SWD_IO/AR_RST#	1	Serial wire debug I/O (SWD IO)/SCB1. See Table 3 through Table 6 or Alpine Ridge Reset.
	SWD_CLK/I2C_CFG_EC	2	SWD Clock/I2C_CFG_EC
Reset	XRES[4]	10	Reset input (active LOW)

Note
4. This is firmware configurable GPIO. By default, this pin is floating. Firmware can add pull-up/pull-down and enable/disable IO buffers.

Table 2. Pinout for CYPD4125-40LQXIT *(continued)*

Group	Pin Name	Pin Number	Description
Power	V5V_P1	8	2.7-V to 5.5-V supply for VCONN FET of Type-C port 1
	VDDIO	32	1.71-V to 5.5-V supply for I/Os
	VCCD	33	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	VDDD	31	VDDD supply I/O (2.7 V to 5.5 V)
	VSS	EPAD	Ground supply
No Connect	NC	22	These pins are not bonded
	NC	23	
	NC	24	

Table 3. Serial Communication Block (SCB1) Configuration

Pin	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
12	UART_TX_SCB1	SPI_MOSI_SCB1	SPI_MOSI_SCB1	VBUS_C_CTRL_P1	VBUS_C_CTRL_P1
14	UART_RX_SCB1	SPI_CLK_SCB1	SPI_CLK_SCB1	VSEL_2_P1/ VCONN_MON_P1	VSEL_2_P1/ VCONN_MON_P1
17	UART_RTS_SCB1	SPI_MISO_SCB1	SPI_MISO_SCB1	I2C_SDA_SCB1	I2C_SDA_SCB1
16	UART_CTS_SCB1	SPI_SEL_SCB1	SPI_SEL_SCB1	I2C_SCL_SCB1	I2C_SCL_SCB1

Table 4. Serial Communication Block (SCB2) Configuration

Pin	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
4	UART_TX_SCB2	SPI_CLK_SCB2	SPI_CLK_SCB2	I2C_SCL_SCB2	I2C_SCL_SCB2
3	UART_RX_SCB2	SPI_MISO_SCB2	SPI_MISO_SCB2	I2C_SDA_SCB2	I2C_SDA_SCB2
6	UART_RTS_SCB2	SPI_SEL_SCB2	SPI_SEL_SCB2	GPIO	GPIO
1	UART_CTS_SCB2	SPI_MOSI_SCB2	SPI_MOSI_SCB2	SWD_IO	SWD_IO

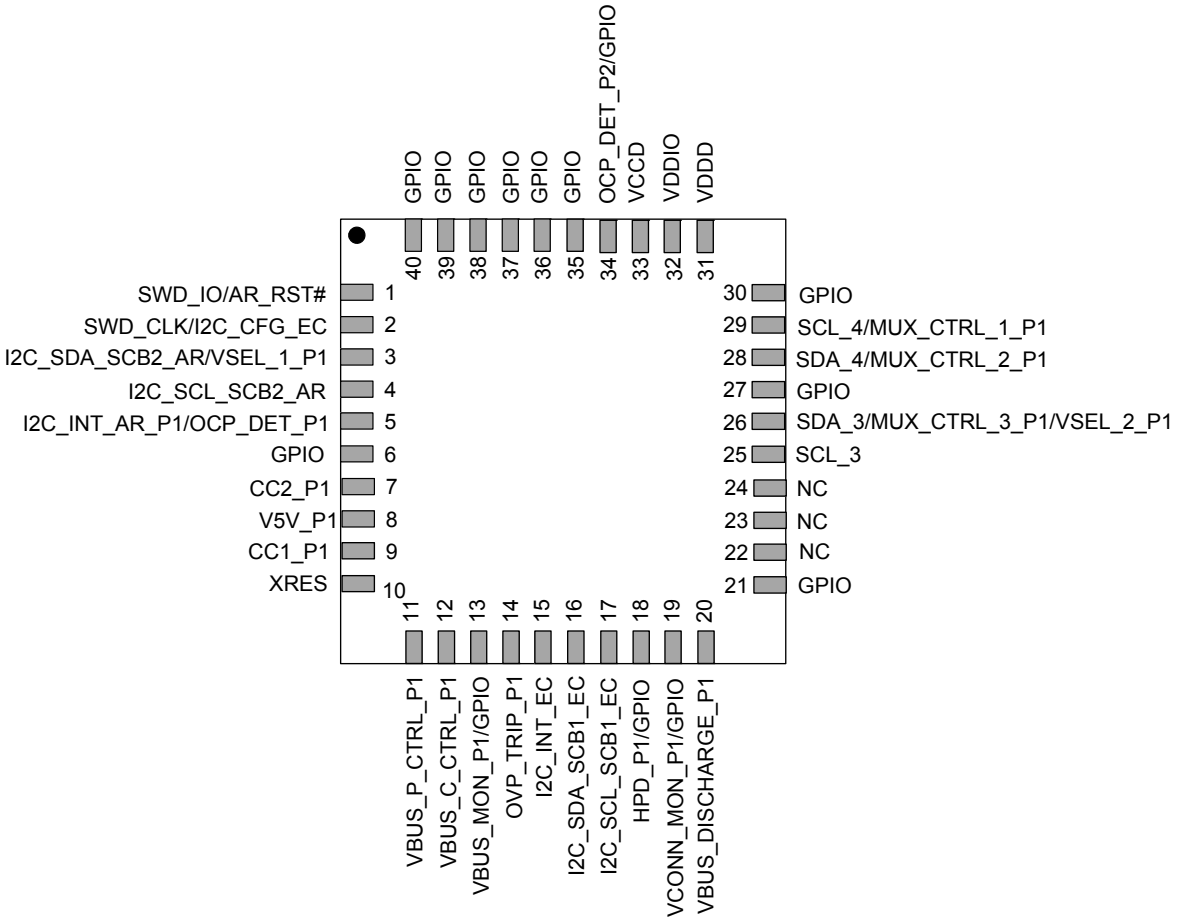
Table 5. Serial Communication Block (SCB3) Configuration

Pin	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
26	UART_TX_SCB3	SPI_MISO_SCB3	SPI_MISO_SCB2	I2C_SDA_SCB3	I2C_SDA_SCB3
25	UART_RX_SCB3	SPI_MOSI_SCB3	SPI_MOSI_SCB3	I2C_SCL_SCB3	I2C_SCL_SCB3
16	UART_RTS_SCB3	SPI_SEL_SCB3	SPI_SEL_SCB3	I2C_SCL_SCB1	I2C_SCL_SCB1
21	UART_CTS_SCB3	SPI_CLK_SCB3	SPI_CLK_SCB3	AR_RST#	AR_RST#

Table 6. Serial Communication Block (SCB4) Configuration

Pin	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
28	UART_TX_SCB4	SPI_MOSI_SCB4	SPI_MOSI_SCB4	I2C_SDA_SCB4	I2C_SDA_SCB4
29	UART_RX_SCB4	SPI_MISO_SCB4	SPI_MISO_SCB4	I2C_SCL_SCB4	I2C_SCL_SCB4
36	UART_RTS_SCB4	SPI_SEL_SCB4	SPI_SEL_SCB4	GPIO	GPIO
35	UART_CTS_SCB4	SPI_CLK_SCB4	SPI_CLK_SCB4	GPIO	GPIO

Figure 4. 40-Pin QFN Pin Map (Top View) for CYPD4125-40LQXIT



Power

The following power system diagram shows the set of power supply pins as implemented in EZ-PD CCG4.

CCG4 shall be able to operate from three possible external supply sources: V5V_P1 for first Type-C port, V5V_P2 for second Type- C port and VDDD.

CCG4 has the power supply input V5V_P1 and V5V_P2 pins for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in CCG4 per Type-C port to power either CC1 or CC2 pin. These FETs are capable of providing a minimum of 1W on the CC1 and CC2 pins for the EMCA cables. In USB-PD applications, the valid levels on V5V_P1 and V5V_P2 supplies can range from 4.85 V to 5.5 V.

The chip's internal operating power supply is derived from VDDD. In UFP mode, CCG4 operates in 2.7 V – 5.5V. In DFP and DRP modes, it operates in the 3.0 V – 5.5 V range.

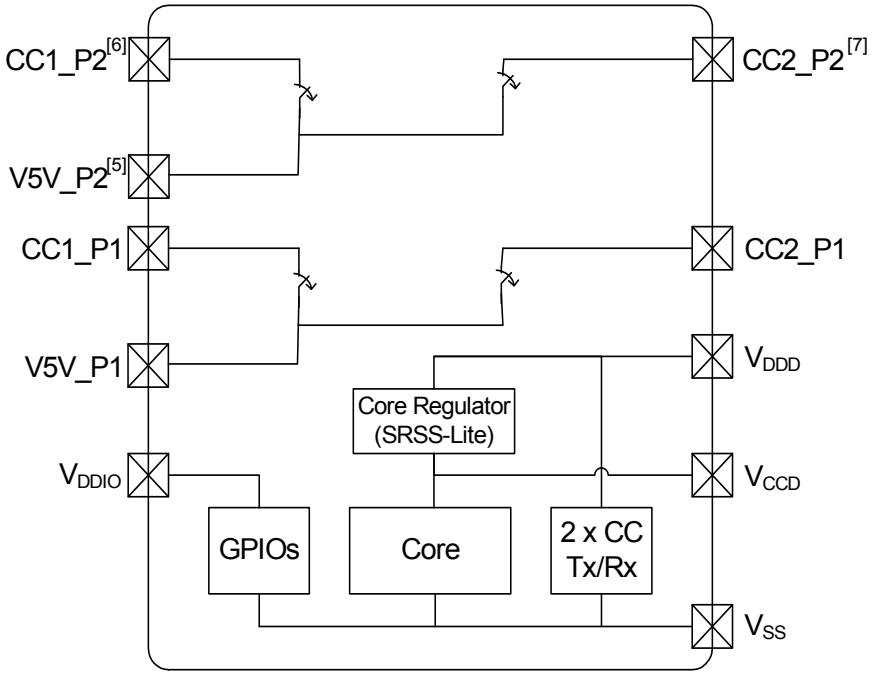
A separate I/O supply pin, VDDIO, allows the GPIOs to operate at levels from 1.71 V to 5.5 V. The VDDIO pin can be equal to or less than the voltages connected to the V5V_P1 or V5V_P2 and VDDD pins. The VDDIO supply should be less than or equal to VDDD supply.

The VCCD output of EZ-PD CCG4 must be bypassed to ground via an external capacitor (in the range of 80 to 120 nF; X5R ceramic or better).

Bypass capacitors must be used from VDDD and V5V_P1 or V5V_P2 pins to ground; typical practice for systems in this frequency range is to use a 0.1-µF capacitor on VDDD, V5V_P1 and V5V_P2. Note that these are simply rules of thumb and that for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 5 shows an example of the power supply bypass capacitors.

Figure 5. EZ-PD CCG4 Power and Bypass Scheme Example



Note
5. V5V_P1 denoted power supply input for Type-C port 1
   V5V_P2 denoted power supply input for Type-C port 2
6. CC1_1:USB PD connector detect/Configuration Channel 1 for Type-C port 1
   CC1_2:USB PD connector detect/Configuration Channel 1 for Type-C port 2
7. CC2_1:USB PD connector detect/Configuration Channel 2 for Type-C port 1
   CC2_2:USB PD connector detect/Configuration Channel 2 for Type-C port 2

Application Diagrams

Figure 6 and Figure 7 show a dual Type-C port and a single Type-C port Notebook DRP application diagram using a CCG4 device. The Type-C port can be used as a power provider or a power consumer.

In each of these applications, CCG4 communicates with the Embedded Controller (EC), which manages the Battery Charger Controller (BCC) to control the charging and discharging of internal battery. It also controls the Data Mux to route the HighSpeed signals either to the USB chipset (during normal mode) or the DisplayPort Chipset (during Alternate Mode).The SBU, SuperSpeed, and HighSpeed lines are routed directly from the Display Mux of the notebook to the Type-C receptacle.

For the dual Type-C notebook application, these Type-C ports can be power providers or power consumers simultaneously. In addition, the CCG4 device controls the transfer of DisplayPort signals over the Type-C interface using the display mux controllers.

Optional FETs are provided for applications that need to provide power for accessories and cables using VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. A VBUS_DISCHARGE FET controlled by CCG4 device is used to quickly discharge VBUS after the Type-C connection is detached.

Figure 6. CCG4 in a Dual Port Notebook Application using CYPD4225-40LQXIT

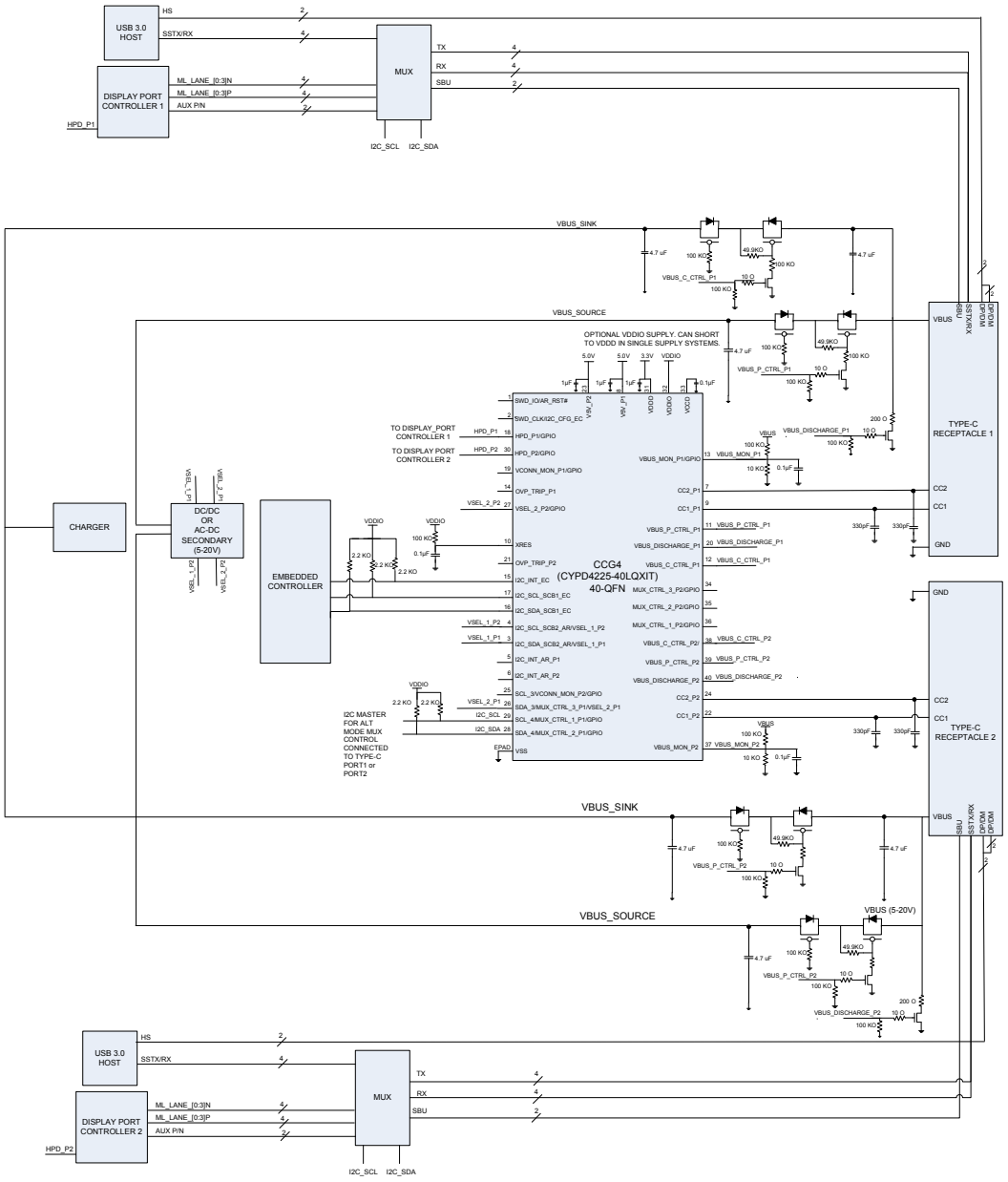
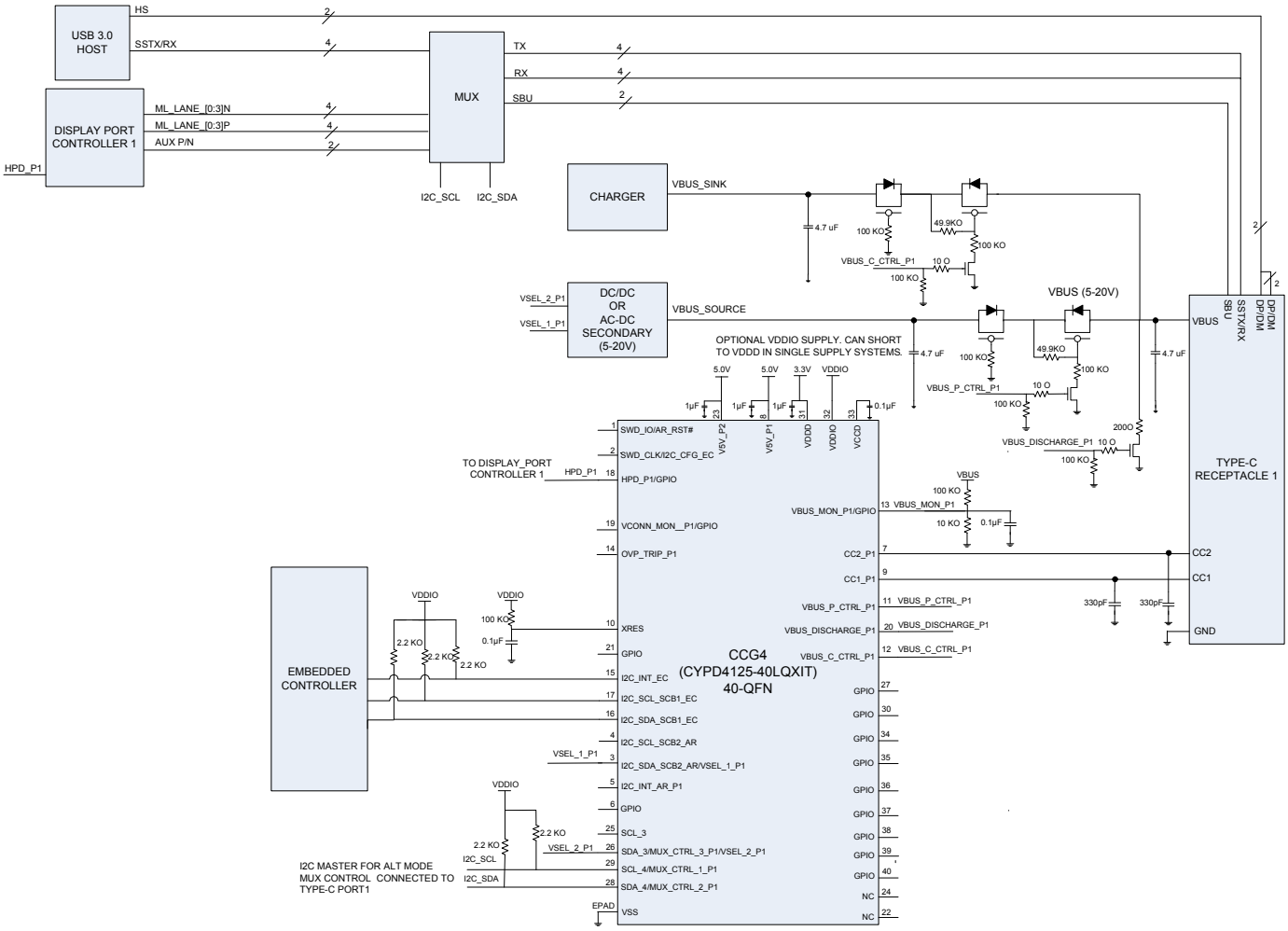


Figure 7. CCG4 in a Single Port Notebook Application using CYPD4125-40LQXIT



Electrical Specifications

Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings[8]

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V5V_P1	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V5V_P2	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute Max
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5	V	Absolute max
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–200	–	200	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for pins CC1, CC2

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 3.0 V to 5.5 V, except where noted.

Table 8. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	UFP applications
SID.PWR#1_A	V_{DDD}	Power supply input voltage	3.0	–	5.5	V	DFP/DRP applications
SID.PWR#26	V5V_P1, V5V_P2	Power supply input voltage	4.85	–	5.5	V	–
PWR#13	V_{DDIO}	GPIO power supply	1.71	–	5.5	V	–
SID.PWR#24	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	–
SID.PWR#15	C_{EFC}	External regulator voltage bypass on V_{CCD}	80	100	120	nF	X5R ceramic or better
SID.PWR#16	C_{EXC}	Power supply decoupling capacitor on V_{DDD}	0.8	1	–	µF	X5R ceramic or better
SID.PWR#27	C_{EXV}	Power supply decoupling capacitor on V5V_P1 and V5V_P2	–	0.1	–	µF	X5R ceramic or better
Active Mode, V_{DDD} = 2.7 to 5.5 V. Typical values measured at V_{DD} = 3.3 V.							
SID.PWR#4	I_{DD12}	Supply current	–	10	–	mA	V5V_P1 and V5V_P2 = 5 V, T_A = 25 °C, CC I/O IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, two PD ports active

Note

8. Usage above the absolute maximum conditions listed in Table 7 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 8. DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Sleep Mode, V_{DDD} = 2.7 to 5.5 V							
SID25A	I_{DD20A}	I^2C wakeup WDT ON IMO at 48 MHz	–	2.5	4.0	mA	V_{DDD} = 3.3 V, T_A = 25 °C, all blocks except CPU are ON, CC I/O ON, no I/O sourcing current
Deep Sleep Mode, V_{DDD} = 2.7 to 3.6 V (Regulator on)							
SID34	I_{DD29}	V_{DDD} = 2.7 to 3.6 V I^2C wakeup and WDT ON	–	80	–	µA	V_{DDD} = 3.3 V, T_A = 25 °C
SID_DS	I_{DD_DS}	V_{DDD} = 2.7 to 3.6 V CC wakeup ON	–	2.5	–	µA	Power source = V_{DDD}, Type-C not attached, CC enabled for wakeup, R_P disabled
SID_DS1	I_{DD_DS1}	V_{DDD} = 2.7 to 3.6 V CC wakeup ON	–	100	–	µA	Power source = V_{DDD}, Type-C not attached, CC enabled for wakeup, R_P and R_D connected at 70 ms intervals by CPU. R_P, R_D connection should be enabled for both PD ports.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	1	10	µA	–

Table 9. AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU frequency	DC	–	48	MHz	3.0 V ≤ V_{DDD} ≤ 5.5 V
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	Guaranteed by characterization
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	24-MHz IMO. Guaranteed by characterization.
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	Guaranteed by characterization
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I2C / CC command”	–	5	25	ms	Guaranteed by characterization

I/O

Table 10. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH}[9]	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.GIO#38	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.GIO#39	V_{IH}[9]	LVTTL input, V_{DDIO} < 2.7 V	0.7× V_{DDIO}	–	–	V	–
SID.GIO#40	V_{IL}	LVTTL input, V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V	–
SID.GIO#41	V_{IH}[9]	LVTTL input, V_{DDIO} ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	V_{IL}	LVTTL input, V_{DDIO} ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	V_{DDIO} –0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	V_{DDIO} –0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDIO}
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3 V V_{DDIO}

Note
9. V_{IH} must not exceed V_{DDIO} + 0.2 V.

Table 10. I/O DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#5	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#6	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDIO} = 3.0 V
SID.GIO#17	C_{IN}	Input capacitance	–	–	7	pF	–
SID.GIO#43	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDIO} \geq 2.7$ V. Guaranteed by characterization.
SID.GPIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDIO}$	–	–	mV	Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DDIO}/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	Guaranteed by characterization

Table 11. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF
SID71	T_{FALLF}	Fall time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF

XRES

Table 12. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	$0.7 \times V_{DDIO}$	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	$0.3 \times V_{DDIO}$	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	–	$0.05 \times V_{DDIO}$	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 13. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	Fc	–	MHz	Fc max = CLK_SYS. Maximum = 48 MHz
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	–	2/Fc	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	–	2/Fc	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	–	1/Fc	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	–	1/Fc	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	–	1/Fc	–	ns	Minimum pulse width between quadrature-phase inputs

I^2C

Table 14. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 15. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 16. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 17. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 18. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	48 + 3 * T_{SCB}	ns	$T_{SCB} = T_{CPU}$ = 1/24 MHz
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	–

Memory

Table 19. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#4	$T_{ROWWRITE}$[10]	Row (block) write time (erase and program)	–	–	20	ms	–
SID.MEM#3	$T_{ROWERASE}$[10]	Row erase time	–	–	13	ms	–
SID.MEM#8	$T_{ROWPROGRAM}$[10]	Row program time after erase	–	–	7	ms	–
SID178	$T_{BULKERASE}$[10]	Bulk erase time (128 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$[10]	Total device program time	–	–	25	seconds	Guaranteed by characterization
SID.MEM#6	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET1}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	F_{RET2}	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization

System Resources

Power-on-Reset (POR) with Brown Out

Table 20. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization

Table 21. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.1	–	1.5	V	Guaranteed by characterization

Note

10. It can take as much as 20 milliseconds to write to flash. During this time the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

SWD Interface

Table 22. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ V_{DDIO} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	1.8 V ≤ V_{DDIO} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 * T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 23. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID229	$T_{JITRMSIMO}$	RMS jitter at 48 MHz	–	145	–	ps	–
F_{IMO}	–	IMO frequency	24	–	48	MHz	–

Internal Low-Speed Oscillator

Table 24. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	ILO Frequency	20	40	80	kHz	–

Power Down

Table 25. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356	µA	–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP Dead Battery CC termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0 V and 1.0 V applied at CC1 or CC2. Applicable for DRP applications only.
SID.PD.15	Vdrop_V5V_CC1	Voltage drop from V5V_P1 and V5V_P2 pins to CC1 pin while sourcing 215 mA. CC1 and CC2 pins of Port1 and Port2 are not short circuit protected. Max allowed sourcing current is 500 mA.	–	–	100	mV	–
SID.PD.16	Vdrop_V5V_CC2	Voltage drop from V5V_P1 and V5V_P2 pins to CC2 pin while sourcing 215 mA CC1 and CC2 pins of Port1 and Port2 are not short circuit protected. Max allowed sourcing current is 500 mA.	–	–	100	mV	–

Analog to Digital Converter

Table 26. ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	bits	–
SID.ADC.2	INL	Integral nonlinearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential nonlinearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1.0	–	1.0	LSB	–

Table 27. ADC AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

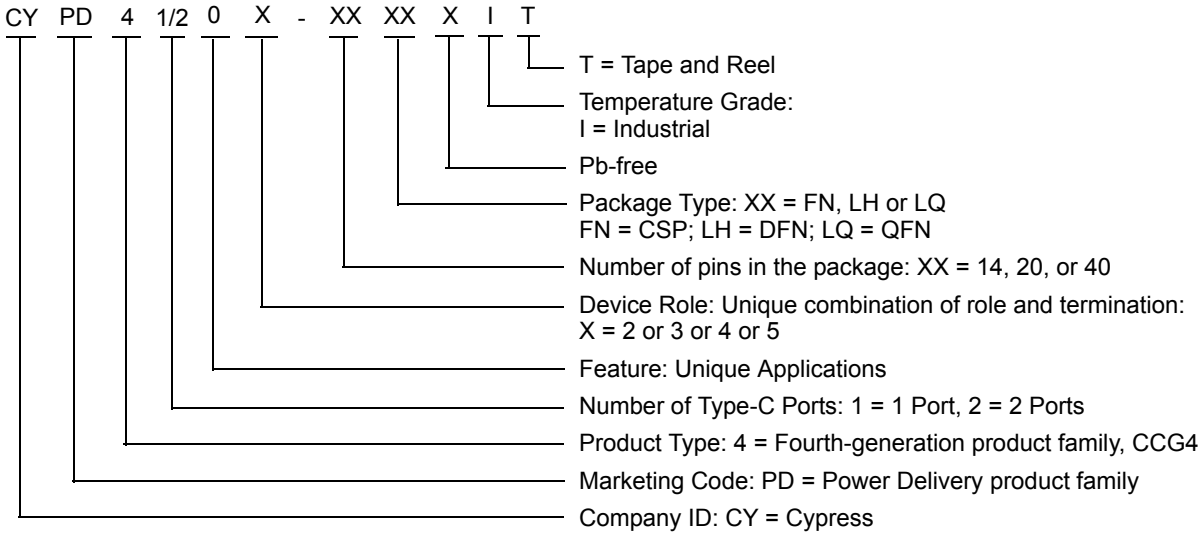
Ordering Information

The EZ-PD CCG4 part numbers and features are listed in Table 28.

Table 28. EZ-PD CCG4 Ordering Information

Part Number	Application	Type-C Ports	TCPWM	PD Spec#	Dead Battery Termination	Termination Resistor	Role	Package
CYPD4125-40LQXIT	Notebooks, docking station	1	4	PD2.0	Yes	RP[11], RD[12]	DRP	40-pin QFN
CYPD4225-40LQXIT	Notebooks, docking station	2	4	PD2.0	Yes	RP[11], RD[12]	DRP	40-pin QFN
CYPD4126-40LQXIT	Notebooks, docking station	1	2	PD3.0	Yes	RP[11], RD[12]	DRP	40-pin QFN
CYPD4226-40LQXIT	Notebooks, docking station	2	2	PD3.0	Yes	RP[11], RD[12]	DRP	40-pin QFN
CYPD4136-40LQXIT	Power adapter	1	2	PD3.0	No	RP[11]	DFP	40-pin QFN
CYPD4236-40LQXIT	Power adapter	2	2	PD3.0	No	RP[11]	DFP	40-pin QFN

Ordering Code Definitions



Notes
11. Termination resistor denoting a downstream facing port.
12. Termination resistor denoting an accessory or upstream facing port.

Packaging

Table 29. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25	85	°C
T_J	Operating junction temperature	–	–40	–	100	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	31	–	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	29	–	°C/W

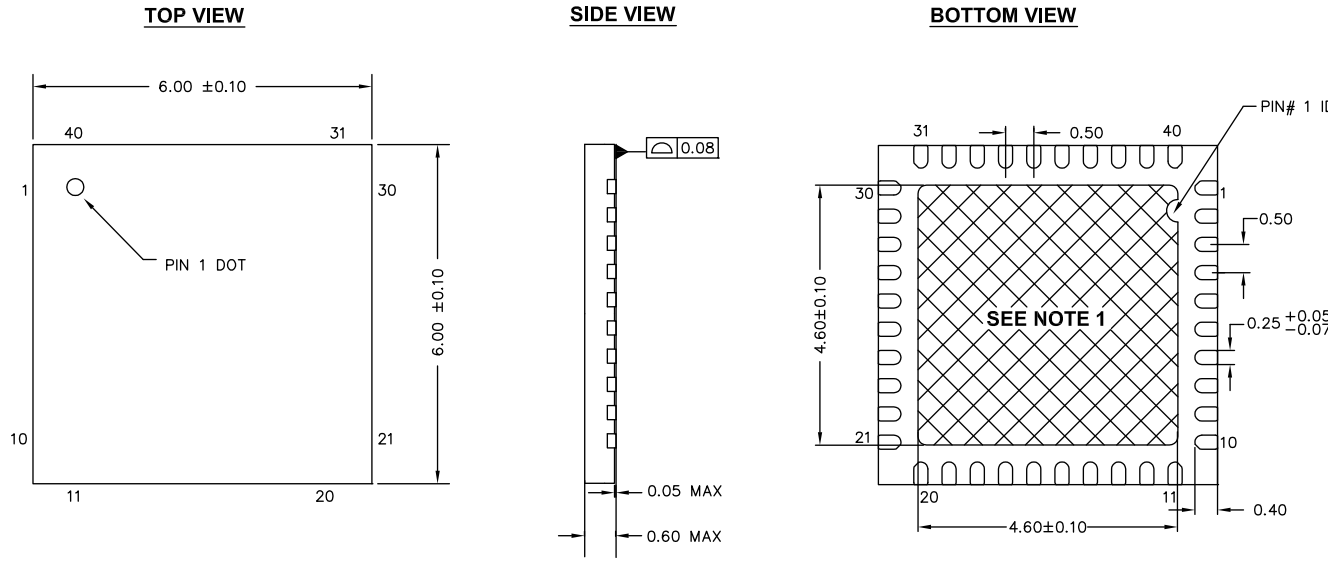
Table 30. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
40-pin QFN	260 °C	30 seconds

Table 31. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
40-pin QFN	MSL 3

Figure 8. 40-Pin QFN (6 × 6 × 0.6 mm), LR40A/LQ40A 4.6 × 4.6 E-PAD (Sawn) Package Outline, 001-80659



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A