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# EZ-PD™ CCG5

## USB Type-C Port Controller

## General Description

EZ-PD™ CCG5 is a dual USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG5 provides a complete dual USB Type-C and USB-Power Delivery port control solution for PCs, notebook, and dock. It can also be used in dual role and downstream-facing port applications. EZ-PD CCG5 uses Cypress' proprietary M0S8 technology with a 32-bit, 48-MHz Arm® Cortex®-M0 processor with 128-KB flash and integrates two complete Type-C Transceivers including the Type-C termination resistors, $R_P$ and $R_D$. CCG5 also integrates high-voltage regulator. CCG5 is available in 40-QFN (1 port) and 96-BGA (2 ports) packages.

## Applications

- PCs, Notebook, and Dock
- Thunderbolt hosts and devices

## Features

### Type-C and USB-PD Support

- Integrated USB Power Delivery (USB-PD) 3.0 support
- Two integrated USB-PD Type-C ports
- Integrated UFP[1] ($R_D$) and current sources for DFP[2] ($R_P$) on both Type-C ports
- Integrated dead battery termination for DRP (Power Source/Sink) applications
- Integrated VCONN FETs to power EMCA cables
- Integrated fast role swap and extended data messaging
- Integrated high-voltage LDO, operational up to 21.5 V
- Integrated 2x USB Analog Mux
- Integrated 2x SBU Analog Mux
- Integrated 2x USB Charger detect blocks – BC v1.2, Apple Charging (source only)
- Integrated overvoltage protection (OVP) and overcurrent protection (OCP) on the VBUS
- Integrated OCP protection on the VCONN
- Integrated high-voltage protection on CC and SBU pins to protect against accidental shorts to the VBUS pin on the Type-C connector
- Integrated current sense amplifier that supports high-side current sensing
- Integrated gate drivers for external VBUS PFET control on Type-C Ports
- Supports high-voltage tolerant PFET-controlled GPIOs

### 32-bit MCU Subsystem

- 48-MHz Arm Cortex-M0 CPU
- 128-KB Flash
- 12-KB SRAM

### Integrated Digital Blocks

- Up to two integrated timers and counters to meet response times required by the USB-PD protocol
- Four run-time serial communication blocks (SCBs) with reconfigurable $I^2C$, SPI, or UART functionality

### Clocks and Oscillators

- Integrated oscillator eliminating the need for an external clock

### Low-Power Operation

- 2.75 V to 21.5 V operation

### System-Level ESD on CC, D±, and SBU Pins

- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C

### Hot-Swappable I/Os

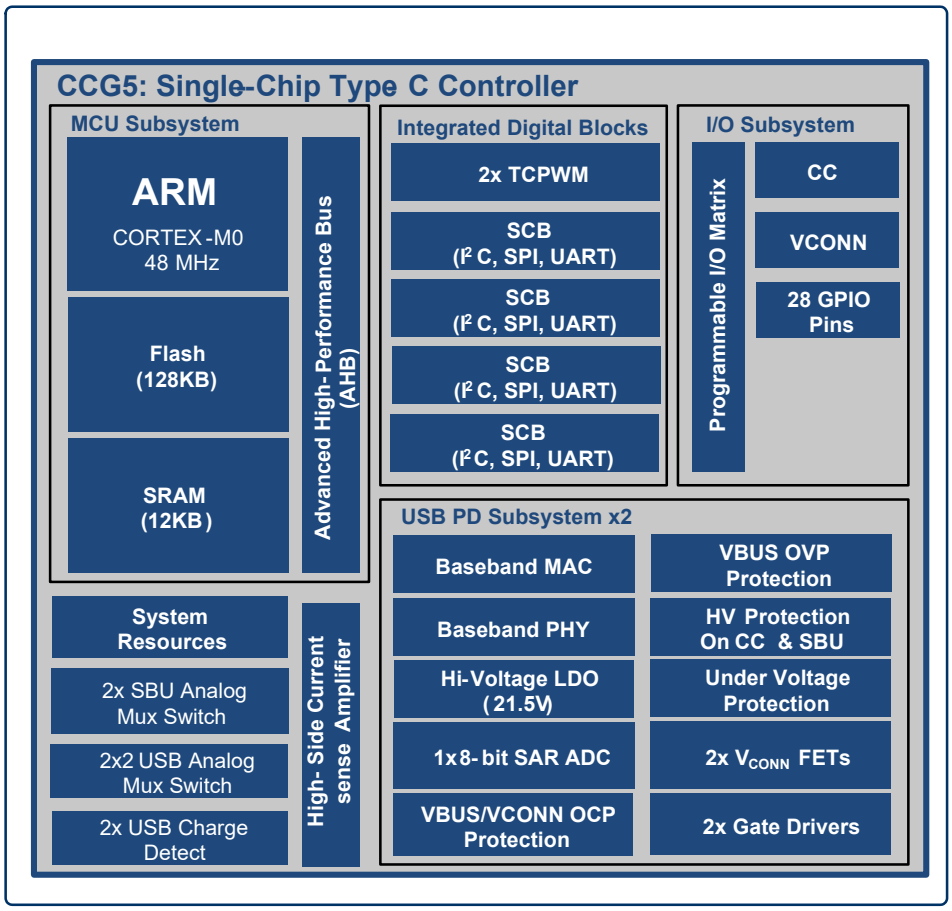
- Port 1 $I^2C$ pins and CC1, CC2 pins are hot-swappable

### Packages

- 6.0 mm × 6.0 mm, 0.6 mm, 40-pin QFN
  6.0 mm × 6.0 mm, 1.0 mm, 96-ball BGA
- Supports industrial temperature range (–40 °C to +85 °C)

**Notes**
1. UFP refers to Power Sink.
2. DFP refers to Power Source.

## Logic Block Diagram



## Contents

# Functional Overview

## USB-PD Subsystem (SS)

*USB-PD Physical Layer*

The CCG5 has two USB-PD subsystems consisting of the USB-PD physical layer (PHY) block and supporting circuits. The USB-PD PHY consists of a transmitter and receiver that communicate BMC and 4b/5b encoded data over the CC channel based on the PD 3.0 standard. All communication is half-duplex. The PHY practices collision avoidance to minimize communication errors on the channel.

In addition, the CCG5 USB-PD block includes all termination resistors ($R_P$ and $R_D$) and their switches as required by the USB Type-C spec. $R_P$ and $R_D$ resistors are required to implement connection detection, plug orientation detection, and for establishing the USB source/sink roles.

The integrated $R_P$ resistor enables CCG5 to be configured as a DFP. The $R_P$ resistor is implemented as a current source and can be programmed to support the complete range of current capacity on the VBUS defined in the USB Type-C Spec.

The $R_D$ resistor is used to identify CCG5 as a UFP in a DRP application. The $R_D$ resistor on CC pins is required even when the part is not powered for dead battery termination detection and charging.

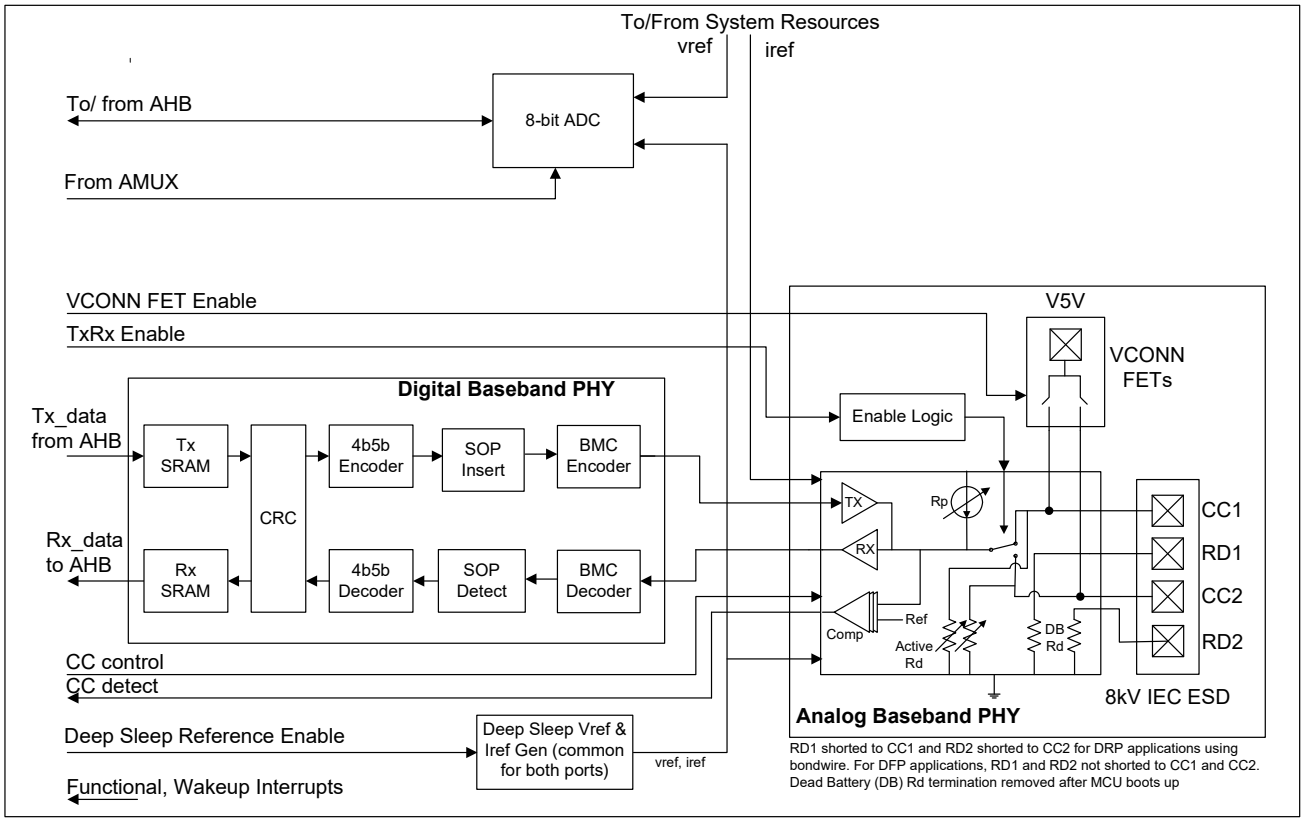
To support the latest USB-PD 3.0 specification, CCG5 has implemented the Fast Role Swap (FRS) feature. The FRS feature enables externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed. CCG5 also supports DeepSleep in notebook systems where CCG5 is expecting FRS detection.

For more details, refer to Section 6.3.17 in the USB-PD 3.0 specification.

CCG5 is designed to be fully interoperable with revision 3.0 of the USB Power Delivery specification as well as revision 2.0 of the USB Power Delivery specification.

CCG5 supports Extended Messages containing data of up to 260 bytes. The Extended Messages will be larger than expected by the USB-PD 2.0 hardware. To accommodate Revision 2.0 based systems, a Chunking mechanism is implemented such that messages are limited to Revision 2.0 sizes unless it is discovered that both systems support longer message lengths.

**Figure 1. USB-PD Subsystem**



*VCONN FET*

CCG5 has two power supply inputs, V5V_P1 and V5V_P2 pins, for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs for each PD port to power either CC1 or CC2 pins. These FETs can provide 1.5-W power over VCONN on the CC1 and CC2 pins for the EMCA cables. CCG5 also supports integrated OCP on VCONN.

*ADC*

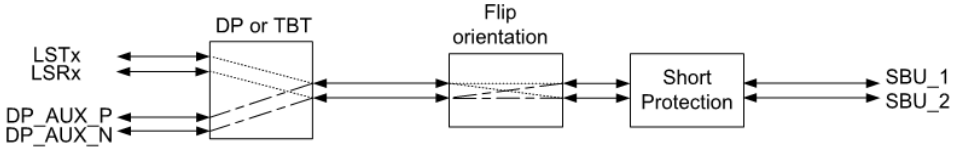
The USB-PD subsystem contains one 8-bit successive approximation register (SAR) for analog-to-digital conversions (ADC). The ADCs include an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage, and an internal voltage proportional to the absolute temperature. All GPIOs on the chip have access to the ADCs through the chip-wide analog mux bus. The CC1 and CC2 pins of both Type-C ports are not available to connect to the mux bus.

*SBU Mux*

The SBU switch mux contains 2x1 Mux and a single 2x2 cross bar SBU switch per the Type-C port. The 2x1 MUX enables you to select between the Display Port or Thunderbolt alternate mode and the single-ended 2x2 switch enables you to route signals to the appropriate SBU1/2 based on CC (Type-C plug) orientation.

The AUX port of the SBU switch supports only differential signals. Non-differential signals on the AUX port cause signal coupling at the output of the SBU switch. The LS port of the SBU switch supports both non-differential and differential signals.

**Figure 2. CCG5 SBU Crossbar Switch Block Diagram**




*USB HS Mux*

The HS Mux contains a 2×2 cross bar switch to route the system D± lines to the Type-C top or bottom ports based on the CC (Type-C plug) orientation. The unused D± top or bottom lines can be connected to a UART (Debug) port. The maximum operating frequency of UART must be 1 Mbps.

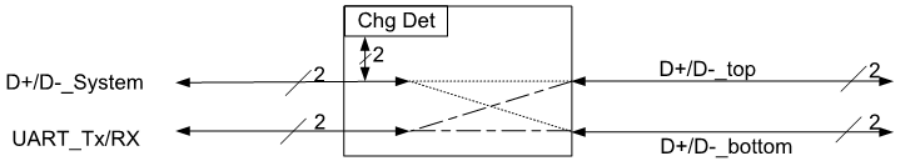
The HS Mux also contains charger detection/emulation for detecting USB BC 1.2 (source only) and Apple terminations. The charger detection block is connected to the D± from the system as shown in Figure 3.

To meet the HS eye diagram requirements with sufficient margin, follow these guidelines:

- Trace lengths of HS signals shall be no more than 2 inches from the USB 2.0 host to the CCG5 device. Similarly, trace length from the CCG5 device to Type-C connector pins shall be no more than 2 inches.
- The differential impedance across the DP/DM signal traces shall be 90 Ω.
- Trace width shall be 6 mils.
- Air Gap (distance between lines) shall be 8 mils.

Increasing the trace length by more than 2 inches on either side of the CCG5 device degrades the HS eye diagram.

**Figure 3. CCG5 DP/DM Switch Block Diagram**




*Overvoltage and Undervoltage Protection on VBUS*

CCG5 implements an undervoltage/overvoltage (UV/OV) detection circuit for the VBUS supply. The threshold for OV and UV detection can be set independently. Both UV and OV detector have programmable thresholds and is controlled by the firmware.

Overcurrent Protection on VBUS

CCG5 integrates a high-side current sense amplifier to detect overcurrent on the VBUS. Overcurrent protection is enabled by sensing the current through the 10-mΩ sense resistor connected between the “CSP_Px” and “CSN_Px” pins.

*VBUS Discharge*

CCG5 also has integrated VBUS discharge FETs and resistors for each port. It is used to discharge VBUS to meet the USB-PD specification timing on a detach condition and negative voltage transition.

*VBUS Regulator*

CCG5 can operate from three power supplies – $V_{SYS}$, $V_{BUS\_P1}$, and $V_{BUS\_P2}$. CCG5 integrates the regulator (that supports up to 21.5 V) to derive operating supply voltage. The $V_{SYS}$ always takes priority over VBUS_P1/VBUS_P2. In the absence of $V_{SYS}$, the regulator powers CCG5 either from VBUS_P1 or VBUS_P2.

*PFET Gate Driver for VBUS*

CCG5 supports the consumer-side and provider-side external power FET Drivers for PFET. The VBUS_P_CTRL and VBUS_C_CTRL gate drivers can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

*Charger Detect*

CCG5 integrates battery charger emulation and detection for USB BC.1.2, Apple charge (source only).

*IEC Compliant VBUS, CC, D±, and SBU Lines*

The chip supports IEC-compliant ESD protection on VBUS, CC, D±, and SBU lines.

*High-Voltage Tolerant SBU and CC Lines*

The chip supports high-voltage tolerant SBU and CC lines. In the case of SBU/CC short to VBUS through connectors, these lines will be protected internally.

## CPU and Memory Subsystem

*CPU*

The Cortex-M0 CPU in EZ-PD CCG5 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG5 has four break-point (address) comparators and two watchpoint (data) comparators.

*Flash*

The EZ-PD CCG5 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait states (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

*SROM*

A supervisory ROM that contains boot and configuration routines is provided.

*SRAM*

CCG5 supports 12-KB SRAM.

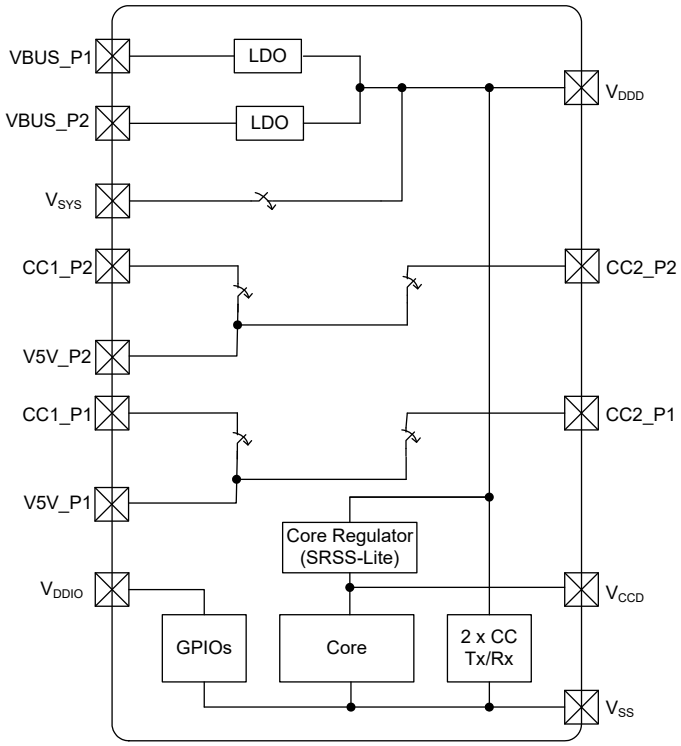
## Power System Overview

Figure 4 provides an overview of the EZ-PD CCG5 power system. CCG5 can operate from three possible external supply sources: $V_{BUS\_P1}$/$V_{BUS\_P2}$ (4 V–21.5 V) or $V_{SYS}$ (2.75 V–5.5 V). The VBUS_P1 and VBUS_P2 supply is regulated inside the chip with a LDO. The switched supply, $V_{DDD}$, is either used directly inside some analog blocks or further regulated down to $V_{CCD}$, which powers majority of the core using the regulators. CCG5 has two different power modes: Active and Deep sleep. Transitions between these power modes are managed by the power system. A separate power domain, $V_{DDIO}$, is provided for the GPIOs. The $V_{DDD}$ and $V_{CCD}$ pins, both outputs of regulators, are brought out for connecting a 1 µF and 0.1 µF capacitor respectively for the regulator stability only. The $V_{CCD}$ pin is not supported as a power supply. $V_{DDD}$ can source 2 mA (max) for external load.

**Table 1. CCG5 Power Modes**

| Mode | Description |
|---|---|
| RESET | Power is valid and XRES is not asserted. An internal reset source is asserted or Sleep Controller is sequencing the system out of reset. |
| ACTIVE | Power is valid and CPU is executing instructions. |
| DEEP SLEEP | Main regulator and most blocks are shut off. Deep Sleep regulator powers logic, but only low-frequency clock if available. |

**Figure 4. EZ-PD CCG5 Power System**



## Peripherals

*Serial Communication Blocks (SCB)*

EZ-PD CCG5 has four SCBs, which can be configured to implement an $I^2C$, SPI, or UART interface. The hardware $I^2C$ blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as a Master/slave.

In the $I^2C$ mode, the SCB blocks are capable of operating at speeds up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support $I^2C$ that creates a mailbox address range in the memory of EZ-PD CCG5 and effectively reduce $I^2C$ communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The $I^2C$ peripherals are compatible with the $I^2C$ Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP $I^2C$-bus specification and user manual (UM10204). The $I^2C$ bus I/Os are implemented with GPIO in open-drain modes.

The $I^2C$ port on SCB 2, SCB 3 and SCB 4 blocks of EZ-PD CCG5 are not completely compliant with the $I^2C$ spec in the following:

- The GPIO cells for SCB 2 to SCB 4 $I^2C$ port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the $I^2C$ system.
- Fast-mode Plus has an $I_{OL}$ specification of 20 mA at a $V_{OL}$ of 0.4 V. The GPIO cells can sink a maximum of 10-mA $I_{OL}$ with a $V_{OL}$ maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

*Timer/Counter/PWM Block (TCPWM)*

EZ-PD CCG5 has up to two TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (TCPWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

## GPIO

EZ-PD CCG5 has 28 GPIOs that includes the $I^2C$ and SWD pins, which can also be used as GPIOs. The $I^2C$ pins from only SCB 1 are overvoltage-tolerant. The number of available GPIOs vary with the part numbers. The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

## Pinouts

**Table 2. Pinout for CYPD5125-40LQXIT**

| Group Name | Pin Name | Port | Pin | Description |
|---|---|---|---|---|
| USB Type-C | CC1 | Analog | 9 | USB PD connector detect/Configuration Channel 1 |
| | CC2 | Analog | 7 | USB PD connector detect/Configuration Channel 2 |
| Mux | DPLUS_SYS | Analog | 23 | USB 2.0 DP from the Host System |
| | DMINUS_SYS | Analog | 24 | USB 2.0 DM from the Host System |
| | UART_TX/GPIO | P4.0 | 29 | UART TX from Host System/GPIO |
| | UART_RX/GPIO | P4.1 | 30 | UART RX from Host System/GPIO |
| | DPLUS_BOT | Analog | 26 | USB 2.0 DP from Bottom of Type-C Connector |
| | DMINUS_BOT | Analog | 25 | USB 2.0 DM from Bottom of Type-C Connector |
| | DMINUS_TOP | Analog | 27 | USB 2.0 DM from Top of Type-C Connector |
| | DPLUS_TOP | Analog | 28 | USB 2.0 DP from Top of Type-C Connector |
| | SBU2 | Analog | 34 | Sideband Use signal |
| | SBU1 | Analog | 35 | Sideband Use signal |
| | AUX_P | Analog | 36 | Auxiliary signal for DisplayPort |
| | AUX_N | Analog | 37 | Auxiliary signal for DisplayPort |
| | LSTX | Analog | 38 | Thunderbolt Link Management UART Rx |
| | LSRX | Analog | 39 | Thunderbolt Link Management UART Tx |
| VBUS Control | VBUS_P_CTRL | Analog | 11 | Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 1<br>0: Path ON<br>High Z: Path OFF |
| | VBUS_C_CTRL | Analog | 12 | Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C port1<br>0: Path ON<br>High Z: Path OFF |
| VBUS OCP | CSP | Analog | 1 | Current Sense positive Input for VBUS side external Rsense |
| | CSN | Analog | 40 | Current sense negative for other side of external Rsense |
| GPIOs and Serial Interfaces | SWD_IO/AR_RST/GPIO | P1.6 | 6 | SWD I/O/GPIO |
| | SWD_CLK/I2C_CFG_EC/ GPIO | P1.0 | 2 | SWD Clock/ $I^2C$ config line.<br>$I^2C$ config line is used to select the $I^2C$ address of HPI interface. The state of line decides the 7 bit $I^2C$ address for HPI.<br>$I^2C$ Config Line Floating: 0x08<br>Pulled up with 1 KW: 0x42<br>Pulled down with 1 KW: 0x40 |
| | I2C_SDA_SCB2_TBT/GPIO | P1.1 | 3 | SCB2 $I^2C$ Data/GPIO |
| | I2C_SCL_SCB2_TBT/GPIO | P1.2 | 4 | SCB2 $I^2C$ Clock/GPIO |
| | I2C_INT_TBT/GPIO | P1.3 | 5 | TBT interrupt for port 1/GPIO |
| | OVP_TRIP/I2C_SDA_SCB4/GPIO | P2.4 | 14 | VBUS overvoltage output indicator for port 1/SCB4 $I^2C$ Data |
| | UV_OCP_TRIP/I2C_SCL_SCB4/GPIO | P2.3 | 13 | VBUS undervoltage or OCP Output Indicator for Port1 / SCB4 $I^2C$ Clock / GPIO |
| | I2C_SDA_SCB1_EC/GPIO | P5.0 | 16 | SCB1 $I^2C$ Data / GPIO |
| | I2C_SCL_SCB1_EC/GPIO | P5.1 | 17 | SCB1 $I^2C$ Clock / GPIO |
| | I2C_INT_EC/GPIO | P2.5 | 15 | Embedded Controller interrupt/GPIO |
| | HPD/GPIO | P3.0 | 18 | Hot Plug Detect I/O for port 1/GPIO |
| | I2C_SDA_SCB3 / GPIO / VSEL_2 | P3.6 | 20 | SCB3 $I^2C$ Data or GPIO or voltage selection control for VBUS |
| | I2C_SCL_SCB3 / GPIO /VSEL_1 | P3.7 | 21 | SCB3 $I^2C$ Clock or GPIO or voltage selection control for VBUS |
| Reset | XRES | Analog | 10 | Reset input (Active LOW) |

**Table 2. Pinout for CYPD5125-40LQXIT** *(continued)*

| Group Name | Pin Name | Port | Pin | Description |
|---|---|---|---|---|
| Power | VBUS | Power | 22 | VBUS Input for Port 1 (4 V to 21.5 V) |
| | VSYS | Power | 19 | 2.75 V to 5.5 V supply for the system |
| | VDDD | Power | 31 | VDDD supply output<br>1. VSYS powered - (Min: VSYS-50 mV) 2.7 V to 5.5 V<br>2. VBUS powered - 3.15 V to 3.6 V |
| | VDDIO | Power | 32 | At system-level short the VDDD to VDDIO |
| | VCCD | Power | 33 | 1.8 V regulator output for filter capacitor. This pin cannot drive external load. |
| | V5V | Power | 8 | 4.85 V to 5.5 V supply for VCONN FET of Type-C Port 1 |
| Ground | VSS | Ground | EPAD | Ground |

**Figure 5. 40-Pin QFN Pin Map (Top View) for CYPD5125-40LQXIT**

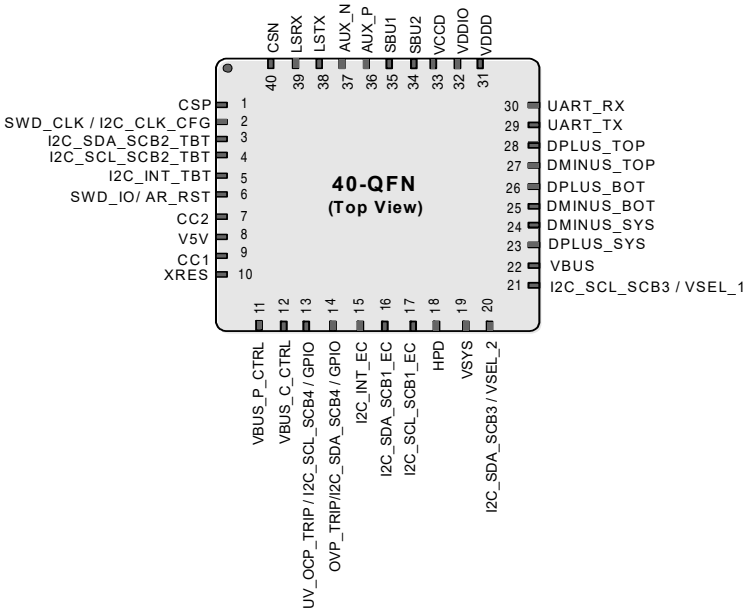


**Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI**

| Group Name | Pin Name | Port | Ball Location | Description |
|---|---|---|---|---|
| USB Type-C Port 1 | CC1_P1 | Analog | K2 | USB PD connector detect/Configuration Channel 1 |
| | CC2_P1 | Analog | H2 | USB PD connector detect/Configuration Channel 2 |
| USB Type-C Port 2 | CC1_P2 | Analog | K9 | USB PD connector detect/Configuration Channel 1 |
| | CC2_P2 | Analog | K10 | USB PD connector detect/Configuration Channel 2 |
| MUX Type-C Port 1 | AUX_P_P1 | Analog | B11 | Auxiliary signal for DisplayPort |
| | AUX_N_P1 | Analog | C11 | Auxiliary signal for DisplayPort |
| | LSRX_P1 | Analog | A11 | Thunderbolt Link Management UART Rx |
| | LSTX_P1 | Analog | A10 | Thunderbolt Link Management UART Tx |
| | SBU1_P1 | Analog | A3 | Sideband Use signal |
| | SBU2_P1 | Analog | A4 | Sideband Use signal |
| | DMINUS_SYS_P1 | Analog | A7 | USB 2.0 DM from the Host System |
| | DPLUS_SYS_P1 | Analog | A6 | USB 2.0 DP from the Host System |
| | UART_RX_P1/GPIO | P4.1 | A9 | UART Rx from Host System/GPIO |
| | UART_TX_P1/GPIO | P4.0 | A8 | UART Tx from Host system/GPIO |
| | DMINUS_BOT_P1 | Analog | C1 | USB 2.0 DM from Bottom of Type-C Connector |
| | DPLUS_BOT_P1 | Analog | B1 | USB 2.0 DP from Bottom of Type-C Connector |
| | DMINUS_TOP_P1 | Analog | A2 | USB 2.0 DM from Top of Type-C Connector |
| | DPLUS_TOP_P1 | Analog | A1 | USB 2.0 DP from Top of Type-C Connector |
| MUX Type-C Port 2 | AUX_P_P2 | Analog | D11 | Auxiliary signal for DisplayPort |
| | AUX_N_P2 | Analog | E11 | Auxiliary signal for DisplayPort |
| | LSRX_P2 | Analog | L11 | Thunderbolt Link Management UART Rx |
| | LSTX_P2 | Analog | K11 | Thunderbolt Link Management UART Tx |
| | SBU1_P2 | Analog | E1 | Sideband Use signal |
| | SBU2_P2 | Analog | F1 | Sideband Use signal |
| | DMINUS_SYS_P2 | Analog | G11 | USB 2.0 DM from the Host System |
| | DPLUS_SYS_P2 | Analog | F11 | USB 2.0 DP from the Host System |
| | UART_RX_P2/GPIO | P0.2 | J11 | UART Rx from Host System/GPIO |
| | UART_TX_P2/GPIO | P0.1 | H11 | UART Tx from Host system/GPIO |
| | DMINUS_BOT_P2 | Analog | L1 | USB 2.0 DM from Bottom of Type-C Connector |
| | DPLUS_BOT_P2 | Analog | K1 | USB 2.0 DP from Bottom of Type-C Connector |
| | DMINUS_TOP_P2 | Analog | H1 | USB 2.0 DM from Top of Type-C Connector |
| | DPLUS_TOP_P2 | Analog | G1 | USB 2.0 DP from Top of Type-C Connector |
| VBUS Control Type-C Port1 | VBUS_P_CTRL_P1 | Analog | K3 | Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 1<br>0: Path ON<br>High Z: Path OFF |
| | VBUS_C_CTRL_P1 | Analog | K4 | Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C Port 1<br>0: Path ON<br>High Z: Path OFF |

**Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI** *(continued)*

| Group Name | Pin Name | Port | Ball Location | Description |
|---|---|---|---|---|
| VBUS Control Type-C Port2 | VBUS_P_CTRL_P2 | Analog | B4 | Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 2.<br>0: Path ON<br>High Z: Path OFF |
| | VBUS_C_CTRL_P2 | Analog | B5 | Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C Port 2.<br>0: Path ON<br>High Z: Path OFF |
| VBUS OCP | CSP_P1 | Analog | J1 | Current Sense Positive Input for P1 |
| | CSN_P1 | Analog | B3 | Current Sense Negative Input for P1 |
| | CSP_P2 | Analog | L2 | Current Sense Positive Input for P2 |
| | CSN_P2 | Analog | K8 | Current Sense Negative Input for P2 |
| GPIOs and Serial Interfaces | GPIO | P3.1 | L7 | GPIO |
| | I2C_SDA_SCB4/OVP_TRIP_P1/GPIO | P2.4 | K5 | VBUS overvoltage output indicator for Port 1 / SCB4 I2C Data/ GPIO |
| | OVP_TRIP_P2 / GPIO | P2.2 | L8 | VBUS overvoltage output indicator for Port 2 / GPIO |
| | VSEL_1_P2 / GPIO | P0.0 | L4 | Voltage selection control for VBUS on Port 2 / GPIO |
| | UV_OCP_TRIP_P1/GPIO | P1.4 | B6 | VBUS undervoltage of OCP output indicator for Port 1/GPIO |
| | HPD_P1/GPIO | P3.0 | K7 | Hot Plug Detect I/O for Port 1 /GPIO |
| | HPD_P2/GPIO | P3.4 | E10 | Hot Plug Detect I/O for Port 2 /GPIO |
| | VCONN_OCP_TRIP_P2/ GPIO | P3.3 | B9 | VCONN OCP output indicator for Port 2 / GPIO |
| | VCONN_OCP_TRIP_P1/GPIO | P3.5 | B8 | VCONN OCP output indicator for Port 1/ GPIO |
| | UV_OCP_TRIP_P2/GPIO | P1.5 | B7 | VBUS undervoltage or OCP output indicator for Port 2/GPIO |
| | VSEL_2_P2 / GPIO | P2.0 | H10 | Voltage selection control for VBUS on Port 2 / GPIO |
| | I2C_SCL_SCB1_EC/ GPIO | P5.1 | L6 | SCB1 $I^2C$ Clock |
| | I2C_SDA_SCB1_EC/ GPIO | P5.0 | K6 | SCB1 $I^2C$ Data |
| | I2C_INT_EC/GPIO | P2.5 | L5 | $I^2C$ interrupt line |
| | I2C_SCL_SCB2_TBT/GPIO | P1.2 | E2 | SCB2 $I^2C$ Clock/GPIO |
| | I2C_SDA_SCB2_TBT/GPIO | P1.1 | D2 | SCB2 $I^2C$ Data /GPIO |
| | I2C_INT_TBT_P1/GPIO | P1.3 | F2 | $I^2C$ interrupt line/GPIO |
| | I2C_INT_TBT_P2/GPIO | P2.1 | G2 | $I^2C$ interrupt line |
| | I2C_SCL_SCB3 / VSEL_1_P1 /GPIO | P3.7 | L10 | SCB3 $I^2C$ Clock/ Voltage selection control for VBUS on Port 1/ GPIO |
| | I2C_SDA_SCB3 / VSEL_2_P1 / GPIO | P3.6 | J10 | SCB3 $I^2C$ Data / Voltage selection control for VBUS on Port 1 /GPIO |
| | I2C_SCL_SCB4/GPIO | P2.3 | F10 | SCB4 $I^2C$ Clock /GPIO |
| | I2C_SDA_SCB4/GPIO | P3.2 | G10 | SCB4 $I^2C$ Data /GPIO |
| | SWD_IO/AR_RST# /GPIO | P1.6 | B2 | SWD I/O / AR Reset / GPIO |
| | SWD_CLK/I2C_CFG_EC/GPIO | P1.0 | C2 | SWD Clock / $I^2C$ config line / GPIO.<br>$I^2C$ config line is used to select the $I^2C$ address of HPI interface. The state of line decides the 7 bit $I^2C$ address for HPI.<br>$I^2C$ Config Line Floating: 0x08<br>Pulled up with 1 KW: 0x42<br>Pulled down with 1 KW: 0x40 |
| Reset | XRES | Analog | H6 | Reset input (Active LOW) |

**Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI** *(continued)*

| Group Name | Pin Name | Port | Ball Location | Description |
|---|---|---|---|---|
| Power | VBUS_P1 | Power | D1 | VBUS Input for Port 1 (4 V to 21.5 V) |
| | VBUS_P2 | Power | L3 | VBUS Input for Port 2 (4 V to 21.5 V) |
| | VSYS | Power | A5 | 2.75 V to 5.5 V supply for the system |
| | VDDD | Power | D10 | VDDD supply output<br>1. VSYS powered - (Min: VSYS-50 mV) 2.7 V to 5.5 V<br>2. VBUS powered - 3.15 V to 3.6 V |
| | VCCD | Power | B10 | 1.8 V regulator output for filter capacitor. This pin cannot drive external load. |
| | VDDIO | Power | C10 | At system-level short the VDDD to VDDIO |
| | V5V_P1 | Power | J2 | 4.85 V to 5.5 V supply for VCONN FET of Type-C Port 1 |
| | V5V_P2 | Power | L9 | 4.85 V to 5.5 V supply for VCONN FET of Type-C Port 2 |
| Ground | GND | Ground | D5 | Ground |
| | GND | Ground | D6 | Ground |
| | GND | Ground | D7 | Ground |
| | GND | Ground | D8 | Ground |
| | GND | Ground | E4 | Ground |
| | GND | Ground | E5 | Ground |
| | GND | Ground | E6 | Ground |
| | GND | Ground | E7 | Ground |
| | GND | Ground | E8 | Ground |
| | GND | Ground | F4 | Ground |
| | GND | Ground | F5 | Ground |
| | GND | Ground | F6 | Ground |
| | GND | Ground | F7 | Ground |
| | GND | Ground | F8 | Ground |
| | GND | Ground | G4 | Ground |
| | GND | Ground | G5 | Ground |
| | GND | Ground | G6 | Ground |
| | GND | Ground | G7 | Ground |
| | GND | Ground | H7 | Ground |
| No Connect | NC | DNU | G8 | Not Connect |
| | NC | DNU | H4 | Not Connect |
| | NC | DNU | H5 | Not Connect |
| | NC | DNU | H8 | Not Connect |

**Figure 6. 96-Pin BGA Pin Map for CYPD5225-96BXZI, CYPD5235-96BZXI, and CYPD5236-96BZXI**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | DPLUS_TOP_P1 | DMIN-US_TOP_P1 | SBU1_P1 | SBU2_P1 | VSYS | DPLUS_SYS_P1 | DMIN-US_SYS-_P1 | UART_Tx-_P1 / P4.0 | UART_Rx-_P1 / P4.1 | LSTx_P1 | LSRx_P1 |
| B | DPLUS_BOT_P1 | SWD_DATA/ TBT_RST# / P1.6 | CSN_P1 | VBUS_P_C-TRL_P2 | VBUS_C_C-TRL_P2 | P1.4 / UV_OCP_TRIP_P1 | P1.5 / UV_OC_TRIP_P2 | P3.5 / VCON_OCP_TRIP_P1 | P3.3 / VCON_OCP_TRIP_P2 | VCCD | AUX_P_P1 |
| C | DMIN-US_BOT_P1 | SWD_CLK/ I2C_CFG_EC/ P1.0 | | | | | | | | VDDIO | AUX_N_P1 |
| D | VBUS_P1 | I2C_S-DA_SCB2_TBT/ P1.1 | | | GND | GND | GND | GND | | VDDD | AUX_P_P2 |
| E | SBU1_P2 | I2C_S-CL_SCB2_TBT/ P1.2 | | GND | GND | GND | GND | GND | | HPD_P2 / P3.4 | AUX_N_P2 |
| F | SBU2_P2 | I2C_INT_TBT_P1/ P1.3 | | GND | GND | GND | GND | GND | | SCL_4 / P2.3 | DPLUS_SYS-_P2 |
| G | DPLUS_TOP_P2 | I2C_INT_TBT_P2/ P2.1 | | GND | GND | GND | GND | DNU | | SDA_4 / P3.2 | DMIN-US_SYS_P2 |
| H | DMIN-US_TOP_P2 | CC2_P1 | | DNU | DNU | XRES | GND | DNU | | VSEL_2_P2/ P2.0 | UART_Tx_P2/ P0.1 |
| J | CSP_P1 | V5V_P1 | | | | | | | | SDA_3/ VSEL_2_P1/ P3.6 | UART_Rx_P2 / P0.2 |
| K | DPLUS_BOT_P2 | CC1_P1 | VBUS_P_C-TRL_P1 | VBUS_C_C-TRL_P1 | I2C_S-DA_SCB4/OVP_TRIP_P1 /P2.4 | I2C_S-DA_SCB1_EC / P5.0 | HPD_P1 / P3.0 | CSN_P2 | CC1_P2 | CC2_P2 | LSTx_P2 |
| L | DMIN-US_BOT_P2 | CSP_P2 | VBUS_P2 | VSEL_1_P2 /P0.0 | I2C_INT_EC / P2.5 | I2C_S-CL_SCB1_EC / P5.1 | P3.1 | OVP_TRIP_P2/P2.2 | V5V_P2 | SCL_3 / VSEL_1_P1/ P3.7 | LSRx_P2 |

| |
|---|
| Type-C Port 1 |
| Type-C Port 2 |
| Power Pins |
| GND |
| GPIOs |

Table 4 through Table 7 provide the various configuration options for the serial interfaces.

**Table 4. Serial Communication Block (SCB1) Configuration**

| QFN Pin | BGA Pin | UART | SPI | I²C | GPIO Functionality |
|---|---|---|---|---|---|
| 16 | K6 | – | – | I2C_SDA_SCB1 | GPIO |
| 17 | L6 | – | – | I2C_SCL_SCB1 | GPIO |
| | B8 | UART_CTS_SCB1 | – | – | VCONN OCP output indicator for port 1/ GPIO |
| 20 | J10 | UART_TX_SCB1 | SPI_SEL_SCB1 | – | I2C_SDA_SCB3/ VSEL_2_P1 /GPIO |
| 21 | L10 | UART_RX_SCB1 | SPI_MISO_SCB1 | – | I2C_SCL_SCB3 / VSEL_1_P1/GPIO |
| 18 | K7 | UART_RTS_SCB1 | – | – | HPD_P1/GPIO |
| 29 | A8 | – | SPI_MOSI_SCB1 | – | UART_TX_P1/GPIO |
| 30 | A9 | – | SPI_CLK_SCB1 | – | UART_RX_P1/GPIO |

**Note:** UART TX and RX of the SCB1 is also the I²C SDA and SCL of the SCB3. So if SCB 3 is in use, then SCB1 cannot be used for UART and SPI.

**Table 5. Serial Communication Block (SCB2) Configuration**

| QFN Pin | BGA Pin | UART | SPI Master | I2C Slave | GPIO Functionality |
|---|---|---|---|---|---|
| 2 | C2 | UART_RX_SCB2 | SPI_SEL_SCB2 | – | SWD_CLK/I2C_CFG_EC/GPIO |
| 3 | D2 | UART_TX_SCB2 | SPI_MOSI_SCB2 | I2C_SDA_SCB2 | I2C_SDA_SCB2_TBT/GPIO |
| 4 | E2 | UART_CTS_SCB2 | SPI_MISO_SCB2 | I2C_SCL_SCB2 | I2C_SCL_SCB2_TBT/GPIO |
| 5 | F2 | UART_RTS_SCB2 | SPI_CLK_SCB2 | – | I2C_INT_TBT_P1/GPIO |

**Table 6. Serial Communication Block (SCB3) Configuration**

| QFN Pin | BGA Pin | UART | SPI Master | I²C Slave | GPIO Functionality |
|---|---|---|---|---|---|
| 20 | J10 | – | – | I2C_SDA_SCB3 | UART_TX_SCB1/VSEL_2_P1 /GPIO |
| 21 | L10 | – | – | I2C_SCL_SCB3 | UART_RX_SCB1 / VSEL_1_P1/GPIO |
| | G2 | UART_CTS_SCB3 | SPI_MISO_SCB3 | – | I2C_INT_TBT_P2/GPIO |
| | H10 | UART_TX_SCB3 | SPI_MOSI_SCB3 | – | VSEL_2_P2 / GPIO |
| | L4 | UART_RX_SCB3 | SPI_SEL_SCB3 | – | VSEL_1_P2 / GPIO |
| | L8 | UART_RTS_SCB3 | SPI_CLK_SCB3 | – | OVP_TRIP_P2 / GPIO |

**Table 7. Serial Communication Block (SCB4) Configuration**

| QFN Pin | BGA Pin | UART | SPI Master | I²C Slave | GPIO Functionality |
|---|---|---|---|---|---|
| 13 | F10 | – | – | I2C_SCL_SCB4 | GPIO |
| 14 | G10 | UART_TX_SCB4 | SPI_MOSI_SCB4 | I2C_SDA_SCB4 | GPIO |
| | L7 | UART_CTS_SCB4 | SPI_MISO_SCB4 | – | GPIO |
| | B9 | UART_RX_SCB4 | SPI_SEL_SCB4 | – | VCONN_OCP_TRIP_P2/GPIO |
| | E10 | UART_RTS_SCB4 | SPI_CLK_SCB4 | – | HPD_P2/GPIO |

## Application Diagrams

Figure 8 and Figure 9 illustrate the Dual Type-C Port and Single Type-C port Thunderbolt Notebook DRP application diagrams using a CCG5 device respectively. The Type-C port can be used as a power provider/power consumer.

The CCG5 device communicates with the embedded controller (EC), which manages the Battery Charger Controller (BCC) to control the charging and discharging of the internal battery. It also updates the Thunderbolt Controller via $I^2C$ to route the High-speed signals coming from the Type-C port to the USB host (during normal mode) or the Graphics processor unit (during Display port Alternate mode) or the Thunderbolt Host (during Thunderbolt Alternate mode) based on the alternate mode negotiation.

For the dual Type-C notebook application (Figure 8), these Type-C ports can be power providers or power consumers simultaneously. The CCG5 device controls the transfer of USB 2.0 D± lines from the top and bottom of the Type-C receptacle to the D± lines of the USB Host controller. CCG5 also handles the routing of SBU1 and SBU2 lines from the Type-C receptacle to the Thunderbolt controller for the Link management. CCG5 offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

The CCG5 device has an integrated VCONN FET for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. The 10 mΩ resistor between the 5 V supply and FETs is used for overcurrent detection on the VBUS. The VBUS_P_CTRL pin of CCG5 has an in-built VBUS monitoring circuit that can detect OVP and UVP on VBUS.

CCG5 also has an in-built VBUS discharge circuit that is used to quickly discharge VBUS after the Type-C connection is detached. The internal resistance (as listed in Table 41) of this VBUS discharge circuit is expected to be sufficient for typical CCG5 applications. However, customers can include an optional VBUS discharge circuit as shown in Figure 7 using any available GPIO. This optional circuit can be added to the design if the discharge time using the in-built VBUS discharge circuit needs to be further reduced; that is, VBUS transition time from higher to lower voltages can be further reduced using the external VBUS discharge circuit shown in Figure 7. This optional external circuit comprises of a N-channel MOSFET and the CCG5 device can be used to enable or disable it as appropriate.

**Figure 7. Optional External VBUS Discharge Circuit**

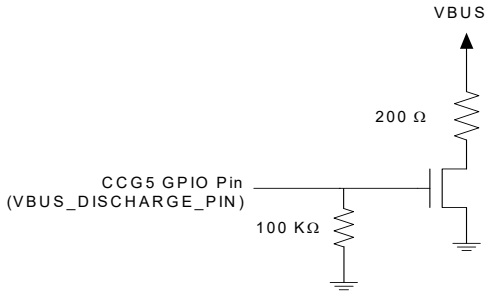


**Figure 8. CCG5 in a Dual Port Notebook Application using CYPD5225-96BZXI**

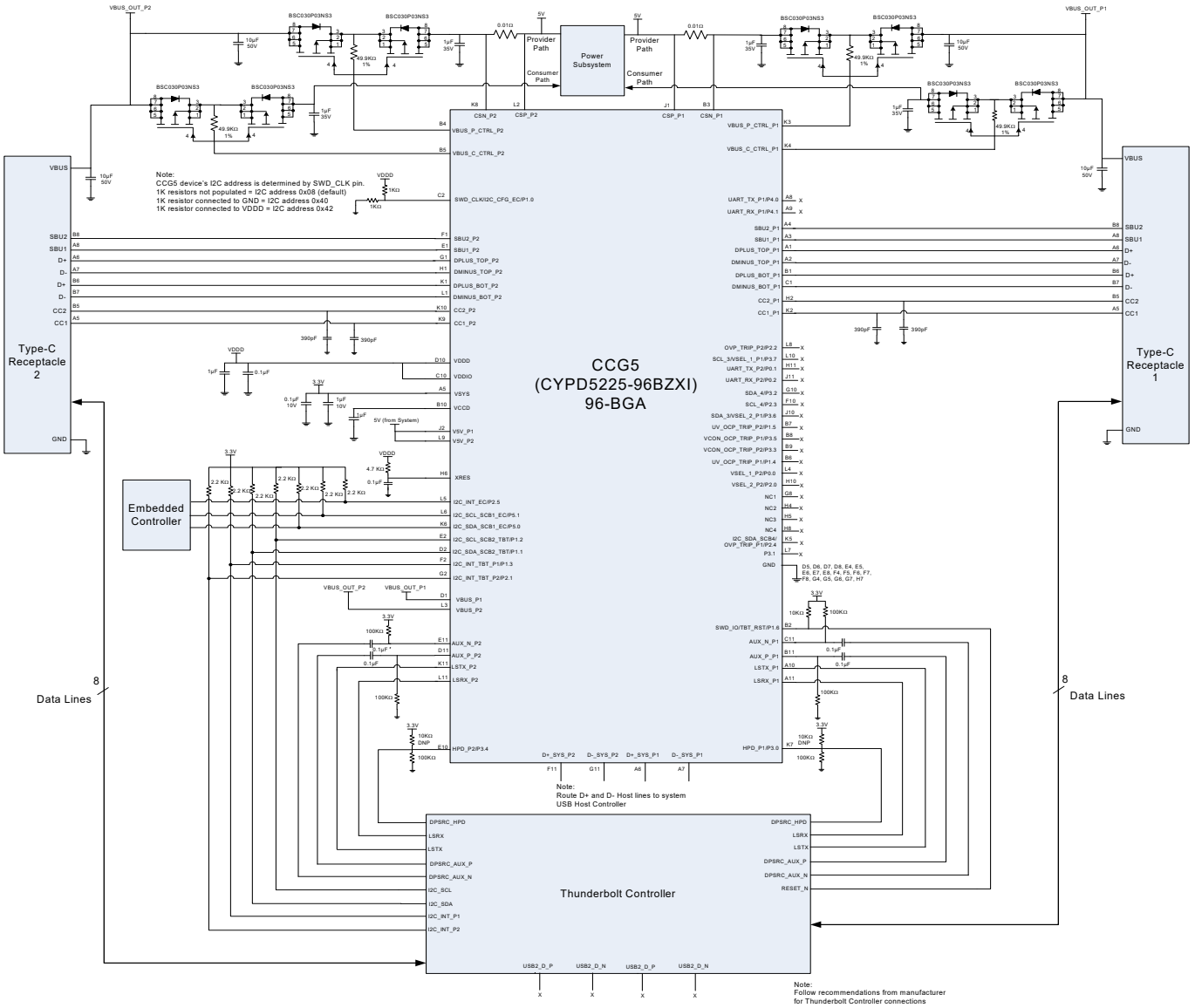


Figure 9 illustrates a Single Port Thunderbolt Notebook DRP application diagram using CYPD5125-40LQXIT.

**Figure 9. CCG5 in a Single Port Notebook Application using CYPD5125-40LQXIT**

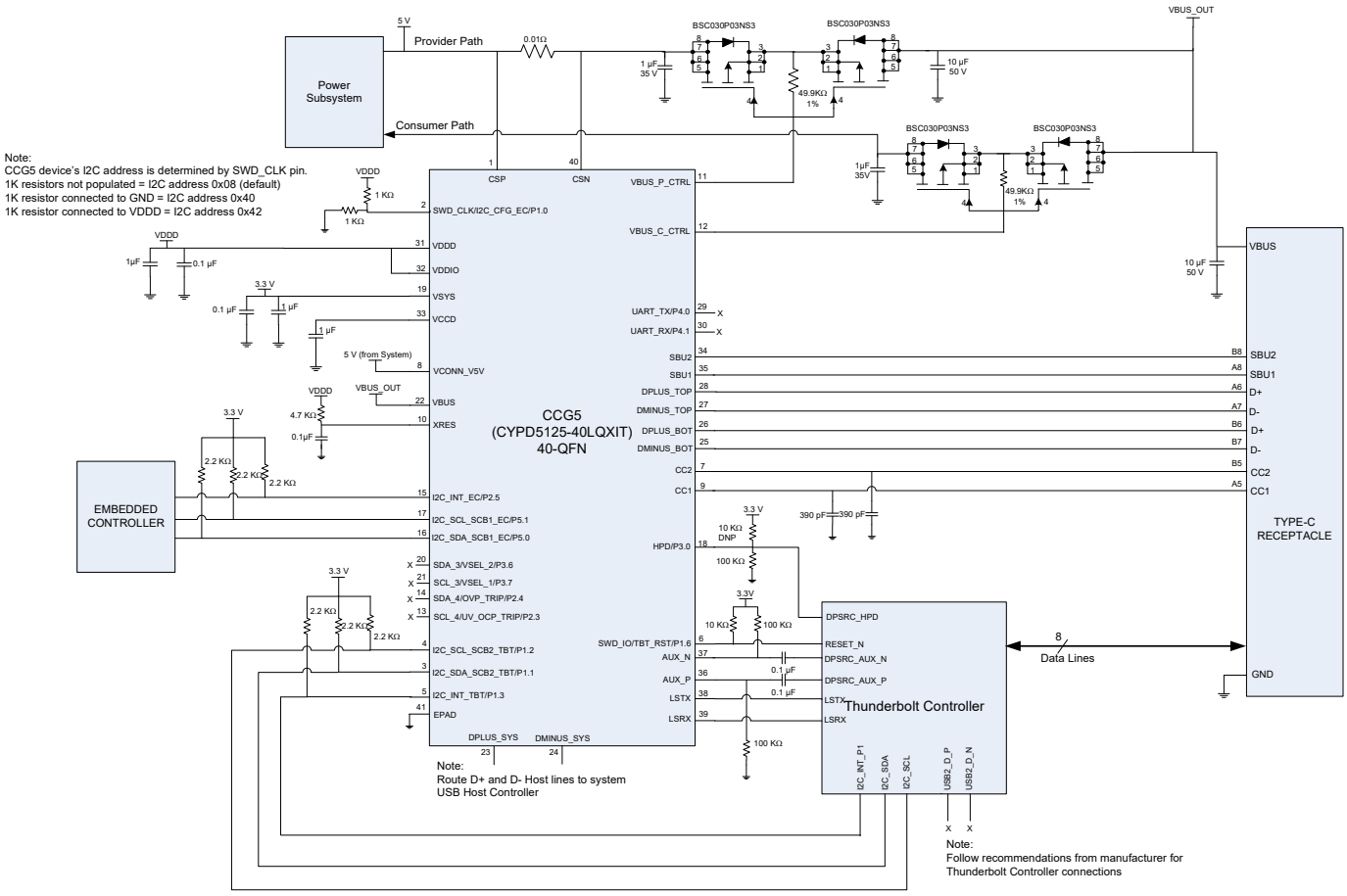


Figure 10 illustrates the Dual Type-C Port Thunderbolt device/dock upstream application diagram using a CCG5 device. The CCG5 device communicates with the power system over I²C, which manages the power provided to the upstream Type-C ports. It also updates the Thunderbolt Controller over I²C based on the alternate mode negotiation to sink Thunderbolt or USB or DisplayPort Data. The CCG5 device controls the transfer of USB 2.0 D± lines from the top and bottom of the Type-C receptacle to the D± lines of the Thunderbolt Controller and Billboard controller. CCG5 also handles the routing of SBU1 and SBU2 lines from the Type-C receptacle to the Thunderbolt controller for the link management. As mentioned in Features, CCG5 offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

**Figure 10. CCG5 in a Dual port Thunderbolt Device/Dock Upstream Port Application using CYPD5235-96BXZI**

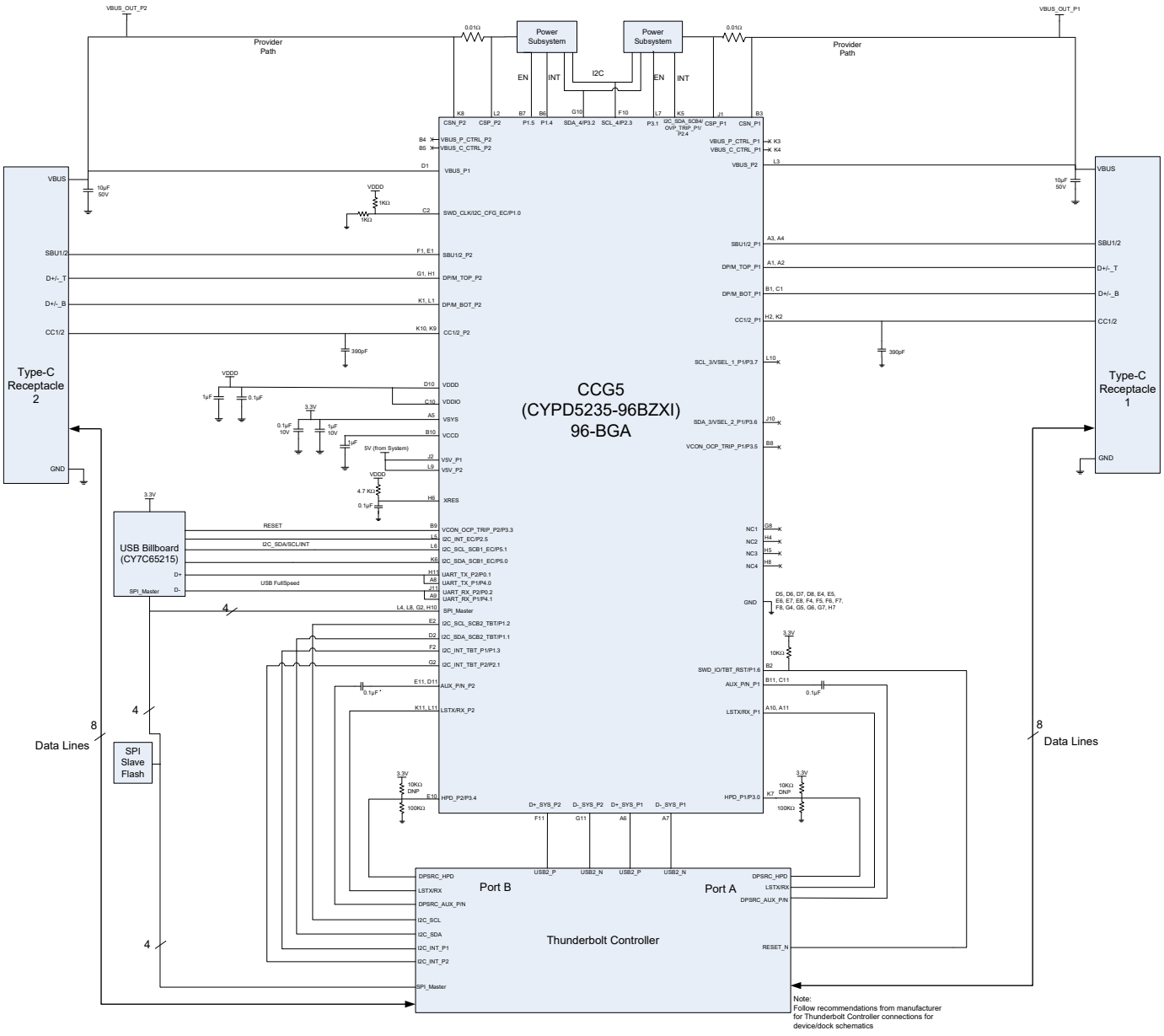
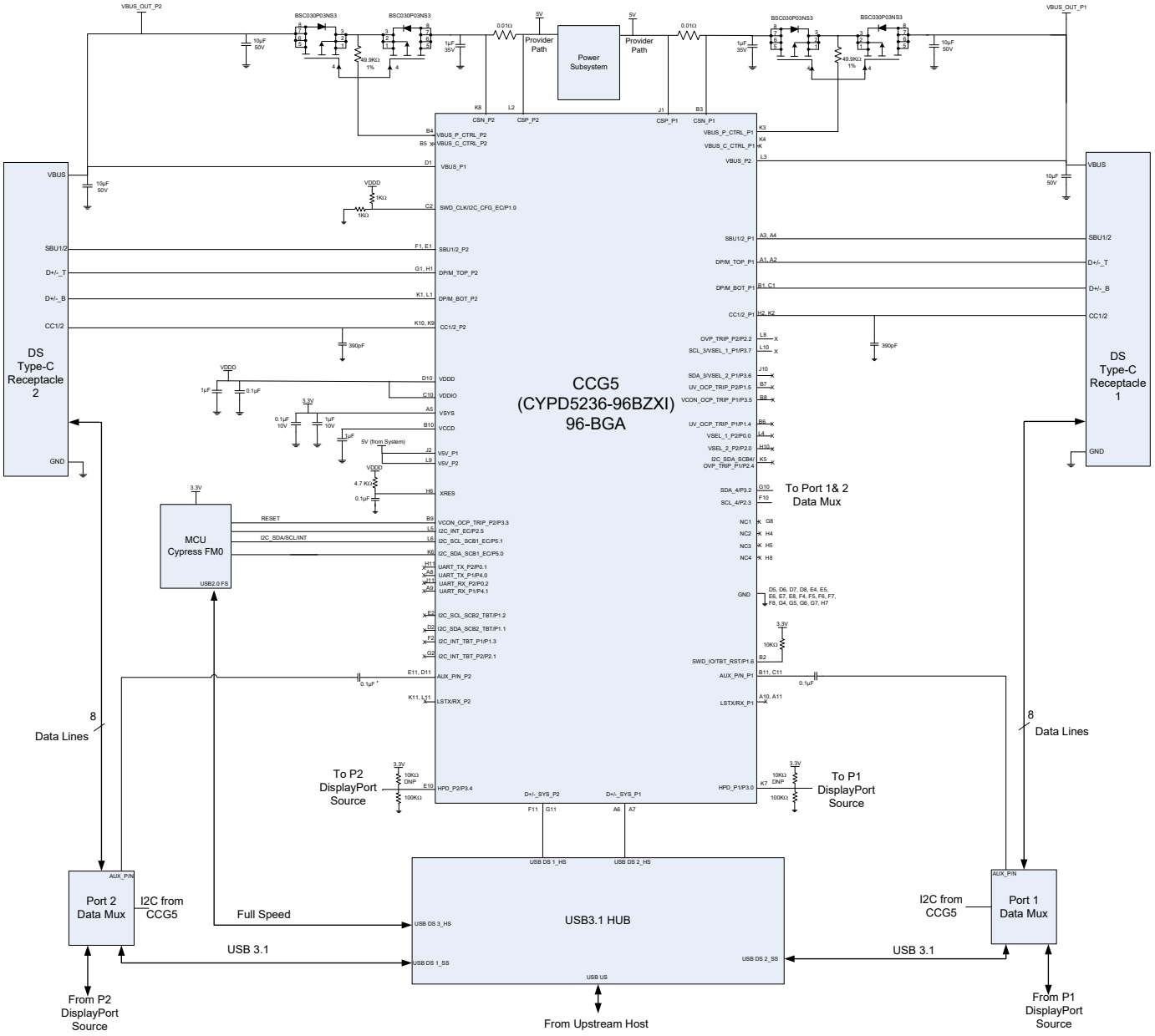


Figure 11 illustrates the Dual Type-C Port dock downstream application diagram using a CCG5 device. The CCG5 negotiates power contract with the connected device on the downstream Type-C port and controls the power system. It also controls the data mux via $I^2C$ based on the alternate mode negotiation to source USB SuperSpeed and/or DisplayPort on the downstream Type-C port. As mentioned above, CCG5 device offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

**Figure 11. CCG5 in a Dual port Dock Downstream Port Application using CYPD5236-96BXZI**



# Electrical Specifications

## Absolute Maximum Ratings

**Table 8. Absolute Maximum Ratings**[3]

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{SYS\_MAX}$ | Digital supply relative to $V_{SS}$ | – | – | 6 | V | Absolute max |
| $V_{5V\_P1\_MAX}$ | Max supply voltage relative to $V_{SS}$ | – | – | 6 | V | |
| $V_{5V\_P2\_MAX}$ | Max supply voltage relative to $V_{SS}$ | – | – | 6 | V | |
| $V_{BUS\_P1\_MAX}$ | Max VBUS voltage relative to Vss | – | – | 24 | V | |
| $V_{BUS\_P2\_MAX}$ | Max VBUS voltage relative to Vss | – | – | 24 | V | |
| $V_{DDIO\_MAX}$ | Max supply voltage relative to $V_{SS}$ | – | – | $V_{DDD}$ | V | |
| $V_{GPIO\_ABS}$ | Inputs to GPIO, DP/DM mux (UART, SYS, DP/DM_top/bot pins), SBU mux (AUX, LS, SBU1/2 pins) | –0.5 | – | $V_{DDIO}$ + 0.5 | V | |
| $I_{GPIO\_ABS}$ | Maximum current per GPIO | –25 | – | 25 | mA | |
| $I_{GPIO\_INJECTION}$ | GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$ | –0.5 | – | 0.5 | mA | Absolute max, current injected per pin |
| ESD_HBM | Electrostatic discharge human body model | 2200 | – | – | V | Applicable for all pins except SBU pins |
| ESD_HBM_SBU[4] | Electrostatic discharge human body model for SBU1, SBU2 pins | 1100 | – | – | V | Only applicable to SBU pins |
| ESD_CDM | Electrostatic discharge charged device model | 500 | – | – | V | – |
| LU | Pin current for latch up | –200 | – | 200 | mA | – |
| ESD_IEC_CON | Electrostatic discharge IEC61000-4-2, contact discharge | 8000 | – | – | V | Contact Discharge for CC1_P1/P2, CC2_P1/P2, VBUS_P1/P2, SBU1_P1/P2, SBU2_P1/P2, DPLUS_TOP/BOT_P1/P2, DMINUX_TOP/BOT_P1/P2 |
| ESD_IEC_AIR | Electrostatic discharge IEC61000-4-2, air discharge | 15000 | – | – | V | Air Discharge for CC1_P1/P2, CC2_P1/P2, VBUS_P1/P2, SBU1_P1/P2, SBU2_P1/P2, DPLUS_TOP/BOT_P1/P2, DMINUX_TOP/BOT_P1/P2 |
| VCC_PIN_ABS | Max voltage on CC1 and CC2 pins | – | – | 24 | V | Absolute max |
| VSBU_PIN_ABS | Max voltage on SBU1 and SBU2 pins | – | – | 24 | V | |
| VGPIO_OVT_ABS | OVT GPIO voltage | –0.5 | – | 6 | V | Absolute maximum for OVT pins K6 and L6 of BGA, pins 16 and 17 of QFN |

**Notes**
3. Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
4. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

## Device-Level Specifications

All specifications are valid for –40 °C ≤ $T_A$ ≤ 85 °C and $T_J$ ≤ 100 °C, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

**Table 9. DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.PWR#23 | $V_{SYS}$ | Power supply input voltage | 2.75 | – | 5.5 | V | UFP applications |
| SID.PWR#23_A | $V_{SYS}$ | Power supply input voltage | 3.15 | – | 5.5 | V | DFP/DRP applications |
| SID.PWR#22 | $V_{BUS}$ | VBUS_P1 and VBUS_P2 valid range | 4 | – | 21.5 | V | – |
| SID.PWR#1 | $V_{DDD}$ | Regulated output voltage when $V_{SYS}$ is powered | $V_{SYS}$ – 0.05 | – | $V_{SYS}$ | V | – |
| SID.PWR#1_A | $V_{DDD}$ | Regulated output voltage when $V_{BUS}$ powered | 3.15 | – | 3.6 | V | – |
| SID.PWR#26 | $V_{5V\_P1}$ and $V_{5V\_P2}$ | Power supply Input voltage | 4.85 | – | 5.5 | V | – |
| SID.PWR#13 | $V_{DDIO}$ | GPIO power supply | $V_{DDD}$ | – | $V_{DDD}$ | V | At system-level short the $V_{DDIO}$ to $V_{DDD}$ |
| SID.PWR#24 | $V_{CCD}$ | Output voltage (for Core Logic) | – | 1.8 | – | V | – |
| SID.PWR#15 | $C_{EFC}$ | External regulator voltage bypass on $V_{CCD}$ | 80 | 100 | 120 | nF | X5R ceramic or better |
| SID.PWR#16 | $C_{EXC}$ | Power supply decoupling capacitor on $V_{DDD}$ | – | 1 | – | µF | |
| SID.PWR#27 | $C_{EXV}$ | Power supply decoupling capacitor on V5V_P1 and V5V_P2 | – | 0.1 | – | µF | |
| SID.PWR#5 | $I_{VDDD\_EXT}$ | External load current on $V_{DDD}$ either in Active or Deep Sleep mode | – | 1 | 2 | mA | – |
| **Active Mode, $V_{SYS}$ = 2.75 to 5.5 V. Typical values measured at $V_{SYS}$ = 3.3 V** | | | | | | | |
| SID.PWR#4 | $I_{DD12}$ | Supply current | – | 10 | – | mA | $T_A$ = 25 °C, CC I/O IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, two PD ports active |
| **Deep Sleep Mode, $V_{SYS}$ = 2.75 to 3.6 V** | | | | | | | |
| SID34 | $I_{DD29}$ | $V_{SYS}$ = 2.75 to 3.6 V, $I^2C$, wakeup and WDT on. | – | 150 | – | µA | $V_{SYS}$ = 3.3 V, $T_A$ = 25 °C, |
| SID34A | $I_{DD29A}$ | | – | 160 | – | µA | $V_{SYS}$ = 3.3 V, $T_A$ = 25 °C for two PD ports |
| SID_DS1 | $I_{DD\_DS1}$ | $V_{SYS}$ = 3.3 V, CC wakeup on, Type-C not connected. | – | 100 | – | µA | Power source = $V_{SYS}$, Type-C not attached, CC enabled for wakeup, Rp and Rd connected at 70-ms intervals by CPU. Rp, Rd connection should be enabled for both PD ports. |
| SID_DS3 | $I_{DD\_DS2}$ | $V_{SYS}$ = 3.3 V, CC wakeup on, DP/DM, SBU ON with ADC/CSA/UVOV On | – | 500 | – | µA | IDD_DS1 + DP/DM, SBU, CC ON, ADC/CSA/UVOV ON |
| **XRES Current** | | | | | | | |
| SID307 | $I_{DD\_XR}$ | Supply current while XRES asserted | – | 130 | – | µA | Power Source = $V_{SYS}$ = 3.3 V, Type-C not attached, $T_A$ = 25 °C |

**Table 10. AC Specifications (Guaranteed by Characterization)**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.CLK#4 | $F_{CPU}$ | CPU input frequency | – | – | 48 | MHz | All $V_{DDD}$ |
| SID.PWR#21 | $T_{DEEPSLEEP}$ | Wakeup from Deep Sleep mode | – | 35 | – | µs | Guaranteed by characterization |
| SYS.XRES#5 | $T_{XRES}$ | External reset pulse width | 5 | – | – | µs | |
| SYS.FES#1 | $T_{\_PWR\_RDY}$ | Power-up to “Ready to accept $I^2C$/CC command” | – | 5 | 25 | ms | |

**Table 11. I/O DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.GIO#37 | $V_{IH\_CMOS}$ | Input voltage HIGH threshold | 0.7 × $V_{DDIO}$ | – | – | V | CMOS input |
| SID.GIO#38 | $V_{IL\_CMOS}$ | Input voltage LOW threshold | – | – | 0.3 × $V_{DDIO}$ | V | CMOS input |
| SID.GIO#39 | $V_{IH\_VDDIO2.7-}$ | LVTTL input, $V_{DDIO}$ < 2.7 V | 0.7 × $V_{DDIO}$ | – | – | V | – |
| SID.GIO#40 | $V_{IL\_VDDIO2.7-}$ | LVTTL input, $V_{DDIO}$ < 2.7 V | – | – | 0.3 × $V_{DDIO}$ | V | – |
| SID.GIO#41 | $V_{IH\_VDDIO2.7+}$ | LVTTL input, $V_{DDIO} \geq$ 2.7 V | 2.0 | – | – | V | – |
| SID.GIO#42 | $V_{IL\_VDDIO2.7+}$ | LVTTL input, $V_{DDIO} \geq$ 2.7 V | – | – | 0.8 | V | – |
| SID.GIO#33 | $V_{OH}$ | Output voltage HIGH level | $V_{DDIO}$ – 0.6 | – | – | V | $I_{OH}$ = –4 mA at 3 V $V_{DDIO}$ |
| SID.GIO#34 | $V_{OH}$ | Output voltage HIGH level | $V_{DDIO}$ – 0.5 | – | – | V | $I_{OH}$ = –1mA at 1.8 V $V_{DDIO}$ |
| SID.GIO#35 | $V_{OL}$ | Output voltage LOW level | – | – | 0.6 | V | $I_{OL}$ = 4 mA at 1.8 V $V_{DDIO}$ |
| SID.GIO#36 | $V_{OL}$ | Output voltage LOW level | – | – | 0.6 | V | $I_{OL}$ = 10 mA (IOL_LED) at 3 V $V_{DDIO}$ |
| SID.GIO#5 | $R_{PU}$ | Pull-up resistor value | 3.5 | 5.6 | 8.5 | kΩ | +25 °C $T_A$, All $V_{DDIO}$ |
| SID.GIO#6 | $R_{PD}$ | Pull-down resistor value | 3.5 | 5.6 | 8.5 | kΩ | +25 °C $T_A$, All $V_{DDIO}$ |
| SID.GIO#16 | $I_{IL}$ | Input leakage current (absolute value) | – | – | 2 | nA | +25 °C $T_A$, 3-V $V_{DDIO}$ |
| SID.GIO#17 | $C_{PIN}$ | Max pin capacitance | – | 3 | 7 | pF | – |
| SID.GIO#43 | $V_{HYSTTL}$ | Input hysteresis, LVTTL | 15 | 40 | – | mV | $V_{DDIO}$ > 2.7 V. Guaranteed by characterization. |
| SID.GIO#44 | $V_{HYSCMOS}$ | Input hysteresis CMOS | 0.05 × $V_{DDIO}$ | – | – | mV | $V_{DDIO}$ < 4.5 V |
| SID.GIO#44A | $V_{HYSCMOS55}$ | Input hysteresis CMOS | 200 | – | – | mV | $V_{DDIO}$ > 4.5 V |

**Table 12. I/O AC Specifications (Guaranteed by Characterization)**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID70 | $T_{RISEF}$ | Rise time in Fast Strong mode | 2 | – | 12 | ns | 3.3-V $V_{DDIO}$, $C_{load}$ = 25 pF |
| SID71 | $T_{FALLF}$ | Fall time in Fast Strong mode | 2 | – | 12 | ns | 3.3-V $V_{DDIO}$, $C_{load}$ = 25 pF |
| SID.GIO#46 | $T_{RISES}$ | Rise time in Slow Strong mode | 10 | – | 60 | ns | 3.3-V $V_{DDIO}$, $C_{load}$ = 25 pF |
| SID.GIO#47 | $T_{FALLS}$ | Fall time in Slow Strong mode | 10 | – | 60 | ns | 3.3-V $V_{DDIO}$, $C_{load}$ = 25 pF |
| SID.GIO#48 | $F_{GPIO\_OUT1}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DDIO}$ ≤ 5.5 V. Fast Strong mode. | – | – | 16 | MHz | 90/10%, 25 pF load |
| SID.GIO#49 | $F_{GPIO\_OUT2}$ | GPIO $F_{OUT}$; 1.7 V ≤ $V_{DDIO}$ ≤ 3.3 V. Fast Strong mode. | – | – | 16 | MHz | 90/10%, 25 pF load |
| SID.GIO#50 | $F_{GPIO\_OUT3}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DDIO}$ ≤ 5.5 V. Slow Strong mode. | – | – | 7 | MHz | 90/10%, 25 pF load |

**Table 12. I/O AC Specifications (Guaranteed by Characterization)** *(continued)*

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.GIO#51 | $F_{GPIO\_OUT4}$ | GPIO $F_{OUT}$; 1.7 V ≤ $V_{DDIO}$ ≤ 3.3 V. Slow Strong mode. | – | – | 3.5 | MHz | 90/10%, 25 pF load |
| SID.GIO#52 | $F_{GPIO\_IN}$ | GPIO input operating frequency; 1.7 V ≤ $V_{DDIO}$ ≤ 5.5 V. | – | – | 16 | MHz | 90/10% $V_{IO}$ |

*XRES*

**Table 13. XRES DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.XRES#1 | $V_{IH}$ | Input voltage HIGH threshold | 0.7 x $V_{DDIO}$ | – | – | V | CMOS input |
| SID.XRES#2 | $V_{IL}$ | Input voltage LOW threshold | – | – | 0.3 x $V_{DDIO}$ | V | CMOS input |
| SID.XRES#3 | $C_{IN}$ | Input capacitance | – | – | 7 | pF | – |
| SID.XRES#4 | $V_{HYSXRES}$ | Input voltage hysteresis | – | 0.05 x $V_{DDIO}$ | – | mV | Guaranteed by characterization |

## Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

*PWM for GPIO Pins*

**Table 14. PWM AC Specifications** (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.TCPWM.3 | $T_{CPWMFREQ}$ | Operating frequency | – | – | Fc | MHz | Fc max = CLK_SYS. Maximum = 48 MHz. |
| SID.TCPWM.4 | $T_{PWMENEXT}$ | Input trigger pulse width | 2/Fc | – | – | ns | For all trigger events |
| SID.TCPWM.5 | $T_{PWMEXT}$ | Output trigger pulse width | 2/Fc | – | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs |
| SID.TCPWM.5A | $T_{CRES}$ | Resolution of counter | 1/Fc | – | – | ns | Minimum time between successive counts |
| SID.TCPWM.5B | $PWM_{RES}$ | PWM resolution | 1/Fc | – | – | ns | Minimum pulse width of PWM output |
| SID.TCPWM.5C | $Q_{RES}$ | Quadrature inputs resolution | 1/Fc | – | – | ns | Minimum pulse width between quadrature-phase inputs |

**Table 15. Fixed $I^2C$ AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID153 | $F_{I2C1}$ | Bit rate | – | – | 1 | Mbps | – |

**Table 16. Fixed UART AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID162 | $F_{UART}$ | Bit rate | – | – | 1 | Mbps | – |

**Table 17. Fixed SPI AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID166 | $F_{SPI}$ | SPI operating frequency (Master; 6X oversampling) | – | – | 8 | MHz | – |

**Table 18. Fixed SPI Master Mode AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID167 | $T_{DMO}$ | MOSI valid after SClock driving edge | – | – | 15 | ns | – |
| SID168 | $T_{DSI}$ | MISO valid before SClock capturing edge | 20 | – | – | ns | Full clock, late MISO sampling |
| SID169 | $T_{HMO}$ | Previous MOSI data hold time | 0 | – | – | ns | Referred to slave capturing edge |

**Table 19. Fixed SPI Slave Mode AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID170 | $T_{DMI}$ | MOSI Valid before Sclock capturing edge | 40 | – | – | ns | – |
| SID171 | $T_{DSO}$ | MISO Valid after Sclock driving edge | – | – | $48 + 3 \times T_{SCB}$ | ns | $T_{SCB} = T_{CPU}$ |
| SID171A | $T_{DSO\_EXT}$ | MISO Valid after Sclock driving edge in Ext Clk mode | – | – | 48 | ns | – |
| SID172 | $T_{HSO}$ | Previous MISO data hold time | 0 | – | – | ns | – |
| SID172A | $T_{SSELSCK}$ | SSEL Valid to first SCK Valid edge | 100 | – | – | ns | – |

*Memory*

**Table 20. Flash AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.MEM#4 | $T_{ROW\_WRITE}$ | Row (Block) write time (erase and program) | – | – | 20 | ms | – |
| SID.MEM#3 | $T_{ROW\_ERASE}$ | Row erase time | – | – | 13 | ms | – |
| SID.MEM#8 | $T_{ROWPROGRAM}$ | Row program time after erase | – | – | 7 | ms | 25 °C to 55 °C, All $V_{DDD}$ |
| SID178 | $T_{BULKERASE}$ | Bulk erase time (128 KB) | – | – | 35 | ms | Guaranteed by design |
| SID180 | $T_{DEVPROG}$ | Total device program time | – | – | 25 | s | Guaranteed by design |
| SID.MEM#6 | $F_{END}$ | Flash endurance | 100k | – | – | cycles | – |
| SID182 | $F_{RET1}$ | Flash retention, $T_A \le 55$ °C, 100K P/E cycles | 20 | – | – | years | – |
| SID182A | $F_{RET2}$ | Flash retention, $T_A \le 85$ °C, 10K P/E cycles | 10 | – | – | years | – |