Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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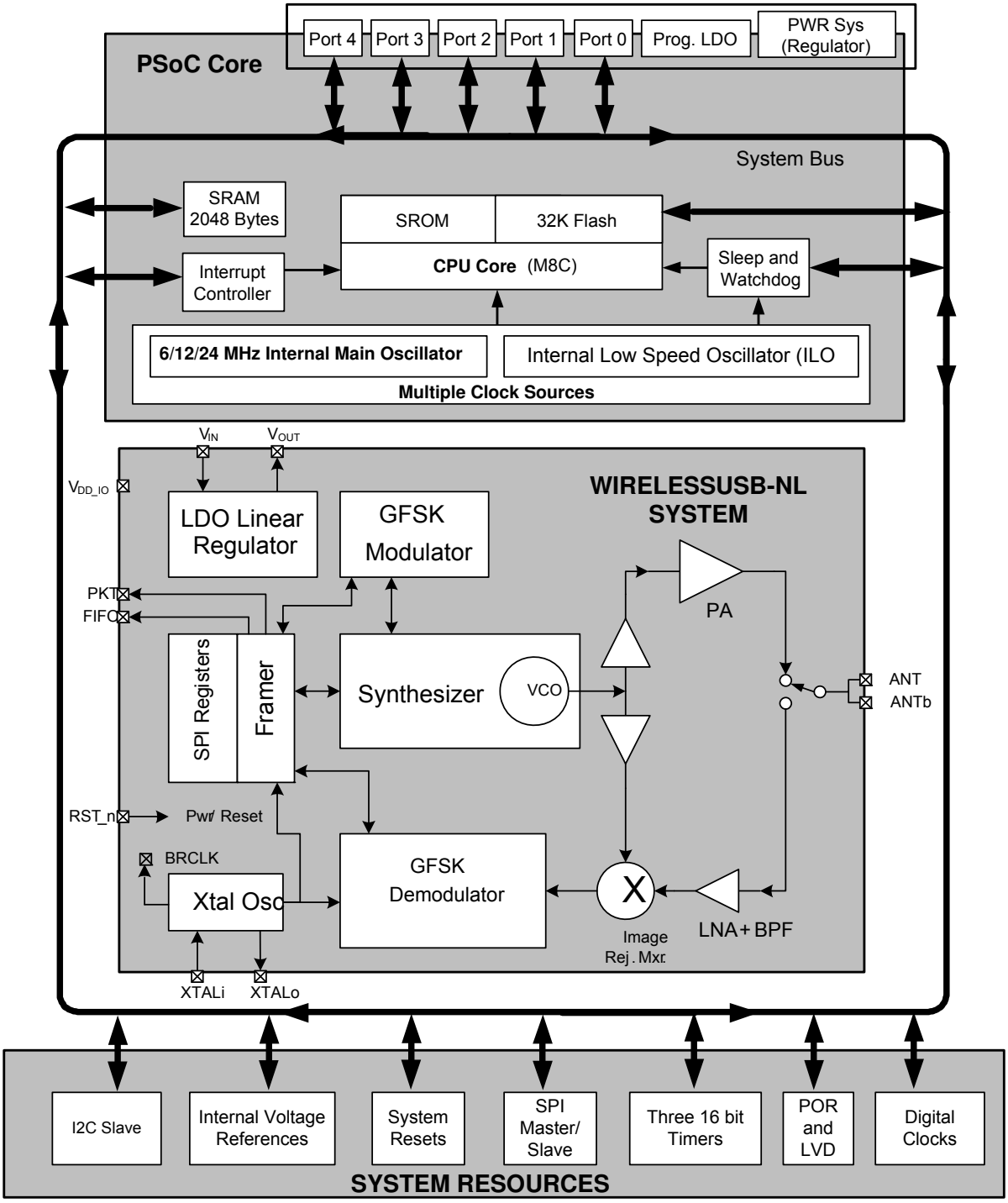
CYRF89135

PRoC™ - Embedded

PRoC™ – Embedded Features

- Single Device, two functions
  - 8-bit flash based MCU function and 2.4-GHz WirelessUSB™ NL radio transceiver function in a single device
- RF Attributes
  - Wide operating range: 1.9 V to 3.6 V
  - 2.4-GHz WirelessUSB NL Transceiver function
  - Operates in the 2.4-GHz ISM Band (2.402 GHz–2.479 GHz)
  - 1-Mbps over-the-air data rate
  - Receive sensitivity typical: –87 dBm
  - 1 µA typical current consumption in sleep state
  - Closed-loop frequency synthesis
  - Supports frequency-hopping spread spectrum
  - On-chip packet framer with 64-byte first in first out (FIFO) data buffer
  - Built-in auto-retry-acknowledge protocol simplifies usage
  - Built-in cyclic redundancy check (CRC), forward error correction (FEC), data whitening
  - Additional outputs for interrupt request (IRQ) generation
  - Digital readout of received signal strength indication (RSSI)
- MCU Attributes
  - Powerful Harvard-architecture processor
  - M8C CPU – Up to 4 MIPS with 24 MHz Internal clock, external crystal resonator or clock signal
  - Low power at high speed
- Temperature range: 0 °C to +70 °C
- Flexible on-chip memory
  - 32 KB Flash/2 KB SRAM
  - 50,000 flash erase/write cycles
  - Partial flash updates
  - Flexible protection modes
  - In-system serial programming (ISSP)
- Precision, programmable clocking
  - Internal main oscillator (IMO): 6/12/24 MHz ± 5%
  - Internal low-speed oscillator (ILO) at 32 kHz for watchdog and sleep timers
  - Precision 32 kHz oscillator for optional external crystal
- Programmable pin configurations
  - Up to 35 general-purpose I/Os (GPIOs)
  - Dual mode GPIO: All GPIOs support digital I/O and analog inputs
  - 25-mA sink current on each GPIO
    - 120 mA total sink current on all GPIOs
  - Pull-up, high Z, open-drain modes on all GPIOs
  - CMOS drive mode –5 mA source current on ports 0 and 1 and 1 mA on port 2
  - 20 mA total source current on port 1.
  - Configurable input threshold for Port 1.
- Versatile analog system
  - Low-dropout voltage regulator for all analog resources
  - High power supply rejection ratio (PSRR) comparator
  - 8 to 10-bit incremental analog-to-digital converter (ADC)
- Additional system resources
  - I^2C slave:
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
  - SPI master and slave: Configurable 46.9 kHz to 12 MHz
  - Three 16-bit timers
  - Watchdog and sleep timers
  - Integrated supervisory circuit
  - Emulated E2PROM using flash memory
- Complete development tools
  - Free development tool (PSoC Designer™)
  - Full-featured, in-circuit emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- Package option
  - 68-pin 8mm × 8mm × 1.0 mm QFN

Logical Block Diagram



Contents

PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logical Block Diagram on page 2, consists of three main areas:

- The Core
- WirelessUSB NL System
- System Resources.

A common, versatile bus allows connection between I/O and the analog system.

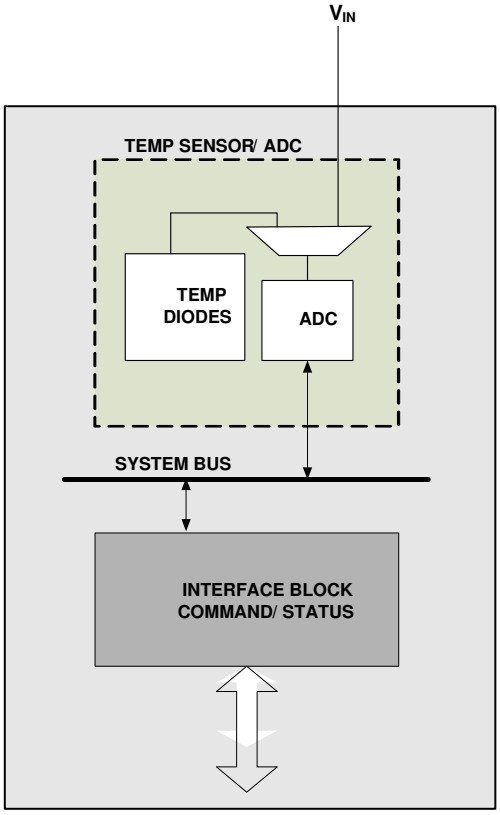
PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

System Resources provide additional capability, such as a configurable I^2C slave and SPI master-slave communication interface and various system resets supported by the M8C.

10 bit ADC

The ADC on PRoC-EMB is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog Mux Bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.



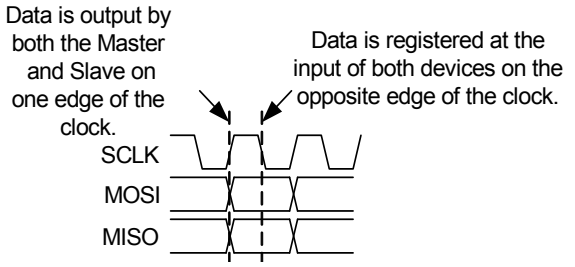
Interface to the M8 C (Processor) Core

The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the Analog Global Input Mux or the temperature sensor with an input voltage range of 0 V to 1.3 V, where 1.3 V is 72% of full scale.

SPI

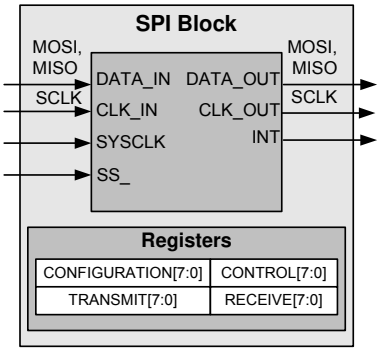
The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

Figure 1. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

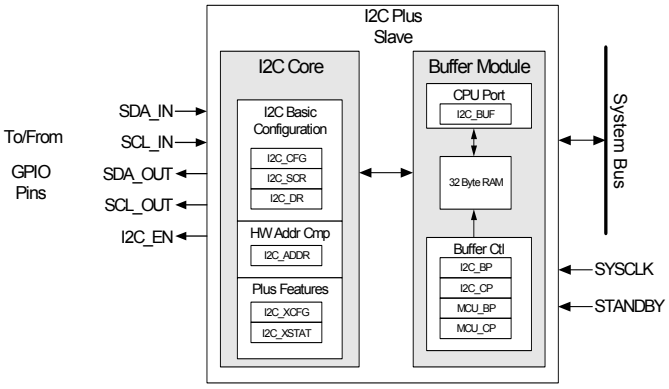
A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.



I²C Slave

The I²C slave enhanced communications block is a serial-to-parallel processor, designed to interface the PRoC-EMB device to a two-wire I²C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I²C-specific support for status detection and generation of framing bits. By default, the I²C Slave Enhanced module is firmware compatible with the previous generation of I²C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing.

Figure 2. I²C Block Diagram



The basic I2C features include

- Slave, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for clock rates of up to 400 kHz
- 7- or 10-bit addressing (through firmware support)
- SMBus operation (through firmware support)

Enhanced features of the I²C Slave Enhanced Module include:

- Support for 7-bit hardware address compare
- Flexible data buffering schemes
- A ‘no bus stalling’ operating mode

A low power bus monitoring modeThe I²C block controls the data (SDA) and the clock (SCL) to the external I²C interface through direct connections to two dedicated GPIO pins. When I²C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V LV CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

WirelessUSB NL System

WirelessUSB NL, optimized to operate in the 2.4-GHz ISM band, is Cypress's third generation of 2.4-GHz low-power RF technology. WirelessUSB NL implements a Gaussian frequency-shift keying (GFSK) radio using a differentiated single-mixer, closed-loop modulation design that optimizes power efficiency and interference immunity. Closed-loop modulation effectively eliminates the problem of frequency drift, enabling WirelessUSB NL to transmit up to 255-byte payloads without repeatedly having to pay power penalties for re-locking the phase-locked loop (PLL) as in open-loop designs

Among the advantages of WirelessUSB NL are its fast lock times and channel switching, along with the ability to transmit larger payloads. Use of longer payload packets, compared to multiple short payload packets, can reduce overhead, improve overall power efficiency, and help alleviate spectrum crowding.

Combined with Cypress's controller, WirelessUSB NL also provides the lowest bill of materials (BOM) cost solution for sophisticated PC peripheral applications such as wireless keyboards and mice, as well as best-in-class wireless performance in other demanding applications. such as toys, remote controls, fitness, automation, presenter tools, and gaming.

With PRoC-EMB 68-pin QFN, the WirelessUSB NL transceiver can add wireless capability to a wide variety of applications.

The WirelessUSB NL is a fully-integrated CMOS RF transceiver, GFSK data modem, and packet framer, optimized for use in the 2.4-GHz ISM band. It contains transmit, receive, RF synthesizer, and digital modem functions, with few external components. The transmitter supports digital power control. The receiver uses extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments.

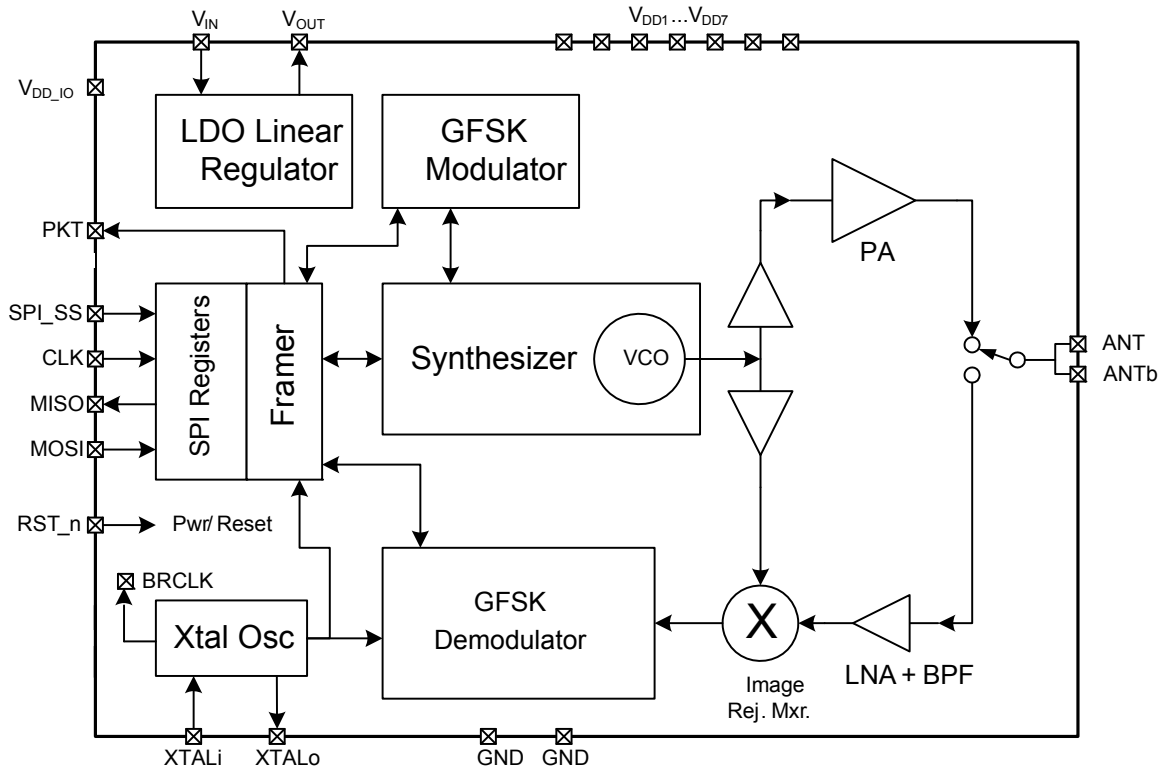
The product transmits GFSK data at approximately 0-dBm output power. Sigma-Delta PLL delivers high-quality DC-coupled transmit data path.

The low-IF receiver architecture produces good selectivity and image rejection, with typical sensitivity of –87 dBm or better on most channels. Sensitivity on channels that are integer multiples of the crystal reference oscillator frequency (12 MHz) may show approximately 5 dB degradation. Digital RSSI values are available to monitor channel quality.

On-chip transmit and receive FIFO registers are available to buffer the data transfer with MCU. Over-the-air data rate is always 1 Mbps even when connected to a slow, low-cost MCU. Built-in CRC, FEC, data whitening, and automatic retry/acknowledge are all available to simplify and optimize performance for individual applications.

For more details on the radio's implementation details and timing requriements, please go through the WirelessUSB NL datasheet in www.cypress.com.

Figure 3. WirelessUSB NL logic Block Diagram



Transmit Power Control

The following table lists recommended settings for register 9 for short-range applications, where reduced transmit RF power is a desirable trade off for lower current.

Table 1. Transmit Power Control

Power Setting Description	Typical Transmit Power (dBm)	Register 9
PA0 - Highest power	+1	0x1820
PA2 - High power	0	0x1920
PA4 - High power	–3	0x1A20
PA8 - Low power	–7.5	0x1C20
PA12 - Lower power	–11.2	0x1E20

Power-on and Register Initialization Sequence

For proper initialization at power up, V_{IN} must ramp up at the minimum overall ramp rate no slower than shown by T_{VIN} specification in the following figure. During this time, the RST_n line must track the V_{IN} voltage ramp-up profile to within approximately 0.2 V. Since most MCU GPIO pins automatically default to a high-Z condition at power up, it only requires a pull-up resistor. When power is stable and the MCU POR releases, and MCU begins to execute instructions, RST_n must then be pulsed low as shown in Figure 13, followed by writing Reg[27 = 0x4200. During or after this SPI transaction, the State Machine status can be read to confirm FRAMER_ST = 1, indicating a proper initialization.

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource:

- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- The 3.6 V maximum input, 1.8, 2.5, or 3 V selectable output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand the PRoC-EMB silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the enCoRe-V LV.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

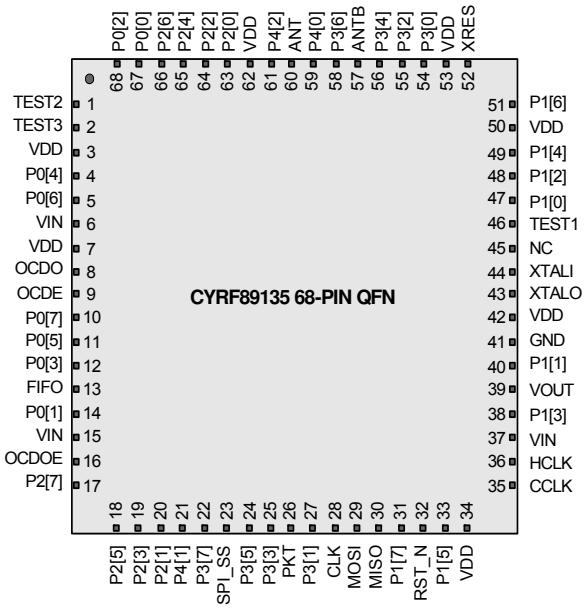
A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. The interface lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pinouts

The CYRF89135-68LTXC PRoC-EMB device is available in a 68-pin QFN package, which is illustrated in the following table. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{DD}, and XRES are not capable of Digital I/O.

Figure 4. 68-pin QFN pinout



Pin Definitions

This table gives the pin definitions. [1, 2]

Pin No.	Pin Name	Description
1	TEST2	Reserved for factory test. Do not connect.
2	TEST3	Reserved for factory test. Do not connect.
3	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin
4	P0[4]	Analog I/O, Digital I/O, VREF
5	P0[6]	Analog I/O, Digital I/O
6	VIN	Unregulated input voltage to the on-chip low drop out (LDO) voltage regulator.
7	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
8	OCDO	OCD odd data IO, NC
9	OCDE	OCD even data output, NC
10	P0[7]	Analog I/O, Digital I/O,SPI CLK
11	P0[5]	Analog I/O, Digital I/O

Notes
1. Connect all VDD pin to VOUT pin.
2. Each of the ANT and ANTB pins much be DC grounded, 20 kΩ or less.

Pin Definitions *(continued)*

This table gives the pin definitions. [1, 2]

Pin No.	Pin Name	Description
12	P0[3]	Analog I/O, Digital I/O, Integrating input
13	FIFO	FIFO status indicator bit
14	P0[1]	Analog I/O, Digital I/O, Integrating input
15	VIN	Unregulated input voltage to the on-chip low drop out (LDO) voltage regulator.
16	OCDOE	OCD mode direction pin, NC
17	P2[7]	Analog I/O, Digital I/O
18	P2[5]	Analog I/O, Digital I/O, XTAL Out
19	P2[3]	Analog I/O, Digital I/O, XTAL In
20	P2[1]	Analog I/O, Digital I/O
21	P4[1]	Analog I/O, Digital I/O
22	P3[7]	Analog I/O, Digital I/O
23	SPI_SS	Enable input for SPI, active low. Also used to bring device out of sleep state.
24	P3[5]	Analog I/O, Digital I/O
25	P3[3]	Analog I/O, Digital I/O
26	PKT	Transmit/receive packet status indicator bit
27	P3[1]	Analog I/O, Digital I/O
28	CLK	Clock input for SPI interface
29	MOSI	Data input for the SPI bus
30	MISO	Data output (tristate when not active)
31	P1[7]	Digital I/O, Analog I/O, I2C SCL, SPI SS
32	RST_N	RST_N Low: Chip shutdown to conserve power. Register values lost RST_N High: Turn on chip, registers restored to default value
33	P1[5]	Digital I/O, Analog I/O, I2C SDA, SPI MISO
34	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
35	CCLK	OCD CPU CLK OUTPUT, NC
36	HCLK	OCD HIGH SPEED CLK, NC
37	VIN	Unregulated input voltage to the on-chip low drop out (LDO) voltage regulator
38	P1[3]	Digital I/O, Analog I/O, SPI CLK
39	VOUT	1.8 V output from on-chip LDO. Connect to all Vdd pins, do not connect to external loads.
40	P1[1]	Digital I/O, Analog I/O, TC CLK, I2C SCL, SPI MOSI
41	GND	Ground Pin
42	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
43	XTALO	Output of the crystal oscillator gain block
44	XTALI	Input to the crystal oscillator gain block
45	NC	No Connect
46	TEST1	Reserved for factory test. Do not connect.
47	P1[0]	Analog I/O, Digital I/O, TC DATA, I2C SDA
48	P1[2]	Analog I/O, Digital I/O
49	P1[4]	Analog I/O, Digital I/O, EXT CLK
50	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.

Pin Definitions *(continued)*

This table gives the pin definitions. [1, 2]

Pin No.	Pin Name	Description
51	P1[6]	Analog I/O, Digital I/O
52	XRES	Active high external reset with internal pull down
53	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
54	P3[0]	Analog I/O, Digital I/O
55	P3[2]	Analog I/O, Digital I/O
56	P3[4]	Analog I/O, Digital I/O.
57	ANTb	Differential RF input/output.
58	P3[6]	Analog I/O, Digital I/O.
59	P4[0]	Analog I/O, Digital I/O.
60	ANT	Differential RF input/output.
61	P4[2]	Analog I/O, Digital I/O.
62	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
63	P2[0]	Analog I/O, Digital I/O
64	P2[2]	Analog I/O, Digital I/O
65	P2[4]	Analog I/O, Digital I/O
66	P2[6]	Analog I/O, Digital I/O
67	P0[0]	Analog I/O, Digital I/O
68	P0[2]	Analog I/O, Digital I/O

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 2. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	25	125	°C
V_{IN}		–	1.9	–	3.63	V
V_{DD}	Supply voltage	–	–0.5	–	1.98	V
V_{IO}	DC input voltage	–	–0.5	–	VDD + 0.5	V
V_{IOZ}[3]	DC voltage applied to tristate	–	–0.5	–	VDD + 0.5	V
I_{MIO}	Maximum current into any port pin	–	–25	–	50	mA
ESD	Electrostatic discharge voltage	Human body model ESD i) RF pins (ANT, ANTb) ii) Analog pins (XTALi, XTALo) iii) Remaining pins	 500 500 2000	–	–	V
LU	Latch-up current	In accordance with JESD78 standard	–	–	140	mA

Operating Temperature

Table 3. Operating Temperature

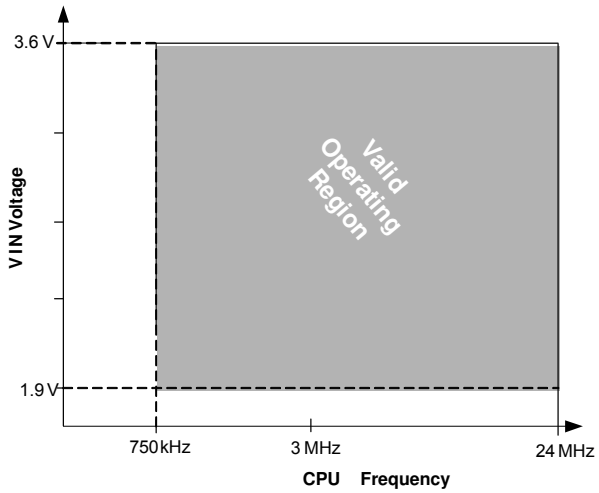
Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature	–	0	–	70	°C

Note
3. Port1 pins are hot-swap capable with I/O configured in High-Z mode, and pin input voltage above V_{IN}.

Electrical Specifications – PSoC Core

This section presents the DC and AC electrical specifications of the CYRF89435-68LTXC PSoC device. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at http://www.cypress.com/psoc.

Figure 5. Voltage versus CPU Frequency



DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 4. DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Vdd [4, 5]	Supply voltage	See table titled DC POR and LVD Specifications on page 20.	1.71	–	3.6	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are Vdd ≤ 3.0 V, T_A = 25 °C, CPU = 24 MHz No I2C/SPI	–	2.9	4.0	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are Vdd ≤ 3.0 V, T_A = 25 °C, CPU = 12 MHz No I2C/SPI	–	1.7	2.6	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are Vdd ≤ 3.0 V, T_A = 25 °C, CPU = 6 MHz No I2C/SPI	–	1.2	1.8	mA
I_{SB1}	Standby current with POR, LVD, and Sleep timer	Vdd ≤ 3.0V, T_A = 25 °C, I/O regulator turned off	–	1.1	1.5	µA
I_{SB0}	Deep sleep current	Vdd ≤ 3.0 V, T_A = 25 °C, I/O regulator turned off	–	0.1	–	µA

Notes

4. If powering down in standby sleep mode, to properly detect and recover from a V_{IN} brown out condition any of the following actions must be taken:
   Bring the device out of sleep before powering down.
   Assure that V_{IN} falls below 100 mV before powering back up.
   Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
   Increase the buzz rate to assure that the falling edge of V_{IN} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register.
   For the referenced registers, refer to the *CY8C20X36 Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{IN} brown out conditions to be detected for edge rates slower than 1V/ms.
5. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
6. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
7. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, or 1.9 V to 2.4 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

Table 5. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} < 10 μA, maximum of 10 mA source current in all I/Os	V_{IN} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V_{IN} – 0.40	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 μA, maximum of 10 mA source current in all I/Os	V_{IN} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{IN} – 0.50	–	–	V
V_{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 μA, V_{IN} > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V_{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{IN} > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.72	V
V_{IH}	Input high voltage	–	1.40	–		V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT2.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	–	–	V
$V_{IHLVT2.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2		–	V

Table 6. 1.9 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 10 μA, maximum of 10 mA source current in all I/Os	V_{IN} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V_{IN} – 0.50	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 100 μA, maximum of 10 mA source current in all I/Os	V_{IN} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{IN} – 0.50	–	–	V
V_{OL}	Low output voltage	I_{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V_{IL}	Input low voltage	–	–	–	0.30 × V_{IN}	V
V_{IH}	Input high voltage	–	0.65 × V_{IN}	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

Analog DC Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 7. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus	–	–	–	800	Ω
R_{GND}	Resistance of initialization switch to GND	–	–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V.

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 8. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V_{IN}	0.0	–	1.8	V
I_{LPC}	LPC supply current	–	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	–	3	30	mV

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: 0 °C ≤ T_A ≤ 70 °C, 1.9 V ≤ V_{IN} ≤ 3.6 V.

Table 9. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to (V_{IN} – 0.2 V)	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	µA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range		–	0	–	1.5	V

ADC Electrical Specifications

Table 10. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	VREFADC	V
C_{IIN}	Input capacitance	–	–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^Resolution/Data Clock)	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^resolution/data clock)	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (VIN > 3.0 V)	–	24	–	dB
		PSRR (VIN < 3.0 V)	–	30	–	dB

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POR1}	2.36 V selected in PSoC Designer PORLEV[1:0] = 00b, HPOR = 1	V_{IN} must be greater than or equal to 1.9 V during startup, reset from the XRES pin, or reset from watchdog.	–	2.36	2.41	V
V_{POR2}	2.60 V selected in PSoC Designer PORLEV[1:0] = 01b, HPOR = 1		–	2.60	2.66	
V_{POR3}	2.82 V selected in PSoC Designer PORLEV[1:0] = 10b, HPOR = 1		–	2.82	2.95	
V_{LVD0}	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V_{LVD1}	2.71 V selected in PSoC Designer		2.64 [8]	2.71	2.78	
V_{LVD2}	2.92 V selected in PSoC Designer		2.85 [9]	2.92	2.99	
V_{LVD3}	3.02 V selected in PSoC Designer		2.95 [10]	3.02	3.09	
V_{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V_{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	

Notes
8. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
9. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
10. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 12. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
VIN	Supply voltage for flash write operations	–	1.91	–	3.6	V
I_{DDP}	Supply current during programming or verify	–	–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See the appropriate DC GPIO Specifications on page 16	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See the appropriate DC GPIO Specifications on page 16	V_{IH}	–	–	V
I_{ILP}	Input current when Applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	+ 0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC GPIO Specifications on page 16. For V_{IN} > 3 V use V_{OH4} in Table 3 on page 13.	V_{OH}	–	VIN	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
$Flash_{DR}$	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

DC I²C Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3, 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, or 1.9 V to 2.4 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

Table 13. DC I²C Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{ILI2C}	Input low level	3.1 V ≤ VIN ≤ 3.6 V	–	–	0.25 × VIN	V
		2.5 V ≤ VIN ≤ 3.0 V	–	–	0.3 × VIN	V
		1.9 V ≤ VIN ≤ 2.4 V	–	–	0.3 × VIN	V
V_{IHI2C}	Input high level	1.9 V ≤ VIN ≤ 3.6 V	0.65 × VIN	–	–	V

DC Reference Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, or 1.9 V to 2.4 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

Table 14. DC Reference Buffer Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{Ref}	Reference buffer output	1.9 V to 3.6 V	1	–	1.05	V
V_{RefHi}	Reference buffer output	1.9 V to 3.6 V	1.2	–	1.25	V

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{IMO24}	IMO frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F_{IMO12}	IMO frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F_{IMO6}	IMO frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F_{CPU}	CPU frequency	–	0.75	–	25.20	MHz
F_{32K1}	ILO frequency	–	19	32	50	kHz
F_{32K_U}	ILO untrimmed frequency	–	13	32	82	kHz
DC_{IMO}	Duty cycle of IMO	–	40	50	60	%
DC_{ILO}	ILO duty cycle	–	40	50	60	%
SR_{POWER_UP}	Power supply slew rate	VIN slew rate during power-up	–	–	250	V/ms
t_{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t_{XRST2}	External reset pulse width after power-up	Applies after part has booted	10	–	–	µs
t_{OS}	Startup time of ECO	–	–	1	–	s
t_{JIT_IMO}	N = 32	6 MHz IMO cycle-to-cycle jitter (RMS)	–	0.7	6.7	ns
		6 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	4.3	29.3	ns
		6 MHz IMO period jitter (RMS)	–	0.7	3.3	ns
		12 MHz IMO cycle-to-cycle jitter (RMS)	–	0.5	5.2	ns
		12 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	2.3	5.6	ns
		12 MHz IMO period jitter (RMS)	–	0.4	2.6	ns
		24 MHz IMO cycle-to-cycle jitter (RMS)	–	1.0	8.7	ns
		24 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	1.4	6.0	ns
		24 MHz IMO period jitter (RMS)	–	0.6	4.0	ns

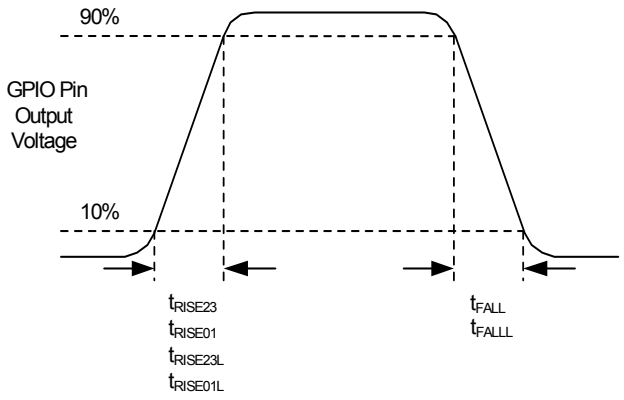
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode Port 0, 1	0 0	– –	6 MHz for 1.9 V <VIN < 2.40 V 12 MHz for 2.40 V < VIN< 3.6 V	MHz MHz
t_{RISE23}	Rise time, strong mode, Cload = 50 pF Port 2 or 3 or 4 pins	VIN = 3.0 to 3.6 V, 10% to 90%	15	–	80	ns
$t_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, Port 2 or 3 or 4 pins	VIN = 1.9 to 3.0 V, 10% to 90%	15	–	80	ns
t_{RISE01}	Rise time, strong mode, Cload = 50 pF, Ports 0 or 1	VIN = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled	10	–	50	ns
$t_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1	VIN = 1.9 to 3.0 V, 10% to 90% LDO enabled or disabled	10	–	80	ns
t_{FALL}	Fall time, strong mode, Cload = 50 pF, all ports	VIN = 3.0 to 3.6 V, 10% to 90%	10	–	50	ns
t_{FALLL}	Fall time, strong mode low supply, Cload = 50 pF, all ports	VIN = 1.9 to 3.0 V, 10% to 90%	10	–	70	ns

Figure 6. GPIO Timing Diagram



AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	µs