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CYRF8935

WirelessUSB™-NL 2.4 GHz Low Power Radio

Features

- Fully integrated 2.4-GHz radio on a chip
- 1-Mbps over-the-air data rate
- Transmit power typical: 0 dBm
- Receive sensitivity typical: –87 dBm
- 1 µA typical [1] current consumption in sleep state
- Closed-loop frequency synthesis
- Supports frequency-hopping spread spectrum
- On-chip packet framer with 64-byte first in first out (FIFO) data buffer
- Built-in auto-retry-acknowledge protocol simplifies usage
- Built-in cyclic redundancy check (CRC), forward error correction (FEC), data whitening
- Supports DC ~ 12-MHz SPI bus interface
- Additional outputs for interrupt request (IRQ) generation
- Digital readout of received signal strength indication (RSSI)
- 4 × 4 mm quad flat no-leads (QFN) package, bare die, or wafer sales

Product Description

WirelessUSB™-NL, optimized to operate in the 2.4-GHz ISM band, is Cypress's third generation of 2.4-GHz low-power RF technology, bringing the next level of low-power performance into a small 4-mm × 4-mm footprint. WirelessUSB-NL implements a Gaussian frequency-shift keying (GFSK) radio using a differentiated single-mixer, closed-loop modulation design that optimizes power efficiency and interference immunity. Closed-loop modulation effectively eliminates the problem of frequency drift, enabling WirelessUSB-NL to transmit up to 255-byte payloads without repeatedly having to pay power penalties for re-locking the phase locked loop (PLL) as in open-loop designs.

Among the advantages of WirelessUSB-NL are its fast lock times and channel switching, along with the ability to transmit larger payloads. Use of longer payload packets, compared to multiple short payload packets, can reduce overhead, improve overall power efficiency, and help alleviate spectrum crowding.

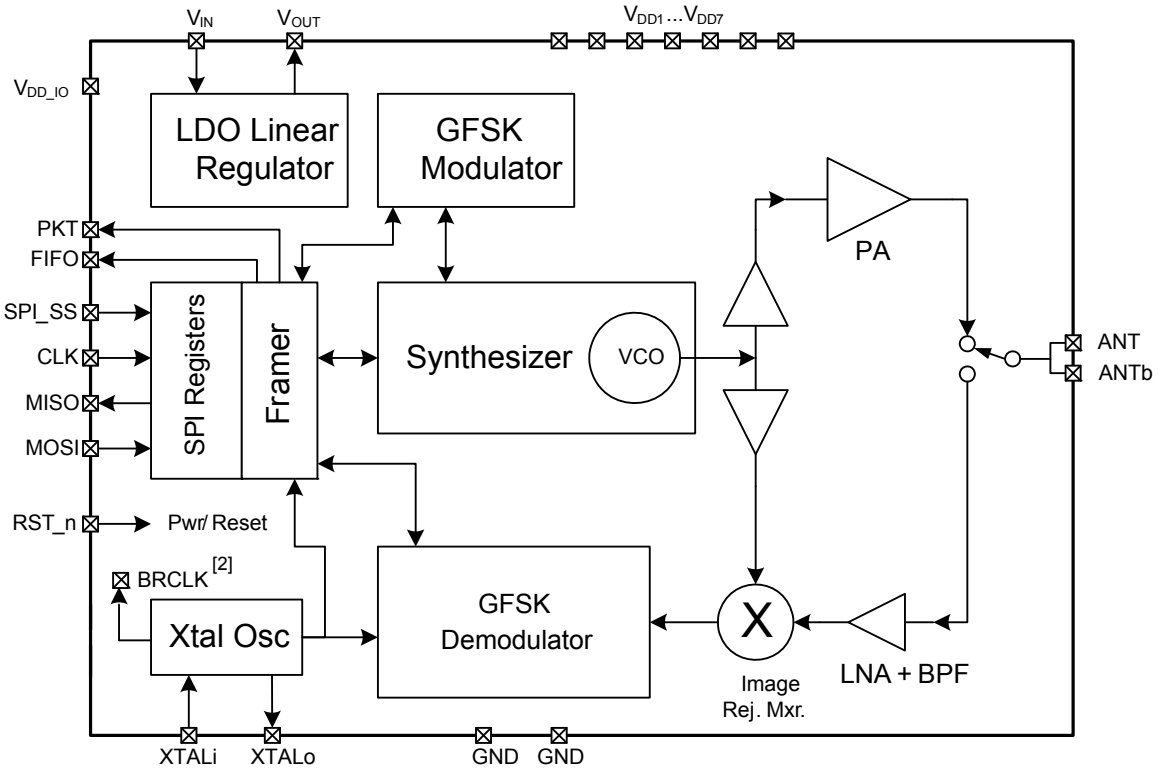
Combined with Cypress's enCoRe™ family of USB and wireless microcontrollers, WirelessUSB-NL also provides the lowest bill of materials (BOM) cost solution for PC peripheral applications such as wireless keyboards and mice, as well as best-in-class wireless performance in other demanding applications such as toys, remote controls, fitness, automation, presenter tools, and gaming.

Applications

- Wireless keyboards and mice
- Handheld remote controls
- Wireless game controllers
- Hobby craft control links
- Home automation
- Industrial wireless links and networks
- Cordless audio and low-rate video

Note
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{IN} = 3 VDC, Ta = +25 °C.

Logic Block Diagram

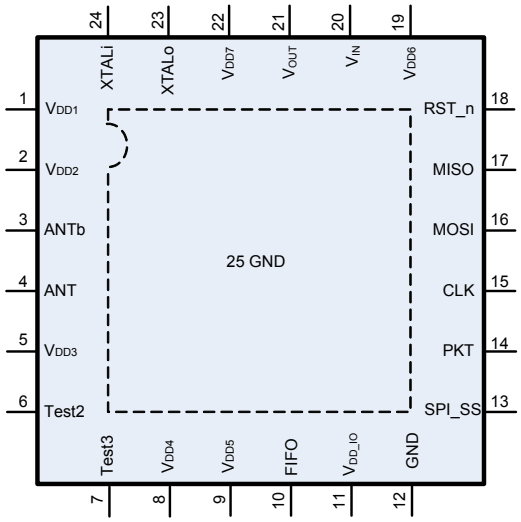


Note
2. BRCLK signal is available on bare die only, not packaged parts.

Contents

Pin Configuration

Figure 1. 24-pin QFN pinout (Top View)



Pin Descriptions

Table 1. CYRF8935 24-pin QFN (4 × 4 mm) pinout

Pin Number	Pin Name	Type	Description
6, 7	Test2, Test3	--	Reserved for factory test. Do not connect.
1, 2, 5, 8, 9, 19, 22	V_{DD1} to V_{DD7}	PWR	Core power supply voltage. Connect all V_{DD} pins to V_{OUT} pin.
3, 4	ANTb, ANT	RF	Differential RF input/output. See Typical Application on page 12 for recommended antenna hookup. Each of these pins must be DC grounded, 20 kΩ or less
10	FIFO	O	FIFO status indicator bit
12, 25	GND	GND	Ground connection
11	V_{DD_IO}	PWR	V_{DD} for the digital interface
13	SPI_SS	I	Enable input for SPI, active low. Also used to bring device out of sleep state.
14	PKT	O	Transmit/receive packet status indicator bit
15	CLK	I	Clock input for SPI interface
16	MOSI	I	Data input for the SPI bus
17	MISO	O/High-Z	Data output (tristate when not active)
18	RST_n	I	RST_n Low: Chip shutdown to conserve power. Register values lost RST_n High: Turn on chip, registers restored to default value
20	V_{IN}	PWR	Unregulated input voltage to the on-chip low drop out (LDO) voltage regulator
21	V_{OUT}	PWR	+1.8 V output from on-chip LDO. Connect to all V_{DD} pins, do not connect to external loads.
23	XTALo	AO	Output of the crystal oscillator gain block
24	XTALi	AI	Input to the crystal oscillator gain block

Functional Description

The CYRF8935 RF transceiver can add wireless capability to a wide variety of applications.

The product is a low-cost, fully-integrated CMOS RF transceiver, GFSK data modem, and packet framer, optimized for use in the 2.4-GHz ISM band. It contains transmit, receive, RF synthesizer, and digital modem functions, with few external components. The transmitter supports digital power control. The receiver uses extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments.

The product transmits GFSK data at approximately 0-dBm output power. Sigma-Delta PLL delivers high-quality DC-coupled transmit data path.

The low-IF receiver architecture produces good selectivity and image rejection, with typical sensitivity of –87 dBm or better on most channels. Sensitivity on channels that are integer multiples of the crystal reference oscillator frequency (12 MHz) may show approximately 5 dB degradation. Digital RSSI values are available to monitor channel quality.

On-chip transmit and receive FIFO registers are available to buffer the data transfer with MCU. Over-the-air data rate is always 1 Mbps even when connected to a slow, low-cost MCU. Built-in CRC, FEC, data whitening, and automatic retry/acknowledge are all available to simplify and optimize performance for individual applications.

Power-on and Register Initialization Sequence

For proper initialization at power up, V_{IN} must ramp up at the minimum overall ramp rate no slower than shown by T_{VIN} specification in the following figure. During this time, the RST_n line must track the V_{IN} voltage ramp-up profile to within approximately 0.2 V. Since most MCU GPIO pins automatically default to a high-Z condition at power up, it only requires a pull-up resistor, as shown in Figure 11 on page 14. When power is stable and the MCU POR releases, and MCU begins to execute instructions, RST_n must then be pulsed low as shown in Figure 2, followed by writing Reg[27] = 0x4200. During or after this SPI transaction, the State Machine status can be read to confirm FRAMER_ST= 1, indicating a proper initialization.

Figure 2. Power-on and Register Programming Sequence

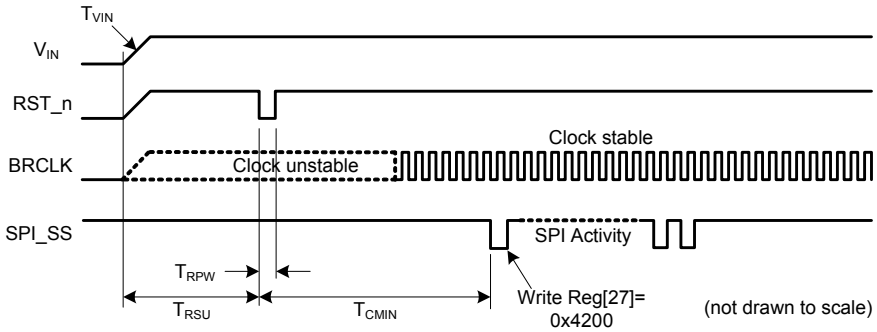


Table 2. Initialization Timing Requirements

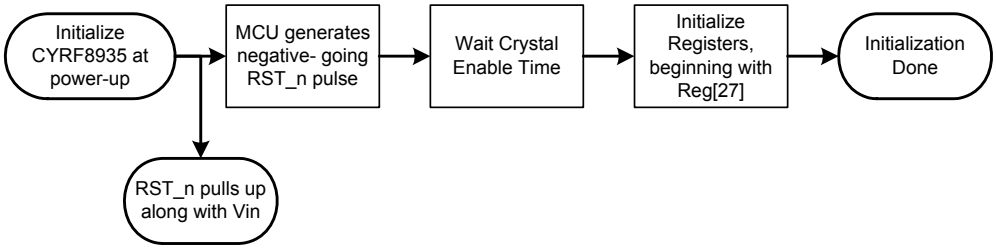
Timing Parameter	Min	Max	Unit	Notes	
T_{RSU}	–	20	ms	$2 < T_{VIN} \le 6.5$ [ms/V]	Reset setup time necessary to ensure complete reset
T_{RPW}	1	10	µs	Reset pulse width necessary to ensure complete reset	
T_{CMIN}	3	–	ms	Minimum recommended crystal oscillator and APLL settling time	
T_{VIN}	–	6.5	ms/V	Maximum ramp time for V_{IN}, measured from 0 to 100% of final voltage. For example, if V_{IN}= 3.3 V, the max ramp time is 6.5 × 3.3 = 21.45 ms. If V_{IN}= 1.9 V, the max ramp time = 6.5 × 1.9 = 12.35 ms.	

■ After RST_n transitions from 0 to 1, BRCLK[3] begins running at 12-MHz clock.

■ After register initialization, CYRF8935 is ready to transmit or receive.

Note
3. BRCLK signal is available on bare die only, not packaged parts.

Figure 3. Initialization Flowchart



Enter Sleep and Wakeup

When the MCU or application writes to the CYRF8935 register 35[14] to enter sleep mode and deasserts SPI_SS, CYRF8935 enters the sleep state where current consumption is extremely low.

Later, when SPI_SS is reasserted, CYRF8935 automatically wakes up from the sleep state. At this time the crystal oscillator is reactivated. The crystal oscillator takes 1 to 3 ms to become fully stable. During wakeup, there is no requirement to clear register 35[14] and no requirement to hold SPI_SS asserted.

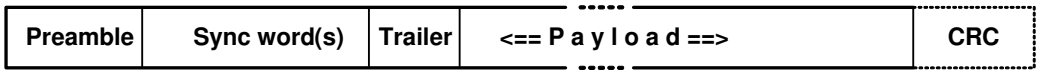
There are two sleep current choices available, selectable by Reg[27] setting: 1 µA[4] and 8 µA. If you use the 1-µA setting, Vin must be greater than or equal to 3.0 VDC. If Vin is ever expected to be < 3.0 VDC during Sleep, use the 8-µA setting. The 1-µA Sleep setting should only be used for long-term sleep such as 8 to 10 seconds or more.

To achieve the lowest sleep current, a special sleep state firmware patch is required. The patch is as follows:

SLEEP PATCH: Before writing register 35 to enter sleep, write Reg[10]= 0x8FFD, wait 30 µs or more, then write Reg[10] back to the default value of 0x7FFD. Next, write Reg[35] to enter sleep, as usual.

Packet Data Structure

Figure 4. Packet Structure



Each over-the-air CYRF8935 packet is structured as follows:

- Preamble: 1 to 8 bytes, programmable
- SYNC: 16/32/48/64 bits, programmable as device sync word
- Trailer: 4 to 18 bits, programmable
- Payload: TX/RX data
- CRC:16-bit CRC (Optional)

FIFO Pointers

The FIFO write pointer must be cleared before the application writes data to FIFO for transmit. This is done by writing '1' to register 52[15].

After receiving a packet, the write pointer at register 52[13:8] indicates how many bytes of receive data are waiting in the FIFO buffer to be read by the user MCU or the application.

The FIFO write pointer is automatically cleared when the receiver receives SYNC.

The FIFO read pointer is automatically cleared when the receiver receives SYNC, or after transmitting SYNC in transmit mode.

Packet Payload Length

There are two ways to handle the TX/RX packet lengths in CYRF8935. If register 41[13] is equal to 1, the CYRF8935 internal framer detects the packet length based on the value of the first payload byte. If register 41[13] is equal to 0, the first byte of the payload has no particular meaning, and packet length is determined by either TX FIFO running empty or TX_EN bit cleared (see Table 3).

Note
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{IN} = 3 VDC, Ta = +25 °C.

Table 3. CYRF8935 Configuration for Packet Length

Register 41[13] PACK_LENGTH_EN	Register 41[12] FW_TERM_TX	CYRF8935 Framer Start/Stop
0 (MCU or application handles packet length)	0	Transmit stops only when Register 7 TX_EN = 0. See FW_TERM_TX = 0 (Transmit) on page 10 for details. Receive stops only when Register 7 RX_EN = 0. See FW_TERM_TX= 0 (Receive) on page 11 for details.
	1	Transmit automatically stops whenever FIFO runs empty. Receive stops only when Register 7 RX_EN = 0. See Receive Timing on page 8.
1 (CYRF8935 framer handles packet length)	x (do not care)	The first byte of payload is regarded as packet length, 0 to 255 bytes. Transmit automatically stops when all 0 to 255 bytes are transmitted. See Framer: Packet Length Handling on page 7 for details.

The following sections show the detailed timing diagrams. All timing diagrams show active high for PKT and FIFO flags. Active low is also available through register 41[10] setting.

Framer: Packet Length Handling

The CYRF8935 framer handles packet length by setting register 41[13] = 1. The first byte of the payload is regarded as packet length (this length byte is not counted in the packet length). The CYRF8935 supports packet lengths up to 255 bytes. The framer handles Tx/Rx start and stop.

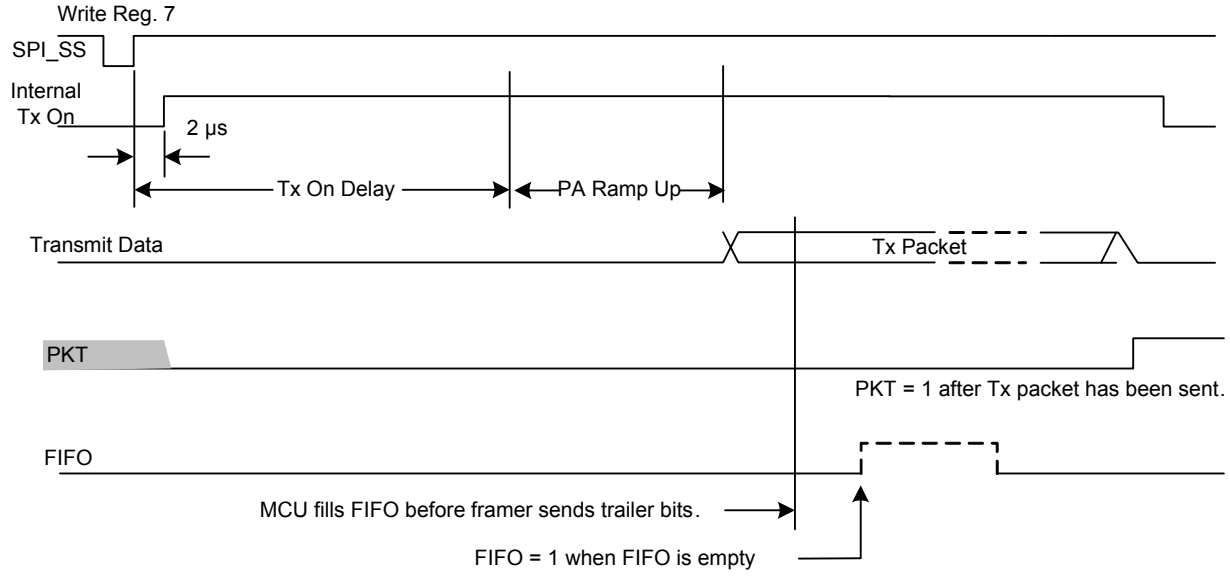
Transmit Timing

The Tx timing diagram is shown in Figure 5. After MCU writes register 7[8]= TX_EN = 1, the framer automatically generates the Tx packet using payload data from the FIFO register. The frequency (RF channel) will be as specified in register 7 at the time TX_EN is written to 1.

The MCU or application must load transmit data into the FIFO register before the framer sends trailer bits. You can do this by loading the transmit payload data into the FIFO register either before or after writing TX_EN = 1. For slower applications, it is easier to load the FIFO register, and then write TX_EN = 1. For the higher frame rate (faster) applications, write register 7 TX_EN = 1, and then load the FIFO register with payload data during the Tx on delay time, as shown in Figure 5.

If the packet length exceeds the FIFO length, the MCU must write FIFO data multiple times. The FIFO flag indicates whether FIFO is empty in transmit state.

Figure 5. Tx Timing Diagram when Register 41[13] = 1 (Framer Handles Packet Length) PKT and FIFO Flags are Active High



Receive Timing

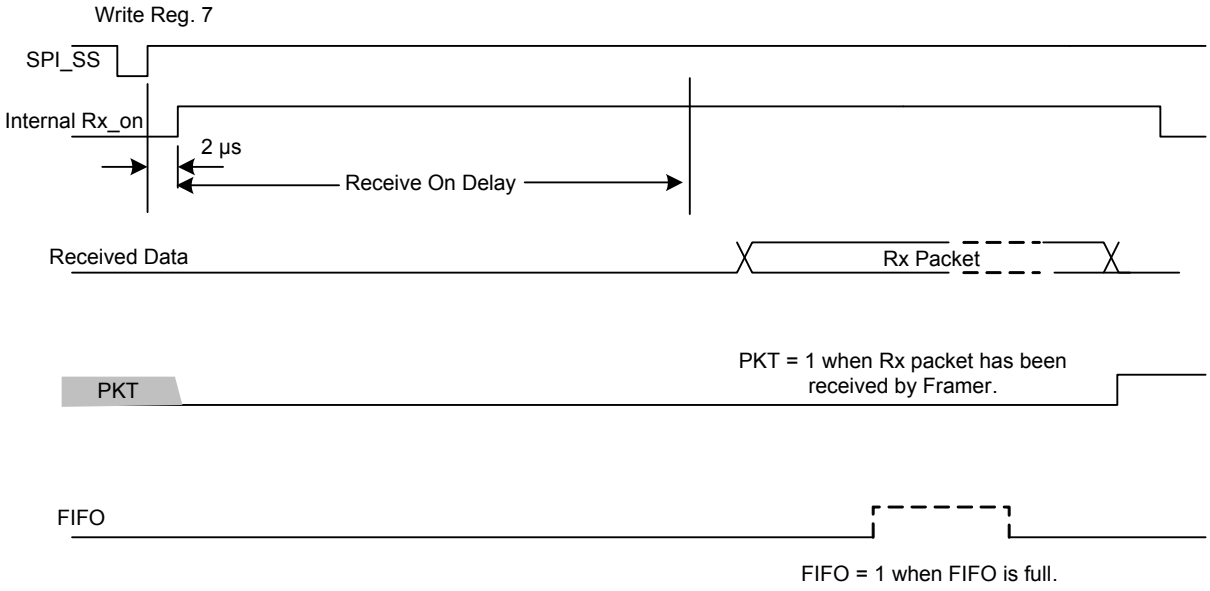
Figure 6 shows the Rx timing diagram. The receive process begins when the MCU writes register 7[7] = 1. At this time, the CYRF8935 framer turns on the receiver and waits while attempting to detect a valid syncword. The receive frequency is specified within register 7. The two register 7 fields of interest, RX_EN and RF_PLL_CH_NO, may be sent to CYRF8935 during the same SPI transaction. If sent in separate SPI transactions, send the RF_PLL_CH_NO first, followed by RX_EN.

If a valid syncword is found, the CYRF8935 framer processes the packet automatically. When the received packet processing is complete, the CYRF8935 framer sets the state to IDLE.

If the received packet length is longer than 63 bytes, the FIFO flag goes active, which means the MCU must read out data from the FIFO.

A valid syncword might not always be found, either due to a weak signal, multi-path cancellation, or devices being out of range. To accommodate such a condition and to prevent lockup, the application or the MCU must incorporate a 'receive timeout' timer to clear RX_EN and return to the IDLE state.

Figure 6. Rx Timing Diagram when Register 41[13] = 1 (Framer Handles Packet Length) PKT and FIFO Flags are Active High



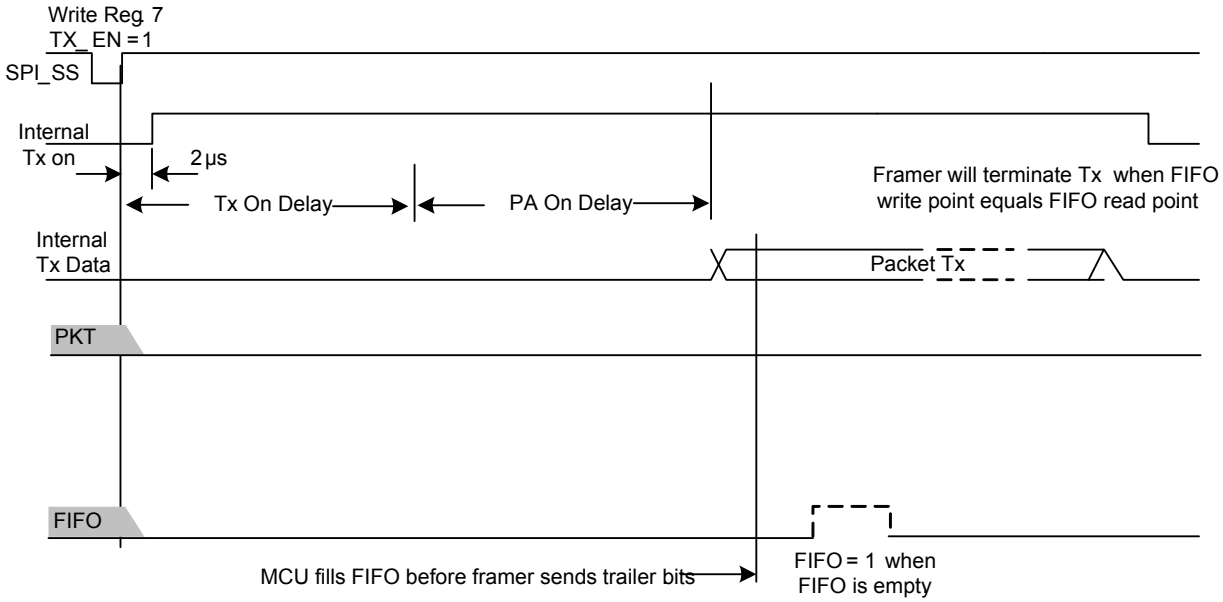
MCU or Application Handles Packet Length

When register 41[13] = 0, the first byte of the payload data has no special significance and the packet length depends on register 41[12].

FW_TERM_TX = 1

If register 41[12] = 1, the CYRF8935 framer continues to compare the FIFO write point and the FIFO read point during packet transmission. If the MCU or application stops writing data to FIFO, the framer eventually detects that there is no data to send (FIFO is empty), and CYRF8935 exits 'cease transmission' automatically (see Figure 7).

Figure 7. Tx Timing When Register 41[13:12] = '01b PKT and FIFO Flags are Set as Active High

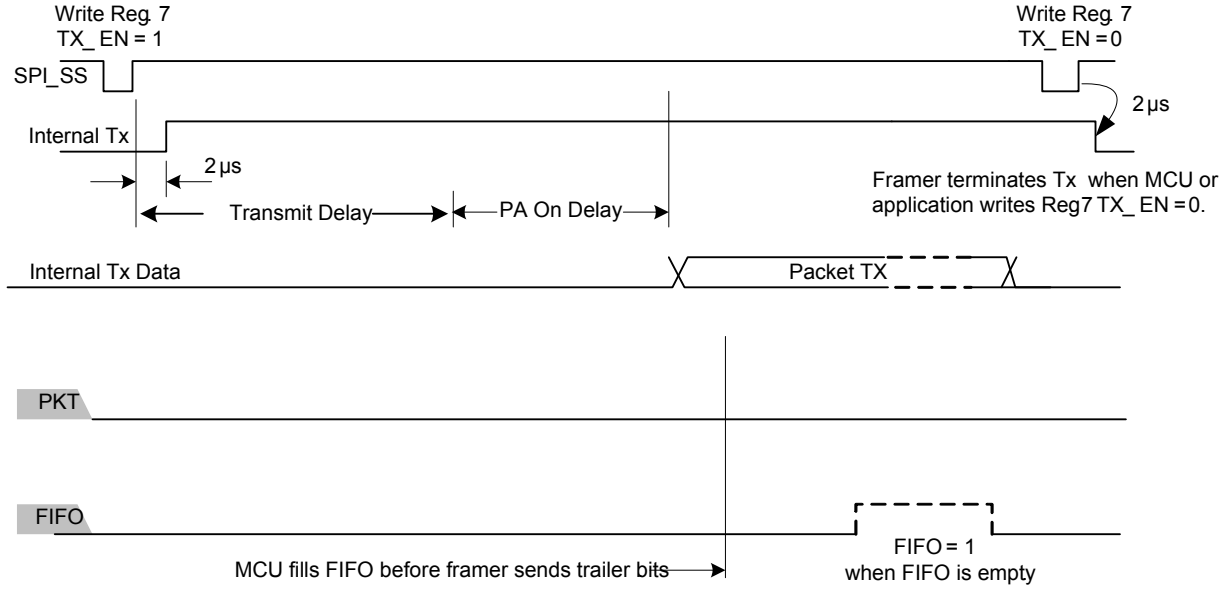


Note When register 41[13] = 0 (MCU or application handles packet length), never let FIFO underflow or overflow. FIFO full and empty thresholds can be controlled using register 40 FIFO_EMPTY_THRESHOLD and FIFO_FULL_THRESHOLD settings. The best value depends on SPI speed and the speed at which the MCU or application can stream the data into FIFO.

FW_TERM_TX = 0 (Transmit)

When register 41[13:12] = '00b, the CYRF8935 framer does not stop packet transmission until MCU or application writes register 7[8] TX_EN bit = 0. Packet transmission continues even if FIFO is empty (see Figure 8).

Figure 8. TX Timing Diagram when Register 41[13:12] = '00b PKT and FIFO Flags are Shown Active High



Note When register 41[13] = 0 (MCU or application handles packet length), never let FIFO underflow or overflow. FIFO full and empty thresholds can be controlled through register 40 FIFO_EMPTY_THRESHOLD and FIFO_FULL_THRESHOLD settings. The best value depends on SPI speed and the speed at which the MCU or application can stream the data into FIFO.

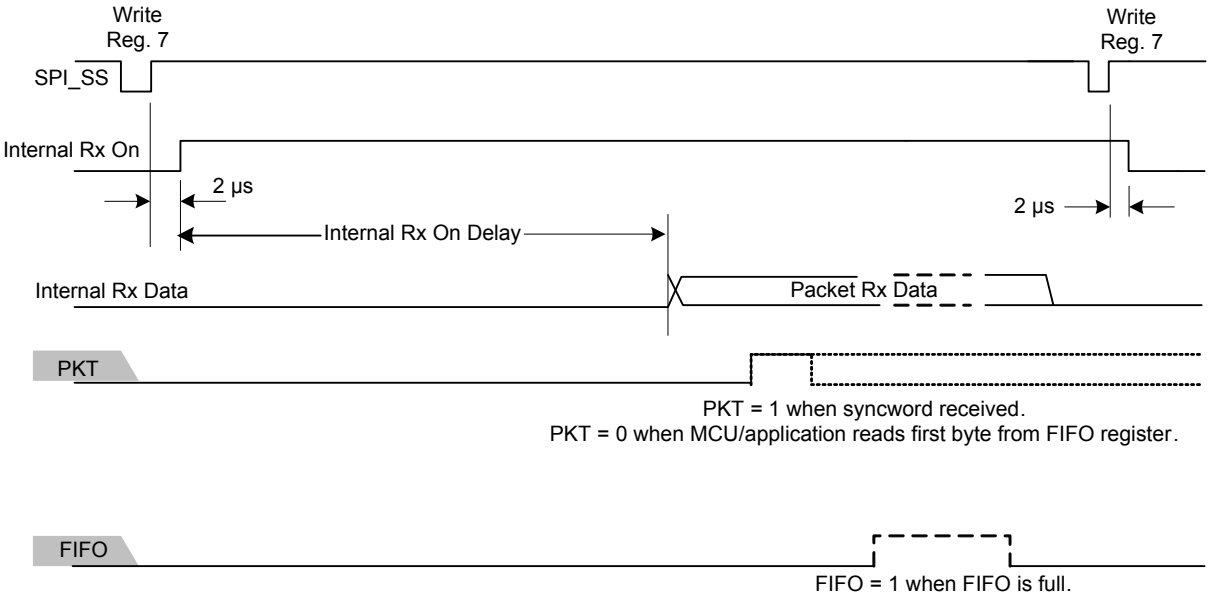
FW_TERM_TX= 0 (Receive)

When register 41[13] = 0, packet reception starts when MCU or application writes register 7[7] RX_EN = 1. At this time, the framer automatically turns on the receiver to the frequency and channel specified in register 7. After waiting for the internal synthesizer and receiver delays, the framer circuitry of the CYRF8935 begins searching the incoming signal for a syncword. When the syncword is detected, the framer sets the PKT flag active, and then starts to fill the FIFO with receive data bytes. The PKT flag remains active until the MCU or application reads out the first byte of data from the FIFO register. After the MCU or application reads the first byte of receive data, the PKT flag goes inactive until the next Tx/Rx period.

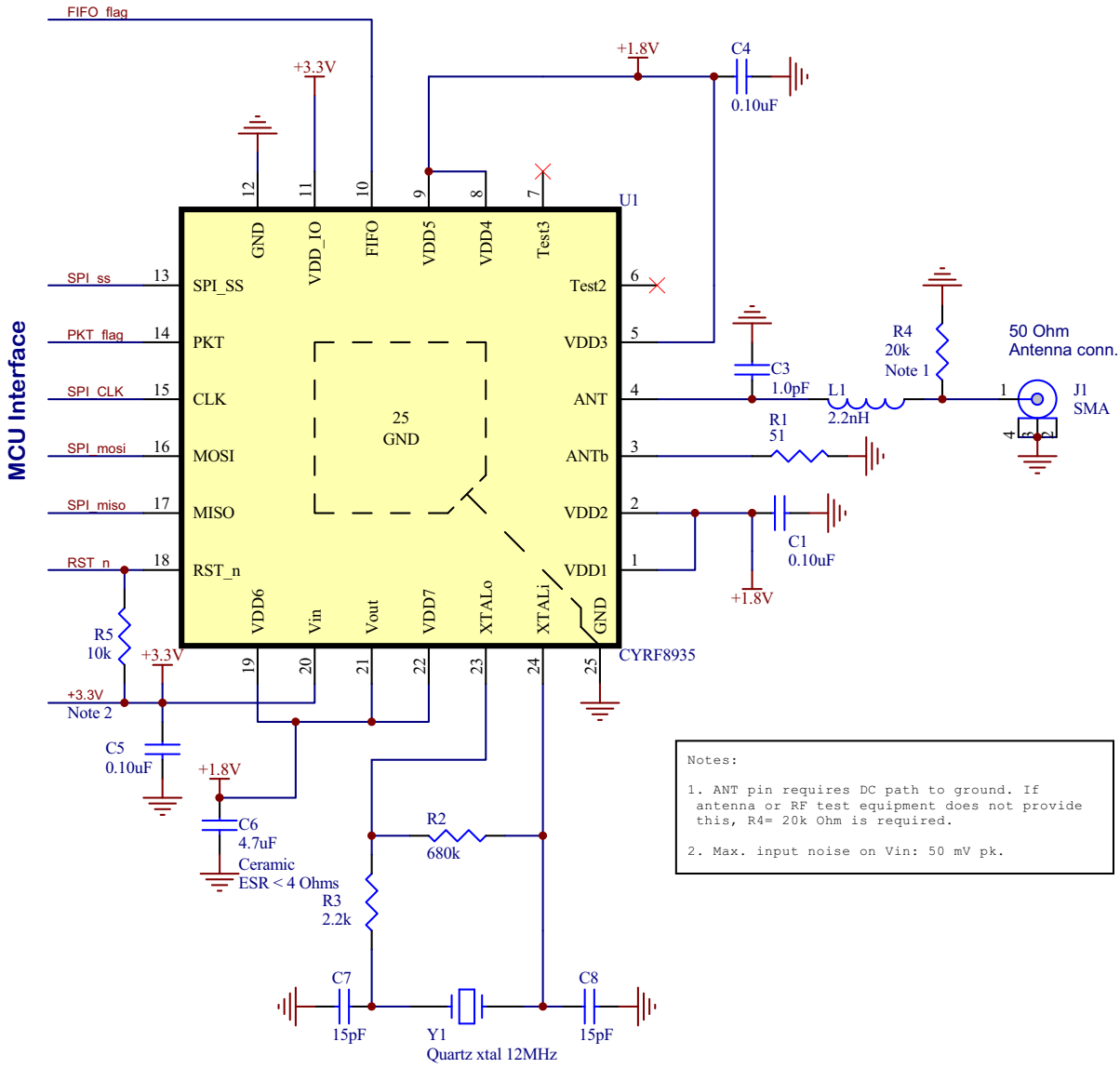
With register 41[13:12] = '00b or '01b, the CYRF8935 framer always needs the MCU or application to write register 7[7] to 0 to stop the Rx state.

The Rx timing diagram is shown in Figure 9.

Figure 9. RX Timing Diagram when Register 41[13:12] = '00b or '01b PKT_flag and FIFO_flag are Active High



Typical Application



Setting the Radio Frequency

Programming by channel number is the easiest way to set frequency. In the CYRF8935, RF carrier frequency and RF channel number are always related by the expression:

```
Freq. = 2402 + Ch. #
```

Channel number is loaded into bits [6:0] of Register 7. Bits 7 and 8 initiate the desired Rx or Tx operation, respectively.

Some sample Register 7 examples are as shown in Table 4.

During Regulatory Compliance testing, you can jump directly to another frequency any time without going through IDLE state. If you change between Tx and Rx, however, you must pass through IDLE state. For IDLE state, write Register 7 to clear bits 8 and 7. Tx or Rx operation is initiated when Register 7 bit 8 or 7 is set. Radio frequency is also determined at that time.

Table 4. Sample Register 7 Settings

Carrier Frequency, MHz	DUT Channel Number (decimal)	DUT Channel Number (hex)	Tx setting: Reg. 7 value for TX_EN= 1	Rx setting: Reg. 7 value for RX_EN= 1
2402	0	00	0100	0080
2403	1	01	0101	0081
2404	2	02	0102	0082
|	|	|	|	|
2434	32	20	0120	00A0
|	|	|	|	|
2441	39	27	0127	00A7
|	|	|	|	|
2480	78	4E	014E	00CE

Crystal Oscillator

The CYRF8935 contains the on-chip gain block for the quartz crystal frequency standard.

Quartz Crystal Application

As shown in Figure 10 on page 14, the series resistor Rs limits power to the crystal and contributes to the phase-shift necessary for oscillation. The ideal Rs value may need to be determined empirically, adjusted for certain crystal manufacturer part numbers and designs. The series equivalent combinations of C1 and C2 largely determine the capacitive load seen by the crystal, which should match the crystal vendor's specification. These capacitor values are chosen to center the crystal oscillator frequency at the correct value, 12 MHz. The feedback resistor Rf from the buffer output to input serves to self-bias the on-chip buffer to the center of the linear region for maximum gain.

Verifying correct crystal oscillator frequency may require special test methods. Because connecting a frequency counter probe to either XTALi or XTALo adds capacitive loading and alters the crystal oscillation frequency, other methods must be used. For bare die applications involving COB packaging, use the BRCLK[5] test point to verify correct frequency of oscillation. This requires register 32[3:1] set accordingly (see Register Definitions on page 21). For 24-QFN packaged parts, the correct crystal frequency is determined by transmitting a continuous carrier frequency (see Register Settings for Test Purposes on page 19) and using a RF frequency counter to ensure correct frequency. Irrespective of which method is used, initial tolerance should be within budget as recommended in Table 5, such that the total frequency error stays within budget.

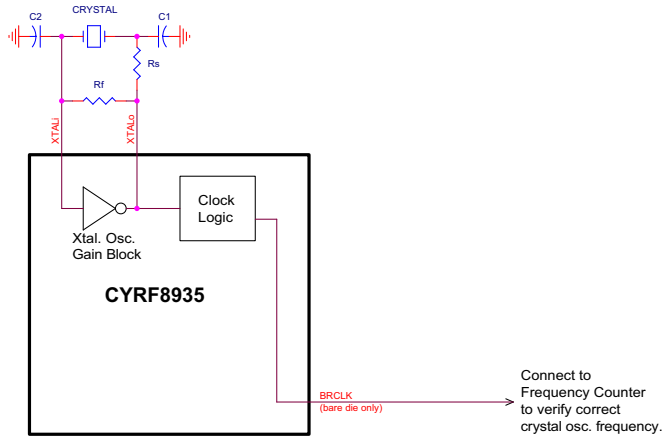
Table 5. Crystal Specifications

Crystal Parameter	Specification
Frequency	12.000 MHz
Initial frequency tolerance	±15 ppm
Frequency tolerance over temperature	±15 ppm
Frequency tolerance after aging	±5 ppm
Frequency drift due to load cap. drift	±5 ppm
Total	**±40 ppm**
Equivalent series resistance	80 Ω max
Resonance mode	Fundamental, parallel resonant
Load capacitance	In accordance with external load capacitors (see C1 and C2 in Figure 10)

Note For proper operation, the total frequency error must not exceed what is shown in Table 5. Individual error contributions can be adjusted; for example 10+20+5+5=40, or 5+30+2+3=40.

Note
5. BRCLK signal is available on bare die only, not packaged parts.

Figure 10. Simplified Schematic of Crystal Oscillator



Note When crystal oscillator is constructed as shown in Typical Application on page 12, Table 5 on page 13, and Figure 10, the oscillation frequency should be stable within 3 mS (max) after startup.

Minimum Pin Count

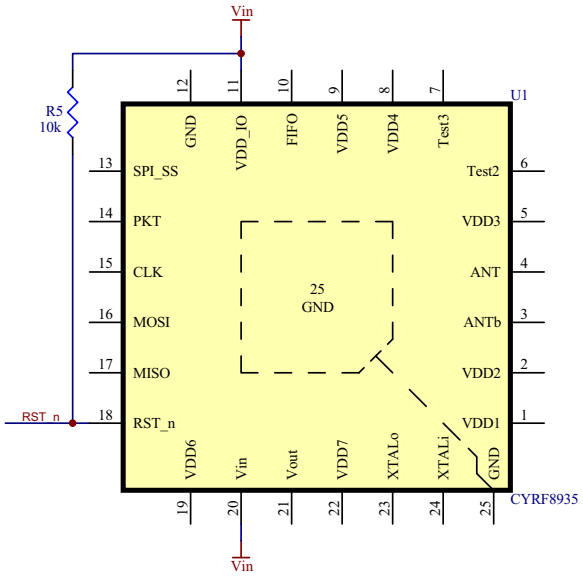
When a low-cost MCU drives the CYRF8935, the MCU pin count must be minimized.

- FIFO pin: Only needed when the Tx or Rx packet length is greater than around 63 bytes, up to infinity. For short packets (< 63 bytes), FIFO is not needed.
- PKT pin: Gives a hardware indication of a packet received. If you are willing to poll register 48 for this information, then this pin is not needed.
- SPI lines: All four lines are needed.

Reset Pull-up

For proper power-up initialization, the RST_n pin must have a pull-up to VIN, as shown in Figure 11. The exact value of the 10-k pull-up resistor is not critical. The pull-up resistor ensures proper operation of the CYRF8935 internal-level shifter circuitry while power is applied. Subsequently, the RST_npulse resets the internal registers to their default state.

Figure 11. Reset Pull-up Circuit



Transmit Power Control

Table 6 lists recommended settings for register 9 for short-range applications, where reduced transmit RF power is a desirable trade off for lower current.:

Table 6. Transmit Power Control

Power Setting Description	Typical Transmit Power (dBm)	Value of Register 9	
		Silicon ID 0x1002 [6]	Silicon ID 0x2002 [6]
PA0 - Highest power	+1	0x1820	0x7820
PA2 - High power	0	0x1920	0x7920
PA4 - High power	–3	0x1A20	0x7A20
PA8 - Low power	–7.5	0x1C20	0x7C20
PA12 - Lower power	–11.2	0x1E20	0x7E20

Reading RSSI

The CYRF8935 contains internal RSSI circuitry that is roughly linearized to 1 dB for every LSB. Results are read from register 6[15:10], RAW_RSSI. See Register Definitions on page 21 for details.

The framer must read the RSSI register after the receiver is enabled and set on frequency using register 7, and after the RF PLL has settled according to the correct receive frequency.

Note
6. Silicon Id can be read from Register 31.

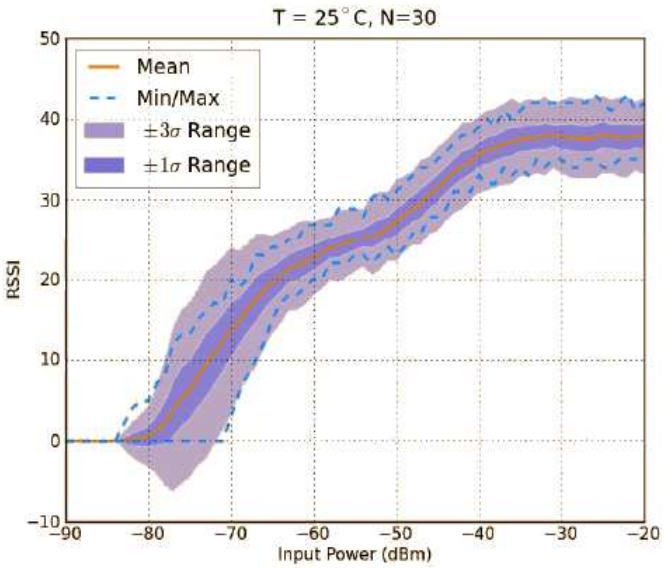
The wait time between programming RX_EN, and reading Register 6, can be determined by any of the following methods, or any desired combination, depending on the application:

- Wait in accordance with RF PLL Settling Time spec. to be sure RF PLL is settled.
- Read register 3[12] RF_SYNTH_LOCK to be sure CYRF8935 RF PLL is settled.
- Read register 48[7] SYNCWORD_RECV to indicate the signal being received is a desired packet.

Note that RSSI can be read without receiving a syncword. In other words, CYRF8935 RSSI circuitry also responds to CW and interference signals.

If the RSSI feature is not needed, disable it to conserve receiver DC current budget. When register 11[9] is changed from 0 to 1, the receiver current consumption decreases by about 0.3 mA.

Figure 12. Typical Room Temperature RSSI Response



Following is the pseudocode for measuring RSSI:

Write Reg11 = 0x0208 ;disable RSSI before reading

Read RSSI = Reg6[15:10] ;do the read

Write Reg11 = 0x0008 ;enable RSSI for next measurement

Automatic ACK

The CYRF8935 provides an automatic retry/acknowledge feature. This means that if the TX packet does not successfully arrive at the receiving end, the TX end automatically attempts a given number of retries. In a weak signal environment, this feature makes the bit error rate (BER) appear to be zero at the expense of the frame error rate (FER). Refer to State Diagram on page 34 for details.

To use automatic retry/acknowledge, see Register Definitions on page 21 for register 41[11] and register 35[11:8].

Receive CRC and FEC Result

The CYRF8935 returns CRC and FEC error check status in register 48[15:14]. For convenience, the entire top byte of register 48 is returned in the SPI status word. These eight bits are normally available from the SPI hardware block of the MCU or application, saving the time necessary to do an additional read of register 48 for the same information.

CRC is calculated only on the payload portion of the packet.

CRC_ERROR only clears after another valid syncword is detected by the receiver or after transmission of a packet payload.

Sync Word Selection

At the beginning of each packet, after transmission of a 01010101 preamble, is a sync word, programmable to be 16, 32, 48, or 64 bits long. For the devices to communicate, these must be programmed to the same value at both ends of the link. The sync word can be thought of as a MAC address in this respect.

In the CYRF8935 receiver, there is an adjustable tolerance for sync word bit errors that may occur. This adjustment is called SYNCWORD_THRESHOLD, set via Register 40, bits 5:0. If set too tight, performance is good but less-than-optimum receive sensitivity and link budget is obtained. If set too loose, Frame Errors increase because of false synchronization.

The situation can sometimes be further complicated if the chosen sync word, combined with the 01010101 preamble, has unusually high auto correlation, or correlation with other devices that may be on the air on a different sync word network. This undesired condition is likely to happen when the sync word bits that immediately follow the 01010101 preamble continues the 1010... sequence. In such cases, it becomes difficult for the receiver to separate the actual sync word from the preamble. The solution is to either tighten the SYNCWORD_THRESHOLD, or choose a better sync word. Sometimes increasing the sync word length is also an option.

Register 36 sets the sync word for the bits that immediately follow the preamble. If a false sync problem is observed, try changing this word first.

The following table summarizes some recommended settings.

Table 7. Recommended SYNCWORD_THRESHOLD Settings

Application	Sync Word Length (see Register 32)	Sync Word Selection	Recommended Reg. 40 SYNCWORD_THRESHOLD setting (decimal)
Simple	32	Better (almost every sync word must work)	1
	32	Good (Most sync words work)	2
Advanced	64	Better (almost every sync word must work)	6 or tighter
	64	Good (Most sync words work)	7

Scramble On/Off Selection

The CYRF8935 incorporates a built-in hardware data scrambling and descrambling function. This function is designed to make the transmit data more random, removing long strings of continuous mark or space. When enabled, it causes payload data to be modified by a PN code that is initialized according to the setting of Register 35 SCRAMBLE_DATA.

Systems based on CYRF8935 will normally function either way, scramble on or off.

Setting SCRAMBLE_ON=1 will indeed cause a small 'token' increase in over-the-air security, similar to what WEP adds to WiFi. In other words, it renders the OTA data coded, but it should not be considered highly secure. For truly secure applications, consider using scramble combined with other security algorithms.

To function properly, both ends of the RF link need the same setting, enabled or disabled. Both ends must also have the same Register 35 SCRAMBLE_DATA setting.

Measuring Receiver Sensitivity

Receive sensitivity and BER can be measured using these methods:

Method 1: Link Budget Method

In this method, another CYRF8935 or a compatible transceiver is used as a transmit packet source. It connects to the device under test (DUT) through a calibrated attenuation path. The transmit power should also be known or measured. The receiver sensitivity can be calculated from the following equation, based on the largest RF attenuation that can be sustained between Tx and Rx, while maintaining adequate link performance.

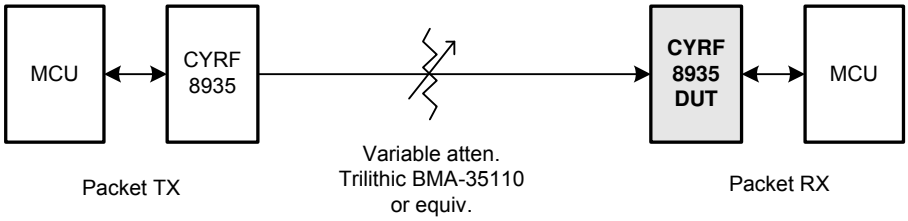
Link_Budget = (TxP – RxSens) [dB]

Where

TxP = Transmit Power [dBm]

RxSens = Receive Sensitivity [dBm]

Figure 13. Measuring Overall Link Budget, Method 1



When using this method, make sure that the RF signal is not leaking around the attenuator or coupling directly into the receiver, which renders the attenuation setting meaningless. You can verify this by simply increasing the attenuation and verifying that the packets cease to be received at higher attenuator settings.

RF leakage around the attenuator can be caused by:

- Loose RF cable connector
- Poorly shielded RF cables
- Poor PCB layout at either Tx or Rx
- RF boards too close together
- Coupling by or over the DC power leads

Note that interference from other 2.4-GHz services could be leaking into the test setup and degrade the BER measurement.

When properly set up and working, the link budget method is a simple and reliable way to test and characterize CYRF8935 RF performance.

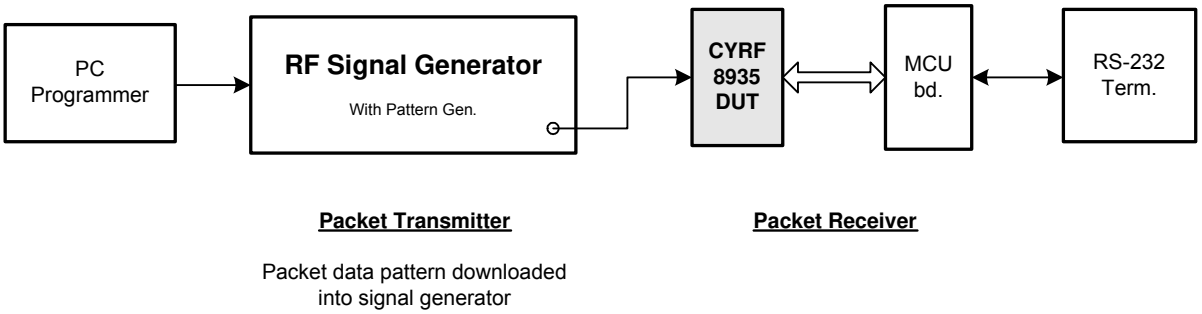
Test Variations

- Automatic loopback can be added to test both Tx and Rx in the same test.
- Frequency hopping can be added to test over the design frequency range.

Method 2: Packet Signal Generator method

In this method, an RF signal generator is used as the packet source. The shielded, adjustable RF output of the signal generator connects to the receiver input. The signal generator must have digital pattern storage ability for the modulation. A packet of valid data is downloaded into the signal generator, and these packets are repetitively sent to the CYRF8935 receiver under test. An MCU or PC program monitors the CYRF8935 PKT flag signal, which causes the MCU or PC to download each packet as it is received, compare the packet against the expected values, and report the packet statistics to the end user.

Figure 14. Measuring Receiver Sensitivity with Signal Generator, Method 2



In this setup, the signal generator is set as follows:

Modulation: GFSK, 2-level, Bt = 0.5, peak deviation 320 kHz, symbol rate 1 Msps.

Frequency, amplitude: As required for test.

Receive Spurious Responses

This receiver, like many other low-cost receivers, may exhibit spurious responses in-band, often at multiples of certain digital frequencies. In the case of the CYRF8935, this response sometimes occurs at multiples of 4 MHz or four channels, offset from the desired receiver passband. During frequency hopping, a signal may be found on the wrong frequency, causing incorrect hopping synchronization.

The workaround for this is to program one of the payload bytes to contain the channel number on which the packet is being transmitted. When a packet is received, this byte is checked to determine if it matches the receive channel setting. If not, the packet should be discarded.

RF VCO Calibration

Over-the-air Transmit and Receive frequencies for the CYRF6935 RF transceiver are derived from the 12 MHz crystal oscillator, multiplied up by the internal fractional-N RF PLL. Low phase noise is obtained by keeping the PLL K_{VCO} relatively low. In order for the VCO to cover the desired frequency range over the expected V_{DD}, temperature, and process extremes, the VCO must be calibrated prior to use. The CYRF8935 contains a fully automatic calibration algorithm, but the algorithm does require approximately 150 us extra time, compared to automatic calibration turned off.

Regulatory Compliance

United States FCC

When operating in the 2402- to 2480-MHz band, the second and third harmonics always fall into what is defined in 47CFR, section 15.205 as 'restricted bands of operation'. The field strength of radiated emissions greater than 1 GHz in a restricted band must not exceed 500 µV/m at a distance of 3 meters. Using the equation for free space propagation, you can translate the field strength to an equivalent RF power level at the DUT, if an assumption is made regarding the effective antenna gain at the second and third harmonic frequencies.

Figure 15. Calculation of Maximum Spurious Level

Parameter		Unit of Measure			
Field Strength	54.0	dBµV/m	or	501	µV/m
			or	0.501	mV/m
Tx antenna gain over isotropic	6	dBi	or	3.981071706	power ratio
Impedance of free space	377	ohms	or	120*pi	ohms
distance	0.003	km	or	3	m
Result					
Tx pwr, desired signal	0	dBm	or	0.001	W
Tx pwr, undesired spurious	**-47.2**	**dBm**	or	1.89287E-08	W
or	**-47.2**	**dBc**			

The antenna gain assumption of +6 dBi is based on the fact that the measurement requires that the position of the DUT and measurement antennae be maximized to yield the highest spurious signal. Since the second and third harmonics, by definition, fall on integer multiples of the carrier wavelength, many common DUT antennae may have good, usable gain at higher frequencies such as 0 dBi. Accounting for the maximization of the measurement, +6 dBi is a good, conservative antenna gain for harmonic frequencies.

In practice, harmonic emissions are much less of a problem, primarily because the antenna is not specifically optimized for such harmonics.

The calculation in Figure 15 shows the maximum spurious level at the antenna as –47 dBm. Because the typical second harmonic is specified as –45 dBm, it follows that an additional 2 dB attenuation could be required. However, no additional attenuation is required to pass the FCC-radiated emissions test. Individual test results may vary.

Table 8 lists a summary of FCC precompliance test results. The antenna used is a common half-wave end-fed dipole. The results easily pass the U.S. FCC test for a Part 15.247 device. If there is a problem with qualification because of spurious emissions in restricted bands, you can add a filter, or perhaps reduce Tx Power through Register 9.

Table 8. FCC Test Results

Run No.	Mode	Channel	Power Setting	Measured Power	Test Performed	Limit	Result/Margin
1a	Non hopping	2402 MHz	Default	NA	Restricted band edge (2390 MHz)	FCC Part 15.209 / 15.247(c)	46.8 dbµV/m at 2390.0 MHz (–7.2 dB)
			Default	NA	Radiated emissions (1–0 GHz)	FCC Part 15.209 / 15.247(c)	45.7 dbµV/m at 4804.1 MHz (–8.3 dB)
1b	Non hopping	2441 MHz	Default	NA	Radiated emissions (1–18 GHz)	FCC Part 15.209 / 15.247(c)	45.0 dbµV/m at 4882.2 MHz (–9.0 dB)
1c	Non hopping	2480 MHz	Default	NA	Restricted band edge (2483.5 MHz)	FCC Part 15.209 / 15.247(c)	47.8 dbµV/m at 2484.1 MHz (–6.2 dB)
			Default	NA	Radiated emissions (1–10 GHz)	FCC Part 15.209 / 15.247(c)	45.3 dbµmV/m at 4960.1 MHz (–8.7 dB)

Register Settings for Test Purposes

To pass various regulatory agency EMC tests, the DUT may need to enter various test states as shown below. After loading the recommended register values shown in Table 12 on page 26, load the registers in the order shown in the following table.

Table 9. Register Settings for Test Purposes

Test State	Notes	Register Settings
Tx continuously, CW mode	Primarily used to verify proper crystal oscillator frequency. The Tx turns on and stays on continuously. There will be no on/off bursting of the carrier. Modulation will be absent. Carrier frequency will be half-way between mark and space. Occasionally used during EMC testing.	Reg. 11= 0x8008 (CW_MODE= 1) Reg. 41= 0xC000 (SCRAMBLE_ON= 1, PACK_LENGTH_EN= 0, and FW_TERM_TX= 0) Reg. 7 as shown in Table 4 on page 13.
Tx continuously, Random data mode	During EMC testing, this is the most commonly used Tx test. Modulation will be normal, GFSK. Tx data will continuously cycle through the FIFO data bits. A data scrambling function will be applied. In other words, even if the FIFO has all zeros (not yet loaded with data), Tx data will appear random. Radiated emissions resemble normal operation except that the carrier is on continuously, which significantly speeds up testing.	Reg. 11= 0x0008 (CW_MODE= 0) Reg. 41= 0xC000 (SCRAMBLE_ON= 1, PACK_LENGTH_EN= 0, and FW_TERM_TX= 0) Reg. 7 as shown in Table 4 on page 13.
Rx continuously	Sometimes required for EMC testing.	Reg. 41= 0xC000 (PACK_LENGTH_EN= 0, and FW_TERM_TX= 0) Reg. 7 as shown in Table 4 on page 13.
Tx and Rx off (IDLE state)	When neither Tx nor Rx is desired.	Reg. 7: clear bits 8 and 7. Reg. 7 binary: xxxx xxx0 0xxx xxxx (x = don't care)

Recommendations for PCB Layout

Though the PCB layout is not too critical, here are some recommendations:

- RF path: Adhere closely to the recommended reference design circuit.
- Clock traces: Keep the quartz crystal traces simple and direct. The self-bias resistor should be close to the XTALi and XTALo pins. The oscillation loop, consisting of the series resistor and crystal, should be a simple, small loop. The crystal-loading capacitors should be near the crystal. The ground connection to these capacitors must be good, clean, and quiet. This prevents noise from being injected into the oscillator. It is best to have one ground plane for the entire RF section.
- Power distribution and decoupling: Capacitors should be located near the V_{DD} pins, as shown in Typical Application on page 12.
- Antenna placement: When using an antenna, follow the manufacturer's recommendation regarding layout.
- Digital interface: To provide a good ground return for the digital lines, it is a good idea to provide at least two pins for ground on the digital interface connector. Good grounding between RF and MCU can help reduce noise 'seen' at the antenna, thus improving performance.

Antenna Type and Location

The most significant factor affecting RF performance for the CYRF8935 or any other over-the-air RF device is the antenna type, placement, and orientation. Antenna gain is normally measured with respect to isotropic, that is, an ideal radiator that sends or receives power equally to or from any direction. An ideal antenna choice for most low-power, short-range wireless applications is the theoretical isotropic reference antenna. Unfortunately, these do not exist in practice. A simple dipole with a theoretical gain of +2 dBi is usually a good choice. However, you should take care when placing the antenna, because dipole antennas have a radiation pattern where the null can be very deep.

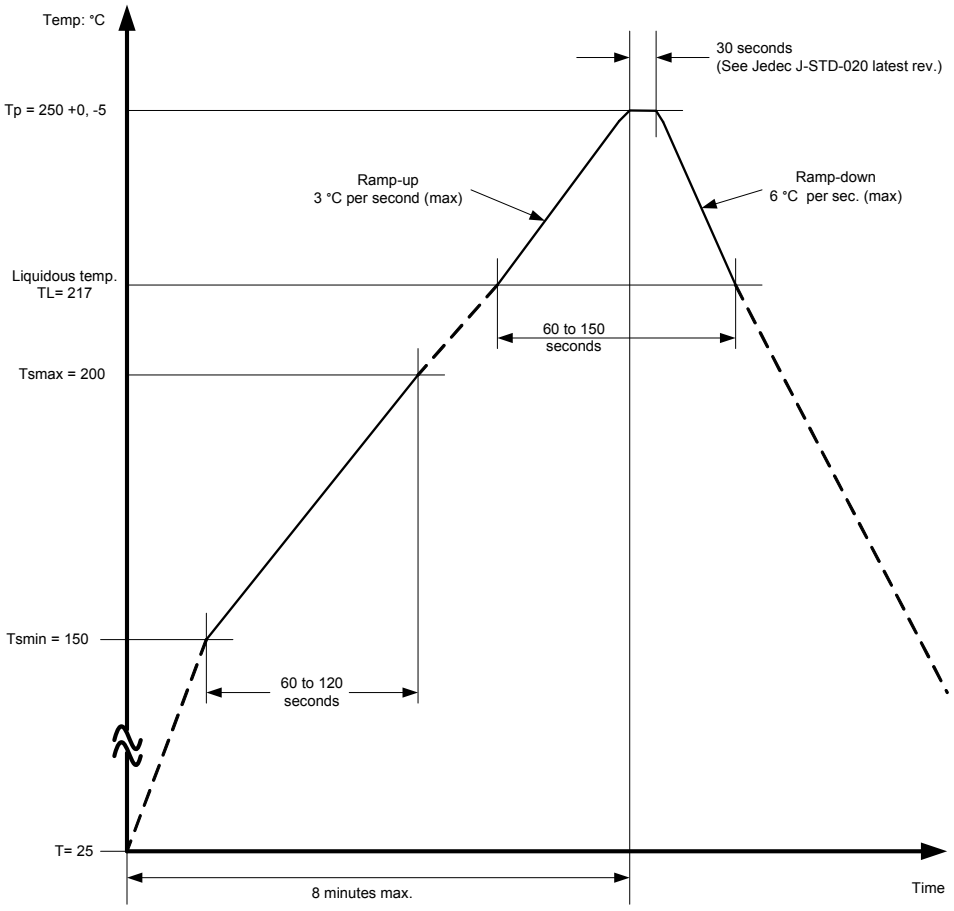
The antenna must be kept away from human tissue, particularly sensitive spots like the heart, brain, and eyes. Violating this design principle makes the end product perform poorly and can be dangerous for the user. Refer to www.fcc.gov/oet/rfsafety for guidance on this subject. For best operation, design the product so that the main antenna radiation is away from the body, or at least not proximity-loaded by the human body or dielectric objects within the product.

Remember to keep the antenna away from clock lines and digital bus signals; otherwise, harmonics of the clock frequency will jam certain receive frequencies.

IR Reflow Standard

■ Reference: IPC/JEDEC J-STD-020D.1

Figure 16. Recommended IR Reflow Profile



Register Definitions

The following registers are accessed using the SPI protocol.

Some of the internal registers and bit fields are not intended for end-user adjustment. Such registers are not described here and should not be altered from the factory-recommended value

Table 10. RF Register Information

Bit No.	Bit Name	Description
Register 3 – Read only		
15:13	(Reserved)	(Reserved)
12	RF_SYNTH_LOCK	Indicates the phase lock status of RF synthesizer. 1: Locked 0: Unlocked
11:0	(Reserved)	(Reserved)
Register 6 – Read only		
15:10	RAW_RSSI[5:0]	Indicates 6-bit raw RSSI value from analog circuit. Each LSB is approximately 1 dB. See Reading RSSI on page 14 for details.
9:0	(Reserved)	(Reserved)
Register 7		
15:9	(Reserved)	(Reserved)
8	TX_EN	Initiates the transmit sequence for state machine control. Note that TX_EN and RX_EN cannot be set to ‘1’ at the same time.
7	RX_EN	Initiates the receive sequence for state machine control. Note that TX_EN and RX_EN cannot be set to ‘1’ at the same time.
6:0	RF_PLL_CH_NO [6:0]	Sets Tx and Rx RF channel number, for example: Write 0 for channel 0 (2402 MHz) Write 39 for channel 39 (2441 MHz) Write 78 for channel 78 (2480 MHz)
Register 9		
15:11	(Reserved)	(Reserved)
10:7	PA_GN[3:0]	PA power level control
6:0	(Reserved)	(Reserved)
Register 10		
15:1	(Reserved)	(Reserved)
0	XTAL_OSC_EN	1: Enable crystal oscillator gain block 0: Disable crystal oscillator gain block
15:1	(Reserved)	(Reserved)
Register 11		
15	CW_MODE	1: Disables Tx modulation; CW only. 0: Normal Tx mode
14:10	(Reserved)	(Reserved)
9	RSSI_DIS	1: Disable RSSI 0: RSSI operates normally.
8:0	(Reserved)	(Reserved)

Table 10. RF Register Information (continued)

Bit No.	Bit Name	Description
Register 23		
15:3	(Reserved)	(Reserved)
2	TXRX_VCO_CAL_EN	1: enable automatic VCO calibration with every Tx/Rx. 0: disable feature
1:0	(Reserved)	(Reserved)
Register 27		
15:11	LDO_SP_SLEEP	Sets LDO sleep current. See Electrical Characteristics on page 28 for Register 27 settings.
10:0	(Reserved)	(Reserved)
Register 29 - Read only - 0x00xx		
15:8	(Reserved)	(Reserved)
7:4	RF_VER_ID [3:0]	This field is used to identify minor RF revisions to the design.
3	(Reserved)	(Reserved)
2:0	Digital version	This field is used to identify minor digital revisions to the design.
Register 30 - Read only - 0xf413		
15:0	(Reserved)	(Reserved)
Register 31 - Read only		
15:0	Silicon ID	This field is used to identify Silicon ID. Valid values are 0x1002 and 0x2002

Table 11. Framer Register Information

Bit No.	Bit Name	R/W	Description	Default
Register 32				
15:13	PREAMBLE_LEN	R/W	000b: 1 byte 001b: 2 bytes 010b: 3 bytes . . 111b: 8 bytes	010b
12:11	SYNCWORD_LEN	R/W	11b: 64 bits {{Reg39[15:0],Reg38[15:0],Reg37[15:0],Reg36[15:0]} 10b: 48 bits, {Reg39[15:0],Reg38[15:0],Reg36[15:0]} 01b: 32 bits, {Reg39[15:0],Reg36[15:0] 00b: 16 bits,{Reg36[15:0]}	11b
10:8	TRAILER_LEN	R/W	000b: 4 bits 001b: 6 bits 010b: 8 bits 011b: 10 bits . . 111b: 18 bits	000b
7:6	DATA_PACKET_TYPE	R/W	00b: Non return to zero (NRZ) law data	00b
5:4	FEC_TYPE	R/W	00b: No FEC 01b: Reserved 10b: FEC23 11b: Reserved	00b
3:1	BRCLK_SEL	R/W	Selects output clock signal to BRCLK[7] pin: 000b: Keep low 001b: Crystal buffer out 010b: Crystal divided by 2 011b: Crystal divided by 4 100b: Crystal divided by 12 101b: TXCLK 1 MHz 110b: APLL_CLK (12 MHz during Tx, Rx) 111b: Keep low	011b
0	(Reserved)	W/R	(Reserved)	0B
Register 35				
15	(Reserved)		(Reserved)	
14	SLEEP_MODE	W	1: Enter SLEEP state (set crystal gain block to off. Keep LDO regulator on (register values will be preserved). Wakeup begins when SPI_SS goes low. This restarts the on-chip clock oscillator to begin normal operation. 0: Normal (IDLE) state	0B
13	(Reserved)		(Reserved)	
12	BRCLK_ON_SLEEP	R/W	1: Crystal running at sleep mode Draws more current but enables fast wakeup 0: Crystal stops during sleep mode Saves current but takes longer to wake up	1B

Note
7. BRCLK signal is available on bare die only, not packaged parts.

Table 11. Framer Register Information (continued)

Bit No.	Bit Name	R/W	Description	Default
11:8	RE-TRANSMIT_TIMES	R/W	Max retransmit packet attempts when AUTO_ACK= 1.	3H
7	MISO_TRI_OPT	R/W	1: MISO drives low-Z even when SPI_SS = 1 (Only one SPI slave device on the SPI) 0: MISO goes tristate when SPI_SS = 1 (Allows multiple SPI slave devices on the SPI)	0B
6:0	SCRAMBLE_DATA	R/W	Whitening seed for data scramble. Must be set the same at both ends of radio link (Tx and Rx). Must be nonzero.	00H
Register 36				
15:0	SYNC_WORD[15:0]	R/W	Least significant bits of sync word are sent first	0000H
Register 37				
15:0	SYNC_WORD[31:16]	R/W	Least significant bits of sync word are sent first	0000H
Register 38				
15:0	SYNC_WORD[47:32]	R/W	Least significant bits of sync word are sent first	0000H
Register 39				
15:0	SYNC_WORD[63:48]	R/W	Least significant bits of sync word are sent first	0000H
Register 40				
15:11	FIFO_EMPTY_THRESHOLD	R/W	During Tx, this field adjusts the point at which the FIFO flag signal notifies the MCU or application to indicate that the FIFO register is almost empty. The best value depends on the individual application and the speed at which the MCU or application can access the FIFO.	00100B
10:6	FIFO_FULL_THRESHOLD	R/W	During Rx, this field adjusts the point at which the FIFO flag signal notifies the MCU or application to indicate that the FIFO register is almost full. The best value depends on the individual application and the speed at which the MCU or application can access the FIFO.	00100B
5:0	SYNCWORD_THRESHOLD	R/W	Sets maximum number of received syncword bits that may be in error to start a packet receive. The number of bits is (SYNCWORD_THRESHOLD - 1). For example, a setting of 7 means up to 6 sync word bits can be in error	07H
Register 41				
15	CRC_ON	R/W	1: CRC on 0: CRC off	1B
14	SCRAMBLE_ON	R/W	Removes long patterns of continuous 0 or 1 in transmit data. Automatically restores original unscrambled data on receive. 1: Scramble on 0: Scramble off	0B
13	PACK_LENGTH_EN	R/W	1: CYRF8935 regards the first byte of payload as packet length descriptor byte.	1B
12	FW_TERM_TX	R/W	1: When FIFO write point equals read point, CYRF8935 terminates Tx when the FW handles packet length. 0: FW (MCU) handles length and terminates Tx	1B
11	AUTO_ACK	R/W	1: After receiving data, automatically send ACK to acknowledge that the packet was received correctly. 0: After receiving data, do not send ACK; just go to IDLE.	1B

Table 11. Framer Register Information (continued)

Bit No.	Bit Name	R/W	Description	Default
10	PKT_FIFO_POLARITY	R/W	1: PKT flag, FIFO flag active low 0: Active high	0B
9:8	(Reserved)	R/W	(Reserved)	00B
7:0	CRC_INITIAL_DATA	R/W	Initialization constant for CRC calculation	00H
Register 48 – Read only				
15	CRC_ERROR	R	Received CRC error	
14	FEC23_ERROR	R	Indicate FEC23 error	
13:8	FRAMER_ST	R	Framer status	
7	SYNCWORD_RECV	R	1: syncword received. It is only available in receive status, After out receive status, always set to ‘0’	
6	PKT_FLAG	R	PKT flag indication	
5	FIFO_FLAG	R	FIFO flag indication	
4:0	(Reserved)	R	(Reserved)	
Register 50				
15:0	TXRX_FIFO_REG	R/W	For MCU read/write data between the FIFO Reading this register removes data from FIFO; Writing to this register adds data to FIFO. **Note** MCU or application access to the FIFO register is byte by byte (8 bits at a time), not 16 bits as with other registers.	00H
Register 52				
15	CLR_W_PTR	W	1: Clear Tx FIFO pointer to 0 when writing this bit to ‘1’ It is not available in RX status.	0B
14	(Reserved)	W		
13:8	FIFO_WR_PTR	R	FIFO write pointer	
7	CLR_R_PTR	W	1: Clear Rx FIFO point to 0 when writing this bit to ‘1’ It is not available in Tx status.	0B
6	(Reserved)			
5:0	FIFO_RD_PTR	R	FIFO read pointer (number of bytes to be read by MCU)	