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CYPRESS
Embedded in Tomorrow™

CYRF9935

WirelessUSB™ NX 2.4 GHz Low Power Radio

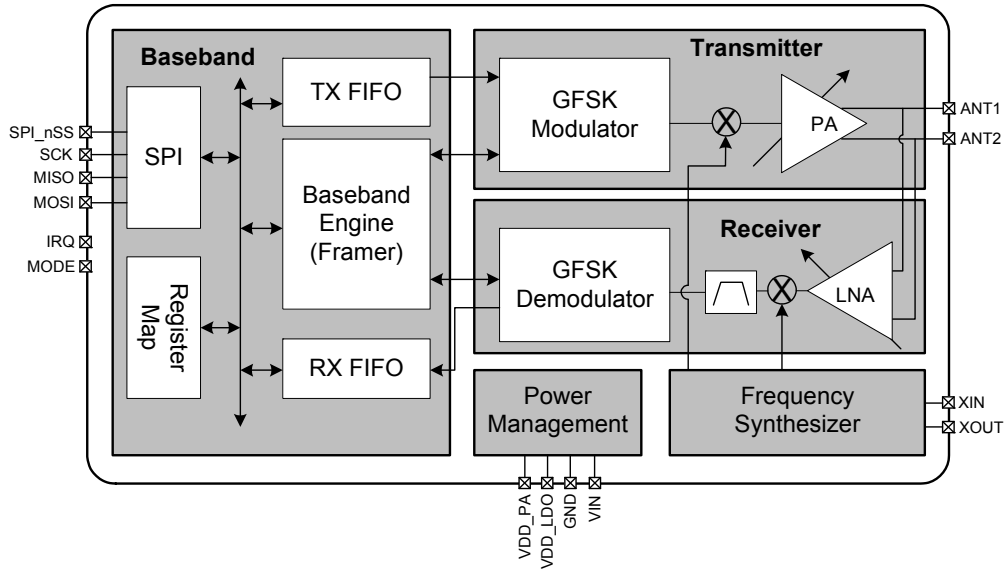
Key Features

- RF channel – 126 (2400 MHz~2525 MHz)
- Programmable Data Rate – 2 Mbps/250 Kbps
- Power Supply Range – 1.9 V to 3.6 V
- Ultra low power operation
  - TX Current 12 mA at 0 dBm output power
  - RX Current 15 mA at 2 Mbps data rate
  - RX Current 14 mA at 250 Kbps data rate
  - Idle current 26 µA (Idle-I mode)
  - Sleep current 900 nA
- Programmable TX Output Power:
  - +4 dBm
  - 0 dBm
  - –8 dBm
  - –14 dBm
  - –20 dBm
- Sensitivity (0.1%BER):
  - –93 dBm at 250 kbps
  - –82 dBm at 2 Mbps
- Digital RSSI
- Programmable Payload length – 1 to 32 bytes
- Programmable Multi-Level FIFO
  - 3 Levels of 32 bytes each
  - 6 Levels of 16 bytes each
- Automatic Packet Acknowledgement
- Automatic Packet Resend
- 8/16 bit hardware CRC
- Up to 8 Pipes for 1:8 Star Network
- 4-pin Hardware SPI Interface
- ±60 ppm 16 MHz crystal
- Compact 24-pin 4 × 4 mm QFN package

Applications

- Wireless mouse, keyboard, gamepad and presenter
- Wireless audio and VoRF
- Remote controller
- Home automation
- Wireless sensor network
- Radio Controlled (R/C) Toy

Block Diagram



Contents

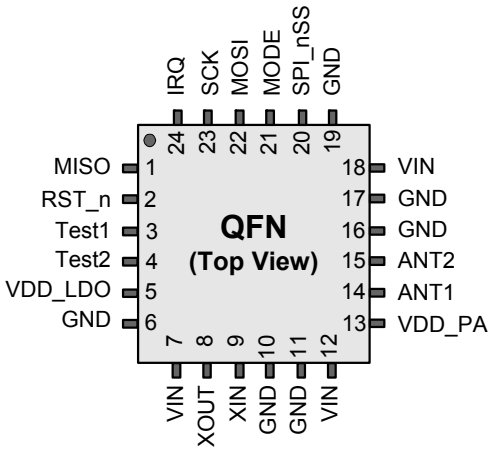
General Description

CYRF9935 is a low power radio transceiver operating in the world wide 2.4–2.5 GHz ISM band. The transceiver contains fully integrated receiver, transmitter, frequency synthesizer and baseband engine. Internal voltage regulators ensure good immunity to power supply noise and wide power supply voltage range.

CYRF9935 offers a high data rate of 2 Mbps. It enables burst transmission to reduce the average power consumption. In addition, the built-in automatic acknowledgement, automatic re-send and low power consumption in Idle-I mode, are very useful features for low power wireless applications.

Pin Configuration

Figure 1. 24-pin QFN Pinout (Top View)



Pin Descriptions

Pin	Name	Function	Description
1	MISO	Digital Output	SPI data output [1]
2	RST_n [2]	Digital Input	Chip reset pin. Active low.
3	Test1	--	Reserved for factory test. Do not connect.
4	Test2	--	Reserved for factory test. Do not connect.
5	VDD_LDO	Power Output	Internal digital supply output (1.8 V) for de-coupling purpose only and cannot be loaded.
6	GND	Power	Ground
7	VIN [3]	Power Input	Power supply (+1.9 VDC ~ +3.6 VDC)
8	XOUT	Analog Output	Crystal pin 2
9	XIN	Analog Input	Crystal pin 1
10	GND	Power	Ground
11	GND	Power	Ground
12	VIN [3]	Power Input	Power supply (+1.9 VDC ~ +3.6 VDC)
13	VDD_PA	Analog Output	Power supply output (+1.8 Vdc) for the internal Power Amplifier, for de-coupling purpose only and cannot be loaded.
14	ANT1	RF	Antenna interface pin 1
15	ANT2	RF	Antenna interface pin 2
16	GND	Power	Ground
17	GND	Power	Ground
18	VIN [3]	Power Input	Power supply (+1.9 VDC ~ +3.6 VDC)
19	GND	Power	Ground
20	SPI_nSS	Digital Input	SPI chip select. Active low.
21	MODE	Digital Input	Chip enable activates RX mode. Active high.
22	MOSI	Digital Input	SPI data input
23	SCK	Digital Input	SPI clock input
24	IRQ	Digital Output	Interrupt pin. Active low (default). Can be programmed to active high by setting internal register (address: 0x02).

Notes
1. MISO pin on the PSoC must be configured in pull-up mode to achieve low current consumption in Idle-I and Sleep modes. If using any other controller an external pull-up may be required.
2. RST_n line has an internal pull-up resistor which will pulls it high, hence the user does not need to pull RST_n high.
3. Pins 7, 12 and 18 i.e. all V_{IN} pins must be shorted to a common power supply.

Functional Overview

Power on Reset

Power on reset is initiated when the voltage on VIN reaches 1.9 V. It takes 50 ms for the power on reset event to complete. After power on reset the radio registers will have default values (refer to Register Sets on page 26) and the radio will be in Idle-I mode. In this mode the radio consumes 26 µA current.

External Reset

CYRF9935 can also be reset anytime by driving the RST_n pin low for a period greater than 5 µs. The reset signal should be followed by a period of inactivity on the SPI or any other input to the radio for about 1.5 milliseconds. This is required for the crystal oscillator to start-up.

External reset is an atomic command (it cannot be interrupted) and will interrupt any other activity on the chip.

Interrupt

In CYRF9935 the interrupt is provided through the IRQ pin. The interrupt can be configured as active low or active high, by clearing or setting bit 7 of direct register 0x02 respectively. Upon reset, it is configured as active low.

There are six interrupt sources in CYRF9935. These interrupts can be enabled or disabled by configuring bits 5:0 of direct register 0x02 (refer to Register Sets on page 26). Table 1 describes the different interrupts that are available.

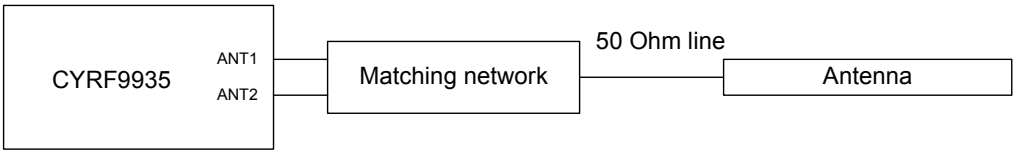
Table 1. Interrupt Sources

Interrupt source	Description	Bit in Register 0x02 for enabling or disabling interrupt	Bit in Register 0x01 (Status) that reflects the state of interrupt
RX_DR	RX data ready	5	5
TX_DS	TX data sent	4	4
TX_MAX_ARSC	Maximum retry reached	3	3
TX_FIFO	Change in TX FIFO state to the state selected by the TX_FIFO_STA_SEL bits in register 0x28	2	1
RX_FIFO	RX FIFO not empty	1	0
RSSI	RSSI refresh done	0	2

If an interrupt is enabled the IRQ pin reflects the state of the corresponding interrupt source in the register 0x01 (refer to Register Sets on page 26). The IRQ pin remains asserted till the interrupt is cleared. To clear an interrupt set the corresponding bit in status register.

RF Pins

The CYRF9935 has two RF pins, ANT1 and ANT2, which are used for differential RF input/output. For optimum performance, an LC network (called a matching network) matches WUSB-NX to a conventional 50-ohm antenna.



The traces to ANT1 and ANT2 pins are RF traces and should be short and direct.

The LC values of the matching network should not be modified from those shown in the Application Circuit on page 33. In addition to matching, they provide attenuation of undesired transmit harmonics. These components should have good high-frequency characteristics, signified by Q factor within the manufacturer datasheets.

On the other side of the matching network is an antenna with 50 Ohm impedance. This trace also should be short, if possible.

However, in many cases, the antenna needs to be placed in a more optimum position on the PCB, so some additional trace length may be necessary. In such cases, the characteristic impedance of trace should also be 50 Ohm.

There should be a solid ground plane on the underside of the matching network. The solid ground plane should extend all the way to the ground pad vias (at the center of the device) on one side and should extend to the 50 Ohm transmission line that connects to the antenna on the other side.

RF Channel

The RF channel frequency determines the center of the channel used. The channel occupies a bandwidth of less than 1 MHz at 250 kbps and a bandwidth of less than 2 MHz at 2 Mbps. CYRF9935 can operate on frequencies from 2.400 GHz to 2.525 GHz. The programming resolution of the RF channel frequency setting is 1MHz.

At 2 Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2 Mbps mode, the channel spacing must be 2 MHz or more. At 250 kbps the occupied channel bandwidth is the same or lower than the resolution of the RF channel frequency setting.

The RF channel frequency is set by the register 0x00 according to the following formula:

Frequency = 2400 + Channel [MHz]

The transmitter and the receiver must be programmed with the same RF channel frequency to communicate with each other.

Table 2. RF channel frequency

Channel Number (Decimal)	Frequency
0	2400 MHz
1	2401 MHz

Table 2. RF channel frequency *(continued)*

Channel Number (Decimal)	Frequency
2	2402 MHz
3	2403 MHz
4	2404 MHz
5	2405 MHz
…….	…….
125	2525 MHz

Table 3. Registers Table for Channel Setting

Address (Hex)	Name	Bits	Init	RW	Description
0x00	Channel	6:0	0101000	R/W	RF Channel Number

Transmit Power control

CYRF9935 supports 5 transmit power levels, which are +4 dBm, 0 dBm, –8 dBm, –14 dBm and –20 dBm.The +4 dBm power output is set using the indirect register 0x04 bit 7 (see Indirect Registers on page 31 for instructions on using the indirect registers). The other four power levels can be set using the bits 4:3 of direct register 0x03.

The table below summarizes the power levels available.

Table 4. For 4 dbm setting

Indirect Register Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
0x04	PA4DBM	7	0	R/W	Enable PA 4 dBm output power. 1: PA output power 4dBm 0: PA output power depends on RF_PWR setting in direct register 0x03.
	Reserved	6:0	0010001	R	Only ‘0010001’ allowed

Table 5. For Other power settings

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
0x03	RF_PWR	3:2	00	R/W	RF output power 00: –20 dBm 01: –14 dBm 10: –8 dBm 11: 0 dBm

RSSI Operation

CYRF9935 supports two types of RSSI measurements namely, RSSI Refresh and Packet RSSI.

RSSI Refresh is used to implement “Channel Assessment”. This means RSSI Refresh can be used to assess whether a channel is clean or not. It is useful to search a clean channel for Frequency Hopping Spread Spectrum implementations. RSSI Refresh requires the user to specify the RF channel for RSSI measurement in the Channel field of register 0x00 prior to RSSI measurements. RSSI Refresh is enabled by setting AUTO_RSSI_EN or RSSI_REFRESH bit fields of register 0x20. When AUTO_RSSI_EN is set, CYRF9935 evaluates RSSI continuously until AUTO_RSSI_EN is cleared. With RSSI_REFRESH enabled, CYRF9935 evaluates RSSI only once, after which RSSI_REFRESH will be cleared automatically. During RSSI evaluation, the RSSI result is updated onto the RSSI_VAL_MSB and RSSI_VAL_LSB bit fields of register 0x20. The RSSI value format is shown as below:

Table 6. RSSI value format

MSB				LSB
Bit 3	Bit 2	Bit 1	Bit 0	Bit 6

For example, when you start a RSSI refresh and get the value “0110_0101” from the register 0x20. The real RSSI value is “01011”.

Packet RSSI can be used to estimate the distance between TXer and RXer. CYRF9935 evaluates RSSI after the address field in packet being received is matched. We can use R_RX_PAYLOAD command to get the Packet RSSI if RSSI_AUTO_EN is set.

Table 7. Registers Table for RSSI Operation

Address (Hex)	Mnemonic	Bits	Init	RW	Description
0x00	Channel	6:0	0101000	R/W	RF channel
0x20	RSSI_VAL_LSB	6	0	R/W	RSSI LSB (Bit 0) Value This value is updated by RSSI Refresh function
	AUTO_RSSI_ EN	5	0	R/W	AUTO RSSI Enable 0: AUTO RSSI Disable 1: AUTO RSSI Enable
	RSSI_REFRESH	4	0	R/W	RSSI Refresh Set to 1 to start RSSI refresh. The bit is auto cleared when RSSI Refresh is done. RSSI Refresh value will update in RSSI_VAL_MSB and RSSI_VAL_LSB
	RSSI_VAL_MSB	3:0	0	R/W	RSSI MSB (Bit 4–1) Value This value is updated by RSSI Refresh function

Power Management

CYRF9935 has a built in state machine that controls the transition between the various operating states/modes of the radio. The state machine takes input from the various register settings, MODE pin and internal signals. The state diagram is shown in the figure below and conditions under which the state transition happens is explained in the table below.

Figure 2. State Diagram

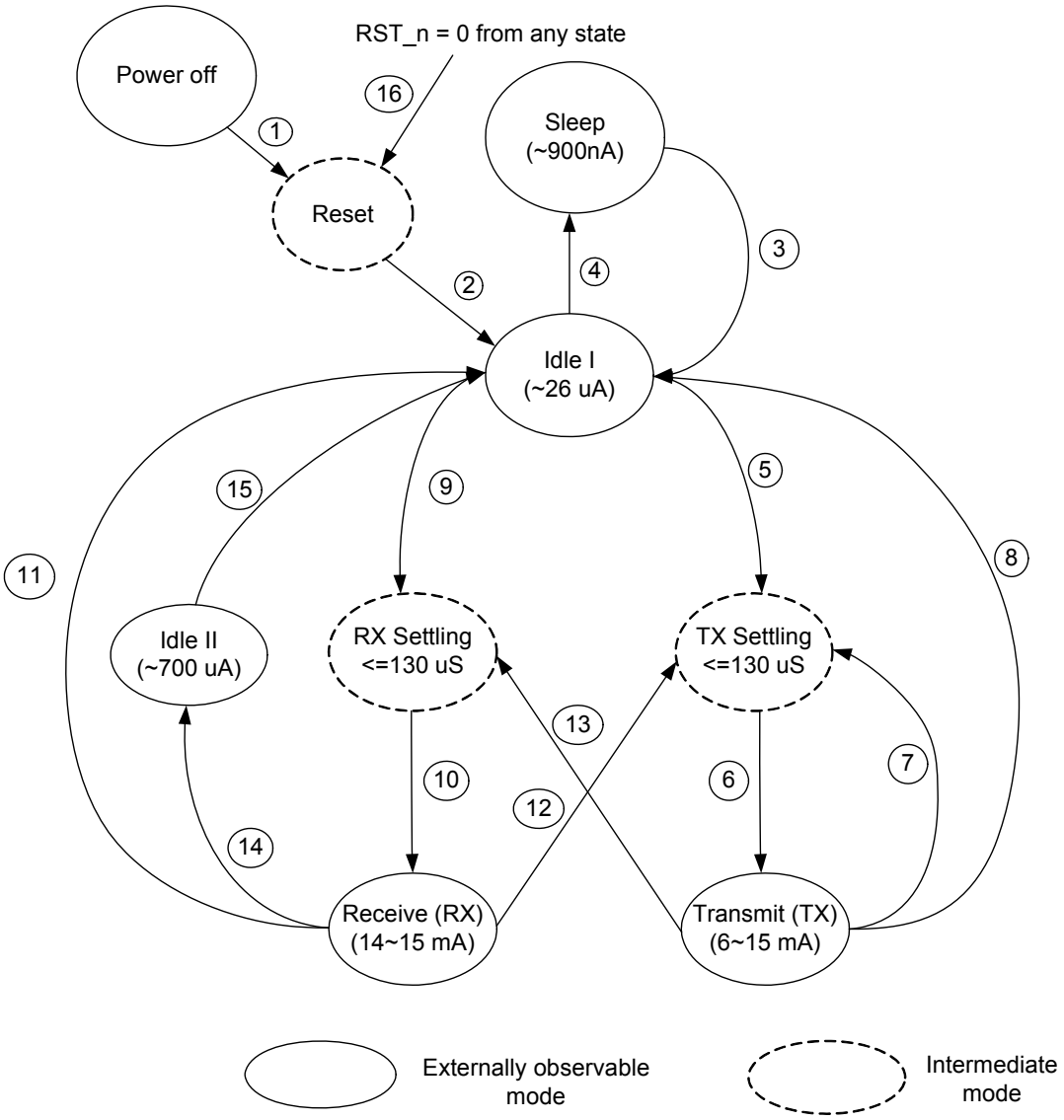


Table 8. States transfer and conditions

Current Mode	Next Mode	Path	Condition
Power Off	Reset	1	When going from Power Off to Reset, VIN is ramped from 0 V to 1.9 V, RST_n =1. Idle-I is reached after a delay of ≤ 50 ms (required for internal POR to be de-asserted) and ≤1.5 ms (required for crystal startup)
Reset	Idle-I	2	When going from Reset to Idle-I mode, RST_n line is released and is internally pulled high.
Sleep	Idle-I	3	Register 0x23 bit 1 is set to value '0' (Note it takes ≤1.5 ms for crystal startup before reaching Idle-I)
Idle-I	Sleep	4	Register 0x23 bit 1 is set to value '1'
Idle-I	Transmit	5–6	TX FIFO not empty (by writing to TX FIFO with W_TX_PAYLOAD SPI command) TX circuitry takes ~130 µs to settle
Transmit	Tx Settling	7	Transmitting next Data Packet on the same TX channel
			While switching between TX channels
Transmit	Receive	13–10	After a TX packet is sent with Auto ACK enabled
			With Auto ACK disabled, a TX packet is sent and RX request is asserted
Transmit	Idle-I	8	TX FIFO is empty with Auto ACK disabled
		13-10-11	With Auto ACK enabled, after receiving the ACK packet and there is no data in the TX FIFO.
Idle-I	Receive	9–10	Mode pin is asserted or Register 0x00 bit 1 is set to value '1'
Receive	Transmit	12-6	With Auto ACK enabled, TXer receives an ACK packet and TX FIFO is not empty.
			With Auto ACK enabled, TXer doesn't receive the ACK packet and retransmit is required.
			With Auto ACK enabled RXer receives a packet correctly & is going to send ACK packet.
			With Auto ACK disabled, RX operation is terminated and TX FIFO not empty.
Receive	Idle-I	11	With Auto ACK enabled TXer receives an ACK packet, TX FIFO empty and new receive is not requested.
			With Auto ACK disabled the receiver operation is terminated and TX FIFO is empty.
		12-6-8	With Auto ACK enabled, after transmitting the ACK packet, TX FIFO is empty and new receive is not requested.
Receive	Idle-II	14	With Auto ACK enabled, TXer times out without receiving ACK.
Idle-II	Idle-I	15	If Register 0x01 bit 3 =1 i.e. TX_MAX_ARSC Flag is cleared
Any mode	Reset	16	RST_n is pulled low for more than 5 µs

Note: RST_n line has an internal pull-up resistor which will pulls it high, hence the user does not need to pull RST_n high.

Idle-I Mode

After power up, CYRF9935 is by default in Idle-I Mode. It will leave the state when the sleep command (Register 0x23 bit 1 i.e. PCEN is set) is received or MCU requests to proceed transmit or receive. In this state, the radio typically consumes 26 µA of current. This state helps in minimizing average current consumption without compromising on start up time.

Sleep Mode

On Sleep Mode, CYRF9935 only consumes 900 nA of current. This mode enables the device to offer ultra-low power consumption. The chip enters the Sleep Mode when Register 0x23 bit 1 (PCEN) is set. The following points describe the behavior of the device in Sleep mode:

- Register values are maintained
- Registers can be accessed over SPI
- FIFO content is maintained
- FIFO content cannot be accessed

CYRF9935 returns to Idle-I Mode when register 0x23 bit 1 (PCEN) is cleared. At this moment, the micro-controller should wait until the crystal is stable before further SPI Access. The wait can be either 1500 µs or 150 µs. Waiting for 1500 µs is necessary if an external crystal used. If you want to reduce the wait time to 150 µs, a stable clock source, like an oscillator, is required.

Table 9. Registers Table for Sleep Enable

Address (Hex)	Mnemonic	Bits	Init	RW	Description
0x23	PCEN	1	0	R/W	Power Control Enable, Set to 1 to enter Sleep mode.

Transmit Mode

In Transmit Mode, CYRF9935 typically consumes 12 mA of current. It quits Idle-I Mode and enters Transmit Mode when there is data in FIFO waiting for transmit. During the transition to Transmit Mode, the radio cannot transmit data immediately because RF Circuit is not stable. The transition period is referred to as TX settling time. CYRF9935 has a short TX settling time of 130 µs.

Note: When CYRF9935 detects Sleep command (Register 0x23 bit 1 i.e. PCEN is set) on Transmit Mode, it will not enter Sleep Mode until the data in FIFO is sent out completely.

Receive Mode

In Receive Mode, CYRF9935 typically consumes 15 mA of current. It quits Idle-I mode and enters Receive Mode when it captures a command, either MODE pin is asserted or RX_ON i.e. bit 7 in register 0x01 is set. During the transition to Receive Mode, the radio cannot receive data immediately because RF Circuit is not stable. The transition period is referred to as RX settling time. CYRF9935 has a short RX settling time of 130 µs.

Note: When CYRF9935 detects Sleep command in Receive Mode, it will not enter Sleep Mode until the current packet receive finishes or Receive Mode is terminated by de-asserting MODE pin.

Idle II Mode

After transmitting with automatic acknowledgement (AUTO ACK) enabled the device goes in to receive mode. If an ACK is not received after exhausting the maximum number of retries the radio enters idle-II mode. The device goes to idle I mode on clearing the TX_MAX_ARSC flag (i.e. setting register 0X01 bit 3 = 1).

Baseband Engine

Packet Format

Table 10. Data Packet Format

Preamble	Address	Control Word	Data Payload	CRC
4~16 bits	4~6 Bytes	10 Bits	0~32 Bytes	1~2 Bytes

Preamble

The preamble length can be configured from 4~16 bits by writing appropriate value to indirect register 0x01.

Table 11. Register Table for Preamble

Indirect Register Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
0x01	Reserved	7:2	001000	R	Only ‘001000’ allowed
	PAL	1:0	11	R/W	Preamble length for TX 00: 4 bits 01: 8 bits 10: 12 bits 11: 16 bits

The preamble pattern is dependent upon the MSB of the group address. For example the preamble pattern (16 bit setting) will be 1010101010101010 if the MSB of the group address is 1. Similarly the preamble pattern will be 0101010101010101 for a group address with MSB 0. Preamble is automatically inserted ahead of the transmitted packet and removed from the received packet by the baseband engine.

Table 12. Register Table for CRC Control

Address (Hex)	Mnemonic	Bits	Init	RW	Description
0x03	CRCEN	1	1	R/W	Set to 1 to enable CRC.
	CRCLNG	0	1	R/W	0: 1-byte CRC 1: 2-byte CRC

Address

Address field consists of Group Address, Destination Pipe Address and Source Pipe Address. Table 13 shows the construction of Address field. The length of Group Address is programmable from 2 bytes to 4 bytes. Both Destination Pipe Address and Source Pipe Address are one byte in length.

Table 13. Address Field Format

Group Address	Destination Pipe Address	Source Pipe Address
2~4 Bytes	1-Byte	1-Byte

Table 14. Registers Table for Address control

Address (Hex)	Mnemonic	Bits	Init	RW	Description
0x03	ADDRLNG	6:5	01(B)	R/W	Group Address length 00: invalid 01: 2 bytes 10: 3 bytes 11: 4 bytes
0x09	GROUP_ADDR_0	7:0	0xE7	R/W	Group Address byte 0
0x0A	GROUP_ADDR_1	7:0	0xE7	R/W	Group Address byte 1
0x0B	GROUP_ADDR_2	7:0	0xE7	R/W	Group Address byte 2
0x0C	GROUP_ADDR_3	7:0	0xE7	R/W	Group Address byte 3
0x0D	ADDR_DEV	7:0	0xE7	R/W	Device PIPE Address
0x0E	ADDR_P1	7:0	0x00	R/W	PIPE 1 Address
0x0F	ADDR_P2	7:0	0x00	R/W	PIPE 2 Address
0x10	ADDR_P3	7:0	0x00	R/W	PIPE 3 Address
0x11	ADDR_P4	7:0	0x00	R/W	PIPE 4 Address
0x12	ADDR_P5	7:0	0x00	R/W	PIPE 5 Address
0x13	ADDR_P6	7:0	0x00	R/W	PIPE 6 Address
0x14	ADDR_P7	7:0	0x00	R/W	PIPE 7 Address
0x15	ADDR_P8	7:0	0x00	R/W	PIPE 8 Address

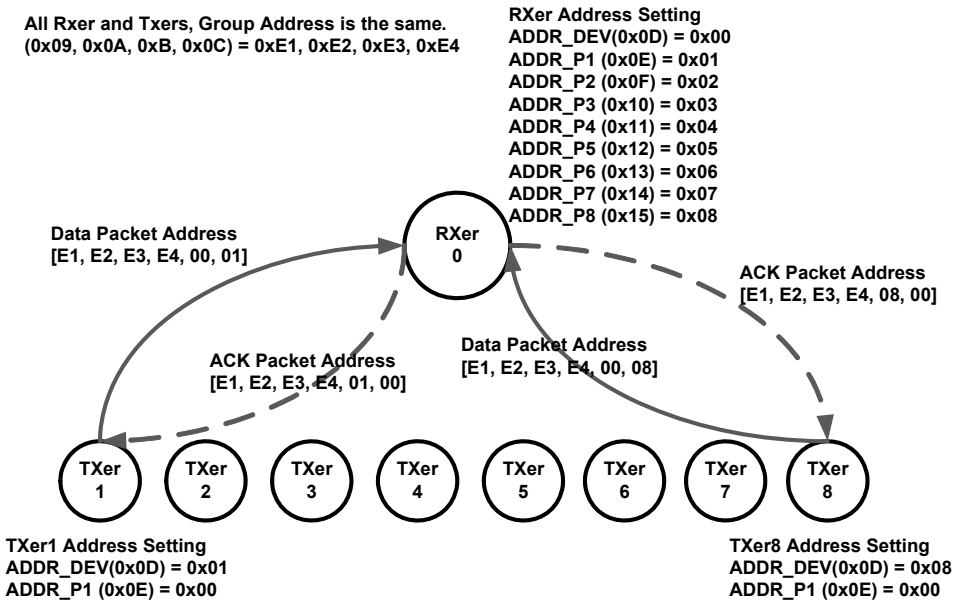
When a data packet is sent by TXer, Destination Pipe Address is obtained from ADDR_P1 or ADDR_P2 etc. depending on the pipe number used in the W_TX_PAYLOAD or W_ACK_PAYLOAD commands. Source Pipe Address is obtained from the register ADDR_DEV.

Source pipe address in the ACK packet send by the RXer is just a copy of the Destination Pipe Address in the received packet and vice versa.

Figure 3 on page 12 shows how to set addresses to work in 8:1 communication. All of TXers and RXer have the same Group Address 0xE1, 0xE2, 0xE3 and 0xE4. RXer can receive the packets coming from TXer1, TXer2…to TXer8. RXer has Device Pipe Address 0x00. Device Pipe Address in both TXer1 and TXer8 are configured with 0x01 and 0x08 respectively. ADDR_P1 on the TXers is set to 0x00 which is the Device Pipe Address for the RXer. Similarly the ADDR_P1 to ADDR_P8 on the RXer are set to the Device Pipe Addresses on TXer1 to TXer8 respectively. For example when TXer1 sends the data packet to RXer, Destination Pipe Address is 0x00 from ADDR_P1. TXer1's Source Pipe Address is 0x01 from ADDR_DEV. When RXer received the data packet from TXer1, it returns ACK packet in which the Source Pipe Address is 0x00 and the destination is the same as the received packet's Source Pipe Address. The same behaviour is followed when TXer8 wants to send the data packet to RXer.

Note: 0xAA and 0x55 are not valid values for GROUP_ADDR_3. These patterns are similar to the patterns used for the preamble and may result in communication failure or high Packet Error Rate.

Figure 3. Concept of address field applied to the 8:1 communication



Packet Control Word

Packet Control Word is a 10 bit field which is automatically attached to the transmitting packet and removed from the received packet by the radio's baseband engine.

Table 15. Packet Control Word Format

Payload Length	PID	NOACK
6 bits	3 bits	1 bit

Payload Length

Payload length is a 6 bit field which is attached if DPL is 1 (refer Register Sets on page 26). It represents the payload length for the data packet. A value of 000000 means 0 byte data payload is carried while a value of 000001 means 1 bytes data payload are carried and so on (values in excess of 100000 are not valid).

PID

The PID is a 3-bit value that ranges from 1~7 and is incremented by 1 for every new packet. For every packet received, if the PID is same as last packet and computed CRC is not same as the previous packet, it is assumed a new packet is received. If both the PID and CRC for the received packet is same as the previous packet then the current packet is assumed to be a re-transmission of the previous packet. PID is always 0 for Auto-ACK packet.

NOACK

The NOACK is a 1 bit field which is inserted to the transmitted packet if DPL is enabled (refer Register Sets on page 26). If NOACK is set to 0 then an ACK packet will be exchanged between the receiver and the transmitter, if an error free payload packet was transmitted. For an Auto-ACK packet or broadcast packet the NOACK is set to 1.

Data Payload

Length is programmable 0 to 32 bytes.

CRC

CRC is an error detection mechanism provided to validate the data correctness of a received packet. CRC length is programmable to be either 1 or 2 bytes long. The CRC value is calculated over the packet control word and payload. The CRC is automatically calculated and appended to the transmitted packet. On the receiver side the CRC is removed from the received packet by the baseband engine. The received packet will be ignored if CRC mismatch happens. The number of bytes in CRC field is set by CRCLNG bit in direct register 0x03 (refer to Register Sets on page 26).

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$, with an initial value of 0xFF.

The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$, with an initial value of 0xFFFF.

Broadcast Address

CYRF9935 can transmit and receive broadcast packets. The bit-field BCEN must be set to enable the function for a RXer. To transmit a broadcast packet, W_TX_PAYLOAD SPI command is used and the TX Pipe Number in the command is set with 0 to indicate this is a broadcast packet. You can use R_RX_PAYLOAD SPI command to receive the broadcast packet if RX Pipe Number in the command is set to 0. The broadcast address is 0xE7, 0x39, 0xCE, 0x73, 0x9C depending on the address length (ADDRLNG register) setting. The address must be reserved for the broadcast use. In a broadcast packet, both Destination Pipe Address and Source Pipe Address are not attached.

Table 16. Registers Table for Broadcast Enable

Address (Hex)	Mnemonic	Bits	Init	RW	Description
0x23	BCEN	0	0	R/W	Broadcasting Listening Enable 0: Broadcasting packets are ignored. 1: Broadcasting packet can be received.

Table 17. Registers Table for Broadcast Address

ADDRLNG	Broadcast Address Length	Broadcast Address
2 Bytes	3	0xE7, 0x39, 0xCE
3 Bytes	4	0xE7, 0x39, 0xCE, 0x73
4 Bytes	5	0xE7, 0x39, 0xCE, 0x73, 0x9C

Auto-Retransmit Mode

CYRF9935 supports Auto-retransmit mode. In this mode, a TXer will re-transmit the packet if it does not receive the ACK packet from a RXer. Before enabling Auto-retransmit mode, the following registers should be configured appropriately.

- Register 0x05 - bit fields in this register are used to enable Auto-Retransmission mode on each pipe for both TXer and RXer.
- Register 0x07 bit field AAWD (Auto-ACK Wait Delay) - TXer will wait for ACK packet arrival for an interval after the packet is sent. AAWD is used to configure the time interval. The interval starts counting at the end of packet transmission. The interval must be larger than 130 µs + the time required to complete the reception of the ACK packet. If TXer cannot receive ACK packet within the interval, TXer terminates RX mode immediately.
- Register 0x07 bit field RSD (Resend Delay) – Idle time between the end of AAWD and the beginning of retransmit.
- Register 0x08 bit field ARSC (Auto Resend Count) – The register is used to configure the maximum number of times to resend the same packet.
- Register 0x08 bit field ARS_CNT (Auto Resend Counting) – The register displays how many times the packet was retransmitted.

Table 18. Registers Table for Auto-Retransmission Mode

Address (Hex)	Mnemonic	Bits	Init	RW	Description
0x05	AA_P8	7	0	R/W	Enable Auto-ACK for PIPE 8
	AA_P7	6	0	R/W	Enable Auto-ACK for PIPE 7
	AA_P6	5	0	R/W	Enable Auto-ACK for PIPE 6
	AA_P5	4	0	R/W	Enable Auto-ACK for PIPE 5
	AA_P4	3	0	R/W	Enable Auto-ACK for PIPE 4
	AA_P3	2	0	R/W	Enable Auto-ACK for PIPE 3
	AA_P2	1	0	R/W	Enable Auto-ACK for PIPE 2
	AA_P1	0	0	R/W	Enable Auto-ACK for PIPE 1
0x07	AAWD	7:4	0000	R/W	Auto-ACK Wait Delay Values in unit of 250 µs. (0000 for 250 µs)
	RSD	3:0	0000	R/W	Resend Delay: 1st resend: AAWD + RSD 2nd resend: AAWD + (2 × RSD) 3rd resend: AAWD + (3 × RSD) 4th resend: AAWD + RSD 5th resend: AAWD + (2 × RSD) And so on. Values in unit of 250 µs. (0000 for 0 µs)
0x08	ARSC	7:4	0000	R/W	Setting the maximum Auto Resend Count
	ARS_CNT	3:0	0000	R	Auto Resend Count

In addition to the register setting appropriately, the user should use the correct SPI command to start the Auto-retransmit mode. In W_TX_PAYLOAD command, bit 7 of the first data byte which is behind the command must be set “0” to command CYRF9935 to send the packet with Auto-Retransmit mechanism.

Timing Diagram of Auto-Retransmit Mode

Figure 4. Timing Diagram of typical radio transmit and receive operation

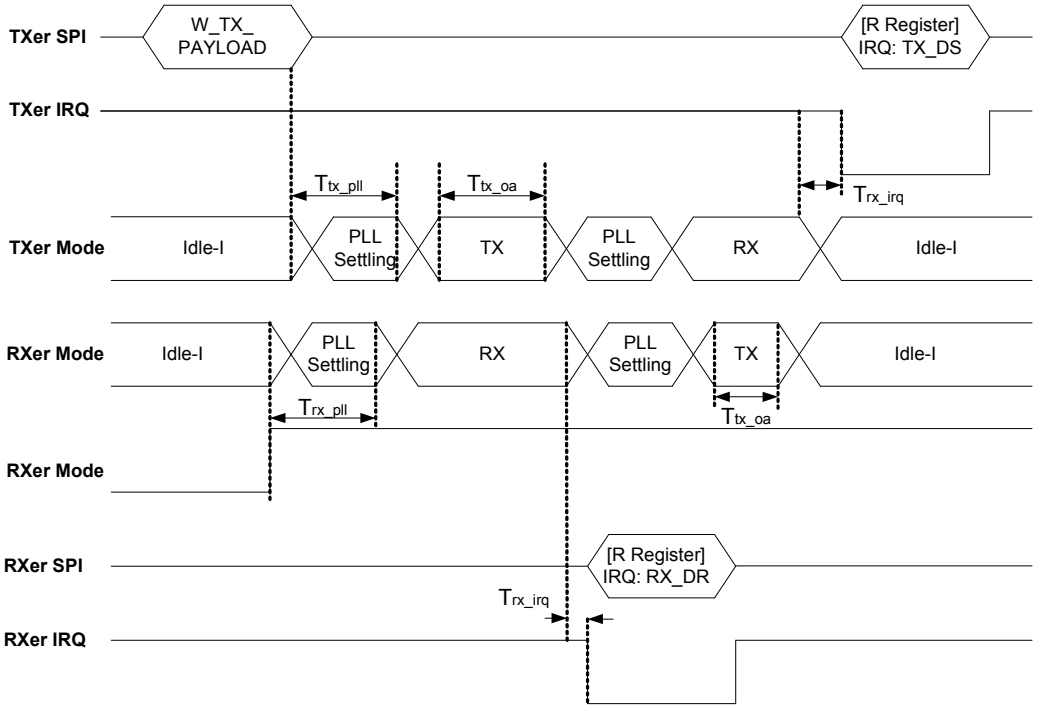


Table 19. Timing Characteristics

Item	Description	Min	Typ	Max
T_{tx_pll}	TX PLL Settling Time PLL turns on because of the assertion of SPI W_TX_PAYLOAD	–	130 µs	–
T_{tx_oa}	Transmit Data On Air It depends on the address length, packet length, data rate, CRC length and so on. Please refer to the Packet Format on page 10 for details. The below equation can be used to calculate the time for transmission of a packet. (Preamble length + Address length + Control Word length + Data Payload length + CRC length) x (1/Data Rate) For example, for a packet having 16 bits preamble, 24 bits Address, 10 bits Control Word, 40 bits Data Payload and 16 bits CRC with 2 Mbps data rate: T_{tx_oa} = (16+24+10+40+16)/(1/2M) = 53 µs	–	–	–
T_{rx_pll}	RX PLL Settling Time PLL turns on when MODE pin is asserted or bit 7 of register 0x00 is set	–	130 µs	–
T_{rx_irq}	RX IRQ Assertion Time The delay from the time the packet is received to IRQ assertion.	0	–	–

Data Packet Loss

The figure below shows CYRF9935 behavior if RXer loses the data packet which is sent by TXer. “Data On Air” represents the transmit sequence on the air including Data Packet and ACK Packet. In the diagram, there are several tags which are used to depict the real scenario during the data packet loss. These are explained below:

1. Data packet is sent by TXer
2. Data packet is interfered with, hence RXer cannot receive the same
3. RXer doesn’t transmit ACK packet on the air
4. TXer aborts the receive and waits for AAWD and then for RSD
5. TXer resends Data packet
6. RXer receives the data packet correctly
7. RXer sends ACK packet on the air
8. TXer receives ACK packet.
9. TXer IRQ asserted because the packet is sent successfully.

Figure 5. Data Packet Loss Scenario

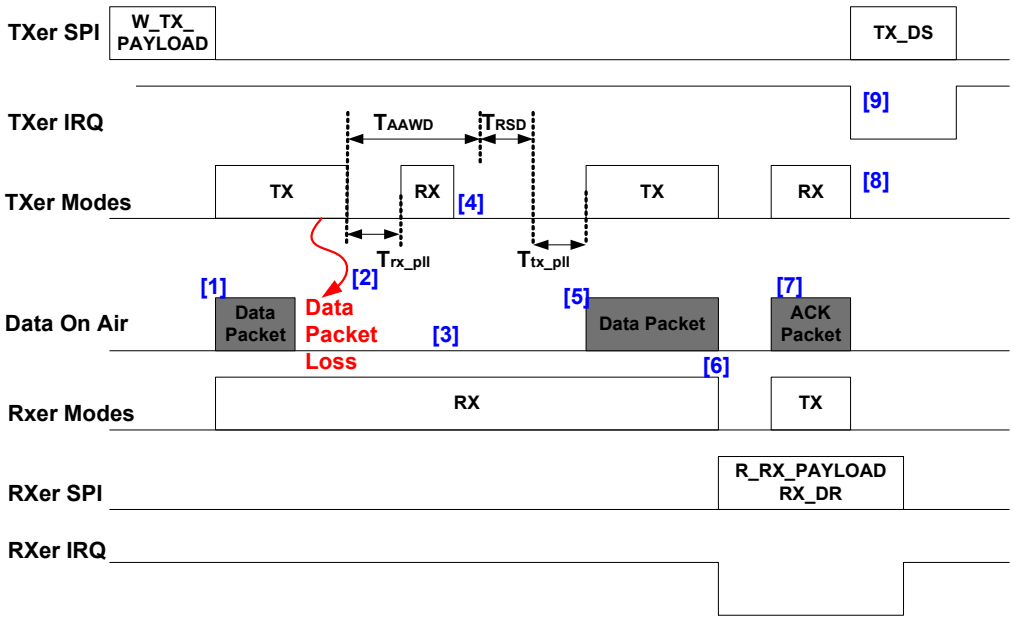


Table 20. Data Packet Loss

Item	Description	Min	Typ	Max
T_{AAWD}	Time for ACK packet wait delay. Please refer to Register 0x07. (Note 4)	–	–	–
T_{RSD}	Time for resend delay. Please refer to Register 0x07	–	–	–

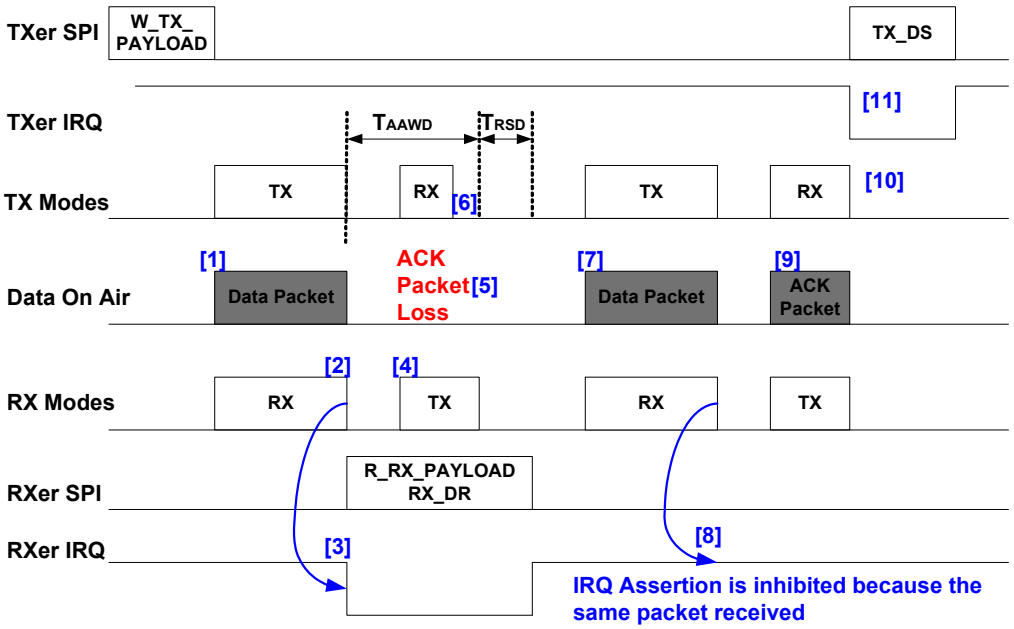
Note
4. T_{AAWD} should be larger than PLL settling time + ACK Packet air time.

ACK Packet Loss

The diagram below shows CYRF9935 behavior if TXer loses the ACK packet which is sent by RXer. “Data On Air” represents the transmit sequence on the air including Data Packet and ACK Packet. In the diagram, there are several tags which are used to depict the scenario during the data packet loss. These are explained below:

1. Data Packet is sent by TXer
2. Data Packet is received correctly by RXer
3. RXer IRQ asserted to indicate that data is ready in FIFO
4. RXer sends ACK packet on the air
5. ACK packet is interfered with
6. TXer aborts the receive and waits for AAWD and then for RSD
7. TXer resends Data Packet
8. RXer doesn’t assert IRQ because the same data packet is received
9. RXer sends ACK packet on the air
10. TXer receives ACK packet
11. TXer IRQ asserted because the packet is sent successfully

Figure 6. ACK Packet Loss Scenario



FIFO Control

Overview

In CYRF9935, there are TX FIFO and RX FIFO to store the transmit data and the receive data respectively. Both TX FIFO and RX FIFO can be programmed in either 3 blocks or 6 blocks configuration. In case of a 3-block configuration each block can store 32 bytes of data whereas in case of a 6-block configuration each block can store 16 bytes of data.

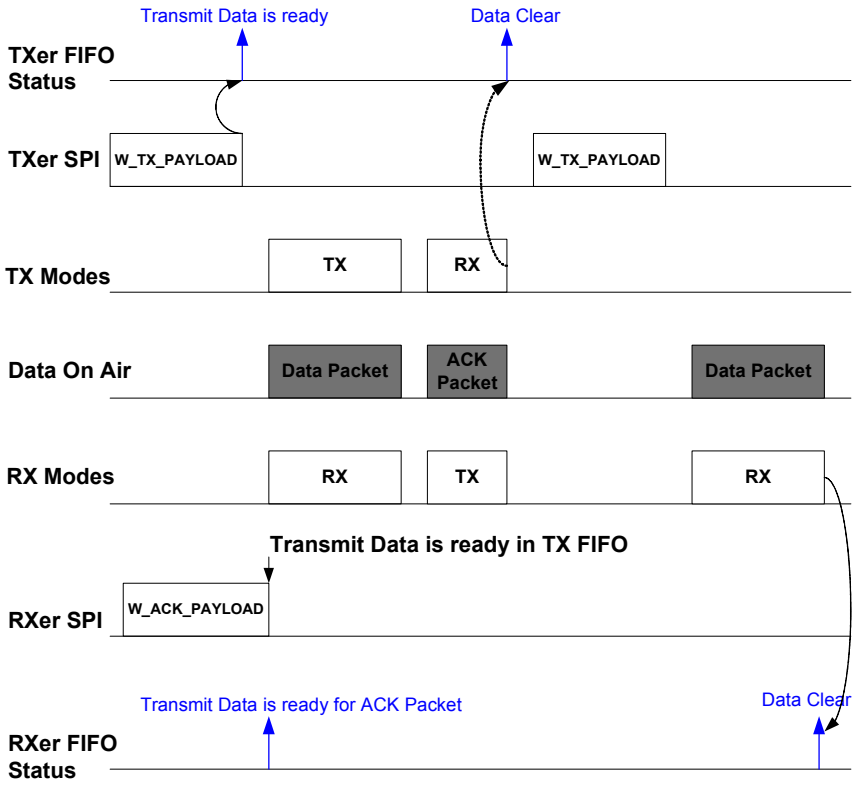
Table 21. Registers Table for FIFO Configuration

Address (Hex)	Mnemonic	Bits	Init	RW	Description
0x1E	TX_FIFO_CONFIG	6	0	R/W	0: 3 Blocks, 32-Byte in each block 1: 6 Blocks, 16-Byte in each block
0x1F	RX_FIFO_CONFIG	6	0	R/W	0: 3 Blocks, 32-Byte in each block 1: 6 Blocks, 16-Byte in each block

TX FIFO Access

We can access TX FIFO with SPI Commands, W_TX_PAYLOAD or W_ACK_PAYLOAD. Figure 7 shows how to use the SPI commands to transmit data in Data Packet and ACK Packet. When a TXer wants to send Data Packet, W_TX_PAYLOAD is available to fill the transmit data into TX FIFO. W_ACK_PAYLOAD is available for RXer to fill the transmit data into TX FIFO. The data in TX FIFO of RXer will be attached to ACK packet.

Figure 7. TX FIFO Access with SPI Commands



Please keep the following in mind when accessing TX FIFO.

- In non-Auto-Retransmit Mode, data in TX FIFO will be cleared immediately when the data is sent
- For a TXer, data in TX FIFO will be held until ACK is received or re-transmit is terminated if Auto-Retransmit Mode is enabled
- For a RXer, data in TX FIFO will be held until a new data packet is received in the same pipe, if auto-ACK with ACK payload is enabled
- The current TX FIFO write is aborted if the written data size is more than TX FIFO block size
- The current TX FIFO write is also aborted if no free blocks are available to store the data
- We can monitor TX FIFO status through the registers
- At least, one byte data write is required

Table 22. Registers Table for FIFO Status

Address (Hex)	Mnemonic	Bits	Init	RW	Description
0x01	TX_FIFO_STATE	1	1	R/W	This bit is set when the FIFO state matches the configuration selected by the TX_FIFO_STA_SEL bits in register 28. This bit is automatically cleared when the condition is not true and cannot be cleared by writing into the register. Refer to Table 23 for TX FIFO State explanation.
0x1F	RX_FIFO_NOT_EMPTY	0	0	R/W	1 indicates the RX_FIFO is not empty. Automatically cleared when RX_FIFO is empty.
0x28	TX_FIFO_STA_SEL	1:0	00	R/W	TX FIFO state selection: 00: TX_FIFO_EMPTY. 01: TX_FIFO_FULL. 10: TX_FIFO_NOT_EMPTY. 11: TX_FIFO_NOT_FULL. Refer to Table 23 for TX FIFO State explanation.

Table 23. TX FIFO State Explanation

TX_FIFO_STA_SEL	TX_FIFO_STATE Output Definition
00	TX FIFO Empty Status 0: One of the blocks in TX FIFO has data 1: All blocks in TX FIFO are empty
01	TX FIFO Full Status 0: At least one of the blocks in TX FIFO is empty 1: All blocks in the TX FIFO are full
10	TX FIFO Not Empty Status 0: All blocks are empty 1: At least one block has data
11	TX FIFO Not Full Status 0: All blocks have data. 1: At least one block is empty in TX FIFO

RX FIFO Access

We can access RX FIFO with SPI command, R_RX_PAYLOAD. We use the SPI command to read data from RX FIFO while IRQ is asserted and RX_DR status bit is set. In CYRF9935, RXer will not receive the packets when RX FIFO is full.

SPI Command

SPI Timing

In general, a SPI Command consists of a command and data part in that order. The command part is used to represent the purpose of the SPI command. For example, in Figure 8, C7–C0 is the command part. D0, D1, D2, and so on are defined as the data part.

Figure 8. SPI Read Timing

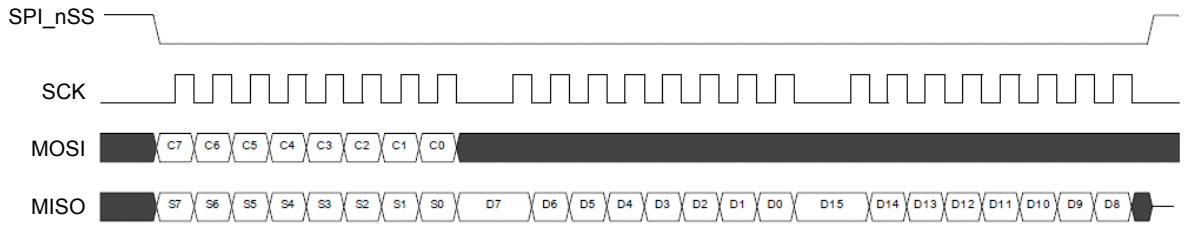


Figure 9. SPI Write Timing

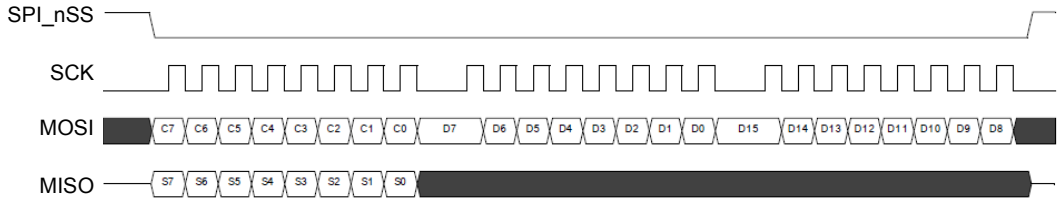


Figure 10. SPI Timing Requirement

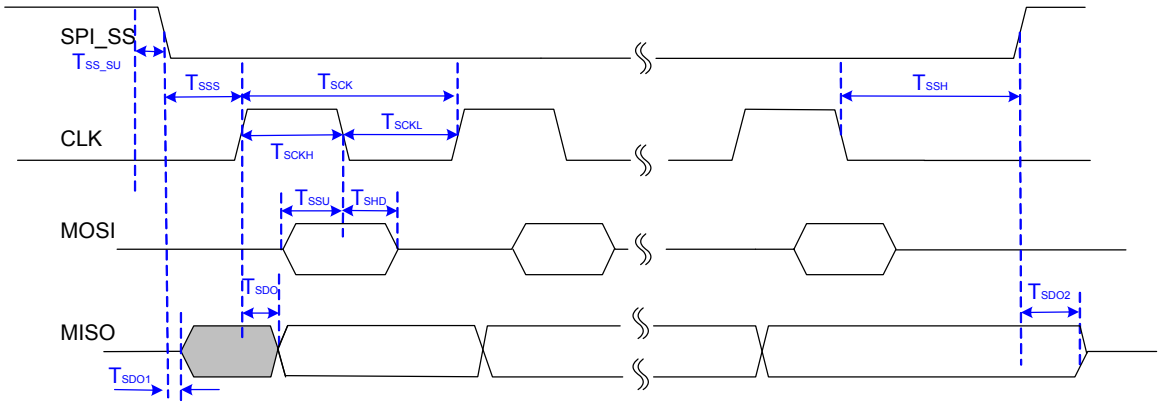


Table 24. SPI Characteristics

Symbol	Description	Minimum	Maximum	Units
T_{ssu}	Data setup time	5	–	ns
T_{shd}	Data hold time	2	–	ns
T_{sdo}	SPI_nSS to data valid	–	60	ns
T_{sckl}	SCK low time	40	–	ns
T_{sckh}	SCK high time	40	–	ns
T_{sck}	SCK frequency	–	8	MHz
T_{r_spi}	SCK rise and fall time	–	35	ns
T_{sss}	SPI_nSS to SCK setup	30	–	ns
T_{ssh}	SCK to SPI_nSS hold	20	–	ns
T_{ss_hd}	SPI_nSS inactive time	50	–	ns

Command List

Table 25 shows all of the commands that CYRF9935 supports. Data Command Word defines the data in command part of SPI command. Command Length defines the length in the data phase.

Table 25. Command List

Command name	Command Word	Data Length	Description
R_REGISTER	00AAAAAA [5]	1 byte	Read register value. Refer to Table 27 on page 23.
W_REGISTER	01AAAAAA [5]	1 byte	Write register value. Refer to Table 28 on page 23.
R_RX_PAYLOAD	10000000	3 to 34 bytes	Read RX_FIFO content. Refer to Table 29 on page 23.
W_TX_PAYLOAD	101PDDDD [6, 7]	2 to 33 bytes	Write TX_FIFO content. Refer to Table 31 on page 24.
W_ACK_PAYLOAD	1110PDDD [6, 8]	1 to 32 bytes	Write ACK data payload to TX_FIFO. Refer to Section Table 32 on page 24.
REUSE_TX_PAYLOAD	11010000	1 byte	The data in TX FIFO is reused. Refer to Section Table 33 on page 24.
FLUSH_TX_FIFO	11000101	None	Flush TX_FIFO
FLUSH_RX_FIFO	11000100	None	FLUSH_RX_FIFO command clears bit 0 (RX_FIFO_NOT_EMPTY) of register 0x01 and bits 0–5 of register 0x1f. The RX_FIFO contents are not valid after this command.
NOP	11111111	None	No operation

Notes
5. AAAAAA: Address of the register being accessed.
6. P: Output power for this packet;
   P = 1 for 0dBm;
   P = 0 for the TX output power as the register RF_PWR assigned.
7. DDDD: Target pipe number;
   DDDD = 0, broadcasting;
   DDDD = 1~8, corresponding pipe
8. DDD: Target pipe number;
   DDD = 0 for pipe 1, DDD = 1 for pipe 2 and so on.

SPI Status in Command Phase

When a command is issued the radio always outputs the register 0x01 value. This helps the MCU to get the radio status without having to ask for it specifically. The NOP command can be used to read radio status without performing operation.

Table 26. SPI Command for NOP

Byte Num.	Phases	B7	B6	B5	B4	B3	B2	B1	B0	Note
Byte 1	Command	1	1	1	1	1	1	1	1	–

SPI Command for Register Read and Write

There are two SPI commands that are used to access the radio register. R_REGISTER is used to read the content of a register. W_REGISTER is used to write data to any register.

Table 27. SPI Command for Register Read

Byte Num.	Phases	B7	B6	B5	B4	B3	B2	B1	B0	Note
Byte 1	Command	0	0	Register Address						–
Byte 2	Data	Register Content								–

Table 28. SPI Command for Register Write

Byte Num.	Phases	B7	B6	B5	B4	B3	B2	B1	B0	Note
Byte 1	Command	0	1	Register Address						–
Byte 2	Data	Register Content								–

SPI Command for RX FIFO Access

There are two commands, R_RX_PAYLOAD and FLUSH_RX_FIFO to handle RX FIFO access. When CYRF9935 receives a data packet, the data will be stored into RX FIFO. R_RX_PAYLOAD command is used to read the data from the RX FIFO. FLUSH_RX_FIFO command clears bit 0 (RX_FIFO_NOT_EMPTY) of register 0x01 and bits 0–5 of register 0x1f. The RX_FIFO contents are not valid after this command.

Table 29. SPI Command for R_RX_PAYLOAD

Byte Num.	Phases	B7	B6	B5	B4	B3	B2	B1	B0	Note
Byte 1	Command	1	0	0	0	0	0	0	0	
Byte 2	Data	Packet RSSI				RX Pipe Number				Note 9, 10
Byte 3	Data	Reserved				Data Length				Note 11
Byte 4–35	Data	Read Data from RX FIFO								

Table 30. SPI Command for FLUSH_RX_FIFO

Byte Num.	Phases	B7	B6	B5	B4	B3	B2	B1	B0	Note
Byte 1	Command	1	1	0	0	0	1	0	0	–

Notes

9. Packet RSSI
   This field contains the RSSI value which was evaluated while receiving the packet.
10. RX Pipe Number
    This field indicates to which pipe the data belongs.
11. Data Length
    This field indicates how many bytes in RX FIFO should be read out. The maximum length is 32 Bytes. The minimum length is 1 Byte. The length from Byte Number 4-35 depends on this field.

SPI Command for TX FIFO Access

There are four commands, W_TX_PAYLOAD, W_ACK_PAYLOAD, REUSE_TX_PAYLOAD and FLUSH_TX_FIFO to handle TX FIFO access. TX FIFO Access on page 19 introduces how to use W_TX_PAYLOAD command and W_ACK_PAYLOAD command. REUSE_TX_PAYLOAD command is useful when CYRF9935 cannot proceed to retransmit the packet because the resend count has reached the maximum value. We can use this command to reuse data from previous packet. The data which is held in TX FIFO is sent again. The FLUSH_TX_FIFO command is used to flush/clear the contents of the TX FIFO.

Table 31. SPI Command for W_TX_PAYLOAD

Byte Num.	Phases	B7	B6	B5	B4	B3	B2	B1	B0	Note
Byte 1	Command	1	0	1	P	TX Pipe Number				Note 12
Byte 2	Data	Note 13	RF Channel (Note 14)							Note 13, 14
Byte 3–34	Data	Write Data to TX FIFO								

Table 32. SPI Command for W_ACK_PAYLOAD

Byte Num.	Phases	B7	B6	B5	B4	B3	B2	B1	B0	Note
Byte 1	Command	1	1	1	0	P	ACK Pipe Number			Note 15, 16
Byte 2–33	Data	Write Data to TX FIFO								

Table 33. SPI Command for REUSE_TX_PAYLOAD

Byte Num.	Phases	B7	B6	B5	B4	B3	B2	B1	B0	Note
Byte 1	Command	1	1	0	1	0	0	0	0	
Byte 2	Data	Note 13	RF Channel							Refer to Table 31 on page 24.

Table 34. SPI Command for FLUSH_TX_FIFO

Byte Num.	Phases	B7	B6	B5	B4	B3	B2	B1	B0	Note
Byte 1	Command	1	1	0	0	0	1	0	1	–

Notes

12. Bit 4, Power
    This bit indicates RF TX Power.
    1: RF TX Power is 0dBm, 0: RX TX Power is decided by the register (0x03, Bit 3-2, RF_PWR)
13. Bit 7 indicates if TXer asks RXer for ACK packet.
    0: RXer should respond with ACK packet to the current data packet, if ACK_EN is set for the corresponding pipe in register 0x05.
    1: RXer not required to respond with ACK packet to the current data packet.
14. Bit 6-0, RF Channels
    The RF Channel setting is only effective for TXer while sending packets and listening to ACK packets.
15. Bit 3, Power
    This bit indicates how to decide RF TX Power.
    1: RF TX Power is 0dBm, 0: RX TX Power is decided by the register (0x03, Bit 3-2, RF_PWR)
16. ACK Pipe Number.
    This register specifies the target pipe number for the TX FIFO write. ACK Pipe number setting is “Source pipe number - 1”. For example, the TXer uses pipe 2 for current transmission, the RXer ACK pipe number setting must be 1.

*Very Important – Further explanation to Pipe Number Setting for SPI Command *

In R_RX_PAYLOAD and W_TX_PAYLOAD commands, there are 4-bits to represent the pipe number. In both cases, a value 0 indicates broadcast packet transmission. Any values between 1 and 8 for this field will initiate data transfer on the corresponding pipe. But for, W_ACK_PAYLOAD only 3-bit pipe numbers are applicable and the command does not support the broadcast packet. The value 0–7 indicates to send the packet to Pipe 1–8. The table below explains the case.

Table 35. Pipe Number Setting

CYRF9935 Pipe Number	R_RX_PAYLOAD RX Pipe Number	W_TX_PAYLOAD TX Pipe Number	W_ACK_PAYLOAD ACK Pipe Number
Broadcast Address	0	0	Not Available
1	1	1	0
2	2	2	1
3	3	3	2
4	4	4	3
5	5	5	4
6	6	6	5
7	7	7	6
8	8	8	7