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CYUSB301X/CYUSB201X

EZ-USB® FX3: SuperSpeed USB Controller

Features

- Universal serial bus (USB) integration
  - USB 3.1, Gen 1 and USB 2.0 peripherals compliant with USB 3.1 Specification Revision 1.0 (TID # 340800007)
  - 5-Gbps SuperSpeed PHY compliant with USB 3.1 Gen 1
  - High-speed On-The-Go (HS-OTG) host and peripheral compliant with OTG Supplement Version 2.0
  - Thirty-two physical endpoints
  - Support for battery charging Specification 1.1 and accessory charger adaptor (ACA) detection
- General Programmable Interface (GPIF™ II)
  - Programmable 100-MHz GPIF II enables connectivity to a wide range of external devices
  - 8-, 16-, 24-, and 32-bit data bus
  - Up to16 configurable control signals
- Fully accessible 32-bit CPU
  - ARM926EJ core with 200-MHz operation
  - 512-KB or 256-KB embedded SRAM
- Additional connectivity to the following peripherals
  - SPI master at up to 33 MHz
  - UART support of up to 4 Mbps
  - I^2C master controller at 1 MHz
  - I^2S master (transmitter only) at sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz
- Selectable clock input frequencies
  - 19.2, 26, 38.4, and 52 MHz
  - 19.2-MHz crystal input support
- Ultra low-power in core power-down mode
  - Less than 60 µA with VBATT on and 20 µA with VBATT off
- Independent power domains for core and I/O
  - Core operation at 1.2 V
  - I2S, UART, and SPI operation at 1.8 to 3.3 V
  - I^2C operation at 1.2 V to 3.3 V
- Package options
  - 121-ball, 10- × 10-mm, 0.8-mm pitch Pb-free ball grid array (BGA)
  - 131-ball, 4.7- × 5.1-mm, 0.4-mm pitch wafer-level chip scale package (WLCSP)
  - See Table 20 for details on the eight FX3 variants
- EZ-USB® Software Development Kit (SDK) for code development of firmware and PC Applications
  - Includes RTOS Framework (using ThreadX Version 5)
  - Firmware examples covering all I/O modules
  - Visual Studio host examples using C++ and C#
- SuperSpeed Explorer Board available for rapid prototyping
  - Several accessory boards also available:
    - Adapter boards for Xilinx/Altera FPGA development
    - Adapter board for Video development
    - CPLD board for concept testing and initial development

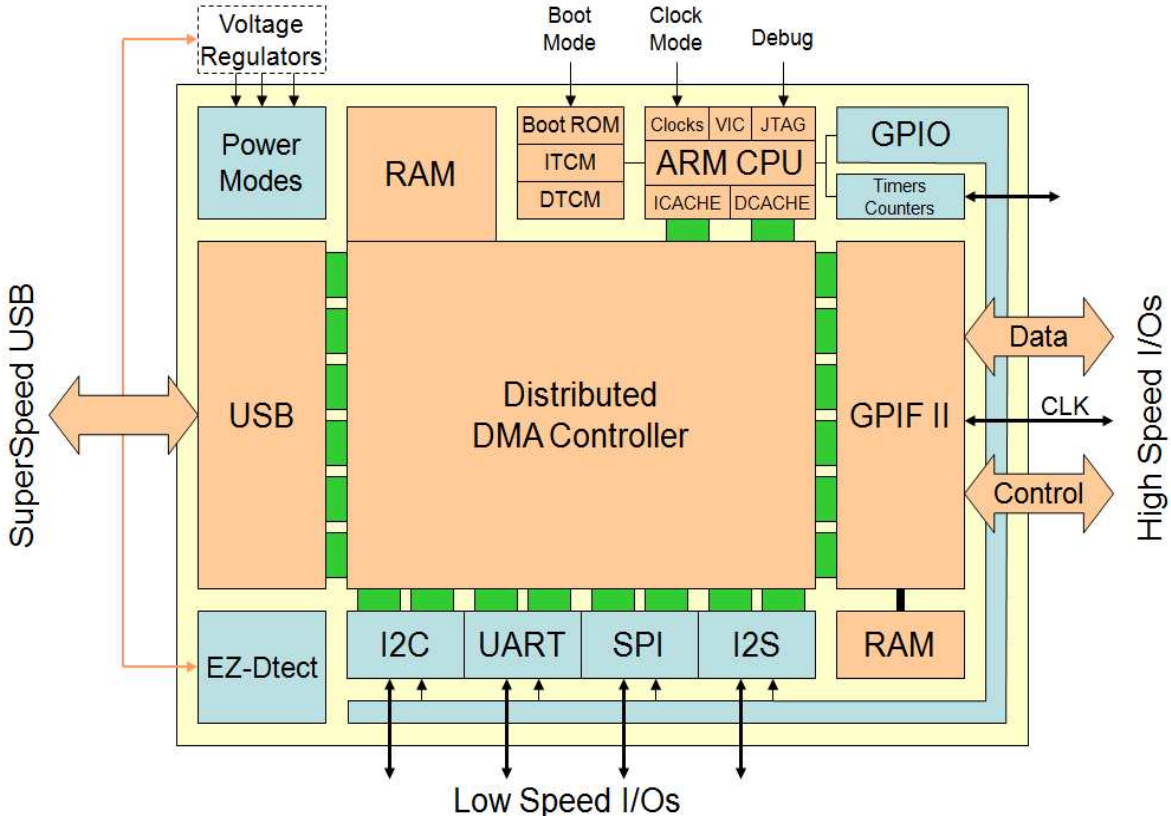
Applications

- Digital video camcorders
- Digital still cameras
- Printers
- Scanners
- Video capture cards
- Test and measurement equipment
- Surveillance cameras
- Personal navigation devices
- Medical imaging devices
- Video IP phones
- Portable media players
- Industrial cameras
- Data loggers
- Data acquisition
- High-performance Human Interface Devices (gesture recognition)

Functional Description

For a complete list of related documentation, click here.

Logic Block Diagram



More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right <product> device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA87889, How to design with FX3/FX3S.

- Overview: USB Portfolio, USB Roadmap
- USB 3.0 Product Selectors: FX3, FX3S, CX3, HX3, West Bridge Benicia
- Application notes: Cypress offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FX3 are:
  - AN75705 - Getting Started with EZ-USB FX3
  - AN76405 - EZ-USB FX3 Boot Options
  - AN70707 - EZ-USB FX3/FX3S Hardware Design Guidelines and Schematic Checklist
  - AN65974 - Designing with the EZ-USB FX3 Slave FIFO Interface
  - AN75779 - How to Implement an Image Sensor Interface with EZ-USB FX3 in a USB Video Class (UVC) Framework
  - AN86947 - Optimizing USB 3.0 Throughput with EZ-USB FX3
  - AN84868 - Configuring an FPGA over USB Using Cypress EZ-USB FX3
  - AN68829 - Slave FIFO Interface for EZ-USB FX3: 5-Bit Address Mode
  - AN73609 - EZ-USB FX2LP/ FX3 Developing Bulk-Loop Example on Linux
  - AN77960 - Introduction to EZ-USB FX3 High-Speed USB Host Controller
  - AN76348 - Differences in Implementation of EZ-USB FX2LP and EZ-USB FX3 Applications
  - AN89661 - USB RAID 1 Disk Design Using EZ-USB FX3S
- Code Examples: < Modify as required >
  - USB Hi-Speed
  - USB Full-Speed
  - USB SuperSpeed
- Technical Reference Manual (TRM):
  - EZ-USB FX3 Technical Reference Manual
- Development Kits:
  - CYUSB3KIT-003, EZ-USB FX3 SuperSpeed Explorer Kit
  - CYUSB3KIT-001, EZ-USB FX3 Development Kit
- Models: IBIS

EZ-USB FX3 Software Development Kit

Cypress delivers the complete software and firmware stack for FX3, in order to easily integrate SuperSpeed USB into any embedded application. The Software Development Kit (SDK) comes with tools, drivers and application examples, which help accelerate application development.

GPIF™ II Designer

The GPIF II Designer is a graphical software that allows designers to configure the GPIF II interface of the EZ-USB FX3 USB 3.0 Device Controller.

The tool allows users the ability to select from one of five Cypress supplied interfaces, or choose to create their own GPIF II interface from scratch. Cypress has supplied industry standard interfaces such as Asynchronous and Synchronous Slave FIFO, Asynchronous and Synchronous SRAM, and Asynchronous SRAM. Designers who already have one of these pre-defined interfaces in their system can simply select the interface of choice, choose from a set of standard parameters such as bus width (x8, 16, x32) endianess, clock settings, and compile the interface. The tool has a streamlined three step GPIF interface development process for users who need a customized interface. Users are able to first select their pin configuration and standard parameters. Secondly, they can design a virtual state machine using configurable actions. Finally, users can view output timing to verify that it matches the expected timing. Once the three step process is complete, the interface can be compiled and integrated with FX3.

Contents

Functional Overview

Cypress's EZ-USB FX3 is a SuperSpeed peripheral controller, providing integrated and flexible features.

FX3 has a fully configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. GPIF II is an enhanced version of the GPIF in FX2LP, Cypress's flagship USB 2.0 product. It provides easy and glueless connectivity to popular interfaces, such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interfaces, and parallel ATA.

FX3 has integrated the USB 3.1 Gen 1 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375-MBps data transfer from GPIF II to the USB interface.

An integrated USB 2.0 OTG controller enables applications in which FX3 may serve dual roles; for example, EZ-USB FX3 may function as an OTG Host to MSC as well as HID-class devices.

FX3 contains 512 KB or 256 KB of on-chip SRAM (see Ordering Information on page 45) for code and data. EZ-USB FX3 also provides interfaces to connect to serial peripherals such as UART, SPI, I^2C, and I^2S.

FX3 comes with application development tools. The software development kit comes with firmware and host application examples for accelerating time to market.

FX3 complies with the USB 3.1, Gen 1.0 specification and is also backward compatible with USB 2.0. It also complies with the Battery Charging Specification v1.1 and USB 2.0 OTG Specification v2.0.

Application Examples

In a typical application (see Figure 1), the FX3 functions as the main processor running the application software that connects external hardware to the SuperSpeed USB connection. Additionally, FX3 can function as a coprocessor connecting via the GPIF II interface to an application processor (see Figure 2) and operates as a subsystem providing SuperSpeed USB connectivity to the application processor.

Figure 1. EZ-USB FX3 as Main Processor

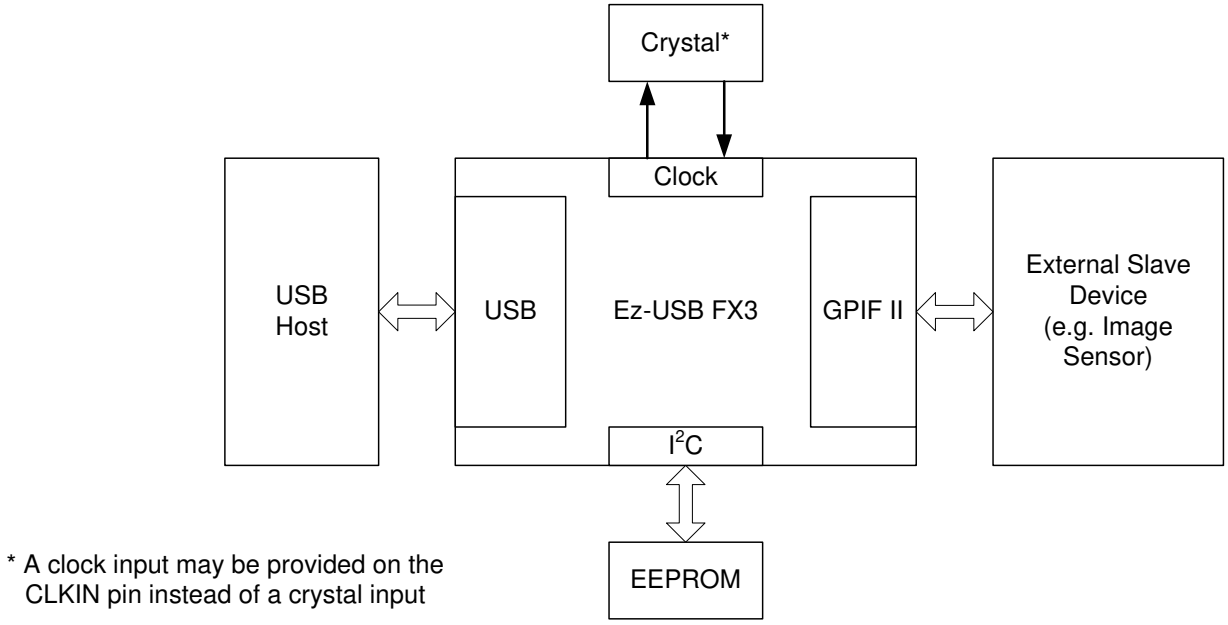
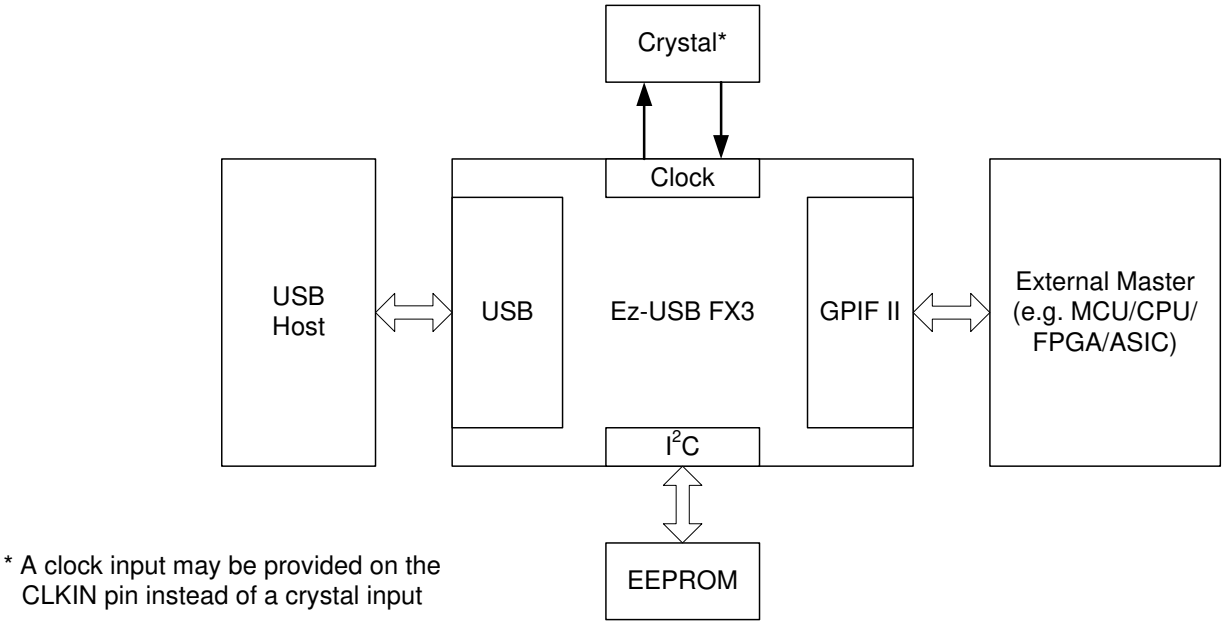


Figure 2. EZ-USB FX3 as a Coprocessor



USB Interface

FX3 complies with the following specifications and supports the following features:

- Supports USB peripheral functionality compliant with USB 3.1 Specification Revision 1.0 and is also backward compatible with the USB 2.0 Specification.
- FX3 Hi-Speed parts (CYUSB201X) only support USB 2.0.
- Complies with OTG Supplement Revision 2.0. It supports High-Speed, Full-Speed, and Low-Speed OTG dual-role device capability. As a peripheral, FX3 is capable of SuperSpeed, High-Speed, and Full-Speed. As a host, it is capable of High-Speed, Full-Speed, and Low-Speed.
- Supports Carkit Pass-Through UART functionality on USB D+/D– lines based on the CEA-936A specification.
- Supports 16 IN and 16 OUT endpoints.
- Supports the USB 3.0 Streams feature. It also supports USB Attached SCSI (UAS) device-class to optimize mass-storage access performance.
- As a USB peripheral, application examples show that the FX3 supports UAS, USB Video Class (UVC), and Mass Storage Class (MSC) USB peripheral classes. All other device classes can be supported by customer firmware; a template example is provided as a starting point.
- As an OTG host, application examples show that FX3 supports MSC and HID device classes.

Note When the USB port is not in use, disable the PHY and transceiver to save power.

OTG

FX3 is compliant with the OTG Specification Revision 2.0. In OTG mode, FX3 supports both A and B device modes and supports Control, Interrupt, Bulk, and Isochronous data transfers.

FX3 requires an external charge pump (either standalone or integrated into a PMIC) to power VBUS in the OTG A-device mode.

The Target Peripheral List for OTG host implementation consists of MSC- and HID-class devices.

FX3 does not support Attach Detection Protocol (ADP).

OTG Connectivity

In OTG mode, FX3 can be configured to be an A, B, or dual-role device. It can connect to the following:

- ACA device
- Targeted USB peripheral
- SRP-capable USB peripheral
- HNP-capable USB peripheral
- OTG host
- HNP-capable host
- OTG device

ReNumeration

Because of FX3's soft configuration, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, FX3 enumerates automatically with the Cypress Vendor ID (0x04B4) and downloads firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and connect. FX3 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration, happens instantly when the device is plugged in.

EZ-Dtect

FX3 supports USB Charger and accessory detection (EZ-Dtect). The charger detection mechanism complies with the Battery Charging Specification Revision 1.1. In addition to supporting this version of the specification, FX3 also provides hardware support to detect the resistance values on the ID pin.

FX3 can detect the following resistance ranges:

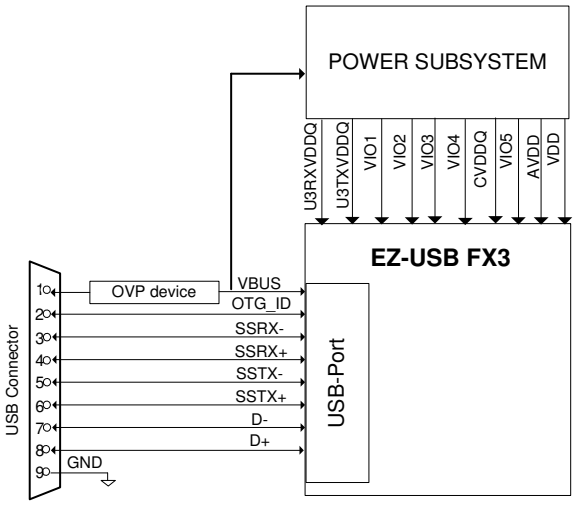
- Less than 10 Ω
- Less than 1 kΩ
- 65 kΩ to 72 kΩ
- 35 kΩ to 39 kΩ
- 99.96 kΩ to 104.4 kΩ (102 kΩ ± 2%)
- 119 kΩ to 132 kΩ
- Higher than 220 kΩ
- 431.2 kΩ to 448.8 kΩ (440 kΩ ± 2%)

FX3's charger detects a dedicated wall charger, Host/Hub charger, and Host/Hub.

VBUS Overvoltage Protection

The maximum input voltage on FX3's VBUS pin is 6 V. A charger can supply up to 9 V on VBUS. In this case, an external overvoltage protection (OVP) device is required to protect FX3 from damage on VBUS. Figure 3 shows the system application diagram with an OVP device connected on VBUS. Refer to Table 8 for the operating range of VBUS and VBATT.

Figure 3. System Diagram with OVP Device For VBUS



Carkit UART Mode

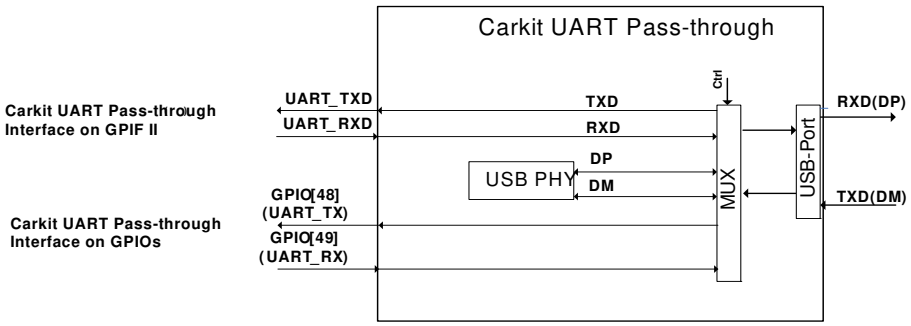
The USB interface supports the Carkit UART mode (UART over D+/D–) for non-USB serial data transfer. This mode is based on the CEA-936A specification.

In the Carkit UART mode, the output signaling voltage is 3.3 V. When configured for the Carkit UART mode, TXD of UART (output) is mapped to the D– line, and RXD of UART (input) is mapped to the D+ line.

In the Carkit UART mode, FX3 disables the USB transceiver and D+ and D– pins serve as pass-through pins to connect to the UART of the host processor. The Carkit UART signals may be routed to the GPIF II interface or to GPIO[48] and GPIO[49], as shown in Figure on page 8.

In this mode, FX3 supports a rate of up to 9600 bps.

Figure 4. Carkit UART Pass-through Block Diagram



GPIF II

The high-performance GPIF II interface enables functionality similar to, but more advanced than, FX2LP's GPIF and Slave FIFO interfaces.

The GPIF II is a programmable state machine that enables a flexible interface that may function either as a master or slave in industry-standard or proprietary interfaces. Both parallel and serial interfaces may be implemented with GPIF II.

Here is a list of GPIF II features:

- Functions as master or slave
- Provides 256 firmware programmable states
- Supports 8-bit, 16-bit, 24-bit, and 32-bit parallel data bus
- Enables interface frequencies up to 100 MHz
- Supports 14 configurable control pins when a 32- bit data bus is used. All control pins can be either input/output or bidirectional.
- Supports 16 configurable control pins when a 16/8 data bus is used. All control pins can be either input/output or bi-directional.

GPIF II state transitions are based on control input signals. The control output signals are driven as a result of the GPIF II state transitions. The INT# output signal can be controlled by GPIF II. Refer to the GPIFII Designer tool. The GPIF II state machine's behavior is defined by a GPIF II descriptor. The GPIF II descriptor is designed such that the required interface specifications are met. 8 KB of memory (separate from the 256/512 KB of embedded SRAM) is dedicated to the GPIF II waveform where the GPIF II descriptor is stored in a specific format.

Cypress's GPIFII Designer Tool enables fast development of GPIF II descriptors and includes examples for common interfaces.

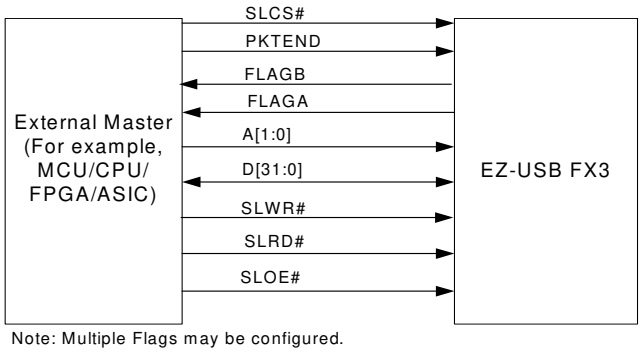
Example implementations of GPIF II are the asynchronous slave FIFO and synchronous slave FIFO interfaces.

Slave FIFO interface

The Slave FIFO interface signals are shown in Figure 5. This interface allows an external processor to directly access up to four buffers internal to FX3. Further details of the Slave FIFO interface are described on page 24.

Note Access to all 32 buffers is also supported over the slave FIFO interface. For details, contact Cypress Applications Support.

Figure 5. Slave FIFO Interface



Note: Multiple Flags may be configured.

CPU

FX3 has an on-chip 32-bit, 200-MHz ARM926EJ-S core CPU. The core has direct access to 16 KB of Instruction Tightly Coupled Memory (TCM) and 8 KB of Data TCM. The ARM926EJ-S core provides a JTAG interface for firmware debugging.

FX3 offers the following advantages:

- Integrates 256/512 KB of embedded SRAM for code and data and 8 KB of Instruction cache and Data cache.
- Implements efficient and flexible DMA connectivity between the various peripherals (such as, USB, GPIF II, I^2S, SPI, UART, I^2C), requiring firmware only to configure data accesses between peripherals, which are then managed by the DMA fabric.
- Allows easy application development using industry-standard development tools for ARM926EJ-S.

Examples of the FX3 firmware are available with the Cypress EZ-USB FX3 Development Kit.

JTAG Interface

FX3's JTAG interface has a standard five-pin interface to connect to a JTAG debugger in order to debug firmware through the CPU-core's on-chip-debug circuitry.

Industry-standard debugging tools for the ARM926EJ-S core can be used for the FX3 application development.

Other Interfaces

FX3 supports the following serial peripherals:

- SPI
- UART
- I^2C
- I^2S

The SPI, UART, and I^2S interfaces are multiplexed on the serial peripheral port.

The CYUSB3012 and CYUSB3014 Pin List on page 15 shows details of how these interfaces are multiplexed. Note that when GPIF II is configured for a 32-bit data bus width (CYUSB3012 and CYUSB3014), then the SPI interface is not available.

SPI Interface

FX3 supports an SPI Master interface on the Serial Peripherals port. The maximum operation frequency is 33 MHz.

The SPI controller supports four modes of SPI communication (see SPI Timing Specification on page 40 for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from four bits to 32 bits.

UART Interface

The UART interface of FX3 supports full-duplex communication. It includes the signals noted in Table 1.

Table 1. UART Interface Signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then FX3's UART only transmits data when the CTS input is asserted. In addition to this, FX3's UART asserts the RTS output signal, when it is ready to receive data.

I²C Interface

FX3's I²C interface is compatible with the I²C Bus Specification Revision 3. This I²C interface is capable of operating only as I²C master; therefore, it may be used to communicate with other I²C slave devices. For example, FX3 may boot from an EEPROM connected to the I²C interface, as a selectable boot option.

FX3's I²C Master Controller also supports multi-master mode functionality.

The power supply for the I²C interface is VIO5, which is a separate power domain from the other serial peripherals. This gives the I²C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I²C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I²C controller supports clock-stretching to enable slower devices to exercise flow control.

The I²C interface's SCL and SDA signals require external pull-up resistors. The pull-up resistors must be connected to VIO5.

I²S Interface

FX3 has an I²S port to support external audio codec devices. FX3 functions as I²S Master as transmitter only. The I²S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). FX3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I²S interface are 32 kHz, 44.1 kHz, and 48 kHz.

Boot Options

FX3 can load boot images from various sources, selected by the configuration of the PMODE pins. Following are the FX3 boot options:

- Boot from USB
- Boot from I²C
- Boot from SPI (SPI devices supported are M25P32 (32 Mbit), M25P16 (16 Mbit), M25P80 (8 Mbit), and M25P40 (4 Mbit)) or their equivalents
- Boot from GPIF II ASync ADMux mode
- Boot from GPIF II Sync ADMux mode
- Boot from GPIF II ASync SRAM mode

Table 2. FX3 Booting Options

PMODE[2:0][1]	Boot From
F00	Sync ADMux (16-bit)
F01	Async ADMux (16-bit)
F11	USB boot
F0F	Async SRAM (16-bit)
F1F	I²C, On Failure, USB Boot is Enabled
1FF	I²C only
0F1	SPI, On Failure, USB Boot is Enabled

Reset

Hard Reset

A hard reset is initiated by asserting the Reset# pin on FX3. The specific reset sequence and timing requirements are detailed in Figure 30 on page 42 and Table 19 on page 42. All I/Os are tristated during a hard reset. Note however, that the on-chip bootloader has control after a hard reset and it will configure I/O signals depending on the selected boot mode; see AN76405 - EZ-USB® FX3™ Boot Options for more details.

Soft Reset

In a soft reset, the processor sets the appropriate bits in the PP_INIT control register. There are two types of Soft Reset:

- CPU Reset – The CPU Program Counter is reset. Firmware does not need to be reloaded following a CPU Reset.
- Whole Device Reset – This reset is identical to Hard Reset.
- The firmware must be reloaded following a Whole Device Reset.

Note
1. F indicates Floating.

Clocking

FX3 allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN_32 pins can be left unconnected if they are not used.

Crystal frequency supported is 19.2 MHz, while the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

FX3 has an on-chip oscillator circuit that uses an external 19.2-MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal- or clock-frequency option. The configuration options are shown in Table 3.

Clock inputs to FX3 must meet the phase noise and jitter requirements specified in Table 4 on page 10.

The input clock frequency is independent of the clock and data rate of the FX3 core or any of the device interfaces. The internal PLL applies the appropriate clock multiply option depending on the input frequency.

Table 3. Crystal/Clock Frequency Selection

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/Clock Frequency
0	0	0	19.2-MHz crystal
1	0	0	19.2-MHz input CLK
1	0	1	26-MHz input CLK
1	1	0	38.4-MHz input CLK
1	1	1	52-MHz input CLK

Table 4. FX3 Input Clock Specifications

Parameter	Description	Specification		Units
		Min	Max	
Phase noise	100-Hz offset	–	–75	dB
	1-kHz offset	–	–104	
	10-kHz offset	–	–120	
	100-kHz offset	–	–128	
	1-MHz offset	–	–130	
Maximum frequency deviation	–	–	150	ppm
Duty cycle	–	30	70	%
Overshoot	–	–	3	
Undershoot	–	–	–3	
Rise time/fall time	–	–	3	ns

32-kHz Watchdog Timer Clock Input

FX3 includes a watchdog timer. The watchdog timer can be used to interrupt the ARM926EJ-S core, automatically wake up the FX3 in Standby mode, and reset the ARM926EJ-S core. The watchdog timer runs a 32-kHz clock, which may be optionally supplied from an external source on a dedicated FX3 pin.

The firmware can disable the watchdog timer. Requirements for the optional 32-kHz clock input are listed in Table 5.

Table 5. 32-kHz Clock Input Requirements

Parameter	Min	Max	Units
Duty cycle	40	60	%
Frequency deviation	–	±200	ppm
Rise time/fall time	–	200	ns

Power

FX3 has the following power supply domains:

- **IO_VDDQ**: This is a group of independent supply domains for digital I/Os. The voltage level on these supplies is 1.8 V to 3.3 V. FX3 provides six independent supply domains for digital I/Os listed as follows (see Table 7 on page 15 for details on each of the power domain signals):
  - VIO1: GPIF II I/O
  - VIO2: IO2
  - VIO3: IO3
  - VIO4: UART-/SPI/I^2S
  - VIO5: I^2C and JTAG (supports 1.2 V to 3.3 V)
  - **CVDDQ**: This is the supply voltage for clock and reset I/O. It should be either 1.8 V or 3.3 V based on the voltage level of the CLKIN signal.
  - **V_{DD}**: This is the supply voltage for the logic core. The nominal supply-voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
    - AVDD: This is the 1.2-V supply for the PLL, crystal oscillator, and other core analog circuits
    - **U3TXVDDQ/U3RXVDDQ**: These are the 1.2-V supply voltages for the USB 3.0 interface.
- **VBATT/VBUS**: This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through FX3's internal voltage regulator. VBATT is internally regulated to 3.3 V.

Power Modes

FX3 supports the following power modes:

- Normal mode: This is the full-functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode.
  - Normal operating power consumption does not exceed the sum of I_{CC} Core max and I_{CC} USB max (see Table 7 on page 15 for current consumption specifications).
  - The I/O power supplies VIO2, VIO3, VIO4, and VIO5 can be turned off when the corresponding interface is not in use. VIO1 cannot be turned off at any time if the GPIF II interface is used in the application.
- Low-power modes (see Table 6 on page 11):
  - Suspend mode with USB 3.0 PHY enabled (L1)
  - Suspend mode with USB 3.0 PHY disabled (L2)
  - Standby mode (L3)
  - Core power-down mode (L4)

Table 6. Entry and Exit Methods for Low-Power Modes

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend Mode with USB 3.0 PHY Enabled (L1)	■ The power consumption in this mode does not exceed ISB_1 ■ USB 3.0 PHY is enabled and is in U3 mode (one of the suspend modes defined by the USB 3.0 specification). This one block alone is operational with its internal clock while all other clocks are shut down ■ All I/Os maintain their previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory, and all internal RAM are maintained ■ All transactions must be completed before FX3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on ARM926EJ-S core can put FX3 into suspend mode. For example, on USB suspend condition, firmware may decide to put FX3 into suspend mode ■ External Processor, through the use of mailbox registers, can put FX3 into suspend mode	■ D+ transitioning to low or high ■ D- transitioning to low or high ■ Impedance change on OTG_ID pin ■ Resume condition on SSRX± ■ Detection of VBUS ■ Level detect on UART_CTS (programmable polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend Mode with USB 3.0 PHY Disabled (L2)	■ The power consumption in this mode does not exceed ISB_2 ■ USB 3.0 PHY is disabled and the USB interface is in suspend mode ■ The clocks are shut off. The PLLs are disabled ■ All I/Os maintain their previous state ■ USB interface maintains the previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory and all internal RAM are maintained ■ All transactions must be completed before FX3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on ARM926EJ-S core can put FX3 into suspend mode. For example, on USB suspend condition, firmware may decide to put FX3 into suspend mode ■ External Processor, through the use of mailbox registers can put FX3 into suspend mode	■ D+ transitioning to low or high ■ D- transitioning to low or high ■ Impedance change on OTG_ID pin ■ Resume condition on SSRX± ■ Detection of VBUS ■ Level detect on UART_CTS (programmable polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#
Standby Mode (L3)	■ The power consumption in this mode does not exceed ISB3 ■ All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor should take care that the data needed is read before putting FX3 into this Standby Mode ■ The program counter is reset after waking up from Standby ■ GPIO pins maintain their configuration ■ Crystal oscillator is turned off ■ Internal PLL is turned off ■ USB transceiver is turned off ■ ARM926EJ-S core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually	■ Firmware executing on ARM926EJ-S core or external processor configures the appropriate register	■ Detection of VBUS ■ Level detect on UART_CTS (Programmable Polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Core Power Down Mode (L4)	■ The power consumption in this mode does not exceed ISB_4 ■ Core power is turned off ■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware ■ In this mode, all other power domains can be turned on/off individually	■ Turn off V_{DD}	■ Reapply VDD ■ Assertion of RESET#

Digital I/Os

FX3 has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMS, and TRST# signals have fixed 50-kΩ internal pull-ups, and the TCK signal has a fixed 10-kΩ pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

GPIOs

EZ-USB enables a flexible pin configuration both on the GPIF II and the serial peripheral interfaces. Any unused control pins (except CTL[15]) on the GPIF II interface can be used as GPIOs. Similarly, any unused pins on the serial peripheral interfaces may be configured as GPIOs. See Pin Configurations for pin configuration options.

All GPIF II and GPIO pins support an external load of up to 16 pF for every pin.

EMI

FX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. FX3 can tolerate EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

System-level ESD

FX3 has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-kV human body model (HBM) based on JESD22-A114 Specification
- ±6-kV contact discharge and ±8-kV air gap discharge based on IEC61000-4-2 level 3A
- ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-kV HBM internal ESD protection.

Pin Configurations

Figure 6. FX3 121-ball BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Figure 7. FX3 131-Ball WLCSP Ball Map (Bottom View)

	12	11	10	9	8	7	6	5	4	3	2	1
A	VSS	VSS	SSRXM		SSTXM	FSLC[0]	AVSS	AVDD	DP	VSS	DM	VDD
B	GPIO[55]	VIO4	SSRXP	R_USB3	SSTXP	FSLC[2]	XTALIN	XTALOUT	NC	R_USB2	NC	VDD
C	GPIO[56]	VIO3	U3RXVDDQ	U3VSSQ	U3TXVDDQ	CVDDQ	CLKIN_32	CLKIN	VSS	OTG_ID	TDO	TRST#
D	GPIO[49]	GPIO[50]	GPIO[53]	GPIO[54]	RESET#	VDD	I2C_GPIO[58]	TMS	VIO5	TCK	I2C_GPIO[59]	VSS
E	GPIO[57]	GPIO[48]	GPIO[51]	GPIO[52]	O[60]	VSS	VSS	VSS	VSS	GPIO[3]	VBATT	VBUS
F	VSS	GPIO[46]	GPIO[47]	FSLC[1]	TDI	VDD	VDD	VDD	VDD	GPIO[4]	GPIO[1]	GPIO[0]
G	VIO2	GPIO[43]	GPIO[44]	GPIO[45]	VSS	VSS	VDD	VSS	GPIO[9]	GPIO[7]	GPIO[6]	GPIO[2]
H	VSS	GPIO[40]	GPIO[41]	GPIO[42]	GPIO[39]	VSS	GPIO[20]	GPIO[18]	GPIO[14]	GPIO[12]	GPIO[8]	VIO1
J	VIO2	GPIO[38]	GPIO[37]	GPIO[36]	GPIO[31]	GPIO[27]	GPIO[25]	GPIO[22]	GPIO[19]	GPIO[15]	GPIO[10]	GPIO[5]
K	GPIO[35]	GPIO[34]	GPIO[33]	GPIO[32]	GPIO[28]	GPIO[26]	GPIO[16]	GPIO[21]	INT#	GPIO[24]	GPIO[11]	VSS
L	VDD	VSS	VDD	GPIO[30]	GPIO[29]	VIO1	GPIO[23]	VSS	VIO1	GPIO[17]	GPIO[13]	VSS

Note No ball is populated at location A9.

Figure 8. FX3 Hi-Speed 121-Ball BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	VDD	NC	NC	NC	NC	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	NC	FSLC[1]	VDD	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Pin Description

Table 7. CYUSB3012 and CYUSB3014 Pin List

BGA	WLCSP	Power Domain	I/O	Name	Description					
					GPIF II Interface			Slave FIFO Interface		
F10	F1	VIO1	I/O	GPIO[0]	DQ[0]			DQ[0]		
F9	F2	VIO1	I/O	GPIO[1]	DQ[1]			DQ[1]		
F7	G1	VIO1	I/O	GPIO[2]	DQ[2]			DQ[2]		
G10	E3	VIO1	I/O	GPIO[3]	DQ[3]			DQ[3]		
G9	F3	VIO1	I/O	GPIO[4]	DQ[4]			DQ[4]		
F8	J1	VIO1	I/O	GPIO[5]	DQ[5]			DQ[5]		
H10	G2	VIO1	I/O	GPIO[6]	DQ[6]			DQ[6]		
H9	G3	VIO1	I/O	GPIO[7]	DQ[7]			DQ[7]		
J10	H2	VIO1	I/O	GPIO[8]	DQ[8]			DQ[8]		
J9	G4	VIO1	I/O	GPIO[9]	DQ[9]			DQ[9]		
K11	J2	VIO1	I/O	GPIO[10]	DQ[10]			DQ[10]		
L10	K2	VIO1	I/O	GPIO[11]	DQ[11]			DQ[11]		
K10	H3	VIO1	I/O	GPIO[12]	DQ[12]			DQ[12]		
K9	L2	VIO1	I/O	GPIO[13]	DQ[13]			DQ[13]		
J8	H4	VIO1	I/O	GPIO[14]	DQ[14]			DQ[14]		
G8	J3	VIO1	I/O	GPIO[15]	DQ[15]			DQ[15]		
J6	K6	VIO1	I/O	GPIO[16]	PCLK			CLK		
K8	L3	VIO1	I/O	GPIO[17]	CTL[0]			SLCS#		
K7	H5	VIO1	I/O	GPIO[18]	CTL[1]			SLWR#		
J7	J4	VIO1	I/O	GPIO[19]	CTL[2]			SLOE#		
H7	H6	VIO1	I/O	GPIO[20]	CTL[3]			SLRD#		
G7	K5	VIO1	I/O	GPIO[21]	CTL[4]			FLAGA		
G6	J5	VIO1	I/O	GPIO[22]	CTL[5]			FLAGB		
K6	L6	VIO1	I/O	GPIO[23]	CTL[6]			GPIO		
H8	K3	VIO1	I/O	GPIO[24]	CTL[7]			PKTEND#		
G5	J6	VIO1	I/O	GPIO[25]	CTL[8]			GPIO		
H6	K7	VIO1	I/O	GPIO[26]	CTL[9]			GPIO		
K5	J7	VIO1	I/O	GPIO[27]	CTL[10]			GPIO		
J5	K8	VIO1	I/O	GPIO[28]	CTL[11]			A1		
H5	L8	VIO1	I/O	GPIO[29]	CTL[12]			A0		
G4	L9	VIO1	I/O	GPIO[30]	PMODE[0]			PMODE[0]		
H4	J8	VIO1	I/O	GPIO[31]	PMODE[1]			PMODE[1]		
L4	K9	VIO1	I/O	GPIO[32]	PMODE[2]			PMODE[2]		
L8	K4	VIO1	I/O	INT#	INT#/CTL[15]			CTL[15]		
					32-bit Data Bus	16 - bit Data Bus + UART+SPI+I2S	16 - bit Data Bus + UART+GPIO	16 - bit Data Bus + SPI+GPIO	16 - bit Data Bus + I2S+GPIO	GPIO only
K2	K10	VIO2	I/O	GPIO[33]	DQ[16]	GPIO	GPIO	GPIO	GPIO	GPIO
J4	K11	VIO2	I/O	GPIO[34]	DQ[17]	GPIO	GPIO	GPIO	GPIO	GPIO
K1	K12	VIO2	I/O	GPIO[35]	DQ[18]	GPIO	GPIO	GPIO	GPIO	GPIO
J2	J9	VIO2	I/O	GPIO[36]	DQ[19]	GPIO	GPIO	GPIO	GPIO	GPIO
J3	J10	VIO2	I/O	GPIO[37]	DQ[20]	GPIO	GPIO	GPIO	GPIO	GPIO

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description					
J1	J11	VIO2	I/O	GPIO[38]	DQ[21]	GPIO	GPIO	GPIO	GPIO	GPIO
H2	H8	VIO2	I/O	GPIO[39]	DQ[22]	GPIO	GPIO	GPIO	GPIO	GPIO
H3	H11	VIO2	I/O	GPIO[40]	DQ[23]	GPIO	GPIO	GPIO	GPIO	GPIO
F4	H10	VIO2	I/O	GPIO[41]	DQ[24]	GPIO	GPIO	GPIO	GPIO	GPIO
G2	H9	VIO2	I/O	GPIO[42]	DQ[25]	GPIO	GPIO	GPIO	GPIO	GPIO
G3	G11	VIO2	I/O	GPIO[43]	DQ[26]	GPIO	GPIO	GPIO	GPIO	GPIO
F3	G10	VIO2	I/O	GPIO[44]	DQ[27]	GPIO	GPIO	GPIO	GPIO	GPIO
F2	G09	VIO2	I/O	GPIO[45]	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
F5	F11	VIO3	I/O	GPIO[46]	DQ[28]	UART_RT S	GPIO	GPIO	GPIO	GPIO
E1	F10	VIO3	I/O	GPIO[47]	DQ[29]	UART_CT S	GPIO	GPIO	GPIO	GPIO
E5	E11	VIO3	I/O	GPIO[48]	DQ[30]	UART_TX	GPIO	GPIO	GPIO	GPIO
E4	D12	VIO3	I/O	GPIO[49]	DQ[31]	UART_R X	GPIO	GPIO	GPIO	GPIO
D1	D11	VIO3	I/O	GPIO[50]	I2S_CLK	I2S_CLK	GPIO	GPIO	GPIO	GPIO
D2	E10	VIO3	I/O	GPIO[51]	I2S_SD	I2S_SD	GPIO	GPIO	GPIO	GPIO
D3	E9	VIO3	I/O	GPIO[52]	I2S_WS	I2S_WS	GPIO	GPIO	GPIO	GPIO
D4	D10	VIO4	I/O	GPIO[53]	UART_RTS	SPI_SCK	UART_RTS	SPI_SCK	GPIO	GPIO
C1	D9	VIO4	I/O	GPIO[54]	UART_CTS	SPI_SSN	UART_CTS	SPI_SSN	I2S_CLK	GPIO
C2	B12	VIO4	I/O	GPIO[55]	UART_TX	SPI_MIS O	UART_TX	SPI_MISO	I2S_SD	GPIO
D5	C12	VIO4	I/O	GPIO[56]	UART_RX	SPI_MOS I	UART_RX	SPI_MOSI	I2S_WS	GPIO
C4	E12	VIO4	I/O	GPIO[57]	I2S_MCLK	I2S_MCL K	GPIO	GPIO	I2S_MCL K	GPIO
					USB Port					
					CYUSB301X			**CYUSB201X**		
A3	A10	U3RXVD DQ	I	SSRXM	SSRX-			NC		
A4	B10	U3RXVD DQ	I	SSRXP	SSRX+			NC		
A6	A8	U3TXVD DQ	O	SSTXM	SSTX-			NC		
A5	B8	U3TXVD DQ	O	SSTXP	SSTX+			NC		
B3	B9	U3TXVD DQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 ±1% resistor between this pin and GND)			NC		
C9	C3	VBUS/ VBATT	I	OTG_ID	OTG_ID					
A9	A4	VBUS/V BATT	I/O	DP	D+					
A10	A2	VBUS/V BATT	I/O	DM	D–					
C8	B3	VBUS/VBAT T	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 k ±1% resistor between this pin and GND)					
					Clock and Reset					
B2	A7	CVDDQ	I	FSLC[0]	FSLC[0]					
C6	B6	AVDD	I/O	XTALIN	XTALIN					
C7	B5	AVDD	I/O	XTALOUT	XTALOUT					
B4	F9	CVDDQ	I	FSLC[1]	FSLC[1]					
E6	B7	CVDDQ	I	FSLC[2]	FSLC[2]					
D7	C5	CVDDQ	I	CLKIN	CLKIN					

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description
D6	C6	CVDDQ	I	CLKIN_32	CLKIN_32
C5	D8	CVDDQ	I	RESET#	RESET#
					I2C and JTAG
D9	D6	VIO5	I/O	I2C_GPIO[58]	I^2C_SCL
D10	D2	VIO5	I/O	I2C_GPIO[59]	I^2C_SDA
E7	F8	VIO5	I	TDI	TDI
C10	C2	VIO5	O	TDO	TDO
B11	C1	VIO5	I	TRST#	TRST#
E8	D5	VIO5	I	TMS	TMS
F6	D3	VIO5	I	TCK	TCK
D11	E8	VIO5	O	O[60]	Charger detect output
					Power
E10	E2	–	PWR	VBATT	–
B10	B1	–	PWR	VDD	–
–	A1	–	PWR	VDD	–
A1	C9	–	PWR	U3VSSQ	–
E11	E1	–	PWR	VBUS	–
D8	C4	–	PWR	VSS	–
H11	H1	–	PWR	VIO1	–
E2	K1	–	PWR	VSS	–
L9	L4	–	PWR	VIO1	–
G1	L5	–	PWR	VSS	–
–	L7	–	PWR	VIO1	–
–	L1	–	PWR	VSS	–
F1	J12	–	PWR	VIO2	–
G11	H12	–	PWR	VSS	–
	G12	–	PWR	VIO2	–
E3	C11	–	PWR	VIO3	–
L1	F12	–	PWR	VSS	–
B1	B11	–	PWR	VIO4	–
L6	A11	–	PWR	VSS	–
–	A12	–	PWR	VSS	–
B6	C7	–	PWR	CVDDQ	–
B5	C8	–	PWR	U3TXVDDQ	–
A2	C10	–	PWR	U3RXVDDQ	–
C11	D4	–	PWR	VIO5	–
L11	A3	–	PWR	VSS	–
A7	A5	–	PWR	AVDD	–
B7	A6	–	PWR	AVSS	–
C3	F4	–	PWR	VDD	–
B8	D1	–	PWR	VSS	–
E9	F5	–	PWR	VDD	–

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description
B9	E4	–	PWR	VSS	–
F11	F6	–	PWR	VDD	–
–	E5	–	PWR	VSS	**GND**
–	F7	–	PWR	VDD	–
–	E6	–	PWR	VSS	GND
–	E7	–	PWR	VSS	GND
H1	G6	–	PWR	VDD	–
L7	D7	–	PWR	VDD	–
J11	L10	–	PWR	VDD	–
L5	L12	–	PWR	VDD	–
K4	H7	–	PWR	VSS	–
L3	G7	–	PWR	VSS	–
K3	L11	–	PWR	VSS	–
L2	G8	–	PWR	VSS	–
A8	G5	–	PWR	VSS	–
–	B4	–	–	NC	No Connect
A11	B2	–	–	NC	No Connect

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Ambient temperature with power supplied (Commercial) ..... 0 °C to +70 °C

Supply voltage to ground potential V_{DD}, A_{VDDQ} ..... 1.25 V

V_{IO1},V_{IO2}, V_{IO3}, V_{IO4}, V_{IO5} ..... 3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ ..... 1.25 V

DC input voltage to any input pin ..... V_{CC} + 0.3 V

DC voltage applied to outputs in high Z state ..... V_{CC} + 0.3 V

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ± 2.2-kV HBM based on JESD22-A114
- Additional ESD protection levels on D+, D–, and GND pins, and serial peripheral pins
- ± 6-kV contact discharge, ± 8-kV air gap discharge based on IEC61000-4-2 level 3A, ± 8-kV contact discharge, and ± 15-kV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current ..... > 200 mA

Maximum output short-circuit current for all I/Os (cumulative) ..... –100 mA

Maximum output current per I/O (source or sink) ..... 20 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial ..... –40 °C to +85 °C

Commercial ..... 0 °C to +70 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$

Supply voltage ..... 1.15 V to 1.25 V

V_{BATT} supply voltage ..... 3.2 V to 6 V

V_{IO1}, V_{IO2}, V_{IO3}, V_{IO4}, C_{VDDQ}

Supply voltage ..... 1.7 V to 3.6 V

V_{IO5} supply voltage ..... 1.15 V to 3.6 V

DC Specifications

Table 8. DC Specifications

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{IO1}	GPIF II I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO2}	IO2 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO3}	IO3 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO4}	UART/SPI/I2S power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C and JTAG voltage supply	1.15	3.6	V	1.2-, 1.8-, 2.5-, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × VCC	VCC + 0.3	V	For 2.0 V ≤ V_{CC} ≤ 3.6 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	VCC – 0.4	VCC + 0.3	V	For 1.7 V ≤ V_{CC} ≤ 2.0 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	0.25 × VCC	V	VCC is the corresponding I/O voltage supply.

Table 8. DC Specifications (continued)

Parameter	Description	Min	Max	Units	Notes
V_{OH}	Output HIGH voltage	0.9 × VCC	–	V	I_{OH} (max) = –100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.
V_{OL}	Output LOW voltage	–	0.1 × VCC	V	I_{OL} (min) = +100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os with a pull-up or pull-down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD}
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/ SSXM/ SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ}
I_{CC} Core	Core and analog voltage operating current	–	200	mA	Total current through A_{VDD}, V_{DD}
I_{CC} USB	USB voltage supply operating current	–	60	mA	–
I_{SB1}	Total suspend current during suspend mode with USB 3.0 PHY enabled (L1)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C)
I_{SB2}	Total suspend current during suspend mode with USB 3.0 PHY disabled (L2)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C)
I_{SB3}	Total standby current during standby mode (L3)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C)
I_{SB4}	Total standby current during core power-down mode (L4)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C)
V_{RAMP}	Voltage ramp rate on core and I/O supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise level permitted on V_{DD} and I/O supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise level permitted on A_{VDD} supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

AC Timing Parameters

GPIF II Timing

Figure 9. GPIF II Timing in Synchronous Mode

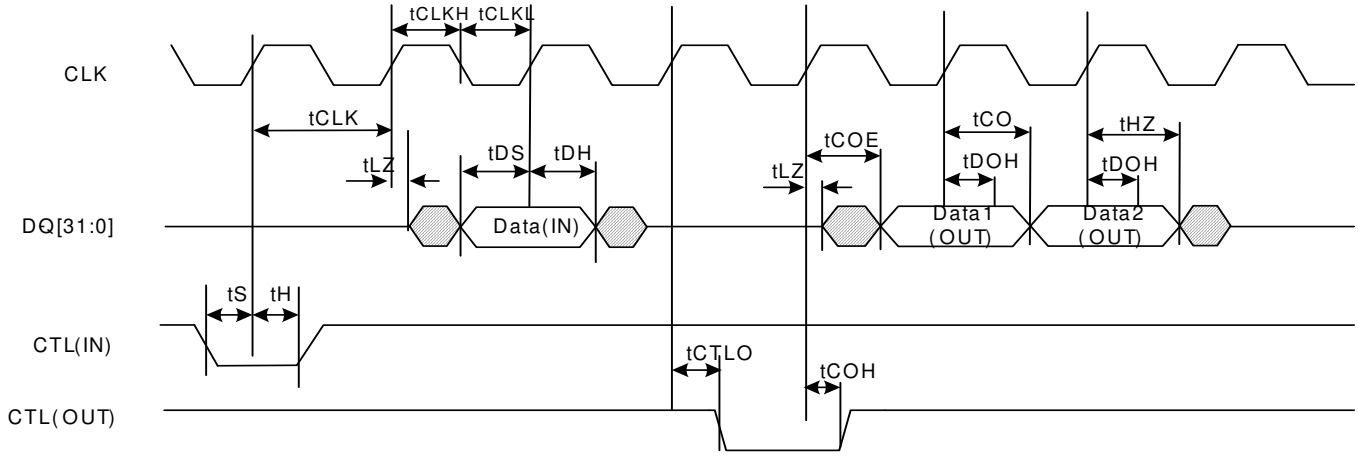


Table 9. GPIF II Timing Parameters in Synchronous Mode [2]

Parameter	Description	Min	Max	Units
Frequency	Interface clock frequency	–	100	MHz
tCLK	Interface clock period	10	–	ns
tCLKH	Clock high time	4	–	ns
tCLKL	Clock low time	4	–	ns
tS	CTL input to clock setup time	2	–	ns
tH	CTL input to clock hold time	0.5	–	ns
tDS	Data in to clock setup time	2	–	ns
tDH	Data in to clock hold time	0.5	–	ns
tCO	Clock to data out propagation delay when DQ bus is already in output direction	–	7	ns
tCOE	Clock to data out propagation delay when DQ lines change to output from tristate and valid data is available on the DQ bus	–	9	ns
tCTLO	Clock to CTL out propagation delay	–	8	ns
tDOH	Clock to data out hold	2	–	ns
tCOH	Clock to CTL out hold	0	–	ns
tHZ	Clock to high-Z	–	8	ns
tLZ	Clock to low-Z	0	–	ns

Note
2. All parameters guaranteed by design and validated through characterization.

Figure 10. GPIF II Timing in Asynchronous Mode

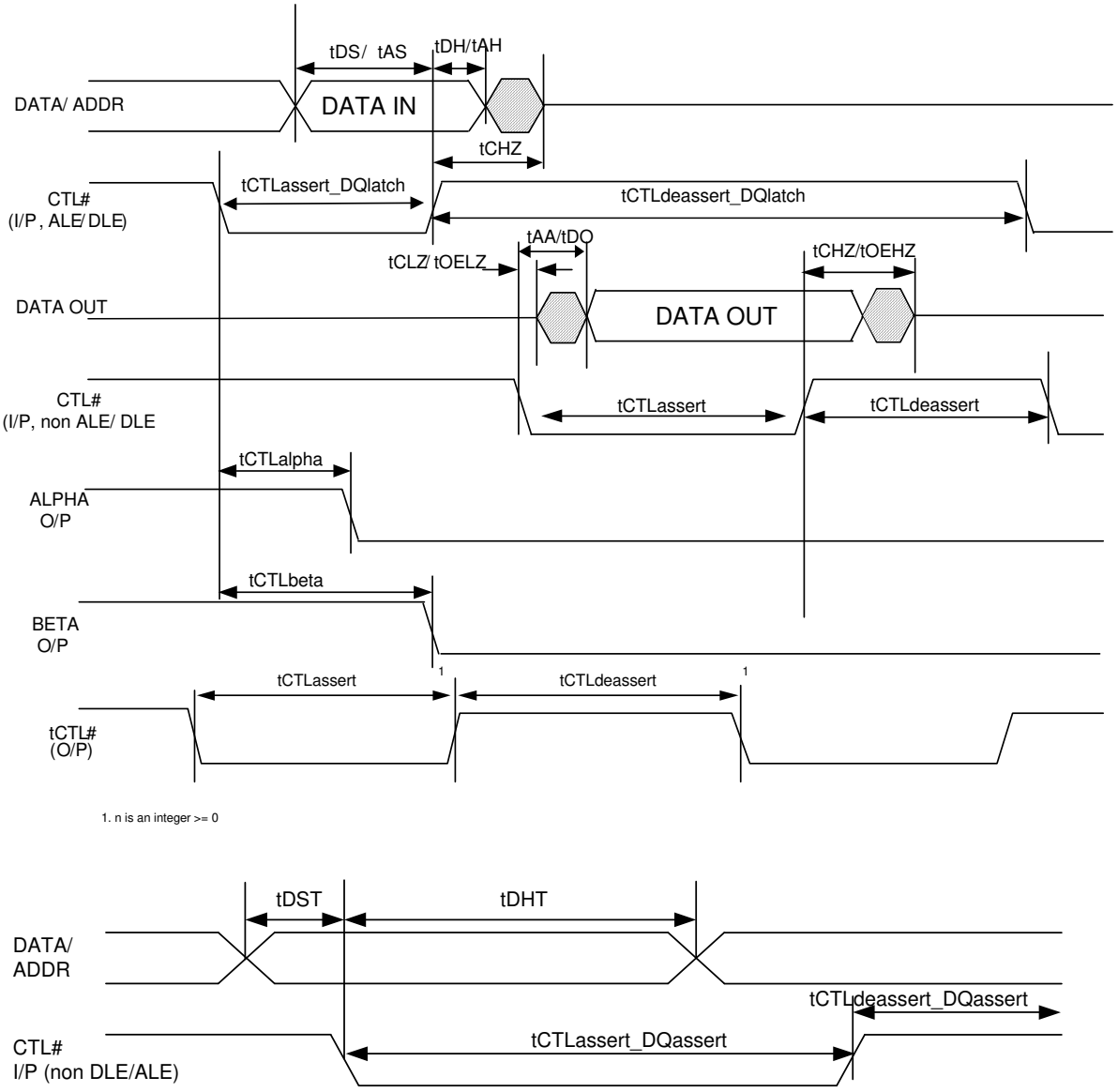


Figure 11. GPIF II Timing in Asynchronous DDR Mode

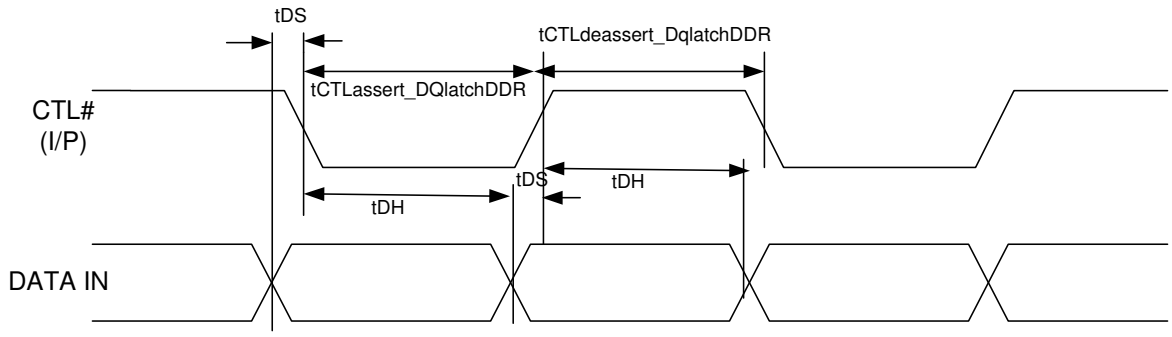


Table 10. GPIF II Timing in Asynchronous Mode[3, 4]

Note The following parameters assume one state transition

Parameter	Description	Min	Max	Units
tDS	Data In to DLE setup time. Valid in DDR async mode.	2.3	–	ns
tDH	Data In to DLE hold time. Valid in DDR async mode.	2	–	ns
tAS	Address In to ALE setup time	2.3	–	ns
tAH	Address In to ALE hold time	2	–	ns
tCTLassert	CTL I/O asserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLdeassert	CTL I/O deasserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLassert_DQassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLdeassert_DQassert	CTL deasserted pulse width for CTL inputs that signify DQ input valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLassert_DQdeassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLdeassert_DQdeassert	CTL deasserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLassert_DQlatch	CTL asserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches are always close at the deasserting edge.	7	–	ns
tCTLdeassert_DQlatch	CTL deasserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches always close at the deasserting edge.	10	–	ns
tCTLassert_DQlatchDDR	CTL asserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tCTLdeassert_DQlatchDDR	CTL deasserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tAA	DQ/CTL input to DQ output time when DQ change or CTL change needs to be detected and affects internal updates of input and output DQ lines.	–	30	ns
tDO	CTL to data out when the CTL change merely enables the output flop update whose data was already established.	–	25	ns
tOELZ	CTL designated as OE to low-Z. Time when external devices should stop driving data.	0	–	ns
tOEHZ	CTL designated as OE to high-Z	8	8	ns
tCLZ	CTL (non-OE) to low-Z. Time when external devices should stop driving data.	0	–	ns
tCHZ	CTL (non-OE) to high-Z	30	30	ns
tCTLalpha	CTL to alpha change at output	–	25	ns
tCTLbeta	CTL to beta change at output	–	30	ns
tDST	Addr/data setup when DLE/ALE not used	2	–	ns
tDHT	Addr/data hold when DLE/ALE not used	20	–	ns

Notes
3. All parameters guaranteed by design and validated through characterization.
4. "alpha" output corresponds to "early output" and "beta" corresponds to "delayed output". Please refer to the GPIFII Designer Tool for the use of these outputs.

Slave FIFO Interface

Synchronous Slave FIFO Read Sequence Description

- FIFO address is stable and SLCS is asserted
- FLAG indicates FIFO not empty status
- SLOE is asserted. SLOE is an output-enable only, whose sole function is to drive the data bus.
- SLRD is asserted

The FIFO pointer is updated on the rising edge of the PCLK, while the SLRD is asserted. This starts the propagation of data from the newly addressed location to the data bus. After a propagation delay of tco (measured from the rising edge of PCLK), the new data value is present. N is the first data value read from the FIFO. To have data on the FIFO data bus, SLOE must also be asserted.

The same sequence of events is applicable for a burst read.

FLAG Usage:

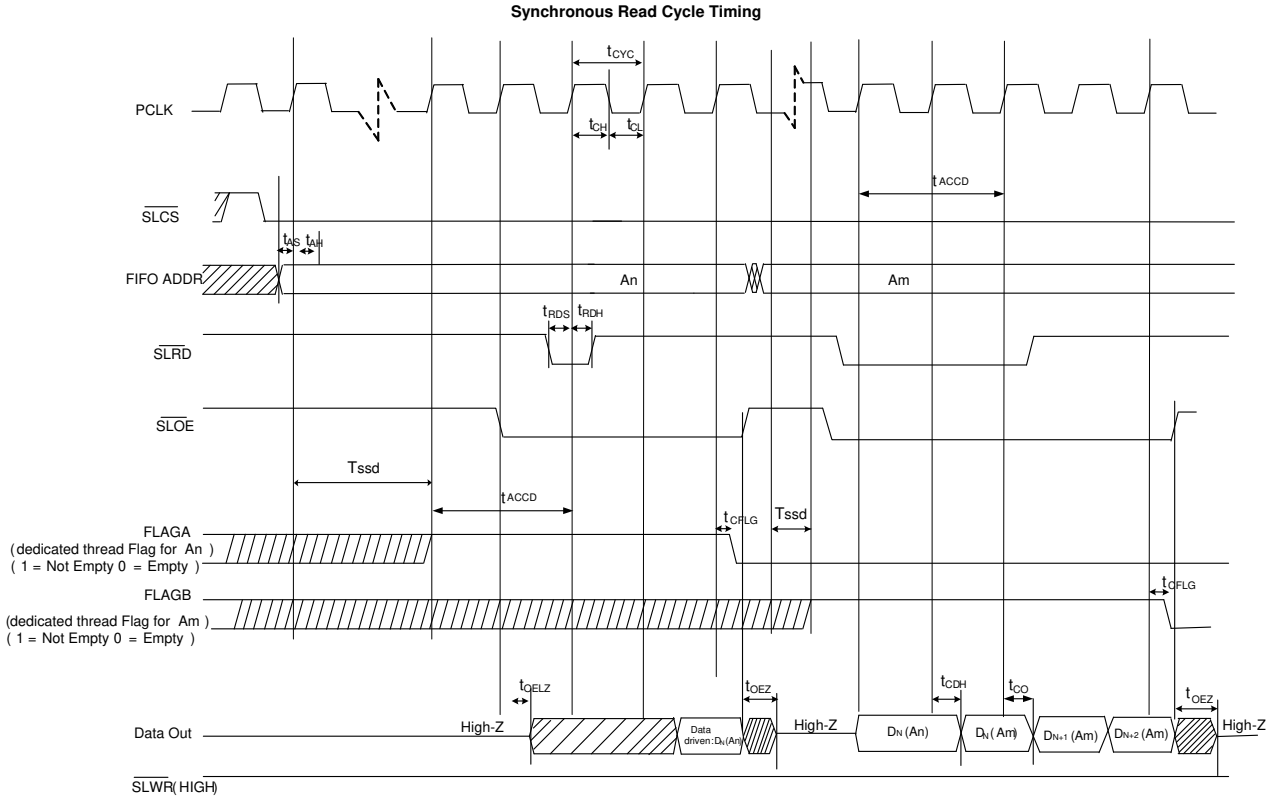
The FLAG signals are monitored for flow control by the external processor. FLAG signals are outputs from FX3 that may be configured to show empty, full, or partial status for a dedicated thread or the current thread that is addressed.

Socket Switching Delay (Tssd):

The socket-switching delay is measured from the time EPSWITCH# is asserted by the master, with the new socket address on the address bus, to the time the Current_Thread_DMA_Ready flag is asserted. For the Producer socket, the flag is asserted when it is ready to receive data in the DMA buffer. For the Consumer socket, the flag is asserted when it is ready to drive data out of the DMA buffer. For a synchronous slave FIFO interface, the switching delay is measured in the number of GPIF interface clock cycles; for an asynchronous slave FIFO interface, in PIB clock cycles. This is applicable only for the 5-bit Slave FIFO interface; there is no socket-switching delay in FX3's 2-bit Slave FIFO interface, which makes use of thread switching in the GPIF™ II state machine.

Note For burst mode, the SLRD# and SLOE# are asserted during the entire duration of the read. When SLOE# is asserted, the data bus is driven (with data from the previously addressed FIFO). For each subsequent rising edge of PCLK, while the SLRD# is asserted, the FIFO pointer is incremented and the next data value is placed on the data bus.

Figure 12. Synchronous Slave FIFO Read Mode



Synchronous Slave FIFO Write Sequence Description

- FIFO address is stable and the signal SLCS# is asserted
- External master or peripheral outputs the data to the data bus
- SLWR# is asserted
- While the SLWR# is asserted, data is written to the FIFO and on the rising edge of the PCLK, the FIFO pointer is incremented
- The FIFO flag is updated after a delay of t_{WFLG} from the rising edge of the clock

The same sequence of events is also applicable for burst write

Note For the burst mode, SLWR# and SLCS# are asserted for the entire duration, during which all the required data values are written. In this burst write mode, after the SLWR# is asserted, the data on the FIFO data bus is written to the FIFO on every rising edge of PCLK. The FIFO pointer is updated on each rising edge of PCLK.

Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a Zero-Length Packet (ZLP) to FX3 simply by asserting PKTEND#, without asserting SLWR#. SLCS# and address must be driven as shown in Figure 13.

Figure 13. Synchronous Slave FIFO Write Mode