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CYP15G0401DXB
CYV15G0401DXB

Quad HOTLink II™ Transceiver

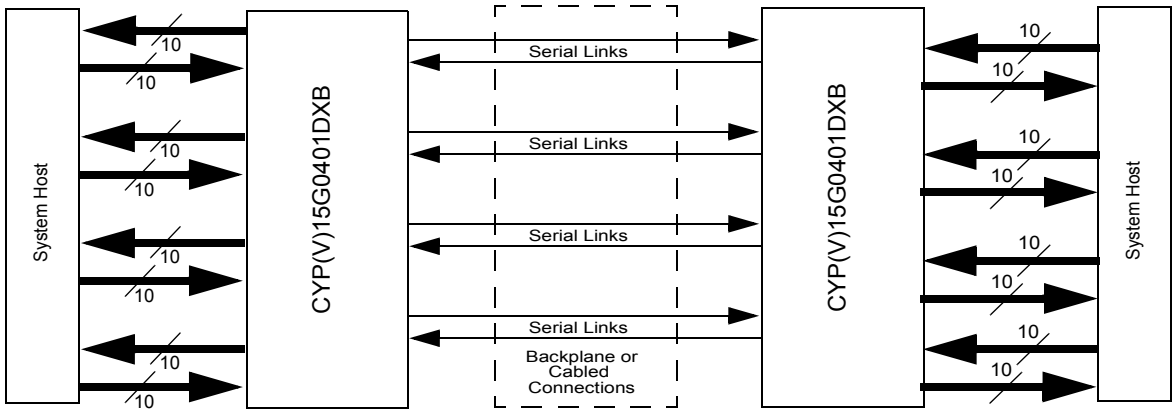
Features

- Second-generation HOTLink® technology
  - Compliant to multiple standards
    - ESCON, DVB-ASI, fibre channel and gigabit ethernet (IEEE802.3z)
    - CPRI™ compliant
    - CYV15G0401DXB compliant to SMPTE 259M and SMPTE 292M
    - 8 B/10 B encoded or 10-bit unencoded data
- Quad channel transceiver operates from 195 to 1500 MBaud serial data rate
  - Aggregate throughput of 12 GB per second
- Selectable parity check/generate
- Selectable multi-channel bonding options
  - Four 8-bit channels
  - Two 16-bit channels
  - One 32-bit channel
  - N × 32-bit channel support (inter-chip)
- Skew alignment support for multiple bytes of offset
- Selectable input/output clocking options
- MultiFrame™ receive framer
  - Bit and byte alignment
  - Comma or full K28.5 detect
  - Single- or multi-byte framer for byte alignment
  - Low-latency option
- Synchronous LVTTL parallel interface
- Optional elasticity buffer in receive path
- Optional phase align buffer in transmit path
- Internal phase-locked loops (PLLs) with no external PLL components
- Dual differential PECL-compatible serial inputs per channel
  - Internal DC-restoration
- Dual differential PECL-compatible serial outputs per channel
  - Source matched for 50 Ω transmission lines
  - No external bias resistors required
  - Signaling-rate controlled edge-rates
- Compatible with
  - Fiber-optic modules
  - Copper cables
  - Circuit board traces
- JTAG boundary scan
- Built-in self-test (BIST) for at-speed link testing
- Per-channel link quality indicator
  - Analog signal detect
  - Digital signal detect
- Low power 2.5 W at 3.3 V typical
- Single 3.3 V supply
- 256-ball thermally enhanced BGA
- Pb-free package option available
- 0.25 µ BiCMOS technology

Functional Description

The CYP(V)15G0401DXB[1] Quad HOTLink II™ Transceiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 195-to-1500 MBaud per serial link.

Figure 1. HOTLink II System Connections



Note
1. CYV15G0401DXB refers to SMPTE 259M and SMPTE 292M compliant devices. CYP15G0401DXB refers to devices not compliant to SMPTE 259M and SMPTE 292M pathological test requirements.

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The CYV15G0401DXB satisfies the SMPTE 259M and SMPTE 292M compliance as per the EG34-1999 Pathological Test Requirements.

The multiple channels in each device may be combined to allow transport of wide buses across significant distances with minimal concern for offsets in clock phase or link delay. Each transmit channel accepts parallel characters in an Input Register, encodes each character for transport, and converts it to serial data. Each receive channel accepts serial data and converts it to parallel data, decodes the data into characters, and presents these characters to an Output Register. Figure 1 illustrates typical connections between independent host systems and corresponding CYP15G0401DXB parts.

As a second-generation HOTLink device, the CYP(V)15G0401DXB extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data, command, and BIST) with other HOTLink devices. The transmit (TX) section of the CYP(V)15G0401DXB Quad HOTLink II consists of four byte-wide channels that can be operated independently or bonded to form wider buses. Each channel can accept either eight-bit data characters or pre-encoded 10-bit transmission characters. Data characters are passed from the Transmit Input Register to an embedded 8B/10B Encoder to improve their serial transmission characteristics. These encoded characters are then serialized and output from dual Positive ECL (PECL)-compatible differential transmission-line drivers at a bit-rate of either 10- or 20-times the input reference clock.

The receive (RX) section of the CYP(V)15G0401DXB Quad HOTLink II consists of four byte-wide channels that can be operated independently or synchronously bonded for greater bandwidth. Each channel accepts a serial bit-stream from one of two PECL-compatible differential line receivers and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. Each recovered serial stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are then written to an internal Elasticity Buffer, and presented to the destination host system. The integrated 8B/10B Encoder/Decoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface.

For those systems using buses wider than a single byte, the four independent receive paths can be bonded together to allow synchronous delivery of data across a two-byte-wide (16-bit) path, or across all four bytes (32-bit). Multiple CYP(V)15G0401DXB devices may be bonded together to provide synchronous transport of buses wider than 32 bits.

The parallel I/O interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. In addition to clocking the transmit path, the receive interface may be configured to present data relative to a recovered clock or to a local reference clock.

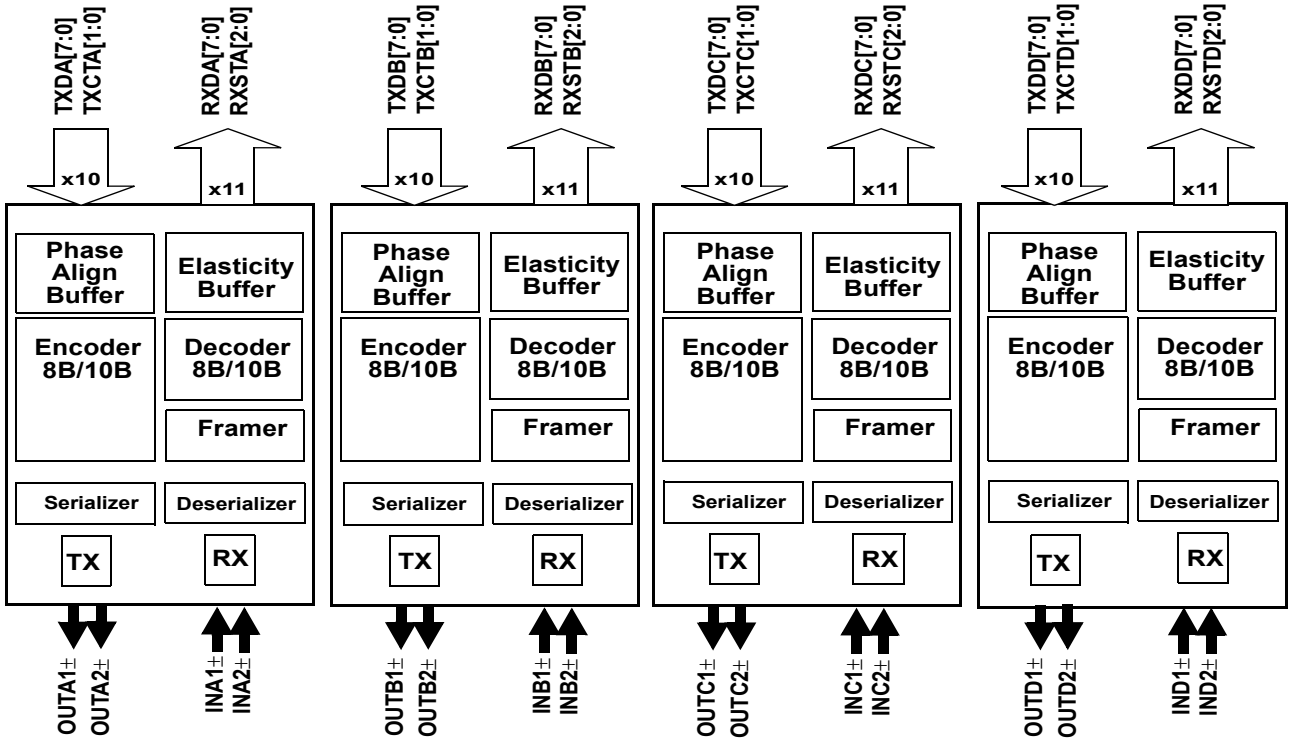
Each transmit and receive channel contains an independent BIST pattern generator and checker. This BIST hardware allows at-speed testing of the high-speed serial data paths in each transmit and receive section, and across the interconnecting links.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting backplanes on switches, routers, servers and video transmission systems.

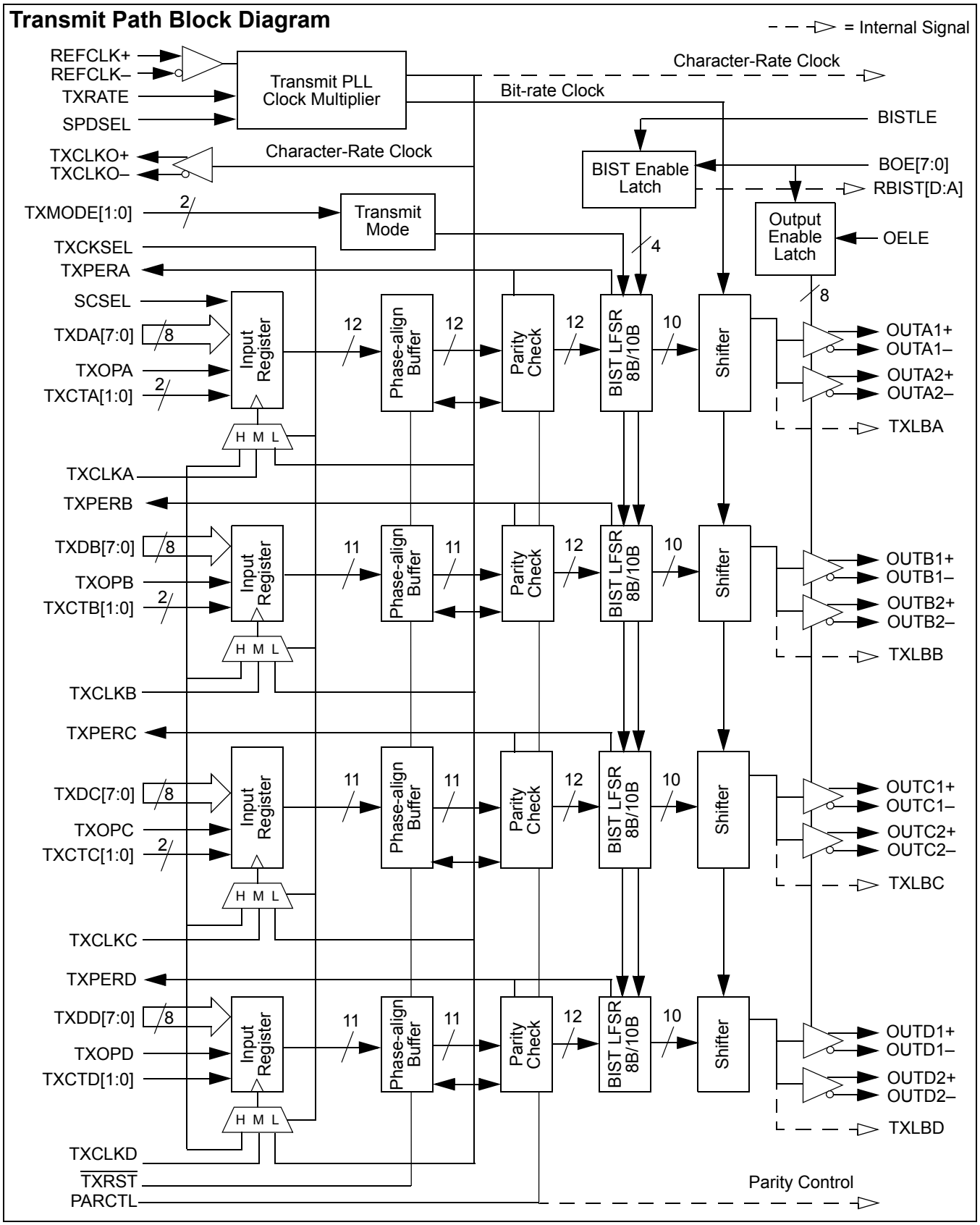
The CYV15G0401DXB is verified by testing to be compliant to all the pathological test patterns documented in SMPTE EG34-1999, for both the SMPTE 259M and 292M signaling rates. The tests ensure that the receiver recovers data with no errors for the following patterns:

1. Repetitions of 20 ones and 20 zeros.
2. Single burst of 44 ones or 44 zeros.
3. Repetitions of 19 ones followed by 1 zero or 19 zeros followed by 1 one.

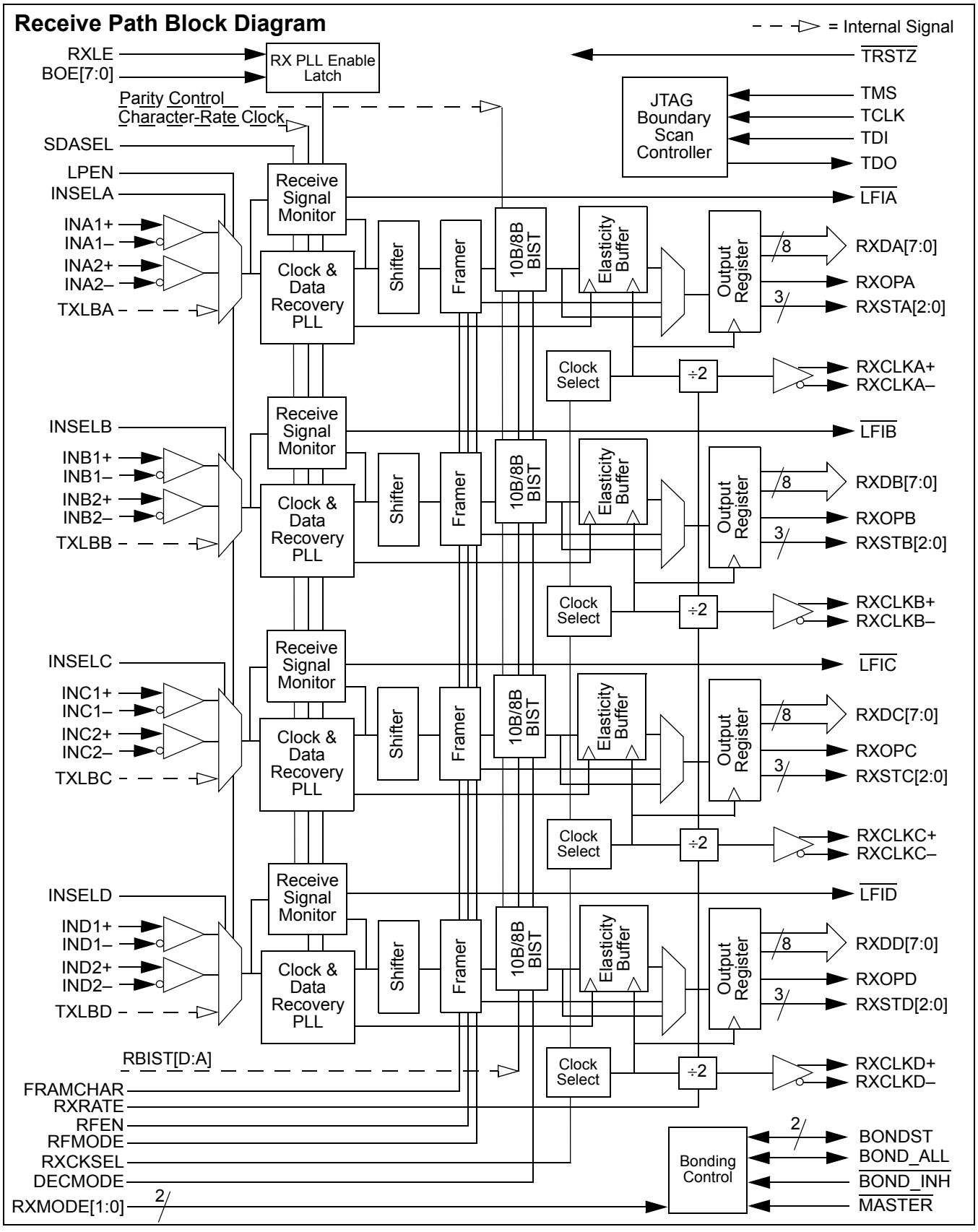
CYP(V)15G0401DXB Transceiver Logic Block Diagram



Transmit Path Block Diagram



Receive Path Block Diagram



Pin Configuration (Top View)[2]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	INC1-	OUT C1-	INC2-	OUT C2-	V_{CC}	IND1-	OUT D1-	GND	IND2-	OUT D2-	INA1-	OUT A1-	GND	INA2-	OUT A2-	V_{CC}	INB1-	OUT B1-	INB2-	OUT B2-
B	INC1+	OUT C1+	INC2+	OUT C2+	V_{CC}	IND1+	OUT D1+	GND	IND2+	OUT D2+	INA1+	OUT A1+	GND	INA2+	OUT A2+	V_{CC}	INB1+	OUT B1+	INB2+	OUT B2+
C	TDI	TMS	INSELC	INSELB	V_{CC}	PAR CTL	SDA SEL	GND	BOE[7]	BOE[5]	BOE[3]	BOE[1]	GND	TX MODE [0]	RX MODE [0]	V_{CC}	TX RATE	RX RATE	LPEN	TDO
D	TCLK	$\overline{\text{TRSTZ}}$	INSELD	INSELA	V_{CC}	RF MODE	SPD SEL	GND	BOE[6]	BOE[4]	BOE[2]	BOE[0]	GND	TX MODE [1]	RX MODE [1]	V_{CC}	$\overline{\text{BOND INH}}$	RXLE	RFEN	$\overline{\text{MAS TER}}$
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	TXPER C	TXOP C	TXDC [0]	RXCK SEL													BISTLE	RXSTB [1]	RXOPB	RXSTB [0]
G	TXDC [7]	TXCK SEL	TXDC [4]	TXDC [1]													DEC MODE	OELE	FRAM CHAR	RXDB [1]
H	GND	GND	GND	GND													GND	GND	GND	GND
J	TXCTC [1]	TXDC [5]	TXDC [2]	TXDC [3]													RXSTB [2]	RXDB [0]	RXDB [5]	RXDB [2]
K	RXDC [2]	RXCLK C–	TXCTC [0]	$\overline{\text{LFIC}}$													RXDB [3]	RXDB [4]	RXDB [7]	RXCLK B+
L	RXDC [3]	RXCLK C+	TXCLK C	TXDC [6]													RXDB [6]	$\overline{\text{LFIB}}$	RXCLK B–	TXDB [6]
M	RXDC [4]	RXDC [5]	RXDC [7]	RXDC [6]													TXCTB [1]	TXCTB [0]	TXDB [7]	TXCLK B
N	GND	GND	GND	GND													GND	GND	GND	GND
P	RXDC [1]	RXDC [0]	RXSTC [0]	RXSTC [1]													TXDB [5]	TXDB [4]	TXDB [3]	TXDB [2]
R	RXSTC [2]	RXOP C	TXPER D	TXOP D													TXDB [1]	TXDB [0]	TXOP B	TXPER B
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	TXDD [0]	TXDD [1]	TXDD [2]	TXCTD [1]	V_{CC}	RXDD [2]	RXDD [1]	GND	RX OPD	BOND _ALL	REF CLK-	TXDA [1]	GND	TXDA [4]	TXCTA [0]	V_{CC}	RXDA [2]	RXOPA	RXSTA [2]	RXSTA [1]
V	TXDD [3]	TXDD [4]	TXCTD [0]	RXDD [6]	V_{CC}	RXDD [3]	RXSTD [0]	GND	RXSTD [2]	BOND ST[0]	REF CLK+	BOND ST[1]	GND	TXDA [3]	TXDA [7]	V_{CC}	RXDA [7]	RXDA [3]	RXDA [0]	RXSTA [0]
W	TXDD [5]	TXDD [7]	$\overline{\text{LFID}}$	RXCLK D–	V_{CC}	RXDD [4]	RXSTD [1]	GND	TXCLK O-	$\overline{\text{TXRST}}$	TXOPA	SCSEL	GND	TXDA [2]	TXDA [6]	V_{CC}	$\overline{\text{LFIA}}$	RXCLK A-	RXDA [4]	RXDA [1]
Y	TXDD [6]	TXCLK D	RXDD [7]	RXCLK D+	V_{CC}	RXDD [5]	RXDD [0]	GND	TXCLK O+	N/C	TXCLK A	TXPER A	GND	TXDA [0]	TXDA [5]	V_{CC}	TXCTA [1]	RXCLK A+	RXDA [6]	RXDA[5]

Note
2. N/C = Do Not Connect

Pin Configuration (Bottom View)[3]

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
OUT B2-	INB2-	OUT B1-	INB1-	V_{CC}	OUT A2-	INA2-	GND	OUT A1-	INA1-	OUT D2-	IND2-	GND	OUT D1-	IND1-	V_{CC}	OUT C2-	INC2-	OUT C1-	INC1-	A
OUT B2+	INB2+	OUT B1+	INB1+	V_{CC}	OUT A2+	INA2+	GND	OUT A1+	INA1+	OUT D2+	IND2+	GND	OUT D1+	IND1+	V_{CC}	OUT C2+	INC2+	OUT C1+	INC1+	B
TDO	LPEN	RX RATE	TX RATE	V_{CC}	RX MODE [0]	TX MODE [0]	GND	BOE[1]	BOE[3]	BOE[5]	BOE[7]	GND	SDA SEL	PAR CTL	V_{CC}	INSELB	INSELC	TMS	TDI	C
$\overline{\text{MASTER}}$	RFEN	RXLE	$\overline{\text{BOND INH}}$	V_{CC}	RX MODE [1]	TX MODE [1]	GND	BOE[0]	BOE[2]	BOE[4]	BOE[6]	GND	SPD SEL	RF MODE	V_{CC}	INSELA	INSELD	$\overline{\text{TRSTZ}}$	TCLK	D
V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}	E
RXSTB [0]	RXOP B	RXSTB [1]	BISTLE													RXCK SEL	TXDC [0]	TXOP C	TXPER C	F
RXDB [1]	FRAM CHAR	OELE	DEC MODE													TXDC [1]	TXDC [4]	TXCK SEL	TXDC [7]	G
GND	GND	GND	GND													GND	GND	GND	GND	H
RXDB [2]	RXDB [5]	RXDB [0]	RXSTB [2]													TXDC [3]	TXDC [2]	TXDC [5]	TXCTC [1]	J
RXCLK B+	RXDB [7]	RXDB [4]	RXDB [3]													$\overline{\text{LFIC}}$	TXCTC [0]	RXCLK C-	RXDC [2]	K
TXDB [6]	RXCLK B-	$\overline{\text{LFIB}}$	RXDB [6]													TXDC [6]	TXCLK C	RXCLK C+	RXDC [3]	L
TXCLK B	TXDB [7]	TXCTB [0]	TXCTB [1]													RXDC [6]	RXDC [7]	RXDC [5]	RXDC [4]	M
GND	GND	GND	GND													GND	GND	GND	GND	N
TXDB [2]	TXDB [3]	TXDB [4]	TXDB [5]													RXSTC [1]	RXSTC [0]	RXDC [0]	RXDC [1]	P
TXPER B	TXOP B	TXDB [0]	TXDB [1]													TXOP D	TXPER D	RXOP C	RXSTC [2]	R
V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}	T
RXSTA [1]	RXSTA [2]	RXOPA	RXDA [2]	V_{CC}	TXCTA [0]	TXDA [4]	GND	TXDA [1]	REF CLK-	BOND _ALL	RXOP D	GND	RXDD [1]	RXDD [2]	V_{CC}	TXCTD [1]	TXDD [2]	TXDD [1]	TXDD [0]	U
RXSTA [0]	RXDA [0]	RXDA [3]	RXDA [7]	V_{CC}	TXDA [7]	TXDA [3]	GND	BOND ST[1]	REF CLK+	BOND ST[0]	RXSTD [2]	GND	RXSTD [0]	RXDD [3]	V_{CC}	RXDD [6]	TXCTD [0]	TXDD [4]	TXDD [3]	V
RXDA [1]	RXDA [4]	RXCLK A-	$\overline{\text{LFIA}}$	V_{CC}	TXDA [6]	TXDA [2]	GND	SCSEL	TXOP A	$\overline{\text{TXRST}}$	TXCLK O-	GND	RXSTD [1]	RXDD [4]	V_{CC}	RXCLK D–	$\overline{\text{LFID}}$	TXDD [7]	TXDD [5]	W
RXDA [5]	RXDA [6]	RXCLK A+	TXCTA [1]	V_{CC}	TXDA [5]	TXDA [0]	GND	TXPER A	TXCLK A	N/C	TXCLK O+	GND	RXDD [0]	RXDD [5]	V_{CC}	RXCLK D+	RXDD [7]	TXCLK D	TXDD [6]	Y

Note
3. N/C = Do Not Connect

Pin Descriptions

CYP(V)15G0401DXB Quad HOTLink II Transceiver

Pin Name	I/O Characteristics	Signal Description
Transmit Path Data Signals		
TXPERA TXPERB TXPERC TXPERD	LVTTL Output, changes relative to REFCLK↑ [4]	**Transmit Path Parity Error**. Active HIGH. Asserted (HIGH) if parity checking is enabled and a parity error is detected at the Encoder. This output is HIGH for one transmit character clock period to indicate detection of a parity error in the character presented to the Encoder. If a parity error is detected, the character in error is replaced with a C0.7 character to force a corresponding bad-character detection at the remote end of the link. This replacement takes place regardless of the encoded/non-encoded state of the interface. When BIST is enabled for the specific transmit channel, BIST progress is presented on these outputs. Once every 511 character times (plus a 16-character Word Sync Sequence when the receive channels are clocked by a common clock, i.e., RXCKSEL = LOW or HIGH), the associated TXPERx signal will pulse HIGH for one transmit-character clock period (if RXCKSEL= MID) or seventeen transmit- character clock periods (if RXCKSEL = LOW or HIGH and Encoder is enabled) to indicate a complete pass through the BIST sequence. Therefore, in this case TXPERx signal will pulse HIGH for one transmit-character clock period. These outputs also provide indication of a transmit Phase-align Buffer underflow or overflow. When the transmit Phase-align Buffers are enabled (TXCKSEL ≠ LOW, or TXCKSEL = LOW and TXRATE = HIGH), if an underflow or overflow condition is detected, TXPERx for the channel in error is asserted and remains asserted until either an atomic Word Sync Sequence is transmitted or TXRST is sampled LOW to re-center the transmit Phase-align Buffers.
TXCTA[1:0] TXCTB[1:0] TXCTC[1:0] TXCTD[1:0]	LVTTL Input, synchronous, sampled by the selected TXCLKx↑ or REFCLK↑ [4]	**Transmit Control**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL, and are passed to the Encoder or Transmit Shifter. They identify how the associated TXDx[7:0] characters are interpreted. When the Encoder is bypassed, these inputs are interpreted as data bits of 10-bit input character. When the Encoder is enabled, these inputs determine if the TXDx[7:0] character is encoded as Data, a Special Character code, a K28.5 fill character or a Word Sync Sequence. See Table 1 for details.
TXDA[7:0] TXDB[7:0] TXDC[7:0] TXDD[7:0]	LVTTL Input, synchronous, sampled by the selected TXCLKx↑ or REFCLK↑ [4]	**Transmit Data Inputs**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL and passed to the Encoder or Transmit Shifter. When the Encoder is enabled (TXMODE[1:0] ≠ LOW), TXDx[7:0] specify the specific data or command character to be sent. When the Encoder is bypassed, these inputs are interpreted as data bits of the 10-bit input character. See Table 1 for details.
TXOPA TXOPB TXOPC TXOPD	LVTTL Input, synchronous, internal pull-up, sampled by the respective TXCLKx↑ or REFCLK↑ [4]	**Transmit Path Odd Parity**. When parity checking is enabled (PARCTL ≠ LOW), the parity captured at these inputs is XORed with the data on the associated TXDx bus (and sometimes TXCT[1:0]) to verify the integrity of the captured character. See Table 2 for details.
SCSEL	LVTTL Input, synchronous, internal pull-down, sampled by TXCLKA↑ or REFCLK↑ [4]	**Special Character Select**. Used in some transmit modes along with TXCTx[1:0] to encode special characters or to initiate a Word Sync Sequence. When the transmit paths are configured for independent input clocks (TXCKSEL = MID), SCSEL is captured relative to TXCLKA↑.

Note
4. When REFCLK is configured for half-rate operation (TXRATE = HIGH), these inputs are sampled (or the outputs change) relative to both the rising and falling edges of REFCLK.

Pin Descriptions (continued)

CYP(V)15G0401DXB Quad HOTLink II Transceiver

Pin Name	I/O Characteristics	Signal Description
$\overline{\text{TXRST}}$	LVTTL Input, asynchronous, internal pull-up, sampled by REFCLK↑ [4]	**Transmit Clock Phase Reset**. Active LOW. When sampled LOW, the transmit Phase-align Buffers are allowed to adjust their data-transfer timing (relative to the selected input clock) to allow clean transfer of data from the Input Register to the Encoder or Transmit Shifter. When $\overline{\text{TXRST}}$ is sampled HIGH, the internal phase relationship between the associated TXCLKx and the internal character-rate clock is fixed and the device operates normally. When configured for half-rate REFCLK sampling of the transmit character stream (TXCKSEL = LOW and TXRATE = HIGH), assertion of $\overline{\text{TXRST}}$ is only used to clear Phase-align buffer faults caused by highly asymmetric REFCLK periods or REFCLKs with excessive cycle-to-cycle jitter. During this alignment period, one or more characters may be added to or lost from all the associated transmit paths as the transmit Phase-align Buffers are adjusted. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive rising edges REFCLK to ensure the reset operation is initiated correctly on all channels. This input is ignored when both TXCKSEL and TXRATE are LOW, since the phase align buffer is bypassed. In all other configurations, $\overline{\text{TXRST}}$ should be asserted during device initialization to ensure proper operation of the Phase-align buffer. $\overline{\text{TXRST}}$ should be asserted after the presence of a valid TXCLKx and after allowing enough time for the TXPLL to lock to the reference clock (as specified by parameter t_{TXLOCK}).
Transmit Path Clock and Clock Control		
TXCKSEL	Three-level Select [5], static control input	**Transmit Clock Select**. Selects the clock source, used to write data into the transmit Input Register of the transmit channel(s). When LOW, REFCLK↑ [4] is used as the Input Register clock for TXDx[7:0] and TXCTx[1:0] of all channels. When MID, TXCLKx↑ is used as the Input Register clock for TXDx[7:0] and TXCTx[1:0]. When HIGH, TXCLKA↑ is used as the Input Register clock for TXDx[7:0] and TXCTx[1:0] of all channels.
TXCLKO±	LVTTL Output	**Transmit Clock Output**. This true and complement output clock is synthesized by the transmit PLL and is synchronous to the internal transmit character clock. It has the same frequency as REFCLK (when TXRATE = LOW), or twice the frequency of REFCLK (when TXRATE = HIGH). This output clock has no direct phase relationship to REFCLK.
TXRATE	LVTTL Input, static control input, internal pull-down	**Transmit PLL Clock Rate Select**. When TXRATE = HIGH, the Transmit PLL multiplies REFCLK by 20 to generate the serial bit-rate clock. When TXRATE = LOW, the transmit PLL multiples REFCLK by 10 to generate the serial bit-rate clock. See Table 11 for a list of operating serial rates. When REFCLK is selected to clock the receive parallel interfaces (RXCKSEL = LOW), the TXRATE input also determines if the clocks on the RXCLKA± and RXCLKC± outputs are full or half-rate. When TXRATE = HIGH (REFCLK is half-rate), the RXCLKA± and RXCLKC± output clocks are also half-rate clocks and follow the frequency and duty cycle of the REFCLK input. When TXRATE = LOW (REFCLK is full-rate), the RXCLKA± and RXCLKC± output clocks are full-rate clocks and follow the frequency and duty cycle of the REFCLK input. When TXCKSEL = MID or HIGH (TXCLKx or TXCLKA selected to clock input register), configuring TXRATE = HIGH (Half-rate REFCLK) is an invalid mode of operation.
TXCLKA TXCLKB TXCLKC TXCLKD	LVTTL Clock Input, internal pull-down	**Transmit Path Input Clocks**. These clocks must be frequency-coherent to TXCLKO±, but may be offset in phase. The internal operating phase of each input clock (relative to REFLCK or TXCLKO±) is adjusted when $\overline{\text{TXRST}}$ = LOW and locked when $\overline{\text{TXRST}}$ = HIGH.

Note
5. Three-level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC}. When not connected or allowed to float, a Three-level select input will self-bias to the MID level.

Pin Descriptions (continued)

CYP(V)15G0401DXB Quad HOTLink II Transceiver

Pin Name	I/O Characteristics	Signal Description
Transmit Path Mode Control		
TXMODE[1:0]	Three-level Select [5] static control inputs	**Transmit Operating Mode**. These inputs are interpreted to select one of nine operating modes of the transmit path. See Table 3 for a list of operating modes.
Receive Path Data Signals		
RXDA[7:0] RXDB[7:0] RXDC[7:0] RXDD[7:0]	LVTTL Output, synchronous to the selected RXCLKx↑ output (or REFCLK↑ input[4] when RXCKSEL = LOW)	**Parallel Data Output**. These outputs change following the rising edge of the selected receive interface clock. When the Decoder is enabled (DECMODE = HIGH or MID), these outputs represent either received data or special characters. The status of the received data is represented by the values of RXSTx[2:0]. When the Decoder is bypassed (DECMODE = LOW), RXDx[7:0] become the higher order bits of the 10-bit received character. See Table 18 for details.
RXSTA[2:0] RXSTB[2:0] RXSTC[2:0] RXSTD[2:0]	LVTTL Output, synchronous to the selected RXCLKx↑ output (or REFCLK↑ input[4] when RXCKSEL = LOW)	**Parallel Status Output**. These outputs change following the rising edge of the selected receive interface clock. When the Decoder is bypassed (DECMODE = LOW), RXSTx[1:0] become the two low-order bits of the 10-bit received character, while RXSTx[2] = HIGH indicates the presence of a Comma character in the Output Register. See Table 18 for details. When the Decoder is enabled (DECMODE = HIGH or MID), RXSTx[2:0] provide status of the received signal. See Table 20, *21* and *22* for a list of Receive Character status.
RXOPA RXOPB RXOPC RXOPD	three-state, LVTTL Output, synchronous to the selected RXCLKx↑ output (or REFCLK↑ input[4] when RXCKSEL = LOW)	**Receive Path Odd Parity**. When parity generation is enabled (PARCTL ≠ LOW), the parity output at these pins is valid for the data on the associated RXDx bus bits. When parity generation is disabled (PARCTL = LOW) these output drivers are disabled (High-Z).
Receive Path Clock and Clock Control		
RXRATE	LVTTL Input, static control input, internal pull-down	**Receive Clock Rate Select**. When LOW, the RXCLKx± recovered clock outputs are complementary clocks operating at the recovered character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–. When HIGH, the RXCLKx± recovered clock outputs are complementary clocks operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–. When REFCLK± is selected to clock the output registers (RXCKSELx = LOW), RXRATEx is not interpreted. The RXCLKA± and RXCLKC± output clocks will follow the frequency and duty cycle of REFCLK±.
FRAMCHAR	Three-level Select [5], static control input	**Framing Character Select**. Used to select the character or portion of a character used for character framing of the received data streams. When MID, the Framer looks for both positive and negative disparity versions of the eight-bit Comma character. When HIGH, the Framer looks for both positive and negative disparity versions of the K28.5 character. Configuring FRAMCHAR to LOW is reserved for component test.
RFEN	LVTTL Input, asynchronous, internal pull-down	**Reframe Enable for All Channels**. Active HIGH. When HIGH, the framers in all four channels are enabled to frame per the presently enabled framing mode as selected by RFMODE and selected framing character as selected by FRAMCHAR.
RXMODE[1:0]	Three-level Select [5], static control inputs	**Receive Operating Mode**. These inputs are interpreted to select one of nine operating modes of the receive path. See Table 14 for details.

Pin Descriptions (continued)

CYP(V)15G0401DXB Quad HOTLink II Transceiver

Pin Name	I/O Characteristics	Signal Description
RXCLKA± RXCLKB± RXCLKC± RXCLKD±	Three-state, LVTTL Output clock or static control input	**Receive Character Clock Output or Clock Select Input**. When configured such that all output data paths are clocked by the recovered clock (RXCKSEL = MID), these true and complement clocks are the receive interface clocks which are used to control timing of output data (RXDx[7:0], RXSTx[2:0] and RXOPx). These clocks are output continuously at either the dual-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATE. When configured such that all output data paths are clocked by REFCLK instead of a recovered clock (RXCKSEL = LOW), the RXCLKA± and RXCLKC± output drivers present a buffered and delayed form of REFCLK. RXCLKA± and RXCLKC± are buffered forms of REFCLK that are slightly different in phase. This phase difference allows the user to select the optimal setup/hold timing for their specific interface. When RXCKSEL = LOW and quad channel bonding is enabled, RXCLKB+ and RXCLKD+ are static control inputs used to select the master channel for bonding and status control. When RXCKSEL = HIGH and quad-channel bonding is enabled, one of the recovered clocks from channels A, B, C or D can be selected to clock the bonded output data. The selection of the recovered clock is made by RXCLKB+ and RXCLKD+ which act as static control inputs in this mode. Both RXCLKA± and RXCLKC± output buffered forms of the recovered clock selected from receive channel A, B, C, or D. See Table 15 for details. When RXCKSEL = HIGH and dual-channel bonding is enabled, one of the recovered clocks from channels A or B is selected to present bonded data from channels A and B, and one of the recovered clocks from channels C or D is selected to present bonded data from channels C and D. RXCLKA± output the recovered clock from either receive channel A or receive channel B as selected by RXCLKB+ to clock the bonded output data from channels A and B, and RXCLKC± output the recovered clock from either receive channel C or receive channel D as selected by RXCLKD+ to the clock the bonded output data from channels C and D. See Table 16 for details.
RXCKSEL	Three-level Select [5], static control input	**Receive Clock Mode**. Selects the receive clock source used to transfer data to the Output Registers. When LOW, all four Output Registers are clocked by REFCLK. RXCLKB± and RXCLKD± outputs are disabled (High-Z), and RXCLKA± and RXCLKC± present buffered and delayed forms of REFCLK. This clocking mode is required for channel bonding across multiple devices. When MID, each RXCLKx± output follows the recovered clock for the respective channel, as selected by RXRATE. When the 10B/8B Decoder and Elasticity Buffer are bypassed (DECMODE = LOW), RXCKSEL must be MID. When HIGH and channel bonding is enabled in dual-channel mode (RX modes 3 and 5), RXCLKA± outputs the recovered clock from either receive channel A or B as selected by RXCLKB+, and RXCLKC± outputs the recovered clock from either receive channel C or D as selected by RXCLKD+. These output clocks may operate at the character-rate or half the character-rate as selected by RXRATE. When HIGH and channel bonding is enabled in quad channel mode (RX modes 6 and 8), or if the receive channels are operated in independent mode (RX modes 0 and 2), RXCLKA± and RXCLKC± output the recovered clock from receive channel A, B, C, or D, as selected by RXCLKB+ and RXCLKD+. This output clock may operate at the character-rate or half the character-rate as selected by RXRATE.

Pin Descriptions (continued)

CYP(V)15G0401DXB Quad HOTLink II Transceiver

Pin Name	I/O Characteristics	Signal Description
DECMODE	Three-level Select [5], static control input	**Decoder Mode Select**. This input selects the behavior of the Decoder block. When LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. When the Decoder is bypassed, RXCKSEL must be MID. When MID, the Decoder is enabled and the Cypress decoder table for Special Code characters is used. When HIGH, the Decoder is enabled and the alternate decoder table for Special Code characters is used. See Table 27 for a list of the Special Codes supported in both encoded modes.
RFMODE	Three-level Select [5], static control input	**Reframe Mode Select**. Used to select the type of character framing used to adjust the character boundaries (based on detection of one or more framing characters in the received serial bit stream). This signal operates in conjunction with the presently enabled channel bonding mode, and the type of framing character selected. When LOW, the Low-Latency Framer is selected. This will frame on each occurrence of the selected framing character(s) in the received data stream. This mode of framing stretches the recovered character-rate clock for one or multiple cycles to align that clock with the recovered data. When MID, the Cypress-mode Multi-Byte parallel Framer is selected. This requires a pair of the selected framing character(s), on identical 10-bit boundaries, within a span of 50 bits, before the character boundaries are adjusted. The recovered character clock remains in the same phase regardless of character offset. When HIGH, the alternate mode Multi-Byte parallel Framer is selected. This requires detection of the selected framing character(s) of the allowed disparities in the received serial bit stream, on identical 10-bit boundaries, on four directly adjacent characters. The recovered character clock remains in the same phase regardless of character offset.
Device Control Signals		
PARCTL	Three-level Select [5], static control input	**Parity Check/Generate Control**. Used to control the different parity check and generate functions. When LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z). When MID, and the 8B/10B Encoder and Decoder are enabled (TXMODE[1] ≠ LOW, DECMODE ≠ LOW), TXDx[7:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[7:0] outputs and presented on RXOPx. When the Encoder and Decoder are disabled (TXMODE[1] = LOW, DECMODE = LOW), theTXDx[7:0] and TXCTx[1:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[7:0] and RXSTx[1:0] outputs and presented on RXOPx. When HIGH, parity checking and generation are enabled. The TXDx[7:0] and TXCTx[1:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[7:0] and RXSTx[2:0] outputs and presented on RXOPx. See Table 2 and *19* for details.
SPDSEL	Three-level Select [5] static control input	**Serial Rate Select**. This input specifies the operating bit-rate range of both transmit and receive PLLs. LOW = 195–400 MBaud, MID = 400–800 MBaud, HIGH = 800–1500 MBaud. When SPDSEL is LOW, setting TXRATE = HIGH (Half-rate Reference Clock) is invalid.
$\overline{\text{TRSTZ}}$	LVTTL Input, internal pull-up	**Device Reset**. Active LOW. Initializes all state machines and counters in the device. When sampled LOW by the rising edge of REFCLK↑, this input resets the internal state machines and sets the Elasticity Buffer pointers to a nominal offset. When the reset is removed ($\overline{\text{TRSTZ}}$ sampled HIGH by REFCLK↑), the status and data outputs will become deterministic in less than 16 REFCLK cycles. The BISTLE, OELE, and RXLE latches are reset by $\overline{\text{TRSTZ}}$. If the Elasticity Buffer or the Phase-align Buffer are used, $\overline{\text{TRSTZ}}$ should be applied after power up to initialize the internal pointers into these memory arrays.

Pin Descriptions (continued)

CYP(V)15G0401DXB Quad HOTLink II Transceiver

Pin Name	I/O Characteristics	Signal Description
REFCLK±	Differential LVPECL or single-ended LVTTL Input Clock	**Reference Clock**. This clock input is used as the timing reference for the transmit PLL. It is also used as the centering frequency of the Range Controller block of the Receive CDR PLLs.This input clock may also be selected to clock the transmit and receive parallel interfaces. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLK input, and leave the alternate REFCLK input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs. When TXCKSEL = LOW, REFCLK is also used as the clock for the parallel transmit data (input) interface. When RXCKSEL = LOW, the Elasticity Buffer is enabled and REFCLK is used as the clock for the parallel receive data (output) interface. If the Elasticity Buffer is used, framing characters will be inserted or deleted to/from the data stream to compensate for frequency differences between the reference clock and recovered clock. When an addition happens, a K28.5 will be appended immediately after a framing is detected in the Elasticity Buffer. When deletion happens, a framing character will be removed from the data stream when detected in the Elasticity Buffer.
Analog I/O and Control		
OUTA1± OUTB1± OUTC1± OUTD1±	CML Differential Output	**Primary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3 V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules.
OUTA2± OUTB2± OUTC2± OUTD2±	CML Differential Output	**Secondary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3 V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules.
INA1± INB1± INC1± IND1±	LVPECL Differential Input	**Primary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The INx1± serial streams are passed to the receiver Clock and Data Recovery (CDR) circuits to extract the data content when INSELx = HIGH.
INA2± INB2± INC2± IND2±	LVPECL Differential Input	**Secondary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The INx2± serial streams are passed to the receiver Clock and Data Recovery (CDR) circuits to extract the data content when INSELx = LOW.
INSELA INSELB INSELC INSELD	LVTTL Input, asynchronous	**Receive Input Selector**. Determines which external serial bit stream is passed to the receiver Clock and Data Recovery circuit. When HIGH, the INx1± input is selected. When LOW, the INx2± input is selected.
SDASEL	Three-level Select [5] static configuration input	**Signal Detect Amplitude Level Select**. Allows selection of one of three predefined amplitude trip points for a valid signal indication, as listed in Table 12.
LPEN	LVTTL Input, asynchronous, internal pull-down	**All-Port Loop-Back Enable**. Active HIGH. When asserted (HIGH), the transmit serial data from each channel is internally routed to the associated receiver Clock and Data Recovery (CAR) circuit. All enabled serial drivers are forced to differential logic “1.” All serial data inputs are ignored.
OELE	LVTTL Input, asynchronous, internal pull-up	**Serial Driver Output Enable Latch Enable**. Active HIGH. When OELE = HIGH, the signals on the BOE[7:0] inputs directly control the OUTxy± differential drivers. When the BOE[x] input is HIGH, the associated OUTxy± differential driver is enabled. When the BOE[x] input is LOW, the associated OUTxy± differential driver is powered down. The specific mapping of BOE[7:0] signals to transmit output enables is listed in Table 10. When OELE returns LOW, the last values present on BOE[7:0] are captured in the internal Output Enable Latch. If the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable all outputs.

Pin Descriptions (continued)

CYP(V)15G0401DXB Quad HOTLink II Transceiver

Pin Name	I/O Characteristics	Signal Description
BISTLE	LVTTL Input, asynchronous, internal pull-up	**Transmit and Receive BIST Latch Enable**. Active HIGH. When BISTLE = HIGH, the signals on the BOE[7:0] inputs directly control the transmit and receive BIST enables. When the BOE[x] input is LOW, the associated transmit or receive channel is configured to generate or compare the BIST sequence respectively. When the BOE[x] input is HIGH, the associated transmit or receive channel is configured for normal data transmission or reception. The specific mapping of BOE[7:0] signals to transmit and receive BIST enables is listed in Table 10. When BISTLE returns LOW, the last values present on BOE[7:0] are captured in the internal BIST Enable Latch. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable BIST on all transmit and receive channels.
RXLE	LVTTL Input, asynchronous, internal pull-up	**Receive Channel Power-control Latch Enable**. Active HIGH. When RXLE = HIGH, the signals on the BOE[7:0] inputs directly control the power enables for the receive PLLs and analog circuitry. When the BOE[7:0] input is HIGH, the associated receive channel A through D PLL and analog circuitry are active. When the BOE[7:0] input is LOW, the associated receive channel A through D PLL and analog circuitry are powered down. The specific mapping of BOE[7:0] signals to the associated receive channel enables is listed in Table 10. When RXLE returns LOW, the last values present on BOE[7:0] are captured in the internal RX PLL Enable Latch. When the device is reset ($\overline{\text{TRSTZ}}$ = LOW), the latch is reset to disable all receive channels.
BOE[7:0]	LVTTL Input, asynchronous, internal pull-up	**BIST, Serial Output, and Receive Channel Enables**. These inputs are passed to and through the Output Enable Latch when OELE is HIGH, and captured in this latch when OELE returns LOW. These inputs are passed to and through the BIST Enable Latch when BISTLE is HIGH, and captured in this latch when BISTLE returns LOW. These inputs are passed to and through the Receive Channel Enable Latch when RXLE is HIGH, and captured in this latch when RXLE returns LOW.
$\overline{\text{LFIA}}$ $\overline{\text{LFIB}}$ $\overline{\text{LFIC}}$ LFID	LVTTL Output, Asynchronous	**Link Fault Indication Output**. Active LOW. $\overline{\text{LFIx}}$ is the logical OR of four internal conditions: 1. Received serial data frequency outside expected range 2. Analog amplitude below expected levels 3. Transition density lower than expected 4. Receive Channel disabled.
Bonding Control		
BONDST[1:0]	Bidirectional Open Drain, internal pull-up	**Bonding Status**. These signals are only used when multiple devices are bonded together. They communicate the status of Elasticity Buffer management events from master device of the bonding domain to the slave devices of the same bonding domain. These outputs change at the same character rate as the receive output data buses, but are connected only to all the slave CYP(V)15G0401DXB devices. When $\overline{\text{MASTER}}$ = LOW, these are output signals and present the Elasticity Buffer status from the selected master receive channel of the device configured as the master. Receive master channel selection is performed using the RXCLKB+ and RXCLKD+ inputs. The BONDST[1:0] Outputs of the master device must be connected to BONDST[1:0] Inputs of all the slave devices in the bonding domain. These status outputs indicate one of four possible conditions, on a synchronous basis, to the slave devices. These conditions are: 00—Reserved 01—Add one K28.5 immediately following the next framing character received 10—Delete next framing character received 11—Normal data. These outputs are driven only when the device is configured as a master, all four channels are bonded together, and the receive parallel interface is clocked by REFCLK↑.

Pin Descriptions (continued)

CYP(V)15G0401DXB Quad HOTLink II Transceiver

Pin Name	I/O Characteristics	Signal Description
$\overline{\text{MASTER}}$	LVTTL Input, static configuration input, internal pull-down	**Master Device Select**. When LOW, the present device is configured as the master, and BONDST[1:0] outputs are driven. When HIGH, the present device is configured as a slave, and BONDST[1:0] are inputs. MASTER is only interpreted when configured for quad channel bonding, and the receive parallel interface is clocked by REFCLK↑.
BOND_ALL	Bidirectional Open Drain, Internal pull-up	**All Channels Bonded Indicator**. Active HIGH, wired AND. BOND_ALL pins from all CYP(V)15G0401DXB devices in the same bonding domain must be wired together. After bonding resolution is completed and when HIGH, all receive channels have detected valid framing. This output is LOW during the bonding resolution process. This output is driven only when configured for four channel bonding, and the receive parallel interface is clocked by REFCLK↑.
$\overline{\text{BOND\_INH}}$	LVTTL Input, static configuration input, Internal pull-up	**Parallel Bond Inhibit**. Active LOW. When asserted (LOW), this signal inhibits the adjustment of character offsets in all receive channels if the Bonding Sequence has *not* been detected in all bonded channels. When HIGH, all channels that have detected the Bonding Sequence are allowed to align their Receive Elasticity Buffer pipelines. For any channels to bond, the selected master channel must be a member of the group. When multiple devices are used together, the $\overline{\text{BOND\_INH}}$ input on all parts must be configured the same.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset. The TAP controller is also reset automatically upon application of power to the device.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**
TDO	Three-state LVTTL Output	**Test Data Out**. JTAG data output buffer which is High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
Power		
V_{CC}		**+3.3 V Power**
GND		**Signal and power ground for all internal circuits**.

CYP(V)15G0401DXB HOTLink II Operation

The CYP(V)15G0401DXB is a highly configurable device designed to support reliable transfer of large quantities of data, using high-speed serial links, from one or multiple sources to one or multiple destinations. This device supports four single-byte or single-character channels that may be combined to support transfer of wider buses.

CYP(V)15G0401DXB **Transmit Data Path**

Operating Modes

The transmit path of the CYP(V)15G0401DXB supports four character-wide data paths. These data paths are used in multiple operating modes as controlled by the TXMODE[1:0] inputs.

Input Register

The bits in the Input Register for each channel support different assignments, based on if the character is unencoded, encoded with two control bits, or encoded with three control bits. These assignments are shown in Table 1. Each Input Register captures a minimum of eight data bits and two control bits on each input clock cycle. When the Encoder is bypassed, the TXCTx[1:0] control bits, are part of the preencoded 10-bit character.

When the Encoder is enabled (TXMODE[1] ≠ LOW), the TXCTx[1:0] bits are interpreted along with the associated TXDx[7:0] character to generate the specific 10-bit transmission character. When TXMODE[0] ≠ HIGH, an additional special character select (SCSEL) input is also captured and interpreted. This SCSEL input is used to modify the encoding of the associated characters. When the transmit Input Registers are clocked by a common clock (TXCLKA↑ or REFCLK↑), this SCSEL input can be changed on a clock-by-clock basis and affects all four channels.

When operated with a separate input clock on each transmit channel, this SCSEL input is sampled synchronous to TXCLKA↑. While the value on SCSEL still affects all channels, it is interpreted when the character containing it is read from the transmit Phase-align Buffer (where all four paths are internally clocked synchronously).

Table 1. Input Register Bit Assignments [6]

Signal Name	Unencoded	Encoded	
		2-bit Control	3-bit Control
TXDx[0] (LSB)	DINx[0]	TXDx[0]	TXDx[0]
TXDx[1]	DINx[1]	TXDx[1]	TXDx[1]
TXDx[2]	DINx[2]	TXDx[2]	TXDx[2]
TXDx[3]	DINx[3]	TXDx[3]	TXDx[3]
TXDx[4]	DINx[4]	TXDx[4]	TXDx[4]
TXDx[5]	DINx[5]	TXDx[5]	TXDx[5]
TXDx[6]	DINx[6]	TXDx[6]	TXDx[6]
TXDx[7]	DINx[7]	TXDx[7]	TXDx[7]
TXCTx[0]	DINx[8]	TXCTx[0]	TXCTx[0]
TXCTx[1] (MSB)	DINx[9]	TXCTx[1]	TXCTx[1]
SCSEL	N/A	N/A	SCSEL

Phase-align Buffer

Data from the Input Registers are passed either to the Encoder or to the associated Phase-align Buffer. When the transmit paths are operated synchronous to REFCLK↑ (TXCKSEL = LOW and TXRATE = LOW), the Phase-align Buffers are bypassed and data is passed directly to the Parity Check and Encoder blocks to reduce latency.

When an Input-Register clock with an uncontrolled phase relationship to REFCLK is selected (TXCKSEL ≠ LOW) or if data is captured on both edges of REFCLK (TXRATE = HIGH), the Phase-align Buffers are enabled. These buffers are used to absorb clock phase differences between the presently selected input clock and the internal character clock.

Initialization of the Phase-align Buffers takes place when the TXRST input is sampled LOW by two consecutive rising edges of REFCLK. When TXRST is returned HIGH, the present input clock phase relative to REFCLK is set. TXRST is an asynchronous input, but is sampled internally to synchronize it to the internal transmit path state machines.

Once set, the input clocks are allowed to skew in time up to half a character period in either direction relative to REFCLK; i.e., ±180°. This time shift allows the delay paths of the character clocks (relative to REFCLK) to change due to operating voltage and temperature, while not affecting the design operation.

If the phase offset, between the initialized location of the input clock and REFCLK↑, exceeds the skew handling capabilities of the Phase-align Buffer, an error is reported on the associated TXPERx output. This output indicates a continuous error until the Phase-align Buffer is reset. While the error remains active, the transmitter for the associated channel will output a continuous C0.7 character to indicate to the remote receiver that an error condition is present in the link.

In specific transmit modes, it is also possible to reset the Phase-align Buffers individually and with minimal disruption of the serial data stream. When the transmit interface is configured for generation of atomic Word Sync Sequences (TXMODE[1] = MID) and a Phase-align Buffer error is present, the transmission of a Word Sync Sequence will re-center the Phase-align Buffer and clear the error condition.[7]

Parity Support

In addition to the ten data and control bits that are captured at each transmit Input Register, a TXOPx input is also available on each channel. This allows the CYP(V)15G0401DXB to support ODD parity checking for each channel. Parity checking is available for all operating modes (including Encoder Bypass). The specific mode of parity checking is controlled by the PARCTL input, and operates per Table 2.

Table 2. Input Register Bits Checked for Parity [8]

Signal Name	Transmit Parity Check Mode (PARCTL)			
	LOW	MID		HIGH
		TXMODE[1] = LOW	TXMODE[1] ≠ LOW	
TXDx[0]		X [9]	X	X
TXDx[1]		X	X	X
TXDx[2]		X	X	X
TXDx[3]		X	X	X
TXDx[4]		X	X	X
TXDx[5]		X	X	X
TXDx[6]		X	X	X
TXDx[7]		X	X	X
TXCTx[0]		X		X
TXCTx[1]		X		X
TXOPx		X	X	X

When PARCTL is MID (open) and the Encoders are enabled (TXMODE[1] ≠ LOW), only the TXDx[7:0] data bits are checked for ODD parity along with the associated TXOPx bit. When PARCTL = HIGH with the Encoder enabled (or MID with the Encoder bypassed), the TXDx[7:0] and TXCTx[1:0] inputs are checked for ODD parity along with the associated TXOPx bit. When PARCTL = LOW, parity checking is disabled.

When parity checking and the Encoder are both enabled (TXMODE[1] ≠ LOW), the detection of a parity error causes a C0.7 character of proper disparity to be passed to the Transmit Shifter. When the Encoder is bypassed (TXMODE[1] = LOW, LOW), detection of a parity error causes a positive disparity version of a C0.7 transmission character to be passed to the Transmit Shifter.

Notes
6. The TXOPx inputs are also captured in the associated Input Register, but their interpretation is under the separate control of PARCTL.
7. One or more K28.5 characters may be added or lost from the data stream during this reset operation. When used with non-Cypress devices that require a complete 16-character Word Sync Sequence for proper Receive Elasticity Buffer alignment, it is recommend that the sequence be followed by a second Word Sync Sequence to ensure proper operation.
8. Transmit path parity errors are reported on the associated TXPERx output.
9. Bits marked as X are XORed together. Result must be a logic-1 for parity to be valid.

Encoder

The character, received from the Input Register or Phase-align Buffer and Parity Check Logic, is then passed to the Encoder logic. This block interprets each character and any associated control bits, and outputs a 10-bit transmission character.

Depending on the configured operating mode, the generated transmission character may be

- The 10-bit pre-encoded character accepted in the Input Register
- The 10-bit equivalent of the eight-bit Data character accepted in the Input Register
- The 10-bit equivalent of the eight-bit Special Character code accepted in the Input Register
- The 10-bit equivalent of the C0.7 SVS character if parity checking was enabled and a parity error was detected
- The 10-bit equivalent of the C0.7 SVS character if a Phase-align Buffer overflow or underflow error is present
- A character that is part of the 511-character BIST sequence
- A K28.5 character generated as an individual character or as part of the 16-character Word Sync Sequence.

The selection of the specific characters generated are controlled by the TXMODE[1:0], SCSEL, TXCTx[1:0], and TXDx[7:0] inputs for each character.

Data Encoding

Raw data, as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee

- a minimum transition density (to allow the serial receive PLL to extract a clock from the data stream).
- a DC-balance in the signaling (to prevent baseline wander).
- run-length limits in the serial data (to limit the bandwidth requirements of the serial link).
- the remote receiver a way of determining the correct character boundaries (framing).

When the Encoder is enabled (TXMODE[1] ≠ LOW), the characters to be transmitted are converted from Data or Special Character codes to 10-bit transmission characters (as selected by their respective TXCTx[1:0] and SCSEL inputs), using an integrated 8B/10B Encoder. When directed to encode the character as a Special Character code, it is encoded using the Special Character encoding rules listed in Table 27. When directed to encode the character as a Data character, it is encoded using the Data Character encoding rules in Table 26.

The 8B/10B Encoder is standards compliant with ANSI/NCITS ASC X3.230-1994 (Fibre Channel), IEEE 802.3z (Gigabit Ethernet), the IBM® ESCON® and FICON™ channels, Digital Video Broadcast (DVB-ASI), and ATM Forum standards for data transport.

Many of the Special Character codes listed in Table 27 may be generated by more than one input character. The CYP(V)15G0401DXB is designed to support two independent (but non-overlapping) Special Character code tables. This allows the CYP(V)15G0401DXB to operate in mixed environments with other Cypress HOTLink devices using the enhanced Cypress command code set, and the reduced command sets of other non-Cypress devices. Even when used in an environment that normally uses non-Cypress Special Character codes, the selective use of Cypress command codes can permit operation where running disparity and error handling must be managed.

Following conversion of each input character from eight bits to a 10-bit transmission character, it is passed to the Transmit Shifter and is shifted out LSB first, as required by ANSI and IEEE standards for 8B/10B coded serial data streams.

Transmit Modes

The operating mode of the transmit path is set through the TXMODE[1:0] inputs. These static three-level select inputs allow one of nine transmit modes to be selected. The transmit modes are listed in Table 3

Table 3. Transmit Operating Modes

TX Mode		Operating Mode		
Mode Number	TXMODE [1:0]	Word Sync Sequence Support	SCSEL Control	TXCTx Function
0	LL	None	None	Encoder Bypass
1	LM	None	None	Reserved for test
2	LH	None	None	Reserved for test
3	ML	Atomic	Special Character	Encoder Control
4	MM	Atomic	Word Sync	Encoder Control
5	MH	Atomic	None	Encoder Control
6	HL	Interruptible	Special Character	Encoder Control
7	HM	Interruptible	Word Sync	Encoder Control
8	HH	Interruptible	None	Encoder Control

The encoded modes (TX Modes 3 through 8) support multiple encoding tables. These encoding tables vary by the specific combinations of SCSEL, TXCTx[1], and TXCTx[0] that are used to control the generation of data and control characters. These multiple encoding forms allow maximum flexibility in interfacing to legacy applications, while also supporting numerous extensions in capabilities.

TX Mode 0—Encoder Bypass

When the Encoder is bypassed, the character captured from the TXDx[7:0] and TXCTx[1:0] inputs is passed directly to the Transmit Shifter without modification. If parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected, the 10-bit character is replaced with the 1001111000 pattern (+C0.7 character).

With the Encoder bypassed, the TXCTx[1:0] inputs are considered part of the data character and do not perform a control function that would otherwise modify the interpretation of the TXDx[7:0] bits. The bit usage and mapping of these control bits when the Encoder is bypassed is shown in Table 4.

In Encoder Bypass mode, the SCSEL input is ignored. All clocking modes interpret the data the same, with no internal linking between channels.

TX Modes 1 and 2—Factory Test Modes

Table 4. Encoder Bypass Mode (TXMODE[1:0] = LL)

Signal Name	Bus Weight	10Bit Name
TXDx[0] (LSB)[10]	2^0	a
TXDx[1]	2^1	b
TXDx[2]	2^2	c
TXDx[3]	2^3	d
TXDx[4]	2^4	e
TXDx[5]	2^5	i
TXDx[6]	2^6	f
TXDx[7]	2^7	g
TXCTx[0]	2^8	h
TXCTx[1] (MSB)	2^9	j

These modes enable specific factory test configurations. They are not considered normal operating modes of the device. Entry or configuration of the device into these modes will not damage the device.

TX Mode 3— Word Sync and SCSEL Control of Special Codes

When configured in TX Mode 3, the SCSEL input is captured along with the associated TXCTx[1:0] data control inputs. These bits combine to control the interpretation of the TXDx[7:0] bits and the characters generated by them. These bits are interpreted as listed in Table 5.

When TXCKSEL = MID, all transmit channels capture data into their Input Registers using independent TXCLKx clocks. In this mode, the SCSEL input is sampled only by TXCLKA↑. When the character (accepted in the Channel-A Input Register) has passed through the Phase-align Buffer and any selected parity validation, the level captured on SCSEL is passed to the Encoder of the remaining channels during this same cycle.

Table 5. TX Modes 3 and 6 Encoding

SCSEL	TXCTx[1]	TXCTx[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
1	0	1	Special character code
X	1	1	16-character Word Sync Sequence

To avoid the possible ambiguities that may arise due to the uncontrolled arrival of SCSEL relative to the characters in the alternate channels, SCSEL is often used as static control input.

Word Sync Sequence

When TXCTx[1:0] = 11, a 16-character sequence of K28.5 characters, known as a Word Sync Sequence, is generated on the associated channel. This sequence of K28.5 characters may start with either a positive or negative disparity K28.5 (as determined by the current running disparity and the 8B/10B coding rules). The disparity of the second and third K28.5 characters in this sequence are reversed from what normal 8B/10B coding rules would generate. The remaining K28.5 characters in the sequence follow all 8B/10B coding rules. The disparity of the generated K28.5 characters in this sequence follow a pattern of either ++−−+−+−+−+−+−+− or −−++−+−+−+−+−+−+.

When TXMODE[1] = MID (open, TX modes 3, 4, and 5), the generation of this character sequence is an atomic (non-interruptible) operation. Once it has been successfully started, it cannot be stopped until all sixteen characters have been generated. The content of the associated Input Registers is ignored for the duration of this 16-character sequence. At the end of this sequence, if the TXCTx[1:0] = 11 condition is sampled again, the sequence restarts and remains uninterruptible for the following fifteen character clocks.

If parity checking is enabled, the character used to start the Word Sync Sequence must also have correct ODD parity. Once the sequence is started, parity is not checked on the following fifteen characters in the Word Sync Sequence.

When TXMODE[1] = HIGH (TX modes 6, 7, and 8), the generation of the Word Sync Sequence becomes an interruptible operation. In TX Mode 6, this sequence is started as soon as the TXCTx[1:0] = 11 condition is detected on a channel. In order for the sequence to continue on that channel, the TXCTx[1:0] inputs must be sampled as 00 for the remaining fifteen characters of the sequence.

If at any time a sample period exists where TXCTx[1:0] ≠ 00, the Word Sync Sequence is terminated, and a character representing the associated data and control bits is generated by the Encoder. This resets the Word Sync Sequence state machine such that it will start at the beginning of the sequence at the next occurrence of TXCTx[1:0] = 11.

When parity checking is enabled and TXMODE[1] = HIGH, all characters (including those in the middle of a Word Sync Sequence) must have correct parity. The detection of a character with incorrect parity during a Word Sync Sequence will interrupt that sequence and force generation of a C0.7 SVS character. Any interruption of the Word Sync Sequence causes the sequence to terminate.

When TXCKSEL = LOW, the Input Registers for all four transmit channels are clocked by REFCLK.[4] When TXCKSEL = HIGH, the Input Registers for all four transmit channels are clocked with TXCLKA↑. In these clock modes all four sets of TXCTx[1:0] inputs operate synchronous to the SCSEL input.[11]

TX Mode 4—Atomic Word Sync and SCSEL Control of Word Sync Sequence Generation

When configured in TX Mode 4, the SCSEL input is captured along with the associated TXCTx[1:0] data control inputs. These bits combine to control the interpretation of the TXDx[7:0] bits

Notes
10. LSB is shifted out first.
11. When operated in any configuration where receive channels are bonded together, TXCKSEL must be either LOW or HIGH (not MID) to ensure that associated characters are transmitted in the same character cycle.

and the characters generated by them. These bits are interpreted as listed in Table 6.

When TXCKSEL = MID, all transmit channels operate independently. In this mode, the SCSEL input is sampled only by TXCLKA↑. When the character accepted in the Channel-A Input Register has passed any selected validation and is ready to be passed to the Encoder, the level captured on SCSEL is passed to the Encoders of the remaining channels during this same cycle.

Table 6. TX Modes 4 and 7 Encoding

SCSEL	TXCTx[1]	TXCTx[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
0	1	1	Special character code
1	X	1	16-character Word Sync Sequence

Changing the state of SCSEL will change the relationship of the characters to other channels. SCSEL should either be used as a static configuration input, or changed only when the state of TXCTx[1:0] on the alternate channels are such that SCSEL is ignored during the change.

TX Mode 4 also supports an Word Sync Sequence. Unlike TX Mode 3, this sequence starts when SCSEL and TXCTx[0] are both high. With the exception of the combination of control bits used to initiate the sequence, the generation and operation of this Word Sync Sequence is the same as for TX Mode 3.

TX Mode 5—Atomic Word Sync generation without SCSEL.

When configured in TX Mode 5, the SCSEL signal is not used. In addition to the standard character encodings, two additional encoding mappings are controlled by the Channel Bonding selection made through the RXMODE[1:0] inputs. For non-bonded operation, the TXCTx[1:0] inputs for each channel control the characters generated by that channel. The specific characters generated by these bits are listed in Table 7.

Table 7. TX Modes 5 and 8 Encoding, Non-bonded (RXMODE[1] = LOW)

SCSEL	TXCTx[1]	TXCTx[0]	Characters Generated
X	0	0	Encoded data character
X	0	1	K28.5 fill character
X	1	0	Special character code
X	1	1	16-character Word Sync Sequence

TX Mode 5 also has the capability of generating an atomic Word Sync Sequence. For the sequence to be started, the TXCTx[1:0] inputs must both be sampled HIGH. The generation and operation of this Word Sync Sequence is the same as TX Mode 3Two additional encoding maps are provided for use when receive channel bonding is enabled. When dual-channel bonding is enabled (RXMODE[1] = MID), the CYP(V)15G0401DXB is configured such that channels A and B are bonded together to form a two-character-wide path, and channels C and D are bonded together to form a second two-character-wide path.

When operated in this two-channel bonded mode, the TXCTA[0] and TXCTB[0] inputs control the interpretation of the data on both the A and B channels, while the TXCTC[0] and TXCTD[0] inputs control the interpretation of the data on both the C and D channels. The characters on each half of these bonded channels are controlled by the associated TXCTx[1] bit. The specific characters generated by these control bit combinations are listed in Table 8.

Note especially that any time TXCTB[0] is sampled HIGH, both channels A and B start generating an atomic Word Sync Sequence, regardless of the state of any of the other bits in the A or B Input Registers. In a similar fashion, anytime TXCTD[0] is sampled HIGH, both the C and D channels start generation of an atomic Word Sync Sequence.

When RXMODE[1] = HIGH, the CYP(V)15G0401DXB is configured for quad-channel bonding, such that channels A, B, C, and D are bonded together to form a four-character-wide path. When operated in this mode, the TXCTA[0] and TXCTB[0] inputs control the interpretation of the data on all four channels. The characters generated on these bonded channels are controlled by the associated TXCTx[1] bit. The specific characters generated by these bits are listed in Table 9.

Unlike dual-channel bonded modes, when all four channels are bonded together, the TXCTC[0] and TXCTD[0] inputs are ignored.

Transmit BIST

Each transmit channel contains an internal pattern generator that can be used to validate both device and link operation. These generators are enabled by the associated BOE[x] signals listed in Table 10 (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to identical LFSR in the attached Receiver(s). If the receive channels are configured for common clock operation (RXCKSEL ≠ MID) and Encoder is enabled (TXMODE[1] ≠ LOW) each pass is preceded by a 16-character Word Sync Sequence to allow Elasticity Buffer alignment and management of clock- frequency variations.

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator in the associated transmit channel (or the BIST checker in the associated receive channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH to open the latch. A device reset (TRSTZ sampled LOW), presets the BIST Enable Latch to disable BIST on all channels.

Table 8. TX Modes 5 and 8, Dual-channel Bonded (RXMODE[1] = MID)

SCSEL	TXCTA[1]	TXCTA[0]	TXCTB[1]	TXCTB[0]	TXCTC[1]	TXCTC[0]	TXCTD[1]	TXCTD[0]	Characters Generated
X	0	0	X	0	X	X	X	X	Encoded data character on channel A
X	0	1	X	0	X	X	X	X	K28.5 fill character on channel A
X	1	0	X	0	X	X	X	X	Special character code on channel A
X	1	1	X	0	X	X	X	X	16-character word sync on channel A
X	X	0	0	0	X	X	X	X	Encoded data character on channel B
X	X	1	0	0	X	X	X	X	K28.5 fill character on channel B
X	X	0	1	0	X	X	X	X	Special character code on channel B
X	X	1	1	0	X	X	X	X	16-character word sync on channel B
X	X	X	X	1	X	X	X	X	16-character word sync on channels A and B
X	X	X	X	X	0	0	X	0	Encoded data character on channel C
X	X	X	X	X	0	1	X	0	K28.5 fill character on channel C
X	X	X	X	X	1	0	X	0	Special character code on channel C
X	X	X	X	X	1	1	X	0	16-character word sync on channel C
X	X	X	X	X	X	0	0	0	Encoded data character on channel D
X	X	X	X	X	X	1	0	0	K28.5 fill character on channel D
X	X	X	X	X	X	0	1	0	Special character code on channel D
X	X	X	X	X	X	1	1	0	16-character word sync on channel D
X	X	X	X	X	X	X	X	1	16-character word sync on channels C and D

Table 9. TX Modes 5 and 8, Quad-Channel Bonded (RXMODE[1] = HIGH)

SCSEL	TXCTA[1]	TXCTA[0]	TXCTB[1]	TXCTB[0]	TXCTC[1]	TXCTC[0]	TXCTD[1]	TXCTD[0]	Characters Generated
X	0	0	X	0	X	X	X	X	Encoded data character on channel A
X	0	1	X	0	X	X	X	X	K28.5 fill character on channel A
X	1	0	X	0	X	X	X	X	Special character code on channel A
X	1	1	X	0	X	X	X	X	16-character word sync on channel A
X	X	0	0	0	X	X	X	X	Encoded data character on channel B
X	X	1	0	0	X	X	X	X	K28.5 fill character on channel B
X	X	0	1	0	X	X	X	X	Special character code on channel B
X	X	1	1	0	X	X	X	X	16-character word sync on channel B
X	X	0	X	0	0	X	X	X	Encoded data character on channel C
X	X	1	X	0	0	X	X	X	K28.5 fill character on channel C
X	X	0	X	0	1	X	X	X	Special character code on channel C
X	X	1	X	0	1	X	X	X	16-character word sync on channel C
X	X	0	X	0	X	X	0	X	Encoded data character on channel D
X	X	1	X	0	X	X	0	X	K28.5 fill character on channel D
X	X	0	X	0	X	X	1	X	Special character code on channel D
X	X	1	X	0	X	X	1	X	16-character word sync on channel D
X	X	X	X	1	X	X	X	X	16-character word sync on channels A, B, C, and D

All data and data-control information present at the associated TXDx[7:0] and TXCTx[1:0] inputs are ignored when BIST is active on that channel.

Serial Output Drivers

The serial interface Output Drivers use high-performance differential CML (Current Mode Logic) to provide source-matched drivers for the transmission lines. These Serial Drivers accept data from the Transmit Shifters. These outputs have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

When configured for local loopback (LPEN = HIGH), all enabled Serial Drivers are configured to drive a static differential logic-1.

Each Serial Driver can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the OELE latch-enable signal. When OELE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Serial Output Enable Latch to control the Serial Driver. The BOE[7:0] input associated with a specific OUTxy± driver is listed in Table 10. When OELE is HIGH and BOE[x] is HIGH, the associated Serial Driver is enabled. When OELE is HIGH and BOE[x] is LOW, the associated Serial Driver is disabled and internally powered down. If both Serial Drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch, and remain there until OELE returns HIGH to enable the latch. A device reset ($\overline{\text{TRSTZ}}$ sampled LOW) clears this latch and disables all Serial Drivers.

Table 10. Output Enable, BIST, and Receive Channel Enable Signal Map

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BOE[7]	OUTD2±	Transmit D	X
BOE[6]	OUTD1±	Receive D	Receive D
BOE[5]	OUTC2±	Transmit C	X
BOE[4]	OUTC1±	Receive C	Receive C
BOE[3]	OUTB2±	Transmit B	X
BOE[2]	OUTB1±	Receive B	Receive B
BOE[1]	OUTA2±	Transmit A	X
BOE[0]	OUTA1±	Receive A	Receive A

Note When all transmit channels are disabled (i.e., both outputs disabled in all channels) and a channel is re-enabled, the data on the Serial Drivers may not meet all timing specifications for up to 200 µs.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiples that clock by 10 or 20 (as selected by TXRATE) to generate a bit-rate clock for use by the Transmit Shifter. It also provides a character-rate clock used by the transmit paths.

This clock multiplier PLL can accept a REFCLK input between 20 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYP(V)15G0401DXB clock multiplier (controlled by TXRATE) and by the level on the SPDSEL input.

When TXRATE = HIGH (Half-rate REFCLK), TXCKSEL = HIGH or MID (TXCLKx or TXCLKA selected to clock input register) is an invalid mode of operation.

SPDSEL is a static three-level select [5] (ternary) input that selects one of three operating ranges for the serial data outputs and inputs. The operating serial signaling-rate and allowable range of REFCLK frequencies are listed in Table 11.

Table 11. Operating Speed Settings

SPDSEL	TXRATE	REFCLK Frequency (MHz)	Signaling Rate (MBaud)
LOW	1	reserved	195–400
	0	19.5–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

The REFCLK± input is a differential input with each input internally biased to 1.4 V. If the REFCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, REFCLK– can be left floating and the input signal is recognized when it passes through the internally biased reference point.

When both the REFCLK+ and REFCLK– inputs are connected, the clock source must be a differential clock. This can be either a differential LVPECL clock that is DC- or AC-coupled, or a differential LVTTL or LVCMOS clock.

By connecting the REFCLK– input to an external voltage source or resistive voltage divider, it is possible to adjust the reference point of the REFCLK+ input for alternate logic levels. When doing so, it is necessary to ensure that the input differential crossing point remains within the parametric range supported by the input.

CYP(V)15G0401DXB Receive Data Path

Serial Line Receivers

Two differential Line Receivers, INx1± and INx2±, are available on each channel for accepting serial data streams. The active Serial Line Receiver on a channel is selected using the associated INSELx input. The Serial Line Receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least VI_{DIFF} > 100 mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3 V powered fiber-optic interface modules (any ECL/PECL family, not limited to 100K PECL) or AC-coupled to +5 V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

The local loopback input (LPEN) allows the serial transmit data to be routed internally back to the Clock and Data Recovery circuit associated with each channel. When configured for local

loopback, all transmit Serial Driver outputs are forced to output a differential logic-1. This prevents local diagnostic patterns from being broadcast to attached remote receivers.

Signal Detect/Link Fault

Each selected Line Receiver (i.e., that routed to the clock and data recovery PLL) is simultaneously monitored for

- Analog amplitude above limit specified by SDASEL
- Transition density greater than specified limit
- Range controller reports the received data stream within normal frequency range (±1500 ppm)[12]
- Receive channel enabled

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFIx (Link Fault Indicator) output associated with each receive channel.

Table 12. Analog Amplitude Detect Valid Signal Levels[13]

SDASEL	Typical signal with peak amplitudes above
LOW	140 mV p-p differential
MID (Open)	280 mV p-p differential
HIGH	420 mV p-p differential

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable. This allows operation with highly attenuated signals, or in high-noise environments. This adjustment is made through the SDASEL signal, a three-level select[5] input, which sets the trip point for the detection of a valid signal at one of three levels, as listed in Table 12. This control input affects the analog monitors for all receive channels.

The Analog Signal Detect Monitors are active for the Line Receiver selected by the associated INSELx input. When the channel is configured for local loopback (LPEN = HIGH), no line receivers are selected, and the LFIx output for each channel reports only the receive VCO frequency out-of-range and transition density status of the associated transmit signal. When local loopback is active, the Analog Signal Detect Monitors are disabled.

Transition Density

The Transition Detection logic checks for the absence of any transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received on a channel, the Transition Detection logic for that channel will assert LFIx. The LFIx output remains asserted until at least one transition is detected in each of three adjacent received characters.

Range Controls

The Clock/Data Recovery (CDR) circuit includes logic to monitor the frequency of the Phase Locked Loop (PLL) Voltage Controlled Oscillator (VCO) used to sample the incoming data stream. This logic ensures that the VCO operates at, or near the rate of the incoming data stream for two primary cases:

- when the incoming data stream resumes after a time in which it has been “missing”
- when the incoming data stream is outside the acceptable frequency range

To perform this function, the frequency of the VCO is periodically sampled and compared to the frequency of the REFCLK input. If the VCO is running at a frequency beyond ±1500 ppm [12] as defined by the reference clock frequency, it is periodically forced to the correct frequency (as defined by REFCLK, SPDSEL, and TXRATE) and then released in an attempt to lock to the input data stream. The sampling and relock period of the Range Control is calculated as follows: RANGE CONTROL SAMPLING PERIOD = (REFCLKPERIOD) * (16000).

During the time that the Range Control forces the PLL VCO to run at REFCLK*10 (or REFCLK*20 when TXRATE = HIGH) rate, the LFIx output will be asserted LOW. While the PLL is attempting to re-lock to the incoming data stream, LFIx may be either HIGH or LOW (depending on other factors such as transition density and amplitude detection) and the recovered byte clock (RXCLKx) may run at an incorrect rate (depending on the quality or existence of the input serial data stream). After a valid serial data stream is applied, it may take up to one RANGE CONTROL SAMPLING PERIOD before the PLL locks to the input data stream, after which LFIx should be HIGH.

Receive Channel Enabled

The CYP(V)15G0401DXB contains four receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the RXLE latch-enable signal. When RXLE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Receive Channel Enable Latch to control the PLLs and logic of the associated receive channel. The BOE[7:0] input associated with a specific receive channel is listed in Table 10.

When RXLE is HIGH and BOE[x] is HIGH, the associated receive channel is enabled to receive and recover a serial stream. When RXLE is HIGH and BOE[x] is LOW, the associated receive channel is disabled and powered down. If a single channel of a bonded-pair or bonded-quad is disabled, the other receive channels may not bond correctly. If the disabled channel is selected as the master channel for insert/delete or recovered clock select, these functions will not work correctly. Any disabled channel indicates an asserted LFIx output. When RXLE returns LOW, the values present on the BOE[7:0] inputs are latched in the Receive Channel Enable Latch, and remain there until RXLE returns HIGH to open the latch again.[14]

Notes

12. REFCLK has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±1500 PPM (±0.15%) of the remote transmitter’s PLL reference (REFCLK) frequency. Although transmitting to a HOTLink II receiver necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500-PPM, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard. For example, to be IEEE 802.3z Gigabit Ethernet compliant, the frequency stability of the crystal needs to be within ±100 PPM.
13. The peak amplitudes listed in this table are for typical waveforms that have generally 3 – 4 transitions for every ten bits. In a worse case environment the signals may have a sign-wave appearance (highest transition density with repeating 0101...). Signal peak amplitudes levels within this environment type could increase the values in the table above by approximately 100 mV.
14. When a disabled receive channel is re-enabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 2 ms.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate Clock/Data Recovery (CDR) block within each receive channel. The clock extraction function is performed by embedded phase-locked loops (PLLs) that track the frequency of the transitions in the incoming bit streams and align the phase of their internal bit-rate clocks to the transitions in the selected serial data streams.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) reference clock from the REFCLK input. This REFCLK input is used to

- ensure that the VCO (within the CDR) is operating at the correct frequency.
- to reduce PLL acquisition time
- and to limit unlocked frequency excursions of the CDR VCO when there is no input data present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits of the range control monitor, the CDR will switch to track REFCLK instead of the data stream. Once the CDR output (RXCLKx) frequency returns back close to REFCLK frequency, the CDR input will be switched back to track the input data stream. In case no data is present at the input this switching behavior may result in brief RXCLKx frequency excursions from REFCLK. However, the validity of the input data stream is indicated by the LFIx output. The frequency of REFCLK is required to be within ±1500 ppm[12] of the frequency of the clock that drives the REFCLK input of the remote transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the $\overline{\text{LFIx}}$ output can be used to select an alternate data stream. When an LFIx indication is detected, external logic can toggle selection of the associated INx1± and INx2± inputs through the associated INSELx input. When a port switch takes place, it is necessary for the receive PLL for that channel to reacquire the new serial stream and frame to the incoming character boundaries. If channel bonding is also enabled, a channel alignment event is also required before the output data may be considered usable.

Deserializer/Framer

Each CDR circuit extracts bits from the associated serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream, looking for one or more Comma or K28.5 characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

Framing Character

The CYP(V)15G0401DXB allows selection of two combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input.

The specific bit combinations of these framing characters are listed in Table 13. When the specific bit combination of the selected framing character is detected by the Framer, the boundaries of the characters present in the received data stream are known.

Table 13. Framing Character Selector

FRAMCHAR	Bits Detected in Framer	
	Character Name	Bits Detected
LOW	Reserved for test	
MID (Open)	Comma+ or Comma–	00111110XX [15] or 11000001XX
HIGH	–K28.5 or +K28.5	0011111010 or 1100000101

Framer

The Framer on each channel operates in one of three different modes, as selected by the RFMODE input. In addition, the Framer itself may be enabled or disabled through the RFEN input. When RFEN = LOW, the framers in all four receive paths are disabled, and no combination of bits in a received data stream will alter the character boundaries. When RFEN = HIGH, the Framer selected by RFMODE is enabled on all four channels.

When RFMODE = LOW, the Low-Latency Framer is selected[16]. This Framer operates by stretching the recovered character clock until it aligns with the received character boundaries. In this mode, the Framer starts its alignment process on the first detection of the selected framing character. To reduce the impact on external circuits that make use of a recovered clock, the clock period is not stretched by more than two bit-periods in any one clock cycle. When operated with a character-rate output clock (RXRATE = LOW), the output of properly framed characters may be delayed by up to nine character-clock cycles from the detection of the selected framing character. When operated with a half-character-rate output clock (RXRATE = HIGH), the output of properly framed characters may be delayed by up to fourteen character-clock cycles from the detection of the selected framing character.

When RFMODE = MID (open), the Cypress-mode Multi-Byte Framer is selected. The required detection of multiple framing characters makes the associated link much more robust to incorrect framing due to aliased framing characters in the data stream. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock does not contain any significant phase changes or hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other external circuits or components using PLL-based clock distribution elements. In this framing mode, the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

Notes
15. The standard definition of a Comma contains only seven bits. However, since all valid Comma characters within the 8B/10B character set also have the eighth bit as an inversion of the seventh bit, the compare pattern is extended to a full eight bits to reduce the possibility of a framing error.
16. When Receive BIST is enabled on a channel, the Low-Latency Framer must not be enabled. The BIST sequence contains an aliased K28.5 framing character, which would cause the Receiver to update its character boundaries incorrectly.

When RFMODE = HIGH, the Alternate-mode Multi-Byte Framer is enabled. Like the Cypress-mode Multi-Byte Framer, multiple framing characters must be detected before the character boundary is adjusted. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, on identical 10-bit boundaries, before character framing is adjusted.

Framing for all channels is enabled when RFEN = HIGH. If RFEN = LOW, the Framer for each channel is disabled. When the framers are disabled, no changes are made to the recovered character boundaries on any channel, regardless of the presence of framing characters in the data stream.

10B/8B Decoder Block

The Decoder logic block performs three primary functions:

- decoding the received transmission characters back into Data and Special Character codes
- comparing generated BIST patterns with received characters to permit at-speed link and device testing
- generation of ODD parity on the decoded characters.

10B/8B Decoder

The framed parallel output of each Deserializer Shifter is passed to the 10B/8B Decoder where, if the Decoder is enabled (DECMODE ≠ LOW), it is transformed from a 10-bit transmission character back to the original Data and Special Character codes. This block uses the 10B/8B Decoder patterns in Table 26 and Table 27 of this data sheet. Valid data characters are indicated by a 000b bit-combination on the associated RXSTx[2:0] status bits, and Special Character codes are indicated by a 001b bit-combination on these same status outputs. Framing characters, invalid patterns, disparity errors, and synchronization status are presented as alternate combinations of these status bits.

The 10B/8B Decoder operates in two normal modes, and can also be bypassed. The operating mode for the Decoder is controlled by the DECMODE input.

When DECMODE = LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. In this mode, channel bonding is not possible, the Receive Elasticity Buffers are bypassed, and RXCKSEL must be MID. This clock mode generates separate RXCLKx± outputs for each receive channel.

When DECMODE = MID (or open), the 10-bit transmission characters are decoded using Table 26 and Table 27. Received Special Code characters are decoded using the Cypress column of Table 27.

When DECMODE = HIGH, the 10-bit transmission characters are decoded using Table 26 and Table 27. Received Special Code characters are decoded using the Alternate column of Table 27.

In all settings where the Decoder is enabled, the receive paths may be operated as separate channels or bonded to form various multi-channel buses.

Receive BIST Operation

The Receiver interfaces contain internal pattern generators that can be used to validate both device and link operation. These generators are enabled by the associated BOE[x] signals listed in Table 10 (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated receive channel becomes a pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo- random sequence that can be matched to an identical LFSR in the attached Transmitter(s). If the receive channels are configured for common clock operation (RXCKSEL ≠ MID) each pass is preceded by a 16-character Word Sync Sequence. When synchronized with the received data stream, the associated Receiver checks each character in the Decoder with each character generated by the LFSR and indicates compare errors and BIST status at the RXSTx[2:0] bits of the Output Register. See Table 22 for details.

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator/checker in the associated Receive channel (or the BIST generator in the associated Transmit channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH. All captured signals in the BIST Enable Latch are set HIGH (i.e., BIST is disabled) following a device reset ($\overline{\text{TRSTZ}}$ is sampled LOW).

When BIST is first recognized as being enabled in the Receiver, the LFSR is preset to the BIST-loop start-code of D0.0. This D0.0 character is sent only once per BIST loop. The status of the BIST progress and any character mismatches is presented on the RXSTx[2:0] status outputs.

Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXSTx[2:0] indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress. These same status values are presented when the Decoder is bypassed and BIST is enabled on a receive channel.

The status reported on RXSTx[2:0] by the BIST state machine are listed in Table 22. When Receive BIST is enabled, the same status is reported on the receive status outputs regardless of the state of DECMODE.

The specific patterns checked by each receiver are described in detail in the Cypress application note “HOTLink Built-In Self-Test.” The sequence compared by the CYP(V)15G0401DXB when RXCKSEL = MID is identical to that in the CY7B933 and CY7C924DX, allowing interoperable systems to be built when used at compatible serial signaling rates.

If the number of invalid characters received ever exceeds the number of valid characters by sixteen, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

When the receive paths are configured for common clock operation (RXCKSEL ≠ MID), each pass must be preceded by a 16-character Word Sync Sequence to allow output buffer alignment and management of clock frequency variations. This