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CYP15G0101DXB
CYV15G0101DXB
CYW15G0101DXB

Single-channel HOTLink II™ Transceiver

Features

- Second-generation HOTLink® technology
- Compliant to multiple standards
  - ESCON®, DVB-ASI, Fibre Channel and Gigabit Ethernet (IEEE802.3z)
  - CPRI™ compliant
  - CYW15G0101DXB compliant to OBSAI-RP3
  - CYV15G0101DXB compliant to SMPTE 259M and SMPTE 292M
  - 8B/10B encoded or 10-bit unencoded data
- Single-channel transceiver operates from 195 to 1500 MBaud serial data rate
  - CYW15G0101DXB operates from 195 to 1540 MBaud
- Selectable parity check/generate
- Selectable input clocking options
- Selectable output clocking options
- MultiFrame™ Receive Framer
  - Bit and Byte alignment
  - Comma or full K28.5 detect
  - Single- or Multi-Byte framer for byte alignment
  - Low-latency option
- Synchronous LVTTL parallel input and parallel output interface
- Internal phase-locked loops (PLLs) with no external PLL components
- Dual differential PECL-compatible serial inputs
  - Internal DC-restoration
- Dual differential PECL-compatible serial outputs
  - Source matched for driving 50Ω transmission lines
  - No external bias resistors required
  - Signaling-rate controlled edge-rates
- Optional Elasticity Buffer in Receive Path
- Optional Phase Align Buffer in Transmit Path
- Compatible with
  - Fiber-optic modules
  - Copper cables
  - Circuit board traces
- JTAG boundary scan
- Built-In Self-Test (BIST) for at-speed link testing
- Per-channel Link Quality Indicator
  - Analog signal detect
  - Digital signal detect
- Low power 1.25W @ 3.3V typical
- Single 3.3V supply
- 100-ball BGA
- Pb-Free package option available
- 0.25µ BiCMOS technology

Functional Description

The CYP(V)15G0101DXB[1] single-channel HOTLink II™ transceiver is a point-to-point communications building block allowing the transfer of data over a high-speed serial link (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 195 to 1500 MBaud.

The transmit channel accepts parallel characters in an Input Register, encodes each character for transport, and converts it to serial data. The receive channel accepts serial data and converts it to parallel data, frames the data to character boundaries, decodes the framed characters into data and special characters, and presents these characters to an Output Register. *Figure 1* illustrates typical connections between independent host systems and corresponding CYP(V)(W)15G0101DXB parts. As a second-generation HOTLink device, the CYP(V)(W)15G0101DXB extends the HOTLink II family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data, command, and BIST) with other HOTLink devices.

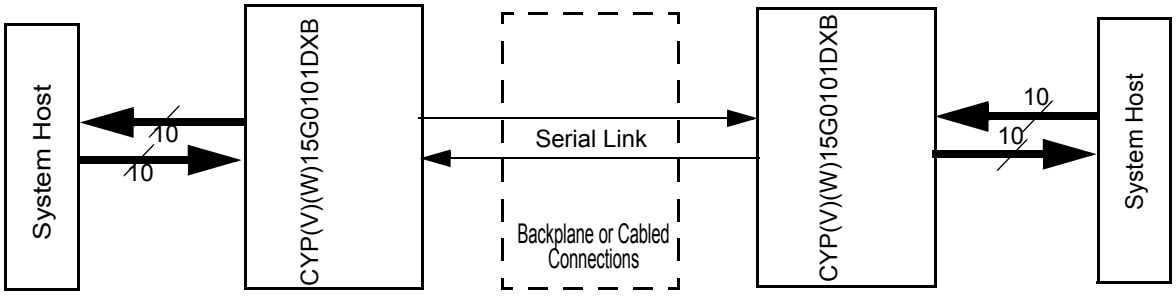


Figure 1. HOTLink II System Connections

Note:

1. CYV15G0101DXB refers to SMPTE 259M and SMPTE 292M compliant devices. CYW15G0101DXB refers to OBSAI RP3 compliant devices (maximum operating data rate is 1540 MBaud). CYP15G0101DXB refers to devices not compliant to SMPTE 259M and SMPTE 292M pathological test requirements and also OBSAI RP3 operating datarate of 1536 MBaud. CYP(V)(W)15G0101DXB refers to all three devices.

The CYW15G0101DXB[1] operates from 195 to 1540 MBaud, which includes operation at the OBSAI RP3 datarate of both 1536 MBaud and 768 MBaud.

The CYV15G0101DXB satisfies the SMPTE 259M and SMPTE 292M compliance as per the EG34-1999 Pathological Test Requirements. The transmit (TX) section of the CYP(V)(W)15G0101DXB single-channel HOTLink II consists of a byte-wide channel. The channel can accept either eight-bit data characters or pre-encoded 10-bit transmission characters. Data characters are passed from the Transmit Input Register to an embedded 8B/10B Encoder to improve their serial transmission characteristics. These encoded characters are then serialized and output from dual Positive ECL (PECL)-compatible differential transmission-line drivers at a bit-rate of either 10 or 20 times the input reference clock.

The receive (RX) section of the CYP(V)(W)15G0101DXB Single-channel HOTLink II consists of a byte-wide channel. The channel accepts a serial bit-stream from one of two PECL-compatible differential Line Receivers and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. The recovered bit-stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are then written to an internal Elasticity Buffer, and presented to the destination host system. The integrated 8B/10B Encoder/Decoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface.

The parallel I/O interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. In addition to clocking the transmit path interfaces from one or multiple sources, the receive interface may be configured to present data relative to a recovered clock or to a local reference clock.

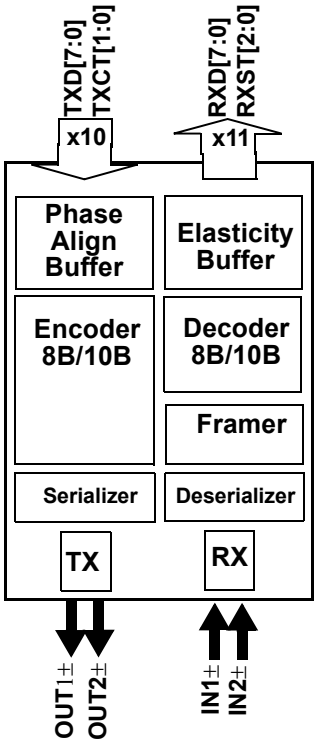
The transmit and the receive channels contain BIST pattern generators and checkers, respectively. This BIST hardware allows at-speed testing of the high-speed serial data paths in both transmit and receive sections, as well as across the inter-connecting links.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting backplanes on switches, routers, base-stations, servers and video transmission systems.

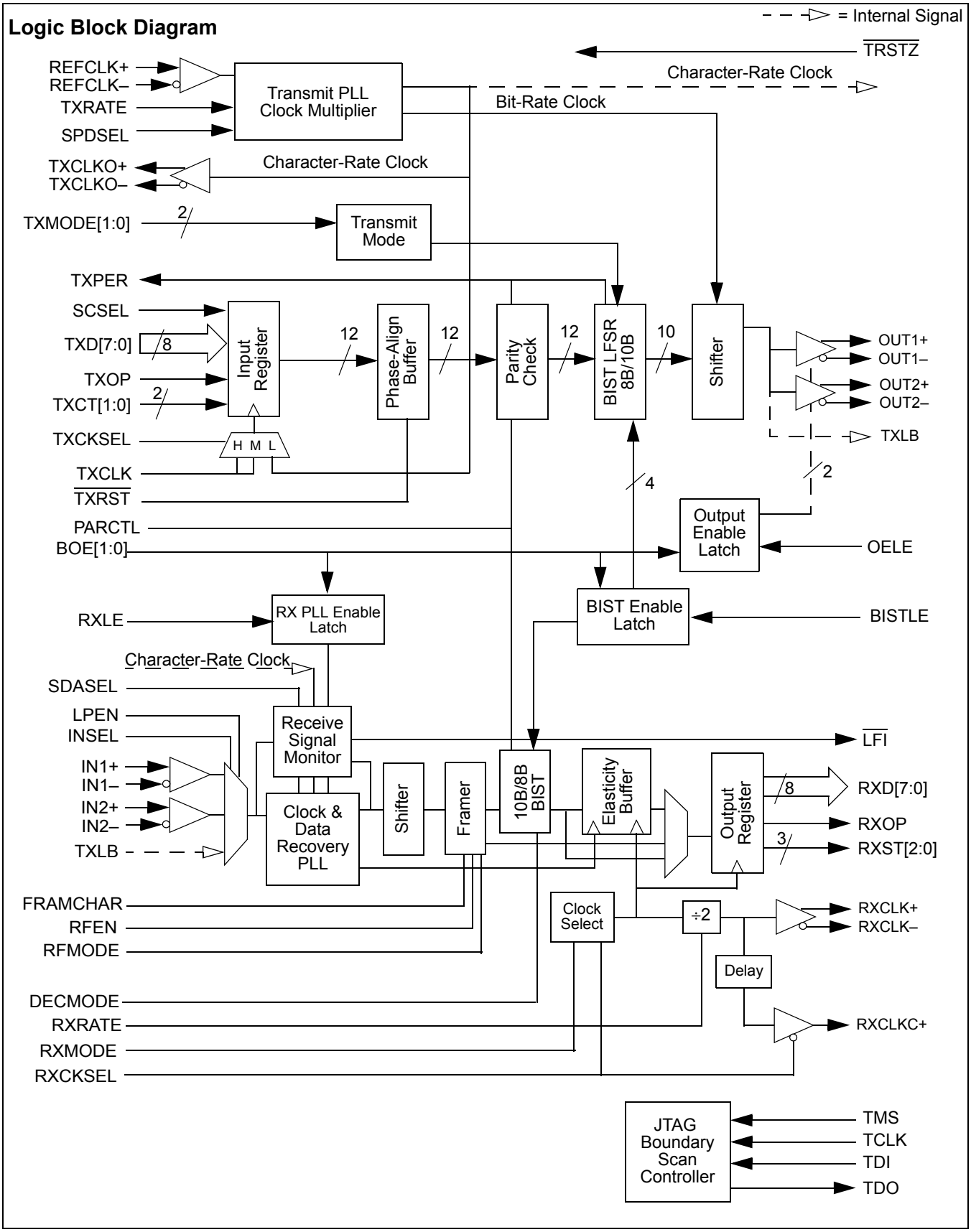
The CYV15G0101DXB is verified by testing to be compliant to all the pathological test patterns documented in SMPTE EG34-1999, for both the SMPTE 259M and 292M signaling rates. The tests ensure that the receiver recovers data with no errors for the following patterns:

1. Repetitions of 20 ones and 20 zeros.
2. Single burst of 44 ones or 44 zeros.
3. Repetitions of 19 ones followed by 1 zero or 19 zeros followed by 1 one.

Transceiver Logic Block Diagram



Logic Block Diagram



Pin Configuration

Top View

	1	2	3	4	5	6	7	8	9	10
A	V_{CC}	IN2+	V_{CC}	OUT2–	RXMODE	TXMODE[1]	IN1+	V_{CC}	OUT1–	V_{CC}
B	V_{CC}	IN2–	TDO	OUT2+	TXRATE	TXMODE[0]	IN1–	#NC[2]	OUT1+	V_{CC}
C	RFEN	LPEN	RXLE	RXCLKC+	RXRATE	SDASEL	SPDSEL	PARCTL	RFMODE	INSEL
D	BOE[0]	BOE[1]	FRAMCHAR	GND	GND	GND	GND	TMS	$\overline{\text{TRSTZ}}$	TDI
E	BISTLE	DECMODE	OELE	GND	GND	GND	GND	TCLK	RXCKSEL	TXCKSEL
F	RXST[2]	RXST[1]	RXST[0]	GND	GND	GND	GND	TXPER	REFCLK–	REFCLK+
G	RXOP	RXD[1]	RXD[5]	GND	GND	GND	GND	TXOP	TXCLKO+	TXCLKO–
H	RXD[0]	RXD[2]	RXD[6]	$\overline{\text{LFI}}$	TXCT[1]	TXD[6]	TXD[3]	TXCLK	$\overline{\text{TXRST}}$	#NC[2]
J	V_{CC}	RXD[3]	RXD[7]	RXCLK–	TXCT[0]	TXD[5]	TXD[2]	TXD[0]	#NC[2]	V_{CC}
K	V_{CC}	RXD[4]	V_{CC}	RXCLK+	TXD[7]	TXD[4]	TXD[1]	V_{CC}	SCSEL	V_{CC}

Bottom View

10	9	8	7	6	5	4	3	2	1	
V_{CC}	OUT1–	V_{CC}	IN1+	TXMODE[1]	RXMODE	OUT2–	V_{CC}	IN2+	V_{CC}	A
V_{CC}	OUT1+	#NC[2]	IN1–	TXMODE[0]	TXRATE	OUT2+	TDO	IN2–	V_{CC}	B
INSEL	RFMODE	PARCTL	SPDSEL	SDASEL	RXRATE	RXCLKC+	RXLE	LPEN	RFEN	C
TDI	$\overline{\text{TRSTZ}}$	TMS	GND	GND	GND	GND	FRAMCHAR	BOE[1]	BOE[0]	D
TXCKSEL	RXCKSEL	TCLK	GND	GND	GND	GND	OELE	DECMODE	BISTLE	E
REFCLK+	REFCLK–	TXPER	GND	GND	GND	GND	RXST[0]	RXST[1]	RXST[2]	F
TXCLKO–	TXCLKO+	TXOP	GND	GND	GND	GND	RXD[5]	RXD[1]	RXOP	G
#NC[2]	$\overline{\text{TXRST}}$	TXCLK	TXD[3]	TXD[6]	TXCT[1]	LFI	RXD[6]	RXD[2]	RXD[0]	H
V_{CC}	#NC[2]	TXD[0]	TXD[2]	TXD[5]	TXCT[0]	RXCLK–	RXD[7]	RXD[3]	V_{CC}	J
V_{CC}	SCSEL	V_{CC}	TXD[1]	TXD[4]	TXD[7]	RXCLK+	V_{CC}	RXD[4]	V_{CC}	K

Note:
2. #NC = Do Not Connect.

Pin Descriptions CYP(V)(W)15G0101DXB Single-channel HOTLink II

Pin Name	I/O Characteristics	Signal Description
Transmit Path Data Signals		
TXPER	LVTTL Output, changes relative to REFCLK↑[3]	**Transmit Path Parity Error**. Active HIGH. Asserted (HIGH) if parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected at the Encoder. This output is HIGH for one transmit character-clock period to indicate detection of a parity error in the character presented to the Encoder. If a parity error is detected, the character in error is replaced with a C0.7 character to force a corresponding bad-character detection at the remote end of the link. This replacement takes place regardless of the encoded/un-encoded state of the interface. When BIST is enabled for the specific transmit channel, BIST progress is presented on this output. Once every 511 character times (plus a 16-character Word Sync Sequence when the receive channel is clocked by REFCLK, i.e., RXCKSEL = LOW), the TXPER signal pulses HIGH for one transmit-character clock period (if RXCKSEL = MID) or seventeen transmit-character clock periods (if RXCKSEL = LOW or HIGH) to indicate a complete pass through the BIST sequence. For RXCKSEL = LOW or HIGH, If TXMODE[1:0] = LL, then no Word Sync Sequence is sent in BIST, and TXPER pulses HIGH for one transmit-character clock period. This output also provides an indication of a Phase-Align Buffer underflow/overflow condition. When the Phase-Align Buffer is enabled (TXCKSEL ≠ LOW, or TXCKSEL = LOW and TXRATE = HIGH), and an underflow/overflow condition is detected, TXPER is asserted and remains asserted until either an atomic Word Sync Sequence is transmitted or $\overline{\text{TXRST}}$ is sampled LOW to recenter the Phase-Align Buffer.
TXCT[1:0]	LVTTL Input, synchronous, sampled by TXCLK↑ or REFCLK↑[3]	**Transmit Control**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL, and are passed to the Encoder or Transmit Shifter. They identify how the TXD[7:0] characters are interpreted. When the Encoder is enabled, these inputs determine if the TXD[7:0] character is encoded as Data, a Special Character code, a K28.5 fill character or a Word Sync Sequence. When the Encoder is bypassed, these inputs are interpreted as data bits. See *Table 1* for details.
TXD[7:0]	LVTTL Input, synchronous, sampled by TXCLK↑ or REFCLK↑[3]	**Transmit Data Inputs**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL, and passed to the Encoder or Transmit Shifter. When the Encoder is enabled (TXMODE[1] ≠ LOW), TXD[7:0] specify the specific data or command character to be sent. When the Encoder is bypassed, these inputs are interpreted as data bits of the 10-bit input character. See *Table 1* for details.
TXOP	LVTTL Input, synchronous, internal pull-up, sampled by TXCLK↑ or REFCLK↑[3]	**Transmit Path Odd Parity**. When parity checking is enabled (PARCTL ≠ LOW), the parity captured at this input is XORed with the data on the TXD bus (and sometimes TXCT[1:0]) to verify the integrity of the captured character. See *Table 2* for details.
SCSEL	LVTTL Input, synchronous, internal pull-down, sampled by TXCLK↑ or REFCLK↑[3]	**Special Character Select**. Used in some transmit modes along with TXCTx[1:0] to encode special characters or to initiate a Word Sync Sequence. When the transmit path is configured to select TXCLK to clock the input register (TXCKSEL = MID or HIGH), SCSEL is captured relative to TXCLK↑.

Note:
3. When REFCLK is configured for half-rate operation (TXRATE = HIGH), this input is sampled (or the outputs change) relative to both the rising and falling edges of REFCLK.

Pin Descriptions CYP(V)(W)15G0101DXB Single-channel HOTLink II (continued)

Pin Name	I/O Characteristics	Signal Description
$\overline{\text{TXRST}}$	LVTTL Input, asynchronous, internal pull-up, sampled by REFCLK↑[3]	**Transmit Clock Phase Reset**. Active LOW. When sampled LOW, the transmit Phase-align Buffer is allowed to adjust its data-transfer timing (relative to the selected input clock) to allow clean transfer of data from the Input Register to the Encoder or Transmit Shifter. When $\overline{\text{TXRST}}$ is sampled HIGH, the internal phase relationship between the TXCLK and the internal character-rate clock is fixed and the device operates normally. When configured for half-rate REFCLK sampling of the transmit character stream (TXCKSEL = LOW and TXRATE = HIGH), assertion of $\overline{\text{TXRST}}$ is only used to clear Phase-align buffer faults caused by highly asymmetric reference clock periods or reference clocks with excessive cycle-to-cycle jitter. During this alignment period, one or more characters may be added to or lost from all the associated transmit paths as the transmit Phase-align Buffers are adjusted. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive rising edges of REFCLK to ensure the reset operation is initiated correctly on all channels. This input is ignored when both TXCKSEL and TXRATE are LOW, since the phase align buffer is bypassed. In all other configurations, $\overline{\text{TXRST}}$ should be asserted during device initialization to ensure proper operation of the Phase-align buffer. $\overline{\text{TXRST}}$ should be asserted after the assertion and deassertion of $\overline{\text{TRSTZ}}$, after the presence of a valid TXCLK and after allowing enough time for the TXPLL to lock to the reference clock (as specified by parameter t_{TXLOCK}).
Transmit Path Clock and Clock Control		
TXCKSEL	3-Level Select static control input[4]	**Transmit Clock Select**. Selects the clock source used to write data into the Transmit Input Register of the transmit channel. When LOW, the Input Register is clocked by REFCLK↑.[3] When HIGH or MID, TXCLK↑ is the Input Register clock for TXD[7:0] and TXCT[1:0]. When TXRATE=HIGH, configuring TXCKSEL = HIGH or MID is an invalid mode of operation.
TXCLKO±	LVTTL Output	**Transmit Clock Output**. This true and complement output clock is synthesized by the transmit PLL and is synchronous to the internal transmit character clock. It has the same frequency as REFCLK (when TXRATE = LOW), or twice the frequency of REFCLK (when TXRATE = HIGH). This output clock has no direct phase relationship to REFCLK.
TXRATE	LVTTL Input, Static Control input, internal pull-down	**Transmit PLL Clock Rate Select**. When TXRATE = HIGH, the Transmit PLL multiplies REFCLK by 20 to generate the serial bit-rate clock. When TXRATE = LOW, the transmit PLL multiplies REFCLK by 10 to generate the serial bit-rate clock. See *Table 9* for a list of operating serial rates. When REFCLK is selected to clock the receive parallel interfaces (RXCKSEL = LOW), the TXRATE input also determines if the clocks on the RXCLK± and RXCLKC+ outputs are full or half-rate. When TXRATE = HIGH (REFCLK is half-rate), the RXCLK± and RXCLKC+ output clocks are also half-rate clocks and follow the frequency and duty cycle of the REFCLK input. When TXRATE = LOW (REFCLK is full-rate), the RXCLK± and RXCLKC+ output clocks are also full-rate clocks and follow the frequency and duty cycle of the REFCLK input. When TXRATE=HIGH, configuring TXCKSEL = HIGH or MID is an invalid mode of operation.
TXCLK	LVTTL Clock Input, internal pull-down	**Transmit Path Input Clock**. This clock must be frequency-coherent to TXCLKO±, but may be offset in phase. The internal operating phase of the input clock (relative to REFLCK or TXCLKO+) is adjusted when $\overline{\text{TXRST}}$ = LOW and locked when $\overline{\text{TXRST}}$ = HIGH.
Transmit Path Mode Control		
TXMODE[1:0]	3-Level Select[4] static control inputs	**Transmit Operating Mode**. These inputs are interpreted to select one of nine operating modes of the transmit path. See *Table 3* for a list of operating modes.

Note:

4. 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC} (power). When not connected or allowed to float, a 3-Level select input will self-bias to the MID level.

Pin Descriptions CYP(V)(W)15G0101DXB Single-channel HOTLink II (continued)

Pin Name	I/O Characteristics	Signal Description
Receive Path Data Signals		
RXD[7:0]	LVTTL Output, synchronous to the RXCLK↑ output (or REFCLK↑ input[3] when RXCKSEL = LOW)	**Parallel Data Output**. These outputs change following the rising edge of the selected receive interface clock. When the Decoder is enabled (DECMODE = HIGH or MID), these outputs represent either received data or a special character. The status of the received data is represented by the values of RXST[2:0]. When the Decoder is bypassed (DECMODE = LOW), RXD[7:0] become the higher order bits of the 10-bit received character. See *Table 13* for details.
RXST[2:0]	LVTTL Output, synchronous to the RXCLK↑ output (or REFCLK↑ input[3] when RXCKSEL = LOW)	**Parallel Status Output**. These outputs change following the rising edge of the selected receive interface clock. When the Decoder is bypassed (DECMODE = LOW), RXST[1:0] become the two low-order bits of the 10-bit received character, while RXST[2] = HIGH indicates the presence of a Comma character in the Output Register. When the Decoder is enabled (DECMODE = HIGH or MID), RXST[2:0] provide status of the received signal. See *Table 16* for a list of Receive Character status.
RXOP	3-state, LVTTL Output, synchronous to the RXCLK↑ output (or REFCLK↑ input[3] when RXCKSEL = LOW)	**Receive Path Odd Parity.** When parity generation is enabled (PARCTL ≠ LOW), the parity output is valid for the data on the RXD bus bits. When parity generation is disabled (PARCTL = LOW), this output driver is disabled (High-Z).
Receive Path Clock and Clock Control		
RXCLK±	3-state, LVTTL Output clock	**Receive Character Clock Output**. When configured such that the output data path is clocked by the recovered clock (RXCKSEL = MID), these true and complement clocks are the receive interface clocks which are used to control timing of output data (RXD[7:0], RXST[2:0] and RXOP). This clock is output continuously at either the dual-character rate ($1/20^{th}$ the serial bit-rate) or character rate ($1/10^{th}$ the serial bit-rate) of the data being received, as selected by RXRATE. When configured such that the output data path is clocked by REFCLK instead of recovered clock (RXCKSEL = LOW), the RXCLK± output drivers present a buffered and delayed form of REFCLK. In this mode, RXCLK± and RXCLKC+ are buffered forms of REFCLK that are slightly different in phase, but follow the frequency and duty cycle of REFCLK. This phase difference allows the user to select the optimal set-up/hold timing for their specific interface.
RXCLKC+	3-state, LVTTL Output	**Delayed REFCLK+ when RXCKSEL = LOW**. Delayed form of REFCLK+, used for transfer of output data to a host system. This output is only enabled when the receive parallel interface is configured to present data relative to REFCLK (RXCKSEL = LOW). When RXCKSEL = LOW, the RXCLKC+ follows the frequency and duty cycle of REFCLK+.
RXRATE	LVTTL Input Static Control Input, internal pull-down	**Receive Clock Rate Select**. When LOW, the RXCLK± recovered clock outputs are complementary clocks operating at the recovered character rate. Data for the receive channel should be latched on either the rising edge of RXCLK+ or falling edge of RXCLK–. When HIGH, the RXCLK± recovered clock outputs are complementary clocks operating at half the character rate. Data for the receive channel should be latched alternately on the rising edge of RXCLK+ and RXCLK–. When the output register is operated with REFCLK clocking (RXCKSEL = LOW), RXRATE is not interpreted and RXCLK± follows the frequency and duty cycle of REFCLK.
RFEN	LVTTL input, asynchronous, internal pull-down	**Reframe Enable**. Active HIGH. When HIGH, the Framer in the receive channel is enabled to frame per the presently enabled framing mode and selected framing character.
RXMODE	3-Level Select[4] static control input	**Receive Operating Mode**. This input selects one of two RXST channel status reporting modes and is only interpreted when the Decoder is enabled (DECMODE ≠ LOW). See *Table 12* for details.

Pin Descriptions CYP(V)(W)15G0101DXB Single-channel HOTLink II (continued)

Pin Name	I/O Characteristics	Signal Description
FRAMCHAR	3-Level Select[4] static control input	**Framing Character Select**. Used to select the character or portion of a character used for character framing of the received data streams. When MID, the Framer looks for both positive and negative disparity versions of the eight-bit Comma character. When HIGH, the Framer looks for both positive and negative disparity versions of the K28.5 character. Configuring FRAMCHAR = LOW is reserved for component test.
RFMODE	3-Level Select static control input[4]	**Reframe Mode Select**. Used to select the type of character framing used to adjust the character boundaries (based on detection of one or more framing characters in the data stream. This signal operates in conjunction with the type of framing character selected. When LOW, the Low-Latency Framer is selected. This will frame on each occurrence of the selected framing character(s) in the received data stream. This mode of framing stretches the recovered character-rate clock for one or multiple cycles to align that clock with the recovered data. When MID, the Cypress-mode Multi-Byte parallel Framer is selected. This requires a pair of the selected framing character(s), on identical 10-bit boundaries, within a span of 50 bits (five characters), before the character boundaries are adjusted. The recovered character clock remains in the same phase regardless of character offset. When HIGH, the Alternate-mode Multi-Byte parallel Framer is selected. This requires detection of the selected framing character(s) in the received data stream, on identical 10-bit boundaries, on four directly adjacent characters. The recovered character clock remains in the same phase regardless of character offset.
PARCTL	3-Level Select static control input[4]	**Parity Check/Generate Control**. Used to control the parity check and generate functions. When LOW, parity checking is disabled, and the RXOP output is disabled (High-Z). When MID, and the 8B/10B Encoder and Decoder are enabled (TXMODE[1] ≠ LOW, DECMODE ≠ LOW), TXD[7:0] inputs are checked (along with TXOP) for valid ODD parity, and ODD parity is generated for the RXD[7:0] outputs and presented on RXOP. When the 8B/10B Encoder and Decoder are disabled (TXMODE[1] = LOW, DECMODE = LOW), the TXD[7:0] and TXCT[1:0] inputs are checked (along with TXOP) for valid ODD parity, and ODD parity is generated for the RXD[7:0] and RXST[1:0] outputs and presented on RXOP. When HIGH, parity generation and checking are enabled. The TXD[7:0] and TXCT[1:0] inputs are checked (along with TXOP) for valid ODD parity, and ODD parity is generated for the RXD[7:0] and RXST[2:0] outputs and presented on RXOP. See *Table 2* and *Table 15* for details.
DECMODE	3-Level Select static control input[4]	**Decoder Mode Select**. When LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. When the Decoder is bypassed, RXCKSEL must be MID. When MID, the Cypress Decoder table for Special Code Characters is used. When HIGH, the alternate Decoder table for Special Code Characters is used. See *Table 21* for a list of the Special Codes supported in both encoded modes.
RXCKSEL	3-Level Select[4] static control input	**Receive Clock Mode**. Selects the receive clock source used to transfer data to the Output Registers and configures the Elasticity Buffer in the receive path. When LOW, the Output Register is clocked by REFCLK. RXCLK± and RXCLKC+ present buffered and delayed forms of REFCLK. When MID, the RXCLK± output follows the recovered clock as selected by RXRATE and the Elasticity Buffer is bypassed. When the 10B/8B Decoder and Elasticity Buffer are bypassed (DECMODE=LOW), RXCKSEL must be MID. Configuring RXCKSEL = HIGH is an invalid mode of operation.
Device Control Signals		
SPDSEL	3-Level Select,[4] static control input	**Serial Rate Select**. This input specifies the operating bit-rate range of both transmit and receive PLLs. LOW = 195–400 MBaud, MID = 400–800 MBaud, HIGH = 800–1500 MBaud (800–1540 MBaud for CYW15G0101DXB). When SPDSEL=LOW, setting TXRATE=HIGH (Half-rate Reference Clock) is invalid.

Pin Descriptions CYP(V)(W)15G0101DXB Single-channel HOTLink II (continued)

Pin Name	I/O Characteristics	Signal Description
REFCLK±	Differential LVPECL or single-ended LVTTL input clock	**Reference Clock**. This clock input is used as the timing reference for the transmit PLL. It is also used as the centering frequency of the Range Controller block of the Receive CDR PLLs. This input clock may also be selected to clock the transmit and receive parallel interfaces. When driven by a single-ended LVCMOS or LVTTL clock source, the clock source may be connected to either the true or complement REFCLK input, with the alternate REFCLK input left open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs. When TXCKSEL = LOW, REFCLK is also used as the clock for the parallel transmit data (input) interface. When RXCKSEL = LOW and Decoder is enabled, the Elasticity buffer is enabled and REFCLK is used as the clock source for the parallel receive data (output) interface. If the Elasticity Buffer is used, framing characters will be inserted or deleted to/from the data stream to compensate for frequency differences between the reference clock and recovered clock. When addition happens, a K28.5 will be appended immediately after a framing character is detected in the Elasticity Buffer. When deletion happens, a framing character will be removed from the data stream when detected in the Elasticity Buffer.
$\overline{\text{TRSTZ}}$	LVTTL Input, internal pull-up	**Device Reset**. Active LOW. Initializes all state machines and counters in the device. When sampled LOW by the rising edge of REFLCK, this input resets the internal state machines and sets the Elasticity Buffer pointers to a nominal offset. When the reset is removed ($\overline{\text{TRSTZ}}$ sampled HIGH by REFCLK↑), the status and data outputs will become deterministic in less than 16 REFCLK cycles. The BISTLE, OELE, and RXLE latches are reset by $\overline{\text{TRSTZ}}$. If the Elasticity Buffer or the Phase-Align Buffer are used, $\overline{\text{TRSTZ}}$ should be applied after power up to initialize the internal pointers into these memory arrays.
Analog I/O and Control		
OUT1±	CML Differential Output	**Primary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules.
OUT2±	CML Differential Output	**Secondary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules.
IN1±	LVPECL Differential Input, with internal DC restoration	**Primary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The IN1± serial stream is passed to the receiver Clock and Data Recovery (CDR) circuit to extract the data content when INSEL = HIGH.
IN2±	LVPECL Differential Input, with internal DC restoration	**Secondary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The IN2± serial stream is passed to the receiver CDR circuit to extract the data content when INSEL = LOW.
INSEL	LVTTL Input, asynchronous	**Receive Input Selector**. Determines which external serial bit stream is passed to the receiver CDR. When HIGH, the IN1± input is selected. When LOW, the IN2± input is selected.
SDASEL	3-Level Select,[4] static control input	**Signal Detect Amplitude Level Select**. Allows selection of one of three predefined amplitude trip points for a valid signal indication, as listed in *Table 10*.
LPEN	LVTTL Input, asynchronous, internal pull-down	**Loop-Back-Enable**. Active HIGH. When asserted (HIGH), the transmit serial data is internally routed to the receiver CDR circuit.All enabled serial drivers are forced to differential logic “1.” All serial data inputs are ignored.
OELE	LVTTL Input, asynchronous, internal pull-up	**Serial Driver Output Enable Latch Enable**. Active HIGH. When OELE = HIGH, the signals on the BOE[1:0] inputs directly control the OUTx± differential drivers. When the BOE[x] input is HIGH, the associated OUTx± differential driver is enabled. When the BOE[x] input is LOW, the associated OUTx± differential driver is powered down. When OELE returns LOW, the last values present on BOE[1:0] are captured in the internal Output Enable Latch. The specific mapping of BOE[1:0] signals to transmit output enables is listed in *Table 8*. If the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable both outputs.

Pin Descriptions CYP(V)(W)15G0101DXB Single-channel HOTLink II (continued)

Pin Name	I/O Characteristics	Signal Description
BISTLE	LVTTL Input, asynchronous, internal pull-up	**Transmit and Receive BIST Latch Enable**. Active HIGH. When BISTLE = HIGH, the signals on the BOE[1:0] inputs directly control the transmit and receive BIST enables. When the BOE[x] input is LOW, the associated transmit or receive channel is configured to generate or compare the BIST sequence. When the BOE[x] input is HIGH, the associated transmit or receive channel is configured for normal data transmission or reception. When BISTLE returns LOW, the last values present on BOE[1:0] are captured in the internal BIST Enable latch. The specific mapping of BOE[1:0] signals to transmit and receive BIST enables is listed in *Table 8*. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable BIST on both the transmit and receive channels.
RXLE	LVTTL Input, asynchronous, internal pull-up	**Receive Channel Power-Control Latch Enable**. Active HIGH. When RXLE = HIGH, the signal on the BOE[0] input directly controls the power enable for the receive PLL and analog logic. When the BOE[0] input is HIGH, the receive channel PLL and analog logic are active. When the BOE[0] input is LOW, the receive channel PLL and analog logic are placed in a non-functional power saving mode. When RXLE returns LOW, the last value present on BOE[0] is captured in the internal RX PLL Enable latch. The specific mapping of BOE[1:0] signals to the receive channel enable is listed in *Table 8*. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable the receive channel.
BOE[1:0]	LVTTL Input, asynchronous, internal pull-up	**BIST, Serial Output, and Receive Channel Enables**. These inputs are passed to and through the output enable latch when OELE = HIGH, and captured in this latch when OELE returns LOW. These inputs are passed to and through the BIST enable latch when BISTLE = HIGH, and captured in this latch when BISTLE returns LOW. These inputs are passed to and through the Receive Channel enable latch when RXLE = HIGH, and captured in this latch when RXLE returns LOW.
LFI	LVTTL Output, Asynchronous	**Link Fault Indication Output**. Active LOW. $\overline{\text{LFI}}$ is the logical OR of four internal conditions: 1. Received serial data frequency outside expected range 2. Analog amplitude below expected levels 3. Transition density lower than expected 4. Receive Channel disabled.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for $\geq$ 5 TCLK cycles, the JTAG test controller is reset. The TAP controller is also reset automatically upon application of power to the device.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**.
TDO	Three-State LVTTL Output	**Test Data Out**. JTAG data output buffer which is High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
Power		
V_{CC}		+3.3V power
GND		Signal and power ground for all internal circuits

CYP(V)(W)15G0101DXB HOTLink II Operation

The CYP(V)(W)15G0101DXB is a highly configurable device designed to support reliable transfer of large quantities of data using high-speed serial links from a single source to one or more destinations.

CYP(V)(W)15G0101DXB Transmit Data Path

Operating Modes

The transmit path of the CYP(V)(W)15G0101DXB supports a single character-wide data path. This data path is used in multiple operating modes as controlled by the TXMODE[1:0] inputs.

Input Register

The bits in the Input Register support different assignments, based on if the character is unencoded, encoded with two control bits, or encoded with three control bits. These assignments are shown in *Table 1*.

Table 1. Input Register Bit Assignments[5]

Signal Name	Unencoded (Encoder Bypassed)	Encoded (Encoder Enabled)	
		Two-bit Control	Three-bit Control
TXD[0] (LSB)	DIN[0]	TXD[0]	TXD[0]
TXD[1]	DIN[1]	TXD[1]	TXD[1]
TXD[2]	DIN[2]	TXD[2]	TXD[2]
TXD[3]	DIN[3]	TXD[3]	TXD[3]
TXD[4]	DIN[4]	TXD[4]	TXD[4]
TXD5]	DIN[5]	TXD[5]	TXD[5]
TXD[6]	DIN[6]	TXD[6]	TXD[6]
TXD[7]	DIN[7]	TXD[7]	TXD[7]
TXCT[0]	DIN[8]	TXCT[0]	TXCT[0]
TXCT[1] (MSB)	DIN[9]	TXCT[1]	TXCT[1]
SCSEL	N/A	N/A	SCSEL

The Input Register captures a minimum of eight data bits and two control bits on each input clock cycle. When the Encoder is bypassed, the TXCT[1:0] control bits are part of the pre-encoded 10-bit data character.

When the Encoder is enabled (TXMODE[1] ≠ LOW), the TXCT[1:0] bits are interpreted along with the TXD[7:0] character to generate the specific 10-bit transmission character. When TXMODE[0] ≠ HIGH, an additional special character select (SCSEL) input is also captured and interpreted. This SCSEL input is used to modify the encoding of the characters.

Phase-Align Buffer

Data from the Input Register is passed either to the Encoder or to the Phase-Align buffer. When the transmit path is operated synchronous to REFCLK↑ (TXCKSEL = LOW and TXRATE = LOW), the Phase-Align Buffer is bypassed and data is passed directly to the Parity Check and Encoder block to reduce latency.

When an Input Register clock with an uncontrolled phase relationship to REFCLK is selected (TXCKSEL ≠ LOW) or if data is captured on both edges of REFCLK (TXRATE = HIGH), the Phase-Align Buffer is enabled. This buffer is used to absorb clock phase differences between the presently selected input clock and the internal character clock.

Initialization of the Phase-Align Buffer takes place when the TXRST input is sampled LOW by two consecutive rising edges of REFCLK. When TXRST is returned HIGH, the present input clock phase relative to REFCLK↑ is set. TXRST is an asynchronous input, but is sampled internally to synchronize it to the internal transmit path state machine.

Once set, the input clock is allowed to skew in time up to half a character period in either direction relative to REFCLK↑; i.e., ±180°. This time shift allows the delay path of the character clock (relative to REFLCK↑) to change due to operating voltage and temperature, while not affecting the design operation.

If the phase offset, between the initialized location of the input clock and REFCLK↑, exceeds the skew handling capabilities of the Phase-Align Buffer, an error is reported on the TXPER output. This output indicates a continuous error until the Phase-Align Buffer is reset. While the error remains active, the transmitter outputs a continuous C0.7 character to indicate to the remote receiver that an error condition is present in the link.

In specific transmit modes, it is also possible to reset the Phase-Align Buffer with minimal disruption of the serial data stream. When the transmit interface is configured for generation of atomic Word Sync Sequences (TXMODE[1] = MID) and a Phase-Align Buffer error is present, the transmission of a Word Sync Sequence will recenter the Phase-Align Buffer and clear the error condition.[6]

Parity Support

In addition to the ten data and control bits that are captured at the transmit Input Register, a TXOP input is also available. This allows the CYP(V)(W)15G0101DXB to support ODD parity checking. Parity checking is available for all operating modes (including Encoder Bypass). The specific mode of parity checking is controlled by the PARCTL input, and operates per *Table 2*.

When PARCTL = MID (open) and the Encoder is enabled (TXMODE[1] ≠ LOW), only the TXD[7:0] data bits are checked for ODD parity along with the TXOP bit. When PARCTL = HIGH with the Encoder enabled (or MID with the Encoder bypassed), the TXD[7:0] and TXCT[1:0] inputs are checked for ODD parity along with the TXOP bit. When PARCTL = LOW, parity checking is disabled.

Notes:

5. The TXOP input is also captured in the Input Register, but its interpretation is under the separate control of PARCTL.
6. One or more K28.5 characters may be added or lost from the data stream during this reset operation. When used with non-Cypress devices that require a complete 16-character Word Sync Sequence for proper receive Elasticity Buffer alignment, it is recommend that the sequence be followed by a second Word Sync Sequence to ensure proper operation.

When parity checking and the Encoder are both enabled (TXMODE[1] ≠ LOW), the detection of a parity error causes a C0.7 character of proper disparity to be passed to the Transmit Shifter. When the Encoder is bypassed (TXMODE[1] = LOW), detection of a parity error causes a positive disparity version of a C0.7 transmission character to be passed to the Transmit Shifter.

Table 2. Input Register Bits Checked for Parity[8]

Signal Name	Transmit Parity Check Mode (PARCTL)			
	LOW	MID		HIGH
		TXMODE[1] = LOW	TXMODE[1] ≠ LOW	
TXD[0]		X[7]	X	X
TXD[1]		X	X	X
TXD[2]		X	X	X
TXD[3]		X	X	X
TXD[4]		X	X	X
TXD[5]		X	X	X
TXD[6]		X	X	X
TXD[7]		X	X	X
TXCT[0]		X		X
TXCT[1]		X		X
TXOP		X	X	X

Encoder

The character, received from the Input Register or Phase-Align Buffer and Parity Check Logic, is then passed to the Encoder logic. This block interprets each character and any control bits, and outputs a 10-bit transmission character.

Depending on the configured operating mode, the generated transmission character may be

- the 10-bit pre-encoded character accepted in the Input Register
- the 10-bit equivalent of the eight-bit data character accepted in the Input Register
- the 10-bit equivalent of the eight -bit special character code accepted in the Input Register
- the 10-bit equivalent of the C0.7 SVS character if parity checking was enabled and a parity error was detected
- the 10-bit equivalent of the C0.7 SVS character if a Phase-Align Buffer overflow or underflow error is present
- a character that is part of the 511-character BIST sequence
- a K28.5 character generated as an individual character or as part of the 16-character Word Sync Sequence.

The selection of the specific characters generated are controlled by the TXMODE[1:0], SCSEL, TXCT[1:0], and TXD[7:0] inputs for each character.

Data Encoding

Raw data, as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee

- a minimum transition density (to allow the serial receive PLL to extract a clock from the data stream)
- a DC-balance in the signaling (to prevent baseline wander)
- run-length limits in the serial data (to limit the bandwidth of the link)
- the remote receiver a way of determining the correct character boundaries (framing).

When the Encoder is enabled (TXMODE[1] ≠ LOW), the characters to be transmitted are converted from Data or Special Character codes to 10-bit transmission characters (as selected by the TXCT[1:0] and SCSEL inputs), using an integrated 8B/10B Encoder. When directed to encode the character as a Special Character code, it is encoded using the special character encoding rules listed in *Table 21*. When directed to encode the character as a Data character, it is encoded using the Data Character encoding rules in *Table 20*.

The 8B/10B Encoder is standards compliant with ANSI/NCITS ASC X3.230-1994 (Fibre Channel), IEEE 802.3z (Gigabit Ethernet), the IBM® ESCON® and FICON™, and Digital Video Broadcast (DVB-ASI) standards for data transport.

Many of the Special Character codes listed in *Table 21* may be generated by more than one input character. The CYP(V)(W)15G0101DXB is designed to support two independent (but non-overlapping) Special Character code tables. This allows the CYP(V)(W)15G0101DXB to operate in mixed environments with other Cypress HOTLink devices using the enhanced Cypress command code set, and the reduced command sets of other non-Cypress devices. Even when used in an environment that normally uses non-Cypress Special Character codes, the selective use of Cypress command codes can permit operation where running disparity and error handling must be managed.

Following conversion of each input character from eight bits to a 10-bit transmission character, it is passed to the Transmit Shifter and is shifted out LSB first, as required by ANSI and IEEE standards for 8B/10B coded serial data streams.

Transmit Modes

The operating mode of the transmit path is set through the TXMODE[1:0] inputs. These 3-level select inputs allow one of nine transmit modes to be selected. The transmit modes are listed in *Table 3*.

The encoded modes (TX Modes 3 through 8) support multiple encoding tables. These encoding tables vary by the specific combinations of SCSEL, TXCT[1], and TXCT[0] that are used to control the generation of data and control characters. These multiple encoding forms allow maximum flexibility in interfacing to legacy applications, while also supporting numerous extensions in capabilities.TX Mode 0—Encoder Bypass

When the Encoder is bypassed, the character captured from the TXD[7:0] and TXCT[1:0] inputs is passed directly to the Transmit Shifter without modification. If parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected, the 10-bit character is replaced with the 1001111000 pattern (+C0.7 character) regardless of the running disparity of the previous character.

Notes:
7. Bits marked as X are XORed together. Result must be a logic-1 for parity to be valid.
8. Transmit path parity errors are reported on the TXPER output.

With the Encoder bypassed, the TXCT[1:0] inputs are considered part of the data character and do not perform a control function that would otherwise modify the interpretation of the TXD[7:0] bits. The bit usage and mapping of these control bits when the Encoder is bypassed is shown in *Table 4*.

In Encoder Bypass mode, the SCSEL input is ignored. All clocking modes interpret the data in the same way.

Table 4. Encoder Bypass Mode (TXMODE[1:0 = LL)

Signal Name	Bus Weight	10B Name
TXD[0] (LSB)[9]	2^0	a
TXD[1]	2^1	b
TXD[2]	2^2	c
TXD[3]	2^3	d
TXD[4]	2^4	e
TXD[5]	2^5	i
TXD[6]	2^6	f
TXD[7]	2^7	g
TXCT[0]	2^8	h
TXCT[1] (MSB)	2^9	j

Table 3. Transmit Operating Modes

TX Mode		Operating Mode		
Mode Number	TXMODE [1:0]	Word Sync Sequence Support	SCSEL Control	TXCT Function
0	LL	None	None	Encoder Bypass
1	LM	None	None	Reserved for test
2	LH	None	None	Reserved for test
3	ML	Atomic	Special Character	Encoder Control
4	MM	Atomic	Word Sync	Encoder Control
5	MH	Atomic	None	Encoder Control
6	HL	Interruptible	Special Character	Encoder Control
7	HM	Interruptible	Word Sync	Encoder Control
8	HH	Interruptible	None	Encoder Control

TX Modes 1 and 2—Factory Test Modes

These modes enable specific factory test configurations. They are not considered normal operating modes of the device. Entry or configuration into these test modes will not damage the device.

TX Mode 3—Atomic Word Sync and SCSEL Control of Special Codes

When configured in TX Mode 3, the SCSEL input is captured along with the TXCT[1:0] data control inputs. These bits combine to control the interpretation of the TXD[7:0] bits and the characters generated by them. These bits are interpreted as listed in *Table 5*.

Note:
9. LSB is shifted out first.

Table 5. TX Modes 3 and 6 Encoding

SCSEL	TXCT[1]	TXCT[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
1	0	1	Special character code
X	1	1	16-character Word Sync Sequence

When TXCKSEL = MID or HIGH, the transmit channel captures data into its Input Register using the TXCLK clock.

Word Sync Sequence

When TXCT[1:0] = 11, a 16-character sequence of K28.5 characters, known as a Word Sync Sequence, is generated on the transmit channel. This sequence of K28.5 characters may start with either a positive or negative disparity K28.5 (as determined by the current running disparity and the 8B/10B coding rules). The disparity of the second and third K28.5 characters in this sequence are reversed from what normal 8B/10B coding rules would generate. The remaining K28.5 characters in the sequence follow all 8B/10B coding rules. The disparity of the generated K28.5 characters in this sequence follow a pattern of either + + – – + – + – + – + – + – or – – + + – + – + – + – + – + –.

When TXMODE[1] = MID (open, TX modes 3, 4 and 5), the generation of this character sequence is an atomic (non-interruptible) operation. Once it has been successfully started, it cannot be stopped until all 16 characters have been generated. The content of the Input Register is ignored for the duration of this 16-character sequence. At the end of this sequence, if the TXCT[1:0] = 11 condition is sampled again, the sequence restarts and remains uninterrupted for the following 15 character clocks.

If parity checking is enabled, the character used to start the Word Sync Sequence must also have correct ODD parity. This is true even though the contents of the TXD[7:0] bits do not directly control the generation of characters during the Word Sync Sequence. Once the sequence is started, parity is not checked on the following 15 characters in the Word Sync Sequence.

When TXMODE[1] = HIGH (TX modes 6, 7, and 8), the generation of the Word Sync Sequence becomes an interruptible operation. In TX Mode 6, this sequence is started as soon as the TXCT[1:0] = 11 condition is detected on the channel. In order for the sequence to continue, the TXCT[1:0] inputs must be sampled as 00 for the remaining 15 characters of the sequence. If at any time a sample period exists where TXCT[1:0] $\neq$ 00, the Word Sync Sequence is terminated, and a character representing the data and control bits is generated by the Encoder. This resets the Word Sync Sequence state machine such that it will start at the beginning of the sequence at the next occurrence of TXCT[1:0] = 11.

When parity checking is enabled and TXMODE[1] = HIGH, all characters (including those in the middle of a Word Sync Sequence) must have correct parity. The detection of a character with incorrect parity during a Word Sync Sequence (regardless of the state of TXCT[1:0]) will interrupt that sequence and force generation of a C0.7 SVS character. Any interruption of the Word Sync Sequence causes the sequence to terminate.

When TXCKSEL = LOW, the Input Register for the transmit channel is clocked by REFCLK.[3] When TXCKSEL = HIGH or MID, the Input Register for the transmit channel is clocked with TXCLK↑.

TX Mode 4—Atomic Word Sync and SCSEL Control of Word Sync Sequence Generation

When configured in TX Mode 4, the SCSEL input is captured along with the TXCT[1:0] data control inputs. These bits combine to control the interpretation of the TXD[7:0] bits and the characters generated by them. These bits are interpreted as listed in *Table 6*.

Table 6. TX Modes 4 and 7 Encoding

SCSEL	TXCT[1]	TXCT[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
0	1	1	Special character code
1	X	1	16-character Word Sync Sequence

TX Mode 4 also supports an Atomic Word Sync Sequence. Unlike TX Mode 3, this sequence is started when both SCSEL and TXCT[0] are sampled HIGH. With the exception of the combination of control bits used to initiate the sequence, the generation and operation of this Word Sync Sequence is the same as that documented for TX Mode 3.

TX Mode 5—Atomic Word Sync, No SCSEL

When configured in TX Mode 5, the SCSEL signal is not used. The TXCT[1:0] inputs control the characters generated by the channel. The specific characters generated by these bits are listed in *Table 7*.

Table 7. TX Modes 5 and 8 Encoding

SCSEL	TXCT[1]	TXCT[0]	Characters Generated
X	0	0	Encoded data character
X	0	1	K28.5 fill character
X	1	0	Special character code
X	1	1	16-character Word Sync Sequence

TX Mode 5 also has the capability of generating an Atomic Word Sync Sequence. For the sequence to be started, the TXCT[1:0] inputs must both be sampled HIGH. The generation and operation of this Word Sync Sequence is the same as that documented for TX Mode 3.

Transmit BIST

The transmit channel contains an internal pattern generator that can be used to validate both device and link operation. This generator is enabled by the BOE[1] signal, as listed in *Table 8* (when the BISTLE latch enable input is HIGH). When enabled, a register in the transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Receiver. If the receive channel is configured for REFCLK clocking (RXCKSEL = LOW), each pass is preceded by a 16-character Word Sync Sequence to allow Elasticity Buffer alignment and management of clock-frequency variations.

When the BISTLE signal is HIGH, if the BOE[1] input is LOW, the BIST generator in the transmit channel is enabled (and if BOE[0] = LOW the BIST checker in the receive channel is enabled). When BISTLE returns LOW, the values of the BOE[1:0] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned high to open the latch again. A device reset (TRSTZ sampled LOW), also presets the BIST Enable Latch to disable BIST on both the transmit and receive channels.

All data and data-control information present at the TXD[7:0] and TXCT[1:0] inputs are ignored when BIST is active on the transmit channel.

Serial Output Drivers

The serial interface Output Drivers use high-performance differential Current Mode Logic (CML) to provide source-matched drivers for the transmission lines. These Serial Drivers accept data from the Transmit Shifter. These outputs have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or AC-coupled transmission lines. To acheive OBSAI RP3 compliancy, the serial output drivers must be AC-coupled to the transmission medium.

When configured for local loop-back (LPEN = HIGH), the enabled Serial Drivers are configured to drive a static differential logic-1.

Each Serial Driver can be enabled or disabled through the BOE[1:0] inputs, as controlled by the OELE latch-enable signal. When OELE = HIGH, the signals present on the BOE[1:0] inputs are passed through the Serial Output Enable latch to control the Serial Driver. The BOE[1:0] input with OUT1± and OUT2± driver is listed in *Table 8*.

Table 8. Output Enable, BIST, and Receive Channel Enable Signal Map

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BOE[1]	OUT2±	Transmit	X
BOE[0]	OUT1±	Receive	Receive

When OELE = HIGH and BOE[x] = HIGH, the associated Serial Driver is enabled to drive any attached transmission line. When OELE = HIGH and BOE[x] = LOW, the associated driver is disabled and internally configured for minimum power

dissipation. If both Serial Drivers for the channel are disabled, the internal logic for the transmit channel is also configured for lowest power operation. When OELE returns LOW, the values present on the BOE[1:0] inputs are latched in the Output Enable Latch, and remain there until OELE returns HIGH to open the latch again. A device reset (TRSTZ sampled LOW) clears this latch and disables both Serial Drivers.

Note. When both serial output drivers are disabled and a driver is re-enabled, the data on the Serial Drivers may not meet all timing specifications for up to 200 μs.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiples that clock by 10 or 20 (as selected by TXRATE) to generate a bit-rate clock for use by the Transmit Shifter. It also provides a character-rate clock used by the transmit path.

This clock multiplier PLL can accept a REFCLK input between 19.5 MHz and 150 MHz (19.5 MHz and 154 MHz for CYW15G0101DXB), however, this clock range is limited by the operating mode of the CYP(V)(W)15G0101DXB clock multiplier (controlled by TXRATE) and by the level on the SPDSEL input.

When TXRATE=HIGH, configuring TXCKSEL = HIGH or MID is an invalid mode of operation.

SPDSEL is a 3-level select[4] (ternary) input that selects one of three operating ranges for the serial data outputs and inputs. The operating serial signaling-rate and allowable range of REFCLK frequencies are listed in *Table 9*.

Table 9. Operating Speed Settings

SPDSEL	TXRATE	REFCLK Frequency (MHz)	Signaling Rate (MBaud)
LOW	1	reserved	195–400
	0	19.5–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500 (800–1540 for CYW15G0101 DXB)
	0	80–150	

The REFCLK± input is a differential input with each input internally biased to 1.4V. If the REFCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point.

When both the REFCLK+ and REFCLK– inputs are connected, the clock source must be a differential clock. This can be either a differential LVPECL clock that is DC- or AC-coupled, or a differential LVTTL or LVCMOS clock.

By connecting the REFCLK– input to an external voltage source or resistive voltage divider, it is possible to adjust the reference point of the REFCLK+ input for alternate logic levels. When doing so, it is necessary to ensure that the 0V-differential crossing point remains within the parametric range supported by the input.

CYP(V)(W)15G0101DXB Receive Data Path

Serial Line Receivers

Two differential Line Receivers, IN1± and IN2±, are available for accepting serial data streams. The active Serial Line Receiver is selected using the INSEL input. Both Serial Line Receivers have differential inputs, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least V_{DIFFS} > 100 mV, or 200-mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules (any ECL/PECL logic family, not limited to 100K PECL) or AC-coupled to +5V-powered optical modules. The common-mode tolerance of the receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

The local loop-back input (LPEN) allows the serial transmit data to be routed internally back to the Clock and Data Recovery circuit. When configured for local loop-back, the transmit Serial Driver outputs are forced to output a differential logic-1. This prevents local diagnostic patterns from being broadcast to attached remote receivers.

Signal Detect/Link Fault

Each selected Line Receiver (i.e., that routed to the Clock and Data Recovery PLL) is simultaneously monitored for

- analog amplitude above limit specified by SDASEL
- transition density greater than specified limit
- range controller reports the received data stream within normal frequency range (±1500 ppm)[10]
- receive channel enabled.

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFI (Link Fault Indicator) output.

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable to allow operation with highly attenuated signals, or in high-noise environments. This adjustment is made through the SDASEL signal, a 3-level select[4] (ternary) input, which sets the trip point for the detection of a valid signal at one of three levels, as listed in *Table 10*.

The Analog Signal Detect monitor is active for the present Line Receiver, as selected by the INSEL input. When configured for local loop-back (LPEN = HIGH), the Analog Signal Detect Monitor is disabled.

Note:

10. REFCLK has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±1500 PPM (±0.15%) of the remote transmitter's PLL reference (REFCLK) frequency. Although transmitting to a HOTLink II receiver necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500-PPM, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard. For example, to be IEEE 802.3z Gigabit Ethernet compliant, the frequency stability of the crystal needs to be within ±100 PPM.

Transition Density

The Transition Detection logic checks for the absence of any transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received (within the referenced period), the Transition Detection logic asserts LFI. The LFI output remains asserted until at least one transition is detected in each of three adjacent received characters.

Table 10. Analog Amplitude Detect Valid Signal Levels[11]

SDASEL	Typical Signal with Peak Amplitudes Above
LOW	140-mV p-p differential
MID (Open)	280-mV p-p differential
HIGH	420-mV p-p differential

Range Control

The Clock/Data Recovery (CDR) circuit includes logic to monitor the frequency of the phase-locked loop (PLL) Voltage Controlled Oscillator (VCO) used to sample the incoming data stream. This logic ensures that the VCO operates at, or near the rate of the incoming data stream for two primary cases:

- when the incoming data stream resumes after a time in which it has been "missing."
- when the incoming data stream is outside the acceptable frequency range.

To perform this function, the frequency of the VCO is periodically sampled and compared to the frequency of the REFCLK input. If the VCO is running at a frequency beyond ±1500ppm[10] as defined by the reference clock frequency, it is periodically forced to the correct frequency (as defined by REFCLK, SPDSEL, and TXRATE) and then released in an attempt to lock to the input data stream. The sampling and relock period of the Range Control is calculated as follows: RANGE CONTROL SAMPLING PERIOD = (REFCLK-PERIOD) * (16000).

During the time that the Range Control forces the PLL VCO to run at REFCLK*10 (or REFCLK*20 when TXRATE = HIGH) rate, the LFIx output will be asserted LOW. While the PLL is attempting to re-lock to the incoming data stream, LFIx may be either HIGH or LOW (depending on other factors such as transition density and amplitude detection) and the recovered byte clock (RXCLK) may run at an incorrect rate (depending on the quality or existence of the input serial data stream). After a valid serial data stream is applied, it may take up to one RANGE CONTROL SAMPLING PERIOD before the PLL locks to the input data stream, after which LFIx should be HIGH.

Receive Channel Enabled

The CYP(V)(W)15G0101DXB receive channel can be enabled and disabled through the BOE[0] input, as controlled by the RXLE latch-enable signal. When RXLE = HIGH, the signal present on the BOE[0] input is passed through the Receive Channel Enable Latch to control the PLL and logic of the receive channel. The BOE[1:0] input functions are listed in *Table 8*.

When RXLE = HIGH and BOE[0] = HIGH, the receive channel is enabled to receive and recover a serial stream from the Line Receiver. When RXLE = HIGH and BOE[0] = LOW, the receive channel is disabled and internally configured for minimum power dissipation. When disabled, the channel indicates a constant LFI output. When RXLE returns LOW, the values present on the BOE[1:0] inputs are latched in the Receive Channel Enable Latch, and remain there until RXLE returns HIGH to open the latch again.[12]

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from a received serial stream is performed by a CDR block within the receive channel. The clock extraction function is performed by a high-performance embedded PLL that tracks the frequency of the transitions in the incoming bit stream and aligns the phase of the internal bit-rate clock to the transitions in the serial data stream.

The CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) reference clock from the REFCLK input. This REFCLK input is used to

- ensure that the VCO (within the CDR) is operating at the correct frequency
- reduce PLL acquisition time
- limit unlocked frequency excursions of the CDR VCO when there is no input data present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits of the range control monitor, the CDR will switch to track REFCLK instead of the data stream. Once the CDR output (RXCLK) frequency returns back close to REFCLK frequency, the CDR input will be switched back to track the input data stream. In case no data is present at the input, this switching behavior may result in brief RXCLK frequency excursions from REFCLK. However, the validity of the input data stream is indicated by the LFIx output. The frequency of REFCLK is required to be within ± 1500 ppm[10] of the frequency of the clock that drives the REFCLK input of the remote transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the $\overline{\text{LFI}}$ output can be used to select an alternate data stream. When an $\overline{\text{LFI}}$ indication is detected, external logic can toggle selection of the IN1± and IN2± inputs through the INSEL input. When a port switch takes place, it is necessary for the receive PLL to reacquire the new serial stream and frame to the incoming character boundaries.

Deserializer/Framer

Each CDR circuit extracts bits from the serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream, looking for one or more Comma or K28.5 characters at all possible bit positions. The location of these characters in the data stream are used to determine the character boundaries of all following characters.

Notes:

11. The peak amplitudes listed in this table are for typical waveforms that have generally 3–4 transitions for every ten bits. In a worse case environment the signals may have a sign-wave appearance (highest transition density with repeating 0101...). Signal peak amplitudes levels within this environment type could increase the values in the table above by approximately 100 mV.
12. When a disabled receive channel is reenabled, the status of the $\overline{\text{LFI}}$ output and data on the parallel outputs may be indeterminate for up to 2 ms.

Framing Character

The CYP(V)(W)15G0101DXB allows selection of two combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input.

The specific bit combinations of these framing characters are listed in *Table 11*. When the specific bit combination of the selected framing character is detected by the Framer, the boundaries of the characters present in the received data stream are known.

Table 11. Framing Character Selector

FRAMCHAR	Bits Detected in Framer	
	Character Name	Bits Detected
LOW	Reserved for test	
MID (Open)	Comma+ Comma–	00111110XX[13] or 11000001XX
HIGH	–K28.5 +K28.5	0011111010 or 1100000101

Framer

The Framer operates in one of three different modes, as selected by the RFMODE input. In addition, the Framer itself may be enabled or disabled through the RFEN input. When RFEN = LOW, the Framer is disabled, and no combination of bits in a received data stream will alter the character boundaries. When RFEN = HIGH, the Framer-mode selected by RFMODE is enabled.

When RFMODE = LOW, the Low-latency Framer is selected. This Framer operates by stretching the recovered character clock until it aligns with the received character boundaries. In this mode, the Framer starts its alignment process on the first detection of the selected framing character. To reduce the impact on external circuits that make use of a recovered clock, the clock period is not stretched by more than two bit-periods in any one clock cycle. When operated with a character-rate output clock (RXRATE = LOW), the output of properly framed characters may be delayed by up to nine character-clock cycles from the detection of the selected framing character. When operated with a half-character-rate output clock (RXRATE = HIGH), the output of properly framed characters may be delayed by up to 14 character-clock cycles from the detection of the selected framing character.[14]

When RFMODE = MID (open), the Cypress-mode Multi-Byte Framer is selected. The required detection of multiple framing characters makes the link much more robust to incorrect framing due to aliased framing characters in the data stream. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock does not contain any significant phase changes or hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other external circuits or components using PLL-based clock distribution elements. In this framing mode, the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

When RFMODE = HIGH, the Alternate-mode Multi-Byte Framer is enabled. Like the Cypress-mode Multi-Byte Framer, multiple framing characters must be detected before the character boundary is adjusted. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, on identical 10-bit boundaries, before character framing is adjusted.

Framing is enabled when RFEN = HIGH. If RFEN = LOW, the Framer is disabled. When the Framer is disabled, no changes are made to the recovered character boundary, regardless of the presence of framing characters in the data stream.

10B/8B Decoder Block

The Decoder logic block performs three primary functions:

- decoding the received transmission characters back into Data and Special Character codes
- comparing generated BIST patterns with received characters to permit at-speed link and device testing
- generation of ODD parity on the decoded characters.

10B/8B Decoder

The framed parallel output of the Deserializer Shifter is passed to the 10B/8B Decoder where, if the Decoder is enabled (DECMODE ≠ LOW), it is transformed from a 10-bit transmission character back to the original Data and Special Character codes. This block uses the 10B/8B Decoder patterns in *Table 20* and *Table 21* of this data sheet. Valid data characters are indicated by a 000b bit-combination on the RXST[2:0] status bits, and Special Character codes are indicated by a 001b bit-combination on these same status outputs. Framing characters, invalid patterns, disparity errors, and synchronization status are presented as alternate combinations of these status bits.

The 10B/8B Decoder operates in two normal modes, and can also be bypassed. The operating mode for the Decoder is controlled by the DECMODE input.

When DECMODE = LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. In this mode, the receive Elasticity Buffers are bypassed, and RXCKSEL must be MID.

When DECMODE = MID (or open), the 10-bit transmission characters are decoded using *Table 20* and *Table 21*. Received Special Code characters are decoded using the Cypress column of *Table 21*.

When DECMODE = HIGH, the 10-bit transmission characters are decoded using *Table 20* and *Table 21*. Received Special Code characters are decoded using the Alternate column of *Table 21*.

Notes:

13. The standard definition of a Comma contains only seven bits. However, since all valid Comma characters within the 8B/10B character set also have the 8th bit as an inversion of the 7th bit, the compare pattern is extended to a full eight bits to reduce the possibility of a framing error.
14. When Receive BIST is enabled on a channel, the Low-Latency Framer must not be enabled. The BIST sequence contains an aliased K28.5 framing character, which would cause the Receiver to update its character boundaries incorrectly.

Receive BIST Operation

The Receiver interface contains an internal pattern generator that can be used to validate both device and link operation. This generator is enabled by the BOE[0] signal as listed in *Table 8* (when the BISTLE latch enable input is HIGH). When enabled, a register in the Receive channel becomes a pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter. If the receive channels are configured for REFCLK clocking (RXCKSEL = LOW), each pass is preceded by a 16-character Word Sync Sequence.

When synchronized with the received data stream, the Receiver checks each character in the Decoder with each character generated by the LFSR and indicates compare errors and BIST status at the RXST[2:0] bits of the Output Register.

When the BISTLE signal is HIGH, if the BOE[0] input is LOW the BIST generator/checker in the Receive channel is enabled (and if BOE[1] = LOW the BIST generator in the transmit channel is enabled). When BISTLE returns LOW, the values of the BOE[1:0] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned high to open the latch again. All captured signals in the BIST Enable Latch are set HIGH (i.e., BIST is disabled) following a device reset ($\overline{\text{TRSTZ}}$ is sampled LOW).

When BIST is first recognized as being enabled in the Receiver, the LFSR is preset to the BIST-loop start-code of D0.0. This D0.0 character is sent only once per BIST loop. The status of the BIST progress and any character mismatches is presented on the RXST[2:0] status outputs.

Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXST[2:0] indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress. These same status values are presented when the Decoder is bypassed and BIST is enabled on the Receive channel.

The status reported on RXST[2:0] by the BIST state machine are listed in *Table 16*. When Receive BIST is enabled, the same status is reported on the receive status outputs regardless of the state of DECMODE.

The specific patterns checked by each receiver are described in detail in the Cypress application note “HOTLink Built-In Self-test.” The sequence compared by the CYP(V)(W)15G0101DXB is identical to that in the CY7B933 and CY7C924DX, allowing interoperable systems to be built when used at compatible serial signaling rates.

If the number of invalid characters received ever exceeds the number of valid characters by 16, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

When the receive paths are configured for REFCLK clocking (RXCKSEL = LOW), each pass must be preceded by a 16-character Word Sync Sequence to allow output buffer alignment and management of clock frequency variations. This is automatically generated by the transmitter when its local RXCKSEL = LOW.

The BIST state machine requires the characters to be correctly framed for it to detect the BIST sequence. If the Low-Latency Framer is enabled (RFMODE = LOW), the Framer will misalign to an aliased framing character within the BIST sequence. If the Alternate-mode Multi-Byte Framer is enabled (RFMODE = HIGH) and the Receiver outputs are clocked relative to a recovered clock (RXCKSEL = MID), it is necessary to frame the Receiver before BIST is enabled. If the Receiver outputs are clocked relative to REFCLK (RXCKSEL = LOW), the transmitter precedes every 511 character BIST sequence with a 16-character Word Sync Sequence.

Receive Elasticity Buffer

The receive channel contains an Elasticity Buffer that is designed to support multiple clocking modes. This buffer allows data to be read using an Elasticity Buffer read-clock that is asynchronous in both frequency and phase from the Elasticity Buffer write clock, or to use a read clock that is frequency coherent but with uncontrolled phase relative to the Elasticity Buffer write clock.

The Elasticity Buffer is 10 characters deep, and supports a 12-bit-wide data path. It is capable of supporting a decoded character, three status bits, and a parity bit for each character present in the buffer. The write clock for this buffer is always the recovered clock for the read channel.

The read clock for the Elasticity Buffer can be set to character-rate REFCLK (RXCKSEL = LOW and DECMODE ≠ LOW). The write clock for the Elasticity Buffer is always recovered clock.

When RXCKSEL = LOW, the Receive channel is clocked by REFCLK. The RXCLK± and RXCLKC+ outputs present buffered and delayed forms of REFCLK. In this mode, the receive Elasticity Buffer is enabled. For REFCLK clocking, the Elasticity Buffer must be able to insert K28.5 characters and delete framing characters as appropriate. The Elasticity Buffer is bypassed whenever the Decoder is bypassed (DECMODE = LOW). When the Decoder and Elasticity Buffer are bypassed, RXCKSELx must be set to MID. When RXCKSEL = MID (or open), the receive channel Output Register is clocked by the recovered clock.

The insertion of a K28.5 or deletion of a framing character can occur at any time. However, the actual timing on these insertions and deletions is controlled in part by the how the transmitter sends its data. Insertion of a K28.5 character can only occur when the receiver has a framing character in the Elasticity Buffer. Likewise, to delete a framing character, one must also be present in the Elasticity Buffer. To prevent an Elasticity Buffer overflow or underflow in the receive channel, a minimum density of framing characters must be present in the received data stream.

Prior to reception of valid data, at least one Word Sync Sequence (or at least four framing characters) must be received to allow the receive Elasticity Buffer to be centered. The Elasticity Buffer may also be centered by a device reset operation initiated through the $\overline{\text{TRSTZ}}$ input. However, following such an event, the CYP(V)(W)15G0101DXB will normally require a framing event before it will correctly decode characters.

Receive Modes

The operating mode of the receive path is set through the RXMODE input. The 'Reserved for test' setting (RXMODE = M) is not allowed, even if the receiver is not being used, as it will stop normal function of the device. When the decoder is disabled, the RXMODE setting is ignored as long as it is not a test mode. These modes determine the RXST status reporting. The different receive modes are listed in *Table 12*.

Table 12. Receive Operating Modes

RX Mode		RXST Status Reporting
Mode Number	RXMODE	
0	L	Status A
1	M	Reserved for test
2	H	Status B

Power Control

The CYP(V)(W)15G0101DXB supports user control of the powered up or down state of the Transmit and Receive channel. The Receive channel is controlled by the RXLE signal and the values present on the BOE[1:0] bus. The Transmit channel is controlled by the OELE signal and the values present on the BOE[1:0] bus. If either the Transmit or the Receive channel is not used, then powering down the unused channel will save power and reduce system heat generation. Controlling system power dissipation will improve the system performance.

Receive Channel

When RXLE = HIGH, the signal on the BOE[0] input directly controls the power enable for the receive PLL and the analog circuit. When BOE[0] = HIGH, the Receive channel and its analog circuits are active. When BOE[0] = LOW, the Receive channel and its analog circuits are powered down. When RXLE returns LOW, the values present on the BOE[1:0] inputs are latched in the Receive Channel Enable Latch. When a disabled receive channel is re-enabled, the status of the LFI output and data on the parallel outputs for the Receive channel may be indeterminate for up to 2 ms.

Transmit Channel

When OELE = HIGH, the signals on the BOE[1:0] inputs directly control the power enables for the Serial Drivers. When a BOE[1:0] input is HIGH, the associated Serial Driver is enabled. When a BOE[1:0] input is LOW, the associated Serial Driver is disabled. When both Serial Drivers are powered down, the logic in the entire transmit channel is also powered down. When OELE returns LOW, the values present on the BOE[1:0] inputs are latched in the Output Enable Latch.

Device Reset State

When the CYP(V)(W)15G0101DXB is reset by assertion of TRSTZ, both the Transmit Enable and Receive Enable Latches are cleared, and the BIST Enable Latch is preset. In this state, the Transmit and Receive channels are disabled, and BIST is disabled.

Following a device reset, it is necessary to enable the transmit and receive channels for normal operation. This can be done by sequencing the appropriate values on the BOE[1:0] inputs while the OELE and RXLE signals are raised and lowered. For systems that do not require dynamic control of power, or want the part to power up in a fixed configuration, it is also possible to strap the RXLE and OELE control signals HIGH to permanently enable their associated latches. Connection of the associated BOE[1:0] signals to a stable HIGH will then enable the Transmit and Receive channels as soon as the TRSTZ signal is deasserted.

Output Bus

The receive channel presents a 12-signal output bus consisting of

- an eight-bit data bus
- a three-bit status bus
- a parity bit.

The bit assignments of the Data and Status are dependent on the setting of DECMODE. This mapping is shown in *Table 13*.

Table 13. Output Register Bit Assignments[15]

Signal Name	DECMODE = LOW	DECMODE = MID or HIGH
RXST[2] (LSB)	COMDET	RXST[2]
RXST[1]	DOUT[0]	RXST[1]
RXST[0]	DOUT[1]	RXST[0]
RXD[0]	DOUT[2]	RXD[0]
RXD[1]	DOUT[3]	RXD[1]
RXD[2]	DOUT[4]	RXD[2]
RXD[3]	DOUT[5]	RXD[3]
RXD[4]	DOUT[6]	RXD[4]
RXD[5]	DOUT[7]	RXD[5]
RXD[6]	DOUT[8]	RXD[6]
RXD[7] (MSB)	DOUT[9]	RXD[7]

When the 10B/8B Decoder is bypassed (DECMODE = LOW), the framed 10-bit character is presented to the receiver Output Register, along with a status output (COMDET) indicating if the character in the Output Register is one of the selected framing characters. The bit usage and mapping of the external signals to the raw 10B transmission character is shown in *Table 14*.

Table 14. Decoder Bypass Mode (DECMODE = LOW)

Signal Name	Bus Weight	10B Name
RXST[2] (LSB)	COMDET	
RXST[1]	2^0	a
RXST[0]	2^1	b
RXD[0]	2^2	c
RXD[1]	2^3	d
RXD[2]	2^4	e
RXD[3]	2^5	i
RXD[4]	2^6	f
RXD[5]	2^7	g
RXD[6]	2^8	h
RXD[7] (MSB)	2^9	j

Note:
15. The RXOP output is also driven from the Output Register, but its interpretation is under the separate control of PARCTL.

The COMDET output is HIGH when the character in the Output Register contains the selected framing character at the proper character boundary, and LOW for all other bit combinations.

When the Low-Latency Framer and half-rate receive port clocking is also enabled (RFMODE = LOW, RXRATE = HIGH, and RXCKSEL = MID), the Framer will stretch the recovered clock to the nearest 20-bit boundary such that the rising edge of RXCLK+ occurs when COMDET = HIGH in the Output Register.

When the Cypress or Alternate-mode Framer is enabled and half-rate receive port clocking is also enabled (RFMODE ≠ LOW and RXRATE = HIGH), the output clock is not modified when framing is detected, but a single pipeline stage may be added or subtracted from the data stream by the Framer logic such that the rising edge of RXCLK+ occurs when COMDET = HIGH in the Output Register. This adjustment only occurs when the Framer is enabled (RFEN = HIGH). When the Framer is disabled, the clock boundaries are not adjusted, and COMDET may be asserted during the rising edge of RXCLK– (if an odd number of characters were received following the initial framing).

Parity Generation

In addition to the eleven data and status bits that are presented, an RXOP parity output is also available. This allows the CYP(V)(W)15G0101DXB to support ODD parity generation. To handle a wide range of system environments, the CYP(V)(W)15G0101DXB supports different forms of parity generation (in addition to no parity). When the Decoder is enabled (DECMODE ≠ LOW), parity can be generated on

- the RXD[7:0] character
- the RXD[7:0] character and RXST[2:0] status.

When the Decoder is bypassed (DECMODE = LOW), parity can be generated on

- the RXD[7:0] and RXST[1:0] bits
- the RXD[7:0] and RXST[2:0] bits.

These modes differ in the number of bits which are included in the parity calculation. For all cases, only ODD parity is provided which ensures that at least one bit of the data bus is always a logic-1. Those bits covered by parity generation are listed in *Table 15*.

Parity generation is enabled through the 3-level select PARCTL input. When PARCTL = LOW, parity checking is disabled, and the RXOP output is disabled (High-Z).

When PARCTL = MID (open) and the Decoder is enabled (DECMODE ≠ LOW), ODD parity is generated for the received and decoded character in the RXD[7:0] signals and is presented on the RXOP output.

When PARCTL = MID (open) and the Decoder is bypassed (DECMODE = LOW), ODD parity is generated for the received and decoded character in the RXD[7:0] and RXST[1:0] bit positions.

Table 15. Output Register Parity Generation

Signal Name	Receive Parity Generate Mode (PARCTL)			
		MID		
	LOW[16]	DECMODE = LOW	DECMODE ≠ LOW	HIGH
RXST[2]				X[17]
RXST[1]		X		X
RXST[0]		X		X
RXD[0]		X	X	X
RXD[1]		X	X	X
RXD[2]		X	X	X
RXD[3]		X	X	X
RXD[4]		X	X	X
RXD[5]		X	X	X
RXD[6]		X	X	X
RXD[7]		X	X	X

When PARCTL = HIGH, ODD parity is generated for the TXD[7:0] and the RXST[2:0] status bits.

Receive Status Bits

When the 10B/8B Decoder is enabled (DECMODE ≠ LOW), each character presented at the Output Register includes three associated status bits. These bits are used to identify

- if the contents of the data bus are valid
- the type of character present
- the state of receive BIST operations (regardless of the state of DECMODE)
- character violations.

These conditions normally overlap; e.g., a valid data character received with incorrect running disparity is not reported as a valid data character. It is instead reported as a Decoder violation of some specific type. This implies a hierarchy or priority level to the various status bit combinations. The hierarchy and value of each status is listed in *Table 16*.

Within these status decodes, there are three forms of status reporting. The two normal or data status reporting modes (Type A and Type B) are selectable through the RXMODE input. These status types allow compatibility with legacy systems, while allowing full reporting in new systems. The third status type is used for reporting receive BIST status and progress.

BIST Status State Machine

When the receive path is enabled to look for and compare the received data stream with the BIST pattern, the RXST[2:0] bits identify the present state of the BIST compare operation.

Notes:

16. Receive path parity output driver (RXOP) is disabled (High-Z) when PARCTL = LOW.
17. When the Decoder is bypassed (DECMODE = LOW) and BIST is not enabled (Receive BIST Latch output is HIGH), RXST[2] is driven to a logic-0, except when the character in the output buffer is a framing character.

The BIST state machine has multiple states, as shown in *Figure 2* and *Table 16*. When the receive PLL detects an out-of-lock condition, the BIST state is forced to the Start-of-BIST state, regardless of the present state of the BIST state machine. If the number of detected errors ever exceeds the number of valid matches by greater than 16, the state machine is forced to the WAIT_FOR_BIST state where it monitors the interface for the first character (D0.0) of the next BIST sequence. Also, if the Elasticity Buffer ever hits and overflow/underflow condition, the status is forced to the BIST_START until the buffer is re-centered (approximately nine character periods).

To ensure compatibility between the source and destination systems when operating in BIST, the sending and receiving ends of the BIST sequence must use the same clock setup (RXCKSEL = MID or RXCKSEL = LOW).

JTAG Support

The CYP(V)(W)15G0101DXB contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, only boundary scan is supported. This capability is present only on the LVTTL inputs, LVTTL outputs and the REFCLK± clock input. The high-speed serial inputs and outputs are not part of the JTAG test chain.

JTAG ID

The JTAG device ID for the CYP(V)(W)15G0101DXB is “1C804069”x.

3-Level Select Inputs

Each 3-Level select input reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11, respectively.

Table 16. Receive Character Status Bits

RXST[2:0]	Priority	Description		
		Type-A Status	Type-B Status	Receive BIST Status (Receive BIST = Enabled)
000	7	**Normal Character Received**. The valid Data character on the output bus meets all the formatting requirements of Data characters listed in *Table 20*.		**BIST Data Compare**. Character compared correctly
001	7	**Special Code Detected**. The valid special character on the output bus meets all the formatting requirements of the Special Code characters listed in *Table 21*, but is not the presently selected framing character or a Decoder violation indication.		**BIST Command Compare**. Character compared correctly
010	2	**Receive Elasticity Buffer Underrun/Overrun Error**. The receive buffer was not able to add/drop a K28.5 or framing character.	RESERVED	**BIST Last Good**. Last Character of BIST sequence detected and valid.
011	5	**Framing Character Detected**. This indicates that a character matching the patterns identified as a framing character (as selected by FRAMCHAR) was detected. The decoded value of this character is present on the output bus.		RESERVED
100	4	**Codeword Violation**. The character on the output bus is a C0.7. This indicates that the received character cannot be decoded into any valid character.		**BIST Last Bad**. Last Character of BIST sequence detected invalid.
101	1	**PLL Out of Lock**. This indicates a PLL Out of Lock condition.		**BIST Start**. Receive BIST is enabled on this channel, but character compares have not yet commenced. This also indicates a PLL Out of Lock condition, and Elasticity Buffer overflow/underflow conditions.
110	6	**Running Disparity Error**. The character on the output bus is a C4.7, C1.7, or C2.7.		**BIST Error**. While comparing characters, a mismatch was found in one or more of the decoded character bits.
111	3	RESERVED		**BIST Wait**. The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

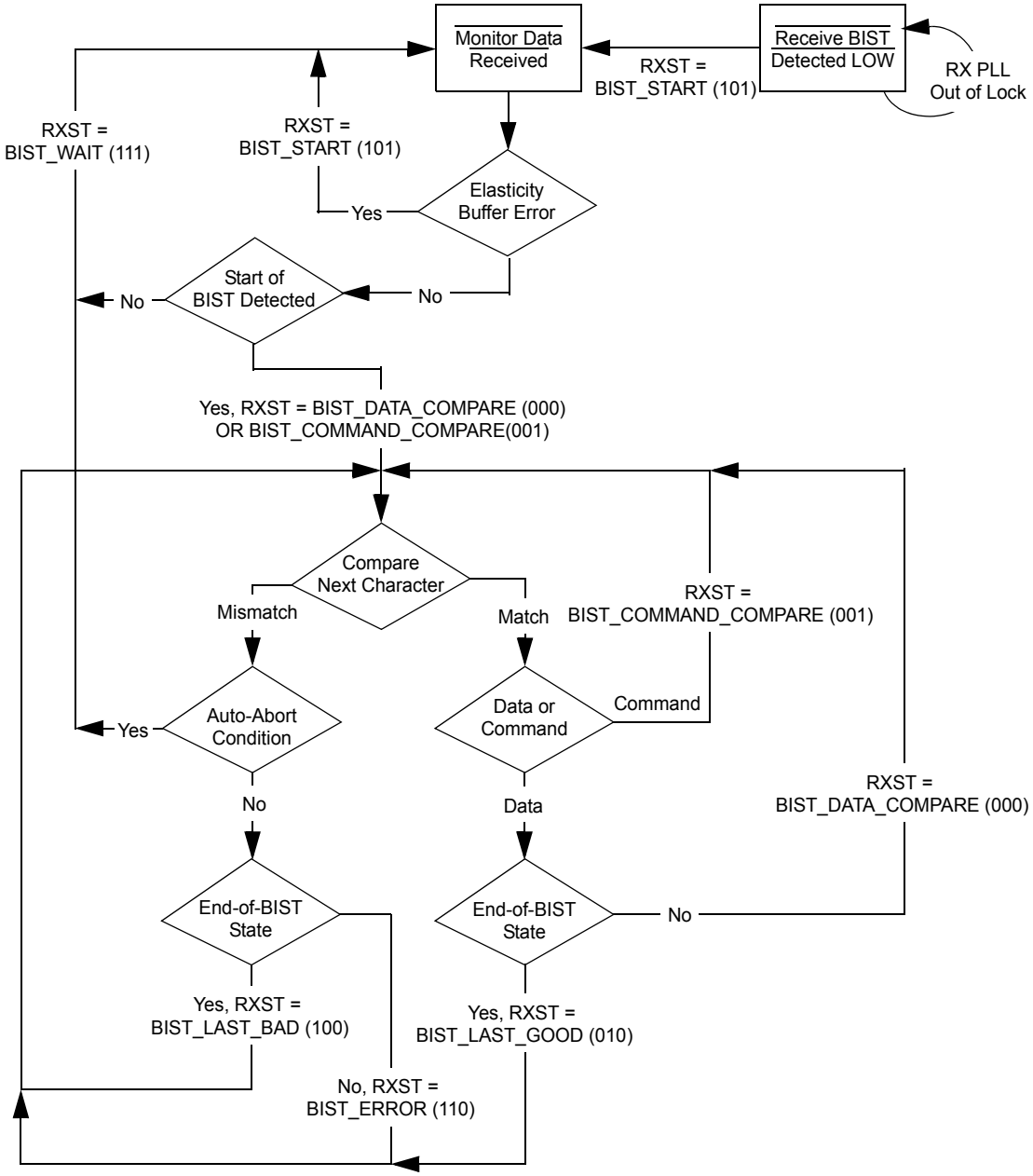


Figure 2. Receive BIST State Machine

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +3.8V

DC Voltage Applied to LVTTL Outputs in High-Z State .....–0.5V to V_{CC} + 0.5V

Output Current into LVTTL Outputs (LOW).....60 mA

DC Input Voltage.....–0.5V to V_{CC} + 0.5V

Static Discharge Voltage..... > 2000 V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Power-up Requirements

The CYP(V)(W)15G0101DXB requires one power-supply. The voltage on any input or I/O pin cannot exceed the power pin during power-up.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ± 5%
Industrial	–40°C to +85°C	+3.3V ± 5%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL-compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = – 4 mA, V_{CC} = Min.	2.4	V_{CC}	V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{CC} = Min.	0	0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[18]	–20	–100	mA
I_{OZL}	High-Z Output Leakage Current		–20	20	µA
LVTTL-compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK Input, V_{IN} = V_{CC}		1.5	mA
		Other Inputs, V_{IN} = V_{CC}		+40	µA
I_{ILT}	Input LOW Current	REFCLK Input, V_{IN} = 0.0V		–1.5	mA
		Other Inputs, V_{IN} = 0.0V		-40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: REFCLK±					
V_{DIFF}[19]	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.2	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		0.0	V_{CC} / 2	V
V_{COMREF}[20]	Common Mode Range		1.0	V_{CC} – 1.2	V
3-Level Inputs					
V_{IHH}	3-Level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	3-Level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	3-Level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}		200	µA
I_{IMM}	Input MID Current	V_{IN} = V_{CC}/2	–50	50	µA
I_{ILL}	Input LOW Current	V_{IN} = GND		–200	µA
Differential CML Serial Outputs: OUT1±, OUT2±					
V_{OHC}	Output HIGH Voltage (V_{CC} referenced)	100Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
		150Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V

Notes:

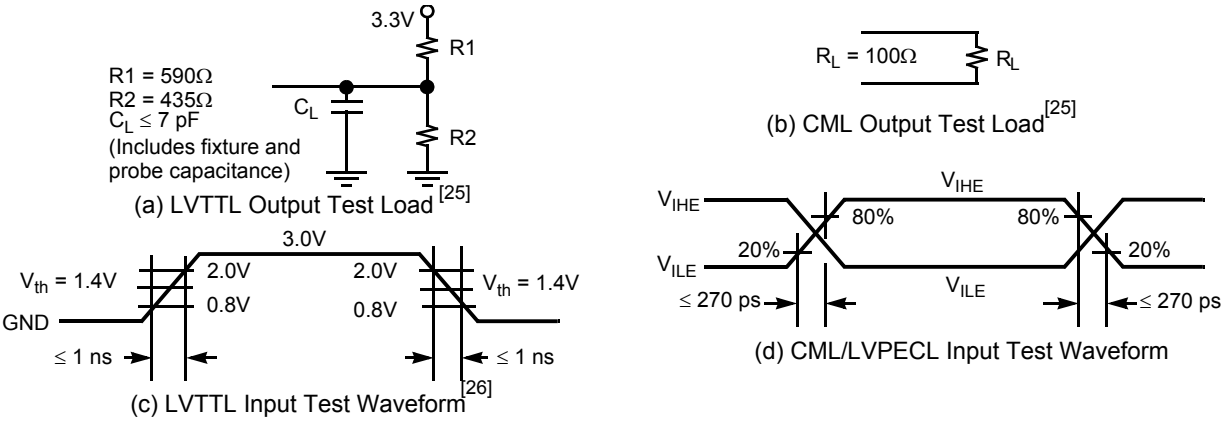
18. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
19. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
20. The common mode range defines the allowable range of REFCLK+ and REFCLK– when REFCLK+ = REFCLK–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

DC Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OLC}	Output LOW Voltage (V_{CC} referenced)	100Ω differential load	V_{CC} – 1.4	V_{CC} – 0.7	V
		150Ω differential load	V_{CC} – 1.4	V_{CC} – 0.7	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100Ω differential load	450	900	mV
		150Ω differential load	560	1000	mV
Differential Serial Line Receiver Inputs: IN1±, IN2±					
V_{DIFFS} [19]	Input Differential Voltage |(IN+) – (IN–)|		100	1200	mV
V_{IHE}	Highest Input HIGH Voltage			V_{CC}	V
V_{ILE}	Lowest Input LOW Voltage		V_{CC} – 2.0		V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHE}$ Max.		1350	µA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILE}$ Min.	–700		µA
V_{COM} [21, 22]	Common Mode Input Range		V_{CC} – 1.95	V_{CC} – 0.05	V

Power Supply			Typ. [24]	Max. [23]	Unit
I_{CC}	Power Supply Current REFCLK= Max.	Commercial	390	500	mA
		Industrial		510	mA
I_{CC}	Power Supply Current REFCLK= 125 MHz	Commercial	390	500	mA
		Industrial		510	mA

AC Test Loads and Waveforms



CYP(V)(W)15G0101DXB AC Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
Transmitter LVTTL Switching Characteristics				
f_{TS}	TXCLK Clock Frequency	19.5	150[27]	MHz
t_{TXCLK}	TXCLK Period	6.66[28]	51.28	ns
t_{TXCLKH} [29]	TXCLK HIGH Time	2.2		ns
t_{TXCLKL} [29]	TXCLK LOW Time	2.2		ns
t_{TXCLKR} [29, 30, 31]	TXCLK Rise Time	0.2	1.7	ns

Notes:

21. The common mode range defines the allowable range of INPUT+ and INPUT– when INPUT+ = INPUT–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.
22. Not applicable for AC-coupled interfaces. For AC-coupled interfaces, V_{DIFFS} requirement still needs to be satisfied.
23. Maximum I_{CC} is measured with V_{CC} = MAX, with all Serial Drivers enabled, parallel outputs unloaded, sending a alternating 01 pattern to the Serial Input Receiver.
24. Typical I_{CC} is measured under similar conditions except with V_{CC} = 3.3V, T_A = 25°C, parallel outputs unloaded, RXCKSEL = MID, and with one Serial Line Driver sending a continuous alternating 01 pattern to the Serial Input Receiver.
25. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only. 5pF differential load reflects tester capacitance, and is recommended at low data rates only.
26. The LVTTL switching threshold is 1.4V. All timing references are made relative to the point where the signal edges crosses this threshold voltage.
27. This parameter is 154 MHz for CYW15G0101DXB.
28. This parameter is 6.49 ns for CYW15G0101DXB.
29. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
30. The ratio of rise time to falling time must not vary by greater than 2:1.
31. For a given operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.

CYP(V)(W)15G0101DXB AC Characteristics Over the Operating Range (continued)

Parameter	Description	Min.	Max.	Unit
t_{TXCLKF} [29, 30, 31]	TXCLK Fall Time	0.2	1.7	ns
t_{TXDS}	Transmit Data Set-Up Time to TXCLK↑ (TXCKSEL ≠ LOW)	1.7		ns
t_{TXDH}	Transmit Data Hold Time from TXCLK↑ (TXCKSEL ≠ LOW)	0.8		ns
f_{TOS}	TXCLKO Clock Frequency = 1x or 2x REFCLK Frequency	19.5	150[27]	MHz
t_{TXCLKO}	TXCLKO Period	6.66[28]	51.28	ns
$t_{TXCLKOD+}$	TXCLKO+ Duty Cycle with 60% HIGH time	–1.0	+0.5	ns
$t_{TXCLKOD–}$	TXCLKO– Duty Cycle with 40% HIGH time	–0.5	+1.0	ns
Receiver LVTTL Switching Characteristics				
f_{RS}	RXCLK Clock Output Frequency	9.75	150[27]	MHz
t_{RXCLKP}	RXCLK Period	6.66[28]	102.56	ns
t_{RXCLKH}	RXCLK HIGH Time (RXRATE = LOW)	2.33 [29]	26.64	ns
	RXCLK HIGH Time (RXRATE = HIGH)	5.66	52.28	ns
t_{RXCLKL}	RXCLK LOW Time (RXRATE = LOW)	2.33 [29]	26.64	ns
	RXCLK LOW Time (RXRATE = HIGH)	5.66	52.28	ns
t_{RXCLKD}	RXCLK Duty Cycle centered at 50%	–1.0	+1.0	ns
t_{RXCLKR}[29]	RXCLK Rise Time	0.3	1.2	ns
t_{RXCLKF}[29]	RXCLK Fall Time	0.3	1.2	ns
$t_{RXDV–}$[32]	Status and Data Valid Time to RXCLK (RXCKSEL = MID)	5UI – 1.5		ns
	Status and Data Valid Time to RXCLK (HALF RATE RECOVERED CLOCK)	5UI – 1.0		ns
t_{RXDV+}[32]	Status and Data Valid Time From RXCLK (RXCKSEL = MID)	5UI – 1.8		ns
	Status and Data Valid Time From RXCLK (HALF RATE RECOVERED CLOCK)	5UI – 2.3		ns
REFCLK Switching Characteristics Over the Operating Range				
f_{REF}	REFCLK Clock Frequency	19.5	150[27]	MHz
t_{REFCLK}	REFCLK Period	6.6[28]	51.28	ns
t_{REFH}	REFCLK HIGH Time (TXRATE = HIGH)	5.9		ns
	REFCLK HIGH Time (TXRATE = LOW)	2.9[29]		ns
t_{REFL}	REFCLK LOW Time (TXRATE = HIGH)	5.9		ns
	REFCLK LOW Time (TXRATE = LOW)	2.9[29]		ns
t_{REFD}[33]	REFCLK Duty Cycle	30	70	%
t_{REFR}[29, 30, 31]	REFCLK Rise Time (20% – 80%)		2	ns
t_{REFF}[29, 30, 31]	REFCLK Fall Time (20% – 80%)		2	ns
t_{TREFDS}	Transmit Data Setup Time to REFCLK (TXCKSEL = LOW)	1.7		ns
t_{TREFDH}	Transmit Data Hold Time from REFCLK (TXCKSEL = LOW)	0.8		ns
t_{RREFDA}[34]	Receive Data Access Time from REFCLK (RXCKSEL = LOW)		9.5	ns
t_{RREFDV}	Receive Data Valid Time from REFCLK (RXCKSEL = LOW)	2.5		ns
$t_{REFDV–}$	Received Data Valid Time to RXCLK (RXCKSEL = LOW)	10UI – 4.7		ns
t_{REFDV+}	Received Data Valid Time from RXCLK (RXCKSEL = LOW)	0.5		ns
$t_{REFCDV–}$	Received Data Valid Time to RXCLKC (RXCKSEL = LOW)	10UI – 4.3		ns
$t_{REFCDV+}$	Received Data Valid Time from RXCLKC (RXCKSEL = LOW)	–0.2		ns
t_{REFRX}[10, 29]	REFCLK Frequency Referenced to Extracted Received Clock Frequency	–1500	+1500	ppm

Notes:

32. Parallel data output specifications are only valid if all inputs or outputs are loaded with similar DC and AC loads.
33. The duty cycle specification is a simultaneous condition with the t_{REFH} and t_{REFL} parameters. This means that at faster character rates the REFCLK duty cycle cannot be as large as 30%–70%.
34. Since this timing parameter is greater than the minimum time period of REFCLK it sets an upper limit to the frequency in which REFCLKx can be used to clock the receive data out of the output register. For predictable timing, users can use this parameter only if REFCLK period is greater than sum of t_{RREFDA} and set-up time of the upstream device. When this condition is not true, RXCLKC± or RXCLKA± (a buffered or delayed version of REFCLK when RXCKSELx = LOW) could be used to clock the receive data out of the device.