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CYW20705

Single-Chip Bluetooth Transceiver and Baseband Processor

The Cypress CYW20705 is a monolithic, single-chip, Bluetooth 4.1 compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. Manufactured using the industry's most advanced 65 nm CMOS low-power process, the CYW20705 employs the highest level of integration, eliminating all critical external components, and thereby minimizing the device's footprint and costs associated with the implementation of Bluetooth solutions.

The CYW20705 is the optimal solution for voice and data applications that require a Bluetooth SIG standard Host Controller Interface (HCI) via USB, UART H4 or H5, and PCM audio interface support. The CYW20705 radio transceiver's enhanced radio performance meets the most stringent industrial temperature application requirements for compact integration into mobile handset and portable devices. The CYW20705 is fully compatible with all standard TCXO frequencies and provides full radio compatibility, enabling it to operate simultaneously with GPS and cellular radios.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20705	CYW20705
BCM20705A1KWFBG	CYW20705A1KWFBG
BCM20705B0KWFBG	CYW20705B0KWFBG

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to:
http://www.cypress.com/glossary

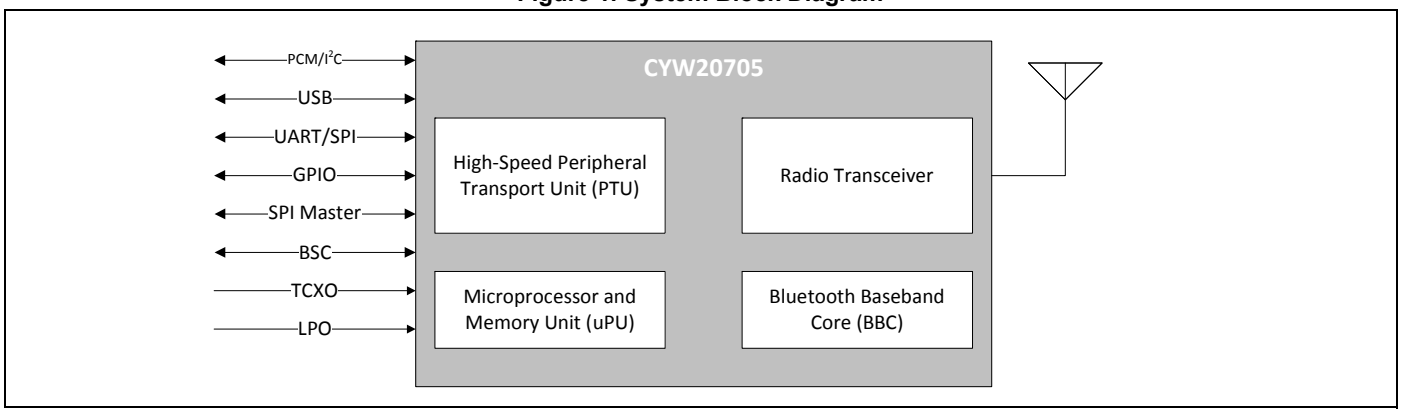
Features

- Bluetooth 4.1 + EDR compliant
- Class 1 capable with built-in PA
- Programmable output power control meets Class 1, Class 2, or Class 3 requirements
- Use supply voltages up to 5.5V
- Supports Cypress SmartAudio™, wide-band speech, SBC codec, and packet loss concealment.
- Fractional-N synthesizer supports frequency references from 12 MHz to 52 MHz
- Automatic frequency detection for standard crystal and TCXO values when an external 32.768 kHz reference clock is provided.
- Ultra-low power consumption
- Supports serial flash interfaces
- Available in a 50-ball FPBGA package.
- ARM7TDMI-S™–based microprocessor with integrated ROM and RAM
- Supports mobile and PC applications without external memory
- A USB hub

Appliactions

- Desktop and laptop personal computers
- Computer peripheral devices (PCMCIA cards, CF cards, and USB dongles)
- Personal digital assistants
- Automotive telematic systems

Figure 1. System Block Diagram



IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

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1. Overview

The Cypress CYW20705 complies with Bluetooth Core Specification, version 4.1 and is designed for use in standard Host Controller Interface (HCI) UART and HCI USB applications. The combination of the Bluetooth Baseband Core (BBC), a Peripheral Transport Unit (PTU), and an ARM®-based microprocessor with on-chip ROM provides a complete lower layer Bluetooth protocol stack, including the Link Controller (LC), Link Manager (LM), and HCI.

1.1 Major Features

Major features of the CYW20705 include:

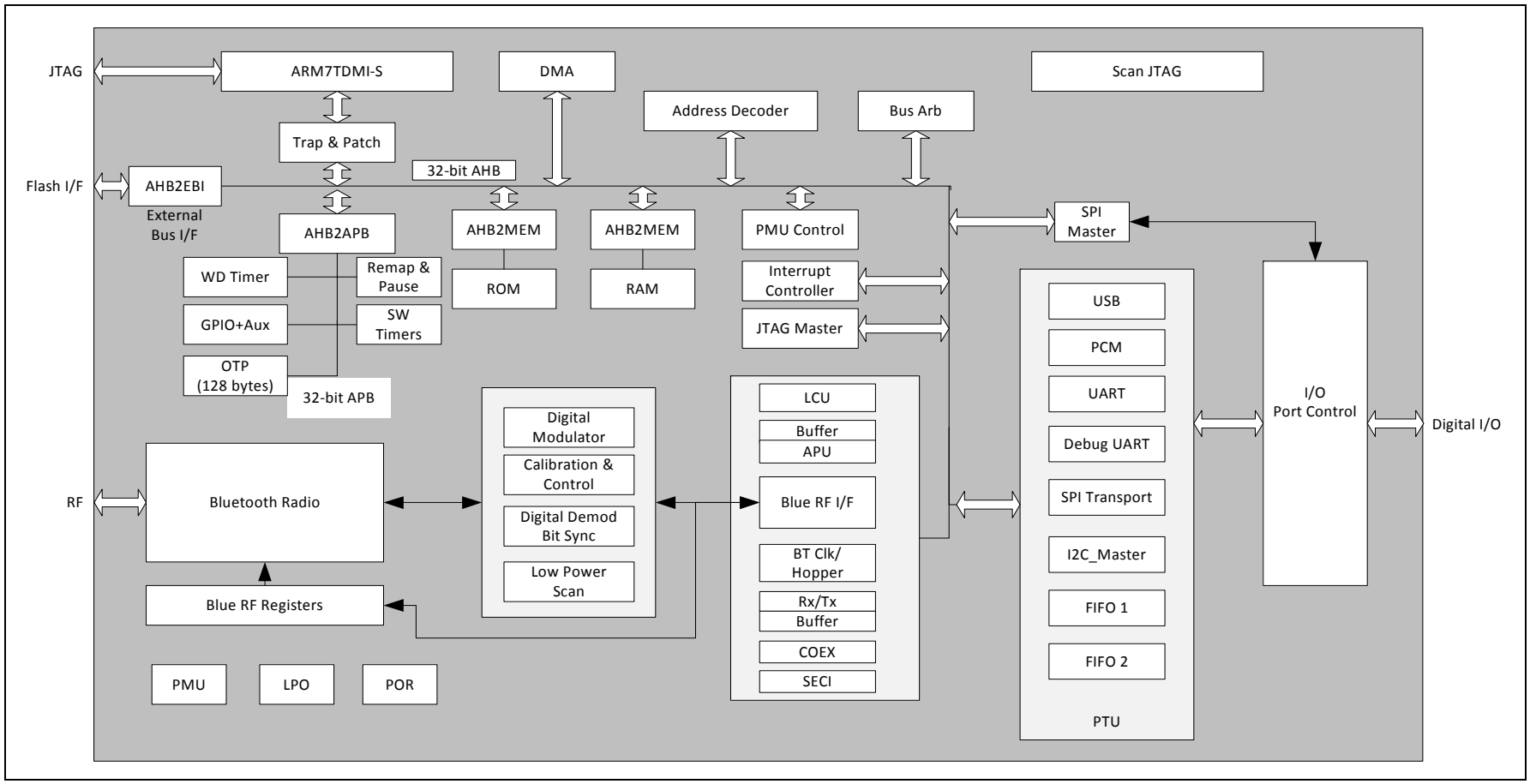
- Support for Bluetooth 4.1 + EDR including the following options:
  - A whitelist size of 25.
  - Enhanced Power Control
  - HCI Read Encryption Key Size command
- Full support for Bluetooth 2.1 + EDR additional features:
  - Secure Simple Pairing (SSP)
  - Encryption Pause Resume (EPR)
  - Enhance Inquiry Response (EIR)
  - Link Supervision Time Out (LSTO)
  - Sniff SubRating (SSR)
  - Erroneous Data (ED)
  - Packet Boundary Flag (PBF)
- Built-in Low Drop-Out (LDO) regulators (2)
  - 1.63 to 5.5V input voltage range
  - 1.8 to 3.3V intermediate programmable output voltage
- Integrated RF section
  - Single-ended, 50 ohm RF interface
  - Built-in TX/RX switch functionality
  - TX Class 1 output power capability
  - RX sensitivity basic rate of –88 dBm
  - RX sensitivity for Low Energy of –92 dBm
- Supports maximum Bluetooth data rates over HCI UART, USB, and SPI interfaces
- Multipoint operation, with up to 7 active slaves
  - Maximum of 7 simultaneous active ACL links
  - Maximum of 3 simultaneous active SCO and eSCO links, with Scatternet support
- Scatternet operation, with up to 4 active piconets (with background scan and support for ScatterMode)
- High-speed HCI UART transport support
  - H4 five-wire UART (four signal wires, one ground wire)
  - H5 three-wire UART (two signal wires, one ground wire)
  - Maximum UART baud rates of 4 Mbps
  - Low-power out-of-band BT_WAKE and HOST_WAKE signaling
  - VSC from host transport to UART
  - Proprietary compressing scheme (allows more than 2 simultaneous A2DP packets and up to 5 devices at a time)
- HCI USB transport support
  - USB version 2.0 full-speed compliant interface
  - Full USB hub
  - UHE (proprietary method for emulating a Human Interface Device (HID) at system bootup)
- Channel Quality-Driven Data Rate (CQDDR) and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features

- Full support for power savings modes:
  - Bluetooth standard sniff
  - Deep sleep modes and regulator shutdown
- Supports Wide-Band Speech (WBS) over PCM and Packet Loss Concealment (PLC) for better audio quality
- 2-, 3-, and 4-wire coexistence
- Power Amplifier (PA) shutdown for externally controlled coexistence, such as WIMAX
- Built-in LPO clock or operation using an external LPO clock
- TCXO input and auto-detection of all standard handset clock frequencies (supports low-power crystal, which can be used during Power Saving mode with better timing accuracy)
- OR gate for combining a host clock request with a Bluetooth clock request (operates even when the Bluetooth core logic is powered off)
- Larger patch RAM space to support future enhancements
- Serial flash Interface with native support for devices from several manufacturers
- One-Time Programmable (OTP) memory

1.2 Block Diagram

Figure 2 shows the interconnect of the major CYW20705 physical blocks and associated external interfaces.

Figure 2. Functional Block Diagram



1.3 Usage Model

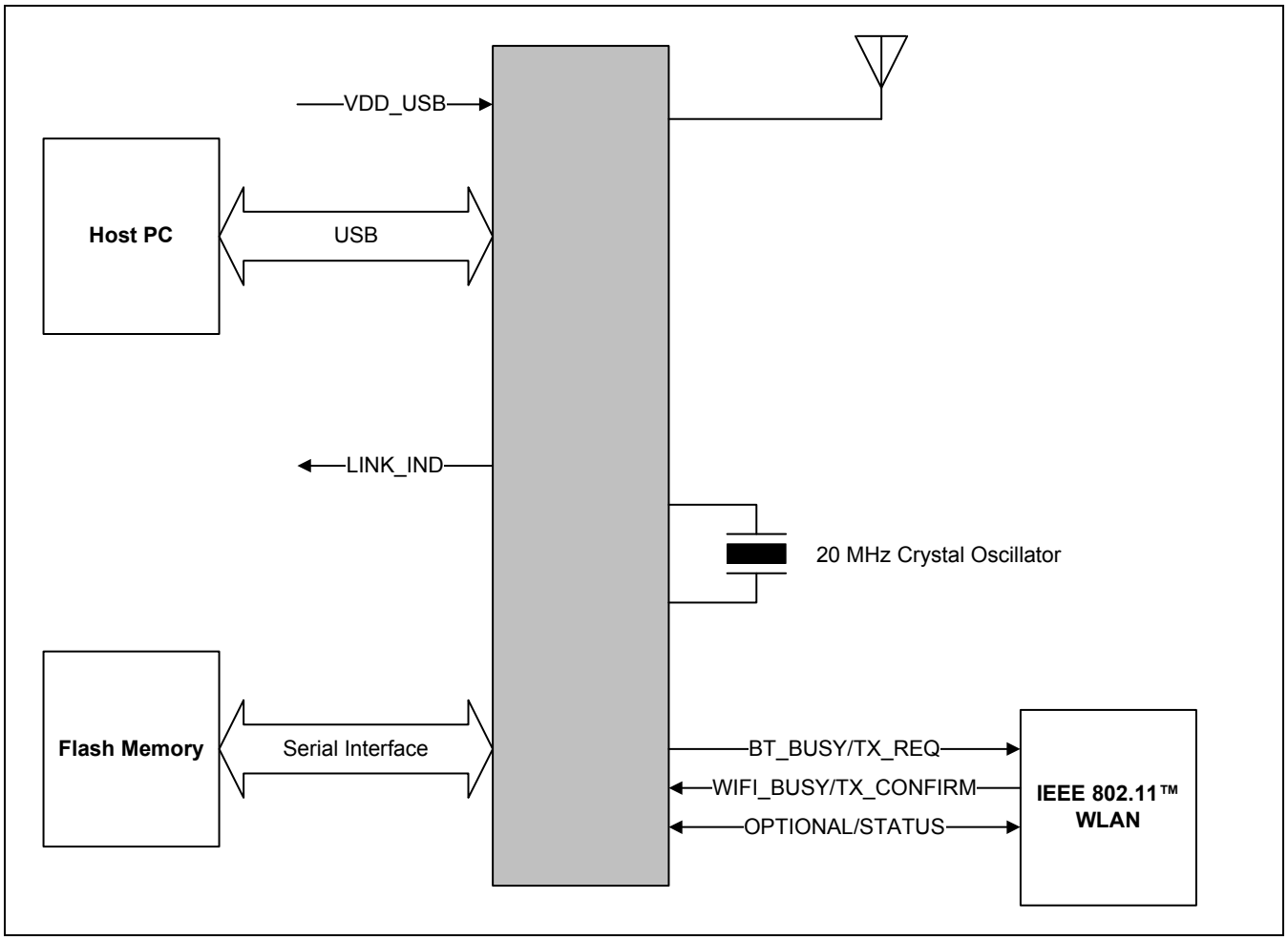
This section contains information on the PC Product Usage Model.

1.3.1 PC Product Usage Model

The CYW20705 can be directly interfaced using the HCI USB interface, providing full support for embedded USB applications like laptops and PC motherboards. The CYW20705 also supports PC applications as an external USB dongle peripheral device.

Figure 3 shows an example of a PC product usage model.

Figure 3. PC Product Usage Model



2. Integrated Radio Transceiver

The CYW20705 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The CYW20705 is fully compliant with the Bluetooth Radio Specification and enhanced data rate specification and meets or exceeds the requirements to provide the highest communication link quality of service.

2.1 Transmitter Path

The CYW20705 features a fully integrated zero IF transmitter. The baseband transmitted data is digitally modulated in the modem block and up-converted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q up-conversion, a high-output power amplifier (PA), and RF filtering.

The CYW20705 also incorporates modulation schemes to support enhanced data rates.

- P/4-DQPSK for 2 Mbps
- 8-DPSK for 3 Mbps

2.1.1 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, Π/4DQPSK, and 8-DPSK signals. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

2.1.2 Power Amplifier

The CYW20705 integrated PA can be configured for Class 2 operation, transmitting up to +4 dBm. The PA can also be configured for Class 1 operation, transmitting up +10 dBm at the chip in gFSK mode, when a minimum supply voltage of 2.5V is applied to VDDTF.

Because of the linear nature of the PA, combined with integrated filtering, minimal external filtering is required to meet Bluetooth and regulatory harmonic and spurious requirements.

Using a highly linearized, temperature compensated design, the PA can transmit +10 dBm for basic rate and +8 dBm for enhanced data rates (2 to 3 Mbps). A flexible supply voltage range allows the PA to operate from 1.2V to 3.3V. A minimum supply voltage of 2.5V is required at VDDTF to achieve +10 dBm of transmit power.

2.2 Receiver Path

The receiver path uses a low IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the device to be used in most applications without off-chip filtering. For integrated handset operation where the Bluetooth function is integrated close to the cellular transmitter, minimal external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

2.2.1 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer uses the low IF received signal to perform an optimal frequency tracking and bit synchronization algorithm.

2.2.2 Receiver Signal Strength Indicator

The CYW20705 radio provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

2.3 Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The device uses fully-integrated PLL loop filters.

2.4 Calibration

The radio transceiver features an automated calibration scheme that is fully self-contained in the radio. User interaction is not required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all major blocks in the radio, including gain and phase characteristics of filters, matching between key components, and key gain blocks. Calibration, which takes process and temperature variations into account, occurs transparently during the settling time of the hops, adjusting for temperature variations as the device cools and heats during normal operation.

2.5 Internal LDO

Two internal Low Drop-Out (LDO) voltage regulators eliminate the need for external voltage regulators and therefore reduce the BOM. The first LDO is a preregulator (HV LDO). The second LDO (Main LDO) supplies the main power to the CYW20705 (see Figure 4).

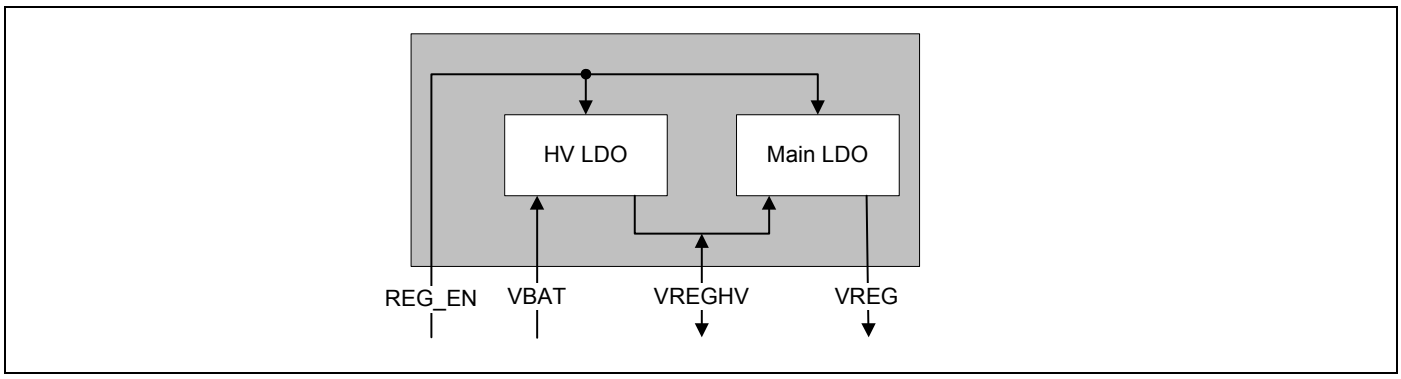
The HV LDO has an input voltage range of 2.3V to 5.5V. The input VBAT is ideal for batteries. The VREGHV output is programmable from 1.8V to 3.3V, in 100 mV steps. The dropout voltage is 200 mV. The HV LDO can supply up to 95 mA, which leaves spare power for external circuitry such as an RF power amp for higher transmit power. If the HV LDO is not used, to turn off the HV LDO and minimize current consumption, connect the VBAT input to the VREGHV output. Firmware can then disable the HV LDO, saving the quiescent current.

The HV LDO default output voltage is 2.9V, allowing this regulator to be used to power external NV memory devices, as well as the VDDO rail. The firmware can then adjust this output to as low as 1.8V, if desired, to power VDDTF.

The main LDO has a 1.22V output (VREG) and is used to supply main power to the CYW20705. The input of this LDO (VREGHV) has an input voltage range of from 1.63V to 3.63V. The output of the HV LDO is internally connected to the input to the main LDO. Power can be applied to VREGHV when the HV LDO is not used. The main LDO supplies power to the entire device for Class 2 operation. The main LDO can drive up to 60 mA, which leaves spare power for external circuitry. The main LDO is bypassed by not connecting anything to its output (VREG) and driving 1.12V–1.32V directly to VDDC and VDDRF.

REG_EN provides a control signal for the host to control power to the CYW20705. When power is enabled, the CYW20705 will require complete initialization.

Figure 4. LDO Functional Block Diagram



3. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements the time critical functions required for high-performance Bluetooth and Low Energy operation. The BBC manages buffering, segmentation, and data routing for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL Tx/Rx transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

3.1 Transmit and Receive Functions

The following transmit and receive functions are implemented in the BBC hardware to increase the reliability and security of the Tx/Rx data before sending the data over the air:

In the transmitter:

- Data framing
- Forward Error Correction (FEC) generation
- Header Error Control (HEC) generation
- Cyclic Redundancy Check (CRC) generation
- Key generation
- Data encryption
- Data whitening

In the receiver:

- Symbol timing recovery
- Data deframing
- FEC
- HEC
- CRC
- Data decryption
- Data dewhitening

3.2 Bluetooth 4.1 + EDR Features

The CYW20705 supports Bluetooth 4.1 + EDR and Low Energy, including the following options:

- A whitelist size of 25
- Enhanced Power Control
- HCI Read Encryption Key Size command

The CYW20705 provides full support for Bluetooth 2.1 + EDR additional features:

- Secure Simple Pairing (SSP)
- Encryption Pause Resume (EPR)
- Enhance Inquiry Response (EIR)
- Link Supervision Time Out (LSTO)
- Sniff SubRating (SSR)
- Erroneous Data (ED)
- Packet Boundary Flag (PBF)

3.3 Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number, based on the link controller state, Bluetooth clock, and device address.

3.4 Link Control Layer

The Link Control layer is part of the Bluetooth link control functions implemented in dedicated logic in the Link Control Unit (LCU). This layer consists of the Command Controller that takes commands from the software and other controllers that are activated or configured by the Command Controller to perform the link control tasks.

There are two major states–Standby and Connection. Each task establishes a different state in the Bluetooth Link Controller. In addition, there are eight substates—Page, Page Scan, Inquiry, Inquiry Scan, Sniff, and Sniff Subrating.

3.5 Test Mode Support

The CYW20705 fully supports Bluetooth Test Mode.

In addition to the standard Bluetooth Test mode, the device supports enhanced testing features to simplify RF debugging and qualification and type approval testing.

These test features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Directs receiver output to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant bit stream transmission
  - Unmodulated, 8-bit fixed pattern, PRBS-9, or PRBS-15
  - Enables modulated signal measurements with standard RF test equipment
- Packetized connectionless transmitter test
  - Hopping or fixed frequency
  - Multiple packet types supported
  - Multiple data patterns supported
- Packetized connectionless receiver test
  - Fixed frequency
  - Multiple packet types supported
  - Multiple data patterns supported

3.6 Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked through power management registers or packet handling in the baseband core. This section contains descriptions of the PMU features.

3.6.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions, accordingly.

3.6.2 Host Controller Power Management

The host can place the device in a sleep state, in which all nonessential blocks are powered off and all nonessential clocks are disabled. Power to the digital core is maintained so that the state of the registers and RAM is not lost. In addition, the LPO clock is applied to the internal sleep controller so that the chip can wake automatically at a specified time or based on signaling from the host. The goal is to limit the current consumption to a minimum, while maintaining the ability to wake up and resume a connection with minimal latency.

If a scan or sniff session is enabled while the device is in Sleep mode, the device automatically will wake up for the scan/sniff event, then go back to sleep when the event is done. In this case, the device uses its internal LPO-based timers to trigger the periodic wake up. While in Sleep mode, the transports are idle. However, the host can signal the device to wake up at any time. If signaled to wake up while a scan or sniff session is in progress, the session continues but the device will not sleep between scan/sniff events. Once Sleep mode is enabled, the wake signaling mechanism can also be thought of as a sleep signaling mechanism, since removing the wake status will often cause the device to sleep.

In addition to a Bluetooth device wake signaling mechanism, there is a host wake signaling mechanism. This feature provides a way for the Bluetooth device to wake up a host that is in a reduced power state.

There are two mechanisms for the device and the host to signal wake status to each other:

USB	When running in USB mode, the device supports the USB version 2.0 full-speed specification, suspend/resume signaling, as well as remote wake-up signaling for power control.
Bluetooth WAKE (BT_WAKE) and Host WAKE (and HOST_WAKE) signaling	The BT_WAKE pin (GPIO_0) allows the host to wake the BT device, and HOST_WAKE (GPIO_1) is an output that allows the BT device to wake the host.

When running in SPI mode, the CYW20705 has a mode where it enters Sleep mode when there is no activity on the SPI interface for a specified (programmable) amount of time. Idle mode is detected when the SPI_CSN is left deasserted. Whether to sleep on an idle interface and the amount of time to wait before entering Sleep mode can be programed by the host. Once the CYW20705 enters sleep, the host can wake it by asserting SPI_CSN. If the host decides to sleep, the CYW20705 will wake up the host by asserting SPI_INT when it has data for it.

Note: Successful operation of the power management handshaking signals requires coordinated support between the device firmware and the host software.

Table 2. Power Control Pin Summary

Pin	Direction	Description
BT_WAKE (GPIO_0)	Host output BT input	Bluetooth device wake-up: Signal from the host to the Bluetooth device that the host requires attention. ■Asserted = Bluetooth device must wake up or remain awake. ■Deasserted = Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. By default, BT_WAKE is active-low (if BT-WAKE is low it requires the device to wake up or remain awake). For USB applications, this can be used for setting Airport mode (radio disable mode).
HOST_WAKE (GPIO_1)	BT output Host input	Host wake-up. Signal from the Bluetooth device to the host indicating that Bluetooth device requires attention. ■Asserted = Host device must wake up or remain awake. ■Deasserted = Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ (GPIO_5)	BT output	Clock request ■Asserted = External clock reference required ■Deasserted = External clock reference may be powered down For the CYW20705A1KWFBG, the polarity of CLK_REQ is active low. For CYW20705B0KWFBG, the CLK_REQ function is only available as a configurable feature after firmware boot, which means it cannot be used to request a clock at boot time.
REG_EN	BT input	Enables the internal preregulator and main regulator outputs. REG_EN is active-high. ■1 = Enabled ■0 = Disabled

3.6.3 BBC Power Management

The device provides the following low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth specified low-power connection mode (Sniff). While in this low-power connection mode, the device runs on the Low Power Oscillator and wakes up after a predefined time period.

3.6.4 Backdrive Protection

The CYW20705 provides a backdrive protection feature that allows the device to be turned off while the host and other devices in the system remain operational. When the device is not needed in the system, VDD_RF and VDDC are shut down and VDDO remains powered. This allows the device to be effectively off, while keeping the I/O pins powered so that they do not draw extra current from other devices connected to the I/O.

Notes:

VDD_RF collectively refers to the VDDTF, VDDIF, VDDLNA, VDDPX, and VDDRF RF power supplies.
Never apply voltage to I/O pins if VDDO is not applied.

During the low power shutdown state and as long as VDDO remains applied to the device, all outputs are tristated and all digital and analog clocks are disabled. Input voltages must remain within the limits defined for normal operation. This is done to either prevent current draw and back loading on digital signals in the system. It also enables the device to be fully integrated in an embedded device and take full advantage of the lowest power savings modes. If VDDC is powered up externally (not connected to VREG), VDDC requires 750K ohms to ground during low-power shutdown. If VDDC is powered up by VREG, VDDC does not require 750K ohms to ground because the internal main LDO has about 750 K ohms to ground when turned off.

Several signals, including the frequency reference input (XTAL_IN) and external LPO input (LPO_IN), are designed to be high-impedance inputs that will not load down the driving signal, even if VDDO power is not applied to the chip. The other signals with back drive prevention are RST_N, COEX_IN, PCM_SYNC, PCM_CLK, PCM_OUT, PCM_IN, UART_RTS_N, UART_CTS_N, UART_RXD, UART_TXD, GPIO_0, GPIO_1, GPIO_4, GPIO_7, HUSB_DP, HUSB_DN, CFG_SEL, and OTP_DIS.

All other I/O signals must remain at VSS until VDDO is applied. Failing to do this can result in unreliable startup behavior.

When powered on, using REG_EN is the same as applying power to the CYW20705. The device does not have information about its state before being powered-down.

3.7 Adaptive Frequency Hopping

The CYW20705 supports host channel classification and dynamic channel classification Adaptive Frequency Hopping (AFH) schemes, as defined in the Bluetooth specification.

Host channel classification enables the host to set a predefined hopping map for the device to follow.

If dynamic channel classification is enabled, the device gathers link quality statistics on a channel-by-channel basis to facilitate channel assessment and channel map selection. To provide a more accurate frequency hop map, link quality is determined using both RF and baseband signal processing.

3.8 Collaborative Coexistence

The CYW20705 provides extensions and collaborative coexistence to the standard Bluetooth AFH for direct communication with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously in a single device. The device supports industry-standard coexistence signaling, including 802.15.2, and supports Cypress and third-party WLAN solutions.

Using a multitiered prioritization approach, relative priorities between data types and applications can be set. This approach maximizes the performance-WLAN data throughput vs. voice quality vs. link performance.

A PA shutdown pin is available to allow full external control of the RF output for other types of coexistence, such as WIMAX.

3.9 Serial Enhanced Coexistence Interface

The Serial Enhanced Coexistence Interface (Serial ECI or SECI) is a proprietary Cypress interface between Cypress WLAN devices and Bluetooth devices. It is an optional replacement to the legacy 3- or 4-wire coexistence feature, which is also available.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over a two-wire interface, one serial input (SECI_IN), and one serial output (SECI_OUT). The pad configuration registers must be programmed to choose the digital I/O pins that serve the SECI_IN and SECI_OUT function.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronizaton upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

3.9.1 SECI Advantages

The advantages of the SECI over the legacy 3-wire coexistence interface are:

- Only two wires are required: SECI_IN and SECI_OUT.
- Up to 48-bits of coexistence data can be exchanged.

Previous Cypress standalone Bluetooth devices such as the CYW2070 supported only a 3-wire or 4-wire coexistence interface. Previous Cypress WLAN and Bluetooth combination devices such as the CYW4325, CYW4329, and CYW4330 support an internal parallel enhanced coexistence interface for more efficient WLAN and Bluetooth information exchange. The SECI allows enhanced coexistence information to be passed to a companion Cypress WLAN chip through a serial interface using fewer I/O than the 3-wire coexistence scheme.

The 48-bits of the SECI significantly enhance WLAN and Bluetooth coexistence by sharing such information as frequencies used and radio usage times. The exact contents of the SECI are Cypress confidential.

3.9.2 SECI I/O

The CYW20705 does not have dedicated SECI_IN or SECI_OUT pins, but the two pin functions can be mapped to the following digital I/O: the UART, GPIO, SPI Master (or BSC), PCM, and COEX pins. Pin function mapping is controlled by the config file that is either stored in NVRAM or downloaded directly into on-chip RAM from the host.

4. Microprocessor Unit

4.1 Overview

The CYW20705 microprocessor unit runs software from the Link Control (LC) layer up to the Host Controller Interface (HCI). The microprocessor is based on the ARM7TDMIS 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The microprocessor also includes 448 KB of ROM memory for program storage and boot ROM, 132 KB of RAM for data scratch-pad, and patch RAM code.

Note: The CYW20705A1KWFBG part only contains 384 KB of ROM and 112 KB of RAM.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations, including automatic host transport selection from SPI, USB, or UART, with or without external NVRAM. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded from the host to the device through the SPI, USB, or UART transports, or using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

4.2 NVRAM Configuration Data and Storage

4.2.1 Serial Interface

The CYW20705 includes an SPI master controller that can be used to access serial flash memory. The SPI master contains an AHB slave interface, transmit and receive FIFOs, and the SPI core PHY logic. Data is transferred to and from the module by the system CPU. DMA operation is not supported.

The CYW20705 supports serial flash vendors Atmel®, MXIC, and Numonyx™. The most commonly used parts from two of these vendors are:

- AT25BCM512B, manufactured by Atmel
- MX25V512ZUI-20G, manufactured by MXIC

4.3 EEPROM

The CYW20705 includes a Broadcom Serial Control (BSC) master interface. The BSC interface supports low-speed and fast mode devices and is compatible with I^2C slave devices. Multiple I^2C master devices and flexible wait state insertion by the master interface or slave devices are not supported. The CYW20705 provides 400 kHz, full speed clock support.

The BSC interface is programmed by the CPU to generate the following BSC transfer types on the bus:

- Read-only
- Write-only
- Combined read/write
- Combined write-read

NVRAM may contain configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- USB enumeration information
- SDP service record
- File system information used for code, code patches, or data

4.4 External Reset

The CYW20705 has an integrated power-on reset circuit which completely resets all circuits to a known power on state. This action can also be driven by an external reset signal, which can be used to externally control the device, forcing it into a power-on reset state. The RST_N signal input is an active-low signal for all versions of the CYW20705. The CYW20705 requires an external pull-up resistor on the RST_N input. Alternatively, the RST_N input can be connected to REG_EN or driven directly by a host GPIO.

4.5 One-Time Programmable Memory

The CYW20705 includes a One-Time Programmable (OTP) memory, allowing manufacturing customization and avoiding the need for an on-board NVRAM.If customization is not required, then the OTP does not need to be programmed. Whether the OTP is programmed or not, it is disabled after the boot process completes to save power.

The OTP size is 128 bytes.

The OTP is designed to store a minimal amount of information. Aside from OTP data, most user configuration information will be downloaded into RAM after the CYW20705 boots up and is ready for host transport communication. The OTP contents are limited to:

- Parameters required prior to downloading user configuration to RAM.
- Parameters unique to each part and each customer (i.e., the BD_ADDR, software license key, and USB PID/VID).

The OTP memory is particularly useful in a PC design with USB transport capability because:

- Some customer-specific information must be configured before enumerating the part on the USB transport.
- Part or customer unique information (BD_ADDR, software license key, and USB PID/VID) do not need to be stored on the host system.

4.5.1 Contents

The following are typical parameters programmed into the OTP memory:

- BD_ADDR
- Software license key
- USB PID/VID
- USB bus/self-powered status
- Output power calibration
- Frequency trimming
- Initial status LED drive configuration

The OTP contents also include a static error correction table to improve yield during the programming process as well as forward error correction codes to eliminate any long-term reliability problems. The OTP contents associated with error correction are not visible by customers.

4.5.2 Programming

OTP memory programming takes place through a combination of Cypress software integrated with the manufacturing test software and code embedded in CYW20705 firmware.

Programming the OTP requires a 3.3V supply. The OTP programming supply comes from the VDD_USB pin. For applications where the OTP is most useful, such as the USB transport application for the PC market, the 3.3V is already required for USB operation from the VDD_USB pin. The OTP power supply is allowed to be as low as 1.8 V to be able to read the contents. See Table 3 for the OTP memory programming supply voltage requirements.

The OTP is enabled by default by setting OTP_DIS to low using an internal pull-down resistor. Leave this pin floating for a default configuration. To disable the OTP, set the OTP_DIS pin to active high. This pin can be configured from the HW to enable or disable OTP.

Typically it won't be necessary to disable the OTP memory, even if it is not programmed during manufacturing. The OTP_DIS package ball only needs to be tied to high if recommended by Cypress.

Table 3. OTP Programming Supply Voltage Requirements[a]

Supply	Minimum[b]	Typical	Maximum[b]	Unit
VDD_USB	TBD	TBD	TBD	V

a. The average and peak current consumptions during OTP memory programming are 20 mA and 70 mA, respectively.
b. Contact your Cypress representative for recommended minimum and maximum supply voltages.

5. Peripheral Transport Unit

This section discusses the PCM, USB, UART, and SPI peripheral interfaces. The CYW20705 has a 1040 byte transmit and receive fifo, which is large enough to hold the entire payload of the largest EDR BT packet (3-DH5).

5.1 PCM Interface

The CYW20705 PCM interface can connect to linear PCM codec devices in master or slave mode. In master mode, the device generates the PCM_BCLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface as inputs to the device.

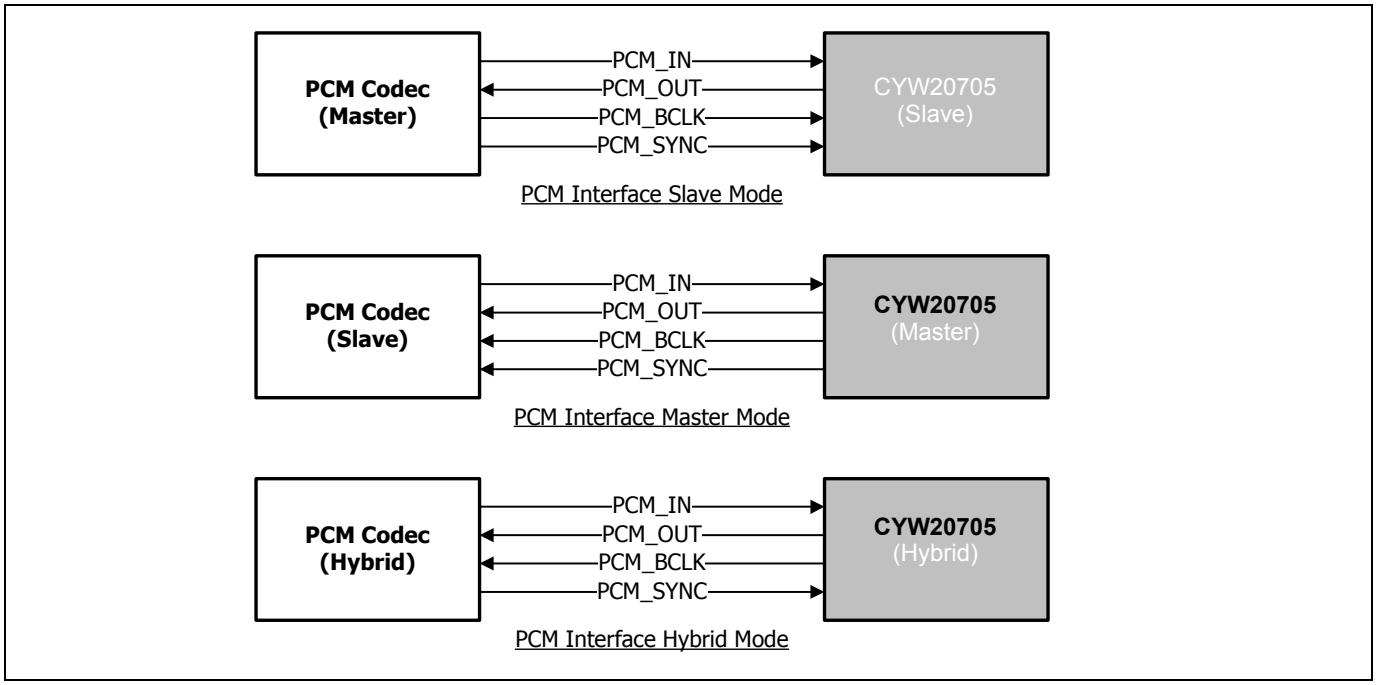
The device supports up to three SCO or eSCO channels through the PCM interface and each channel can be independently mapped to any available slot in a frame.

The host can adjust the PCM interface configuration using vendor-specific HCI commands or it can be setup in the configuration file.

5.1.1 System Diagram

Figure 5 shows options for connecting the device to a PCM codec device as a master or a slave.

Figure 5. PCM Interface with Linear PCM Codec



5.1.2 Slot Mapping

The device supports up to three simultaneous, full-duplex SCO or eSCO channels. These channels are time-multiplexed onto the PCM interface using a time slotting scheme based on the audio sampling rate, as described in Table 4.

Table 4. PCM Interface Time Slotting Scheme

Audio Sample Rate	Time Slotting Scheme
8 kHz	The number of slots depends on the selected interface rate, as follows: **Interface rate** **Slot** 128 1 256 2 512 4 1024 8 2048 16
16 kHz	The number of slots depends on the selected interface rate, as follows: **Interface rate** **Slot** 256 1 512 2 1024 4 2048 8

Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tri-states its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tri-states its output after the falling edge of the PCM clock during the last bit of the slot.

5.1.3 Wideband Speech

The CYW20705 provides support for Wideband Speech (WBS) in two ways:

■ Transparent mode :

The host encodes WBS packets and the encoded packets are transferred over the PCM bus for SCO or eSCO voice connections. In Transparent mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate.

■ On-chip SmartAudio® technology:

The CYW20705 can perform Subband-Codec (SBC) encoding and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

5.1.4 Frame Synchronization

The device supports both short and long frame synchronization types in both master and slave configurations. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate (which is a single bit period in width) and synchronized to the rising edge of the bit clock. The PCM slave expects PCM_SYNC to be high on the falling edge of the bit clock and the first bit of the first slot to start at the next rising edge of the clock. In the long frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate. However, the duration is 3-bit periods and the pulse starts coincident with the first bit of the first slot.

5.1.5 Data Formatting

The device can be configured to generate and accept several different data formats. The device uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits is configurable to support various data formats on the PCM interface. The remaining three bits are ignored on the input, and may be filled with zeros, ones, a sign bit, or a programmed value on the output. The default format is 13-bit two's complement data, left justified, and clocked most significant bit first.

5.2 HCI Transport Detection Configuration

The CYW20705 supports the following interface types for the HCI transport from the host:

- UART (H4 and H5)
- USB
- SPI

Only one host interface can be active at a time. The firmware performs a transport detect function at boot-time to determine which host is the active transport. It can auto-detect UART and USB interfaces, but the SPI interface must be selected by strapping the SCL pin to 0.

The complete algorithm is summarized as follows:

1. Determine if SCL is pulled low. If it is, select SPI as HCI host transport.
2. Determine if any local NVRAM contains a valid configuration file. If it does and a transport configuration entry is present, select the active transport according to entry, and then exit the transport detection routine.
3. Look for start-of-frame (SOF) on the USB interface. If it is present, select USB.
4. Look for CTS_N = 0 on the UART interface. If it is present, select UART.
5. Repeat Step 3 and Step 4 until transport is determined.

5.3 USB Interface

5.3.1 Features

The following USB interface features are supported:

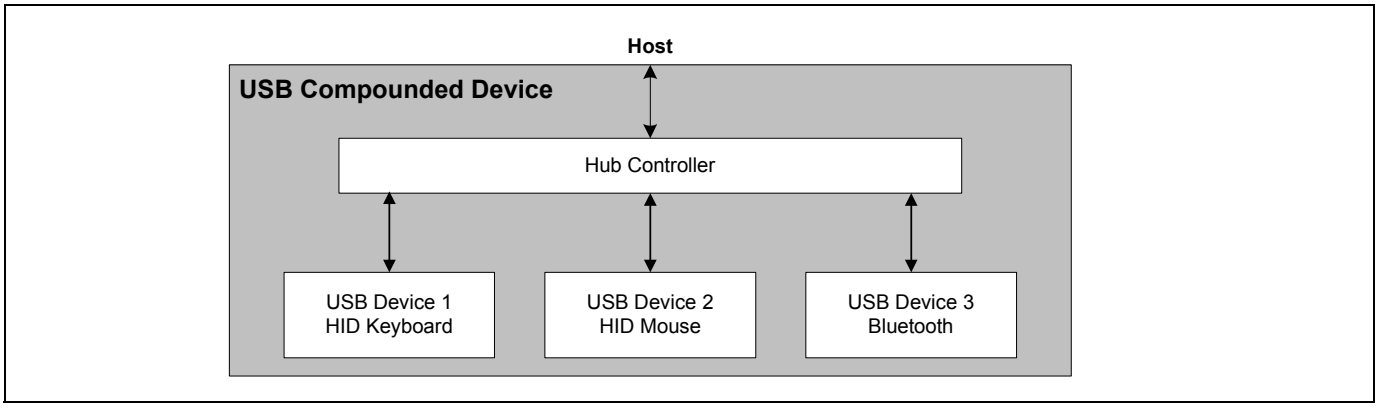
- USB Protocol, Revision 2.0, full-speed compliant including the hub
- Optional hub compound device with up to three device cores internal to device.
- Bus or self-power, dynamic configuration for the hub
- Global and selective suspend and resume with remote wakeup
- Bluetooth HCI
- HID, DFU, UHE (proprietary method to emulate an HID device at system boot)
- Integrated detach resistor

5.3.2 Operation

Note: The USB and HCI UART interfaces cannot be used simultaneously. For designs that do not use the USB interface, VDD_USB, HUSB_DP and HUSB_DN must be connected to ground.

The CYW20705 can be configured to boot up as either a single USB peripheral or a USB hub with several USB peripherals attached. As a single peripheral, the host detects a single USB Bluetooth device. In Hub mode, the host detects a hub with one to three of the ports already connected to USB devices (see Figure 6).

Figure 6. USB Compounded Device Configuration



Depending on the desired hub mode configuration, the CYW20705 can boot up showing the three ports connected to logical USB devices internal to the CYW20705—a generic Bluetooth device, a mouse, and a keyboard. In this mode, the mouse and keyboard are emulated devices, since they connect to real HID devices via a Bluetooth link. The Bluetooth link to these HID devices is hidden from the USB host. To the host, the mouse and/or keyboard appear to be directly connected to the USB port. This Cypress proprietary architecture is called USB HID Emulation (UHE).

The USB device, configuration, and string descriptors are fully programmable, allowing manufacturers to customize the descriptors, including vendor and product IDs, the CYW20705 uses to identify itself on the USB port. To make custom USB descriptor information available at boot time, stored it in external NVRAM.

Despite the mode of operation (Single Peripheral or Hub), the Bluetooth device is configured to include the following interfaces:

Interface 0	Contains a Control endpoint (Endpoint 0x00) for HCI commands, a Bulk In Endpoint (Endpoint 0x82) for receiving ACL data, a Bulk Out Endpoint (Endpoint 0x02) for transmitting ACL data, and an Interrupt Endpoint (Endpoint 0x81) for HCI events.
Interface 1	Contains Isochronous In and Out endpoints (Endpoints 0x83 and 0x03) for SCO traffic. Several alternate Interface 1 settings are available for reserving the proper bandwidth of isochronous data (depending on the application).
Interface 2	Contains Bulk In and Bulk Out endpoints (Endpoints 0x84 and 0x04) used for proprietary testing and debugging purposes. These endpoints can be ignored during normal operation.

5.3.3 USB Hub and UHE Support

The CYW20705 supports the USB hub and device model (USB, Revision 2.0, full-speed compliant). Optional mouse and keyboard devices utilize Cypress's proprietary USB HID Emulation (UHE) architecture, which allows these devices appear as standalone HID devices even though connected through a Bluetooth link.

The presence of UHE devices requires the hub to be enabled. The CYW20705 cannot appear as a single keyboard or a single mouse device without the hub. Once either mouse or keyboard UHE device is enabled, the hub must also be enabled.

When the hub is enabled, the CYW20705 handles all standard USB functions for the following devices:

- HID keyboard
- HID mouse
- Bluetooth

All hub and device descriptors are firmware-programmable. This USB compound device configuration (see Figure 6 on page 21) supports up to three downstream ports. This configuration can also be programmed to a single USB device core. The device automatically detects activity on the USB interface when connected. Therefore, no special configuration is needed to select HCI as the transport.

The hub's downstream port definition is as follows:

- Port 1 USB lite device core (for HID applications)
- Port 2 USB lite device core (for HID applications)
- Port 3 USB full device core (for Bluetooth applications)

When operating in Hub mode, all three internal devices do not have to be enabled. Each internal USB device can be optionally enabled. The configuration record in NVRAM determines which devices are present.

5.4 UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate can be selected via a vendor-specific UART HCI command. The interface supports Bluetooth UART HCI (H4) specifications. The default baud rate for H4 is 115.2 Kbaud.

The following baud rates are supported:

- 9600
- 14400
- 19200
- 28800
- 38400
- 57600
- 115200
- 230400
- 460800
- 921600
- 144444
- 150000
- 2000000
- 3000000
- 3250000
- 3692000
- 4000000

Normally, the UART baud rate is set by a configuration record downloaded after reset or by automatic baud rate detection. The host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is provided through a vendor-specific command.

The CYW20705 UART operates with the host UART correctly, provided the combined baud rate error of the two devices is within ±2%.

5.4.1 HCI 3-Wire Transport (UART H5)

The CYW20705 supports H5 UART transport for serial UART communications. H5 reduces the number of signal lines required by eliminating CTS and RTS, when compared to H4.

H5 requires the use of an external LPO. CTS must be pulled low.

5.5 SPI

The CYW20705 supports a slave SPI HCI transport with an input clock range of up to 16 MHz. Higher clock rates may be possible. The physical interface between the SPI master and the CYW20705 consists of the four SPI signals (SPI_CSB, SPI_CLK, SPI_SI, and SPI_SO) and one interrupt signal (SPI_INT). The CYW20705 can be configured to accept active-low or active-high polarity on the SPI_CSB chip select signal. It can also be configured to drive an active-low or active-high SPI_INT interrupt signal. Bit ordering on the SPI_SI and SPI_SO data lines can be configured as either little-endian or big-endian. Additionally, proprietary sleep mode, half-duplex handshaking is implemented between the SPI master and the CYW20705.

SPI_INT is required to negotiate the start of a transaction. The SPI interface does not require flow control in the middle of a payload. The FIFO is large enough to handle the largest packet size. Only the SPI master can stop the flow of bytes on the data lines, since it controls SPI_CSB and SPI_CLK. Flow control should be implemented in higher layer protocols.

5.6 Simultaneous UART Transport and Bridging

The CYW20705 supports UART or USB interfaces that can function as the host controller interface (HCI). Typically, a customer application would choose one of the two interfaces and the other would be idle. The CYW20705 allows the UART transport to operate simultaneously with the USB. To operate this way, the assumption is that the USB would function as the primary host transport, while the UART would function as a secondary communication channel that can operate at the same time. This can enable the following applications:

- Bridging primary HCI transport traffic to another device via the UART
- Generic communication to an external device for a vendor-supported application via the UART

Simultaneous UART transport and bridging is enabled by including:

- Two dedicated 64-byte FIFOs, one for the input and one for the output
- Additional DMA channels
- Additional vendor-supported commands over the HCI transport

6. Frequency References

The CYW20705 uses two different frequency references for normal and low-power operational modes. An external crystal or frequency reference driven by a Temperature Compensated Crystal Oscillator (TCXO) signal is used to generate the radio frequencies and normal operation clocking. Either an external 32.768 kHz or fully integrated internal Low-Power Oscillator (LPO) is used for low-power mode timing.

6.1 Crystal Interface and Clock Generation

The CYW20705 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing, enabling it to operate from any of a multitude of frequency sources. The source can be external, such as a TCXO, or a crystal interfaced directly to the device.

The default frequency reference setting is for a 20 MHz crystal or TCXO. The signal characteristics for the crystal interface are listed in Table 5 on page 25.

Table 5. Crystal Interface Signal Characteristics

Parameter	Crystal	External Frequency Reference	Units
Acceptable frequencies	12–52 MHz in 2 ppm[a] steps	12–52 MHz in 2 ppm[a] steps	–
Crystal load capacitance	12 (typical)	N/A	pF
ESR	60 (max)	–	Ω
Power dissipation	200 (max)	–	µW
Input signal amplitude	N/A	400 to 2000 2000 to 3300 (requires a 10 pF DC blocking capacitor to attenuate the signal)	mVp-p
Signal type	N/A	Square-wave or sine-wave	–
Input impedance	N/A	≥1 ≤ 2	MΩ pF
Phase noise @ 1 kHz @ 10 kHz @ 100 kHz @ 1 MHz	N/A N/A N/A N/A N/A	– < –120[b] < –131[b] < –136[b] < –136[b]	– dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Auto-detection frequencies when using external LPO[c]	12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 33.6, 37.4, and 38.4	12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 33.6, 37.4, and 38.4	MHz
Tolerance without frequency trimming[d]	±20	±20	ppm
Initial frequency tolerance trimming range	±50	±50	ppm

a. The frequency step size is approximately 80 Hz resolution.
b. With a 26 MHz reference clock. For a 13 MHz clock, subtract 6 dB. For a 52 MHz clock, add 6 dB.
c. Auto-detection of the frequency requires the crystal or external frequency reference to have less than ±50 ppm of variation and also requires an external LPO frequency which has less than ±250 ppm of variation at the time of detection.
d. AT-Cut crystal or TXCO recommended.