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Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

The following document contains information on Cypress products. Although the document is marked with the name "Broadcom", the company that originally developed the specification, Cypress will continue to offer these products to new and existing customers.

CONTINUITY OF SPECIFICATIONS

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

CONTINUITY OF ORDERING PART NUMBERS

Cypress continues to support existing part numbers. To order these products, please use only the Cypress Ordering Part Number listed in the table.

Broadcom Ordering Part Number	Cypress Ordering Part Number
BCM20707UA1KFFB4GT	CYW20707UA1KFFB4GT
BCM20707UA1KFFB4G	CYW20707UA1KFFB4G
BCM20707VA1PKWBG	CYW20707VA1PKWBG
BCM20707UA2KFFB4GT	CYW20707UA2KFFB4GT
BCM20707VA1PKWBGT	CYW20707VA1PKWBGT
BCM20707UA2KFFB4G	CYW20707UA2KFFB4G
BCM20707UA1KFFB1G	CYW20707UA1KFFB1G

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BROADCOM®

BCM20707

Bluetooth SoC for Embedded Wireless Devices

GENERAL DESCRIPTION

The Broadcom® BCM20707 is a single-chip Bluetooth 4.2-compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. Manufactured using the industry's most advanced 40 nm CMOS low-power process, the BCM20707 employs the highest level of integration to eliminate all critical external components, thereby minimizing the device's footprint and the costs associated with implementing Bluetooth solutions.

The BCM20707 is the optimal solution for embedded and IoT applications. Built-in firmware adheres to the Bluetooth Low Energy (BLE) profile

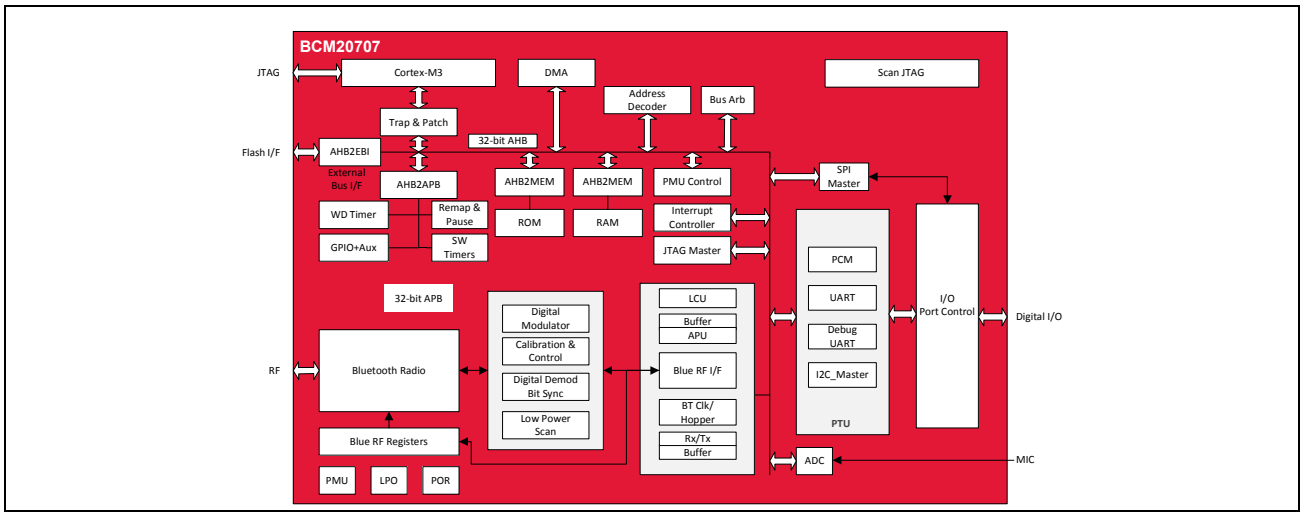
APPLICATIONS

- Home automation
- Point-of-sale input devices
- Blood pressure monitors
- “Find me” devices
- Heart rate monitors
- Proximity sensors
- Thermometers
- Wearables

FEATURES

- Complies with Bluetooth Core Specification version 4.2 including BR/EDR/BLE
- Broadcom proprietary LE data rate up to 2 Mbps
- BLE HID profile version 1.00 compliant
- Bluetooth Device ID profile version 1.3 compliant
- Supports Generic Access Profile (GAP)
- Supports Adaptive Frequency Hopping (AFH)
- Excellent receiver sensitivity
- Programmable output power control
- Integrated ARM Cortex-M3 microprocessor core
- On-chip power-on reset (POR)
- Support for EEPROM and serial flash interfaces
- Integrated low dropout regulators (LDO)
- On-chip software controlled PMU
- PCM/I^2S Interface
- Infrared modulator
- IR learning
- On-chip support for SPI (master/slave modes)
- Broadcom Serial Communications interface (compatible with NXP I^2C slaves)
- Package types:
  - 49-pin FBGA package (4.5 mm x 4.0 mm) Bluetooth 4.2-compliant
  - 36-pin WLBGA package (2.8 mm x 2.5 mm) Bluetooth 4.2-complaint
  - RoHS compliant

Figure 1: Functional Block Diagram



Revision History

Revision	*Date*	*Change Description*
20707-DS106-R	05/27/16	**Updated:** • Cover page minor edits. • Figure 2: “Reset Timing,” on page 13. • Figure 3: “LDO Functional Block Diagram,” on page 16. • Figure 8: “BCM20707 49-Pin FBGA Ball Map,” on page 35. • Table 9: “Power Supply Specifications,” on page 37. • Table 10: “VDDC LDO Electrical Specifications,” on page 38. • Ambient operating temperatures in Section 5: “Ordering Information,” on page 61. **Added:** • “Link Control Layer” on page 11. • Table 11: “BTLDO_2P5 Electrical Specifications,” on page 39.
20707-DS105-R	04/20/16	**Added:** • 36-pin WLBGA Package (2.8mm x2.5mm) feature bullet on cover page • Added informative notes in “One-Time Programmable Memory” on page 12 and “Clock Frequencies” on page 21 • “36-Pin WLBGA Package” on page 23 • Table 7: “BCM20707 36-Pin WLBGA List,” on page 32 • Figure 21: “BCM20707 36-pin WLBGA Package (2.8 mm x 2.5 mm),” on page 59 • 36-pin WLBGA part to Section 5: “Ordering Information,” on page 61
20707-DS104-R	04/07/16	**Updated:** • Figure 19: “BCM20707 49-pin FBGA Package (4.5 mm x 4.0 mm),” page 51
20707-DS103-R	03/24/16	**Updated:** • Table 6: “BCM20707 49-Ball Pin List,” on page 26
20707-DS102-R	10/02/15	**Updated:** • Table 6: “BCM20707 49-Ball Pin List,” on page 27
20707-DS101-R	06/15/15	**Updated:** • “Internal LDO” on page 14 • Figure 3: “LDO Functional Block Diagram,” on page 15 (added) • “Collaborative Coexistence” on page 15 (added) • “Global Coexistence Interface” on page 15 (added) • “SECI I/O” on page 15 (added) • Table 6: “BCM20707 49-Ball Pin List,” on page 27 • Table 8: “Power Supply Specifications,” on page 33 • Section 5: “Ordering Information,” on page 55
20707-DS100-R	04/17/15	Initial release

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About This Document

Purpose and Audience

The data sheet provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM20707 device. It is intended for hardware, design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. Acronyms and abbreviations in this document are also defined in Appendix A: “Acronyms and Abbreviations,” on page 62.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

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Section 1: Functional Description

Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL and TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types. The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Bluetooth 4.2 Features

Both the BCM20707 36-pin WLBGA package and the 49-pin FBGA package support all Bluetooth 4.2 and legacy features, with the following benefits:

- Dual-mode Bluetooth low energy (BT and BLE operation)
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption pause resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link supervision time out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link timeout supervision.
- Quality of service (QoS) enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.
- Secure connections (BR/EDR)
- Fast advertising interval
- Piconet clock adjust
- Connectionless broadcast
- LE privacy v1.1
- Low duty cycle directed advertising
- LE dual mode topology

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state in the Bluetooth Link Controller.

- States:
  - Standby
  - Connection
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff
  - Advertising
  - Scanning

Test Mode Support

The BCM20707 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the BCM20707 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth clock, and device address.

Microprocessor Unit

The BCM20707 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is based on the Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The microprocessor also includes 848 KB of ROM memory for program storage and boot ROM, 352 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

NVRAM Configuration Data and Storage

NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The BCM20707 can use SPI Flash or I^2C EEPROM/serial flash for NVRAM storage.

One-Time Programmable Memory

The BCM20707 includes 2 Kbytes of one-time programmable (OTP) memory allow manufacturing customization and to avoid the need for an on-board NVRAM. If customization is not required, then the OTP does not need to be programmed. Whether the OTP is programmed or not, to save power it is disabled when the boot process is complete. The OTP is designed to store a minimal amount of information. Aside from OTP data, most user configuration information will be downloaded to RAM after the BCM20707 boots and is ready for host transport communication.

Note: The OTP is disabled internally for the 36-Pin WLBGA package.

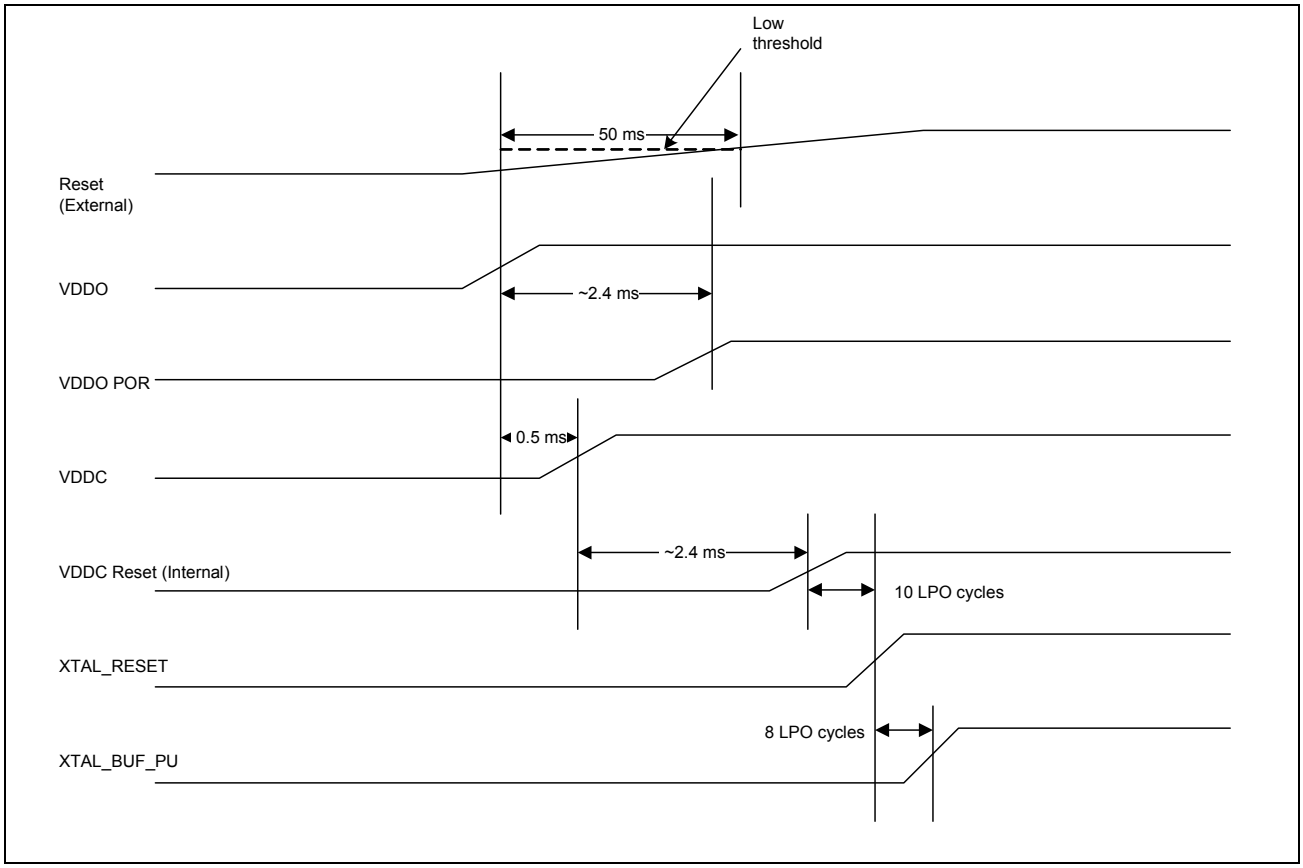
The OTP contents are limited to:

- Parameters required prior to downloading the user configuration to RAM.
- Parameters unique to each part and each customer (for example, the Bluetooth device address and/or the software license key).

External Reset

An external active-low reset signal, RESET_N, can be used to put the BCM20707 in the reset state. An external voltage detector reset IC with 50 ms delay is needed on the RESET_N. The RESET_N should be released only after the VDDO supply voltage level has been stabilized for 50 ms.

Figure 2: Reset Timing



Note: The Reset signal should remain below this threshold 50 ms after VDDO is stable. Note that the representation of this signaling diagram is extended and not drawn to scale.

Integrated Radio Transceiver

The BCM20707 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The BCM20707 is fully compliant with the Bluetooth Radio Specification and enhanced data rate (EDR) specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmit

The BCM20707 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the BLE specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the BCM20707 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the BCM20707 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM20707 uses an internal RF and IF loop filter.

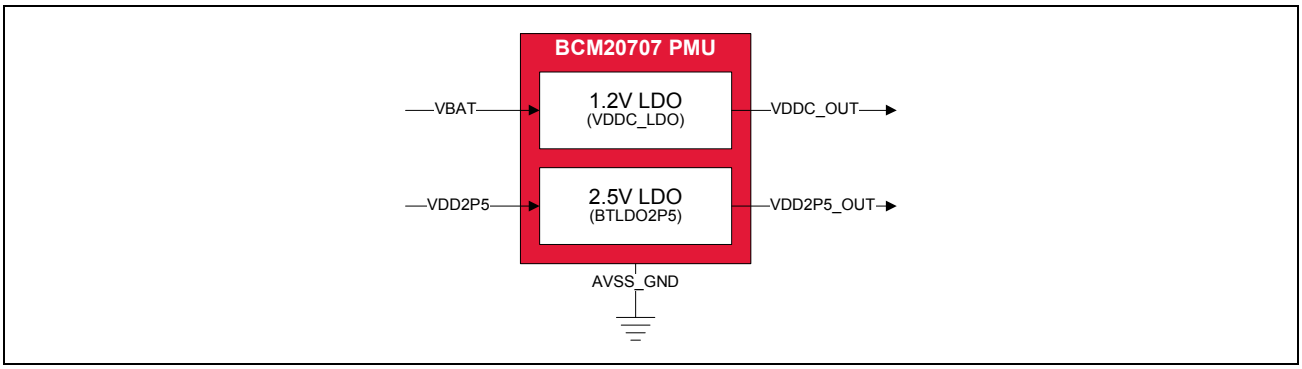
Calibration

The BCM20707 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration tunes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops, and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Internal LDO

The BCM20707 uses two LDOs - one for 1.2V and the other for 2.5V. The 1.2V LDO provides power to the baseband and radio and the 2.5V LDO powers the PA.

Figure 3: LDO Functional Block Diagram



Collaborative Coexistence

The BCM20707 provides extensions and collaborative coexistence to the standard Bluetooth AFH for direct communication with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously in a single device. The device supports industry-standard coexistence signaling, including 802.15.2, and supports Broadcom and third-party WLAN solutions.

Global Coexistence Interface

The BCM20707 supports the proprietary Broadcom Global Coexistence Interface (GCI) which is a 2-wire interface.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over GCI_SECI_IN and GCI_SECI_OUT a two-wire interface, one serial input (GCI_SECI_IN), and one serial output (GCI_SECI_OUT). The pad configuration registers must be programmed to choose the digital I/O pins that serve the GCI_SECI_IN and GCI_SECI_OUT function.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronization upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

SECI I/O

The BCM20707 devices have dedicated GCI_SECI_IN and GCI_SECI_OUT pins. The two pin functions can be mapped to any of the Broadcom Global Coexistence Interface (GCI) GPIO. Pin function mapping is controlled by the configuration file that is stored in either NVRAM or downloaded directly into on-chip RAM from the host.

Peripheral Transport Unit

Broadcom Serial Communications Interface

The BCM20707 provides a 2-pin master BSC interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as trackball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I^2C slave devices. BSC does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by BSC:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I^2C-compatible speed.)
- 1 MHz (Compatibility with high-speed I^2C-compatible devices is not guaranteed.)

The following transfer types are supported by BSC:

- Read (Up to 127 bytes can be read.)
- Write (Up to 127 bytes can be written.)
- Read-then-Write (Up to 127 bytes can be read and up to 127 bytes can be written.)
- Write-then-Read (Up to 127 bytes can be written and up to 127 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the BCM20707 are required on both the SCL and SDA pins for proper operation.

UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 38400 bps to 6 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The BCM20707 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 6 Mbps. The baud rate of the BCM20707 UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Table 1 contains example values to generate common baud rates with a 24 MHz UART clock.

Table 1: Common Baud Rate Examples, 24 MHz Clock

	Baud Rate Adjustment			
Baud Rate (bps)	***High Nibble***	***Low Nibble***	***Mode***	***Error (%)***
6M	0xFF	0xF8	High rate	0.00
4M	0xFF	0xF4	High rate	0.00
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16
38400	0x01	0x00	Normal	0.00

Table 2 contains example values to generate common baud rates with a 48 MHz UART clock.

Table 2: Common Baud Rate Examples, 48 MHz Clock

Baud Rate (bps)	High Rate	Low Rate	Mode	Error (%)
6M	0xFF	0xF8	High rate	0
4M	0xFF	0xF4	High rate	0
3M	0x0	0xFF	Normal	0
2M	0x44	0xFF	Normal	0
1.5M	0x0	0xFE	Normal	0
1M	0x0	0xFD	Normal	0
921600	0x22	0xFD	Normal	0.16
230400	0x0	0xF3	Normal	0.16
115200	0x1	0xE6	Normal	–0.08
57600	0x1	0xCC	Normal	0.04
38400	0x11	0xB2	Normal	0

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The BCM20707 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Peripheral UART Interface

The BCM20707 has a second UART that may be used to interface to other peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin as shown in Table 3.

Table 3: BCM20707 Peripheral UART

Pin Name	pUART_TX	pUART_RX	pUART_CTS_N	pUART_RTS_N
Configured pin name	P0	P2	P3	P6
	P31	P33	–	P30

Note: Not all of the GPIOs above are available on the 36-pin WLBGA package.

PCM Interface

The BCM20707 includes a PCM interface that shares pins with the I^2S interface. The PCM Interface on the BCM20707 can connect to linear PCM codec devices in master or slave mode. In master mode, the BCM20707 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM20707.

Slot Mapping

The BCM20707 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The BCM20707 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three-bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The BCM20707 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the BCM20707 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked MSB first.

Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

Clock Frequencies

The BCM20707 49-pin FBGA package supports 20, 24, and 40 MHz crystals (XTAL) by selecting the correct crystal strapping options. Other frequencies also supported by firmware configuration. Table 4 lists the strapping options.

Table 4: Crystal Strapping Options for the 49-Pin FBGA Package

Strapping Option Pin		
BT_XTAL_STRAP_1	***BT_XTAL_STRAP_0***	***XTAL Frequency***
Pull Low	Pull Low	40 Mhz
Pull Low	Pull High	24 MHz
Pull High	Pull Low	20 MHz
Pull High	Pull High	Read from serial flash or EEPROM

Note: Only the Read from Serial flash or EEPROM option is available for the 36-pin WLBGA package. The strapping is set internally in the package.

Crystal Oscillator

The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see Figure 4).

Figure 4: Recommended Oscillator Configuration—12 pF Load Crystal

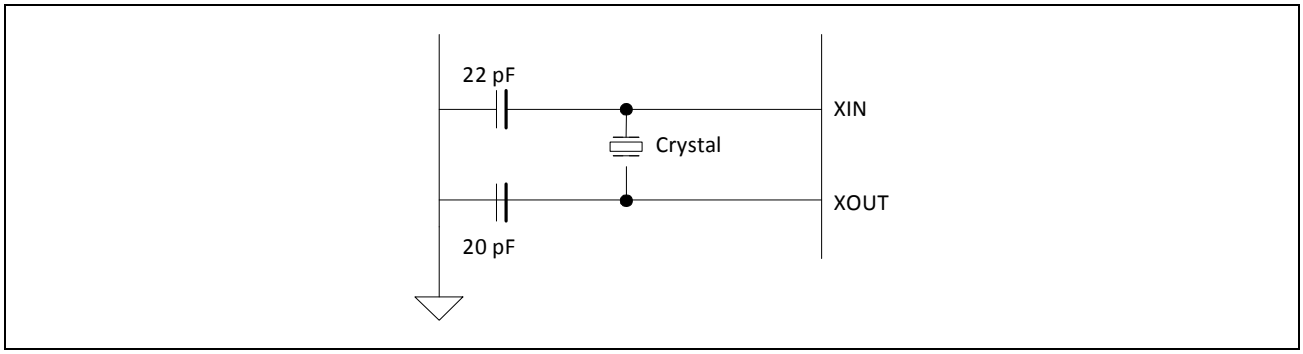


Table 5 shows the recommended crystal specifications.

Table 5: Reference Crystal Electrical Specifications

Parameter	*Conditions*	*Minimum*	*Typical*	*Maximum*	*Unit*
Nominal frequency	–	20	24	40	MHz
Oscillation mode	–	Fundamental			–
Frequency tolerance	@25°C	–	±10	–	ppm
Tolerance stability over temp	@0°C to +70°C	–	±10	–	ppm
Equivalent series resistance	–	–	–	60	W
Load capacitance	–	–	12	–	pF
Operating temperature range	–	0	–	+70	°C
Storage temperature range	–	–40	–	+125	°C
Drive level	–	–	–	200	µW
Aging	–	–	–	±10	ppm/year
Shunt capacitance	–	–	–	2	pF

HID Peripheral Block

The peripheral blocks of the BCM20707 all run from a single 128 kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case, in that it may drop its clock request line even when enabled, and then reassert the clock request line if a keypress is detected.

GPIO Ports

49-Pin FBGA Package

The BCM20707 49-pin FBGA package has 24 general-purpose I/Os (GPIOs). All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3V or 4 mA at 1.8V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3V or 8 mA at 1.8V. The following GPIOs are available:

- BT_GPIO_0/P36/P38 (triple bonded; only one of three is available)
- BT_GPIO_1/P25/P32 (triple bonded; only one of three is available)
- BT_GPIO_3/P27/P33 (triple bonded; only one of three is available)
- BT_CLK_REQ/P4/P24 (triple bonded; only one of three is available)
- BT_GPIO_5/P15 (dual bonded; only one of two is available)
- BT_GPIO_6/P11/P26 (triple bonded; only one of three is available)
- BT_GPIO_7/P30 (Dual bonded; only one of two is available)
- BT_CLK_REQ/P4/P24 (triple bonded; only one of three is available)
- I2S_PCM_IN/P12 (dual bonded; only one of two is available)
- I2S_PCM_OUT/P3/P29/P35 (quadruple bonded; only one of four is available)
- I2S_PCM_CLK/P2/P28/P37 (quadruple bonded; only one of four is available)
- I2S_WS_PCM_SYNC/P0/P34 (triple bonded; only one of three is available)

All of these pins can be programmed as ADC inputs.

Port 26–Port 29

P[26:29] consist of four pins. All pins are capable of sinking up to 16 mA for LEDs. These pins also have PWM functionality, which can be used for LED dimming.

36-Pin WLBGA Package

The BCM20707 36-pin WLBGA package has seven GPIOs. All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3V or 4 mA at 1.8V. The following GPIOs are available:

- BT_GPIO_3/P0/LPO_IN (triple bonded; only one of three is available)
- BT_GPIO_5/P8/P33 (triple bonded; only one of three is available)
- I2S_DI/PCM_OUT_P3 (triple bonded; only one of three is available)
- I2S_DO/PCM_OUT/BT_GPIO_6/P9 (quadruple bonded; only one of four is available)
- I2S_CLK/PCM_CLK/BT_GPIO_4/P1 (quadruple bonded; only one of four is available)
- I2S_WS/PCM_SYNC/P11 (triple bonded; only one of three is available)

PWM

The BCM20707 has four internal PWMs. The PWM module consists of the following:

- PWM1–4
- Each of the four PWM channels, PWM1–4, contains the following registers:
  - 10-bit initial value register (read/write)
  - 10-bit toggle register (read/write)
  - 10-bit PWM counter value register (read)
- PWM configuration register shared among PWM1–4 (read/write). This 12-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 5 shows the structure of one PWM.

Figure 5: PWM Block Diagram