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CONTINUITY OF ORDERING PART NUMBERS

Cypress continues to support existing part numbers. To order these products, please use only the Cypress Ordering Part Number listed in the table.

Broadcom Ordering Part Number	Cypress Ordering Part Number
BCM43340XKUBGT	CYW43340XKUBGT
BCM43340HKUBG	CYW43340HKUBG
BCM43340XKUBG	CYW43340XKUBG
BCM43340HKUBGT	CYW43340HKUBGT

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Data Sheet

BCM43340

Single-Chip, Dual-Band (2.4 GHz/5 GHz) IEEE 802.11 a/b/g/n MAC/Baseband/Radio with Integrated Bluetooth 4.0 and FM Receiver

GENERAL DESCRIPTION

The Broadcom® BCM43340 single–chip quad–radio device provides the highest level of integration for a mobile or handheld wireless system, with integrated dual band (2.4 GHz / 5 GHz) IEEE 802.11 a/b/g and single–stream IEEE 802.11n MAC/baseband/radio, Bluetooth 4.0, and FM radio receiver. The BCM43340 includes integrated power amplifiers and LNAs for the 2.4 GHz and 5 GHz WLAN bands, and an integrated 2.4 GHz T/R switch. This greatly reduces the external part count, PCB footprint, and cost of the solution.

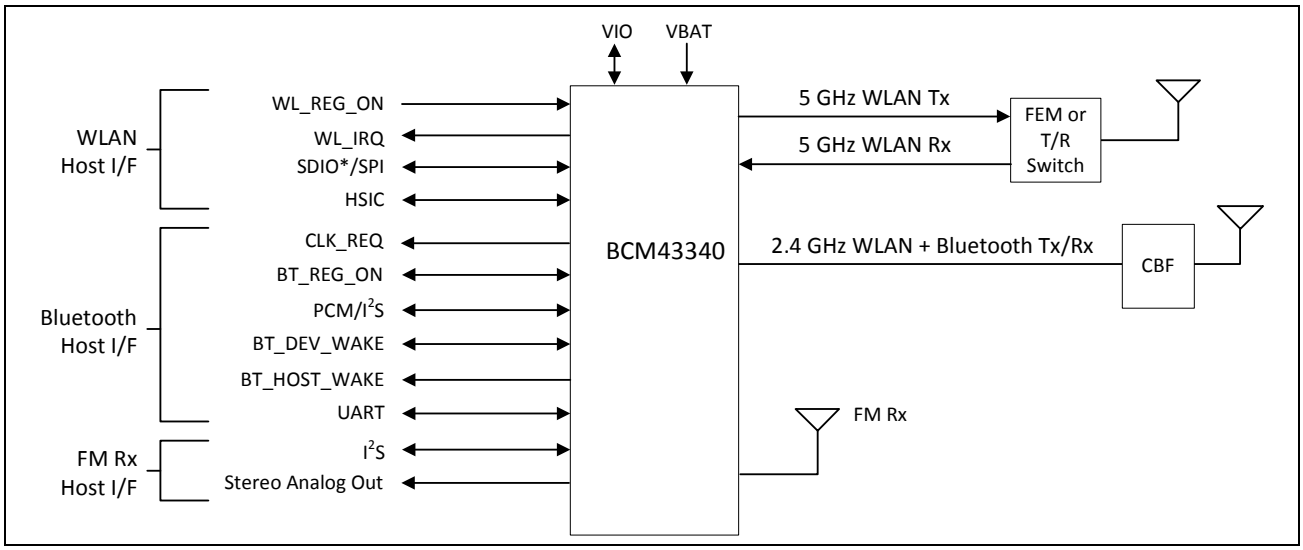
Using advanced design techniques and process technology to reduce active and idle power, the BCM43340 is designed to address the needs of mobile devices that require minimal power consumption and compact size. It includes a power management unit which simplifies the system power topology and allows for operation directly from a mobile platform battery while maximizing battery life.

FEATURES

The BCM43340 implements the highly sophisticated Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative Bluetooth coexistence scheme along with coexistence support for external radios (such as cellular and LTE, GPS, WiMAX, and Ultra–Wideband) and a single shared 2.4 GHz antenna for Bluetooth and WLAN. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a handheld system is achieved.

For the WLAN section, two host interface options are included: an SDIO v2.0 interface (including gSPI) and a High-Speed Inter-Chip (HSIC) interface (a USB 2.0 derivative for short-distance on-board connections). An independent, high-speed UART is provided for the Bluetooth host interface.

Figure 1: Functional Block Diagram



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FEATURES

IEEE 802.11x Key Features

- Dual–band 2.4 GHz and 5 GHz IEEE 802.11 a/b/g/n
- Single–stream IEEE 802.11n support for 20 MHz and 40 MHz channels provides PHY layer rates up to 150 Mbps for typical upper–layer throughput in excess of 90 Mbps.
- Supports the IEEE 802.11n STBC (space–time block coding) RX and LDPC (low–density parity check) TX options for improved range and power efficiency.
- Supports a single 2.4 GHz antenna shared between WLAN and Bluetooth.
- Shared Bluetooth and 2.4 GHz WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
- Internal fractional nPLL allows support for a wide range of reference clock frequencies
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co–located wireless technologies such as GPS, WiMAX, or UWB
- Supports standard SDIO v2.0 and gSPI (48 MHz) host interfaces.
- Alternative host interface supports HSIC v1.0 (short–distance USB device)
- Integrated ARM® Cortex–M3™ processor and on–chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features. On–chip memory includes 512 KB SRAM and 640 KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices.

FEATURES

Bluetooth and FM Key Features

- Complies with Bluetooth Core Specification Version 4.0 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation
- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Interface support: Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data
- The FM receiver unit supports HCI for communication.
- Low power consumption improves battery life of handheld devices.
- FM receiver: 76 MHz to 108 MHz FM bands; supports the European Radio Data Systems (RDS) and the North American Radio Broadcast Data System (RBDS) standards
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values

General Features

- Supports battery voltage range from 2.9V to 4.8V supplies with internal switching regulator.
- Programmable dynamic power management
- 3072-bit OTP for storing board parameters
- Routable on low–cost 1x1 PCB stack–ups
- 141-ball WLBGA package(5.67 mm × 4.47 mm, 0.4 mm pitch)
- Security:
  - WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
  - AES in WLAN hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)
  - Reference WLAN subsystem provides Wi–Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design

Revision History

Revision	*Date*	*Change Description*
43340-DS109-R	01/28/15	**Updated:** • Table 18: “WLBGA Signal Descriptions,” on page 85
43340-DS107-R	07/07/14	**Updated:** • Figure 65: “WLBGA Keep-Out Areas for PCB Layout — Bottom View,” on page 177
43340-DS107-R	04/07/14	**Updated:** • Table 28: “WLAN GPIO Functions and Strapping Options (Advance Information),” on page 144 • Title change (2.5 GHz to 2.4 GHz) for Figure 55 on page 169
43340-DS106-R	03/04/14	Figure 39: “141-Bump BCM43340 WLBGA Ball Map (Bottom View),” on page 84 and Table 18: “WLBGA Signal Descriptions,” on page 85: Updated signal names for No Connect, VDDC, VDDIO, VSS, VSSC, and WRF_PA5G_VBAT_GND3P3 pins.
43340-DS105-R	02/14/14	**Updated:** • Section 26: “Ordering Information,” on page 194.
43340-DS104-R	12/03/13	**Updated:** • Proprietary protocols in “Standards Compliance” on page 21. • Table 24: “ESD Specifications,” on page 102. • Table 33: “WLAN 2.4 GHz Transmitter Performance Specifications,” on page 124. • Table 35: “WLAN 5 GHz Transmitter Performance Specifications,” on page 129.
43340-DS103-R	08/30/13	Removed ‘Preliminary’ from the document type.

Revision	*Date*	*Change Description*
43340-DS102-R	04/22/13	**Updated:** • Figure 1: “Functional Block Diagram,” on page 1. • AES feature description on page 5. • VBAT voltage range changed from 2.3–4.8V to 2.9–4.8V. • Figure 4: “Typical Power Topology,” on page 29. • “Link Control Layer” on page 51: substates. • Table 33: “Bluetooth Receiver RF Specifications,” on page 131. • Figure 52: “WLAN Port Locations (5 GHz),” on page 142. • Table 34: “Bluetooth Transmitter RF Specifications,” on page 135: Power control step. • Table 36: “BLE RF Specifications,” on page 136: Rx sense. • Table 37: “FM Receiver Specifications,” on page 137. • Table 39: “WLAN 2.4 GHz Receiver Performance Specifications,” on page 144. • Table 40: “WLAN 2.4 GHz Transmitter Performance Specifications,” on page 148. • Table 42: “WLAN 5 GHz Transmitter Performance Specifications,” on page 153. • Table 50: “Typical WLAN Power Consumption,” on page 162.
43340-DS101-R	12/21/12	**Updated:** • HCI high-speed UART: H4+ mode no longer supported. • General Description on page 1. • “IEEE 802.11x Key Features” on page 5: shared Bluetooth and 2.4 GHz WLAN signal path. • Figure 11: “Startup Signaling Sequence,” on page 54. • “External Coexistence Interface” on page 80. • Table 26: “WLBGA and WLCSP Signal Descriptions,” on page 127. • Table 27: “WLAN GPIO Functions and Strapping Options (Advance Information),” on page 140. • Table 31: “I/O States,” on page 145 . • Table 32: “Absolute Maximum Ratings,” on page 149. • Table 36: “Bluetooth Receiver RF Specifications,” on page 154. • Table 37: “Bluetooth Transmitter RF Specifications,” on page 158. • Table 53: “Typical WLAN Power Consumption,” on page 185. • Table 54: “Bluetooth and FM Current Consumption,” on page 187.
43340–DS100-R	7/9/12	Initial Release

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About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM43340. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

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In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

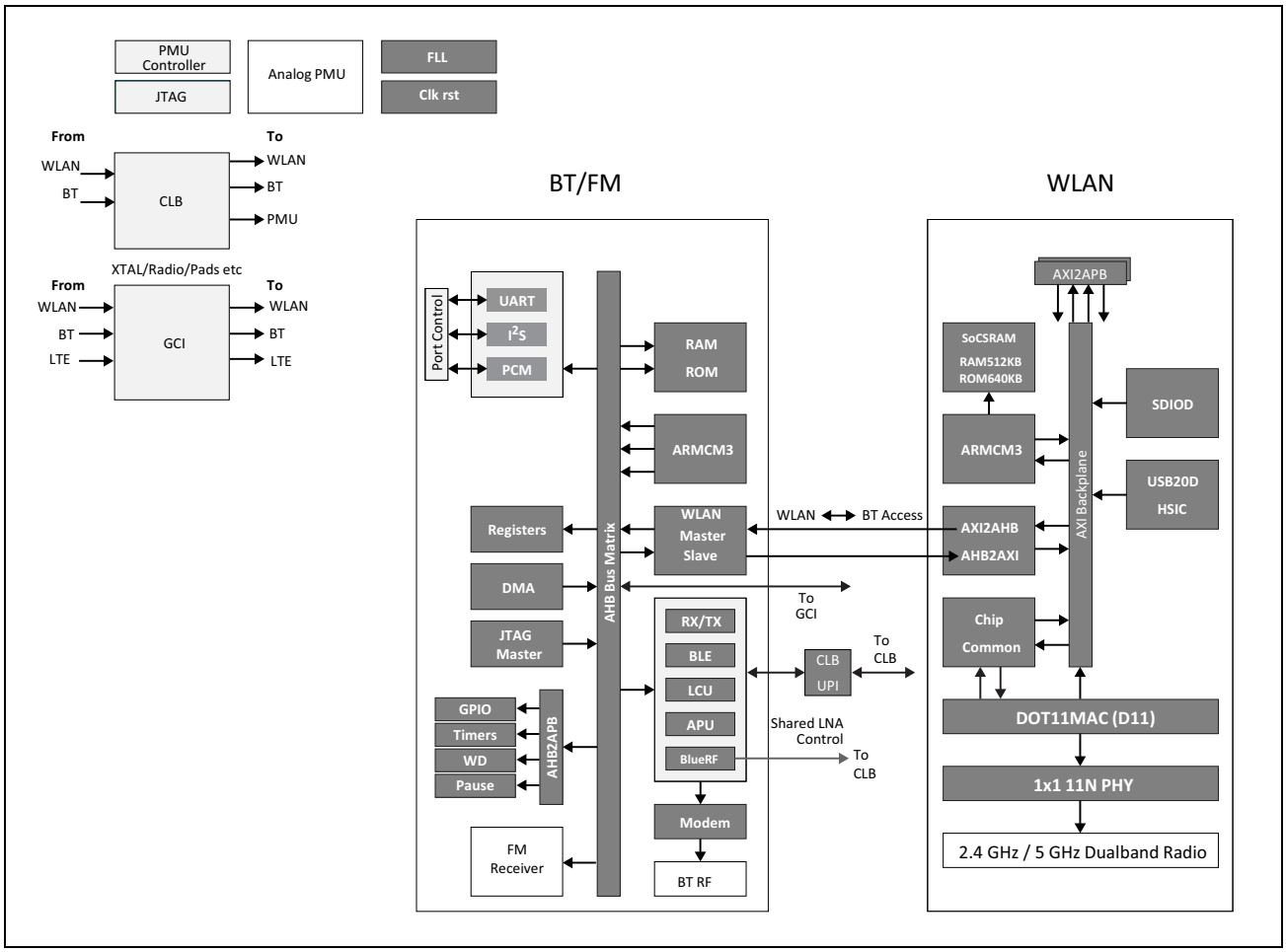
Section 1: Introduction

Overview

The Broadcom® BCM43340 single-chip device provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.1 a/b/g/n MAC/baseband/radio, Bluetooth 4.0, and FM RX. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the BCM43340 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2: BCM43340 Block Diagram



Features

The BCM43340 supports the following WLAN, Bluetooth, and FM features:

- IEEE 802.11a/b/g/n dual-band radio with internal Power Amplifiers, LNAs, and T/R switches
- Bluetooth v4.0 with integrated Class 1 PA
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Single- and dual-antenna support
  - Single antenna with shared LNA
  - Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
  - SDIO v2.0, including default and high-speed timing.
  - gSPI—up to 48 MHz clock rate
  - HSIC (USB device interface for short distance on-board applications)
- BT host digital interface (can be used concurrently with above interfaces):
  - UART (up to 4 Mbps)
- ECI—enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- I^2S/PCM for FM/BT audio, HCI for FM block control
- HCI high-speed UART (H4, H5) transport support
- Wideband speech support (16 bits linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I^2S and PCM interface)
- Bluetooth SmartAudio® technology improves voice and music quality to headsets
- Bluetooth low power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- Bluetooth Wideband Speech (WBS)
- FM advanced internal antenna support
- FM auto search/tuning functions
- FM multiple audio routing options: I^2S, PCM, eSCO, A2DP
- FM mono-stereo blend and switch, and soft mute support
- FM audio pause detect support
- Audio rate-matching algorithms
- Multiple simultaneous A2DP audio stream
- FM over Bluetooth operation and on-chip stereo headset emulation

Standards Compliance

The BCM43340 supports the following standards:

- Bluetooth 4.0 (including Bluetooth Low Energy)
- 76 MHz to 108 MHz FM bands (US, Europe, and Japan)
- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11a
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The BCM43340 will support the following future drafts/standards:

- IEEE 802.11r—Fast Roaming (between APs)
- IEEE 802.11k—Resource Management
- IEEE 802.11w—Secure Management Frames
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
  - IEEE 802.11h 5 GHz Extensions
  - IEEE 802.11i MAC Enhancements
  - IEEE 802.11r Fast Roaming Support
  - IEEE 802.11k Radio Resource Measurement

The BCM43340 supports the following security features and proprietary protocols:

- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - WAPI
  - AES (Hardware Accelerator)
  - TKIP (host-computed)
  - CKIP (SW Support)

- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
- IEEE 802.15.2 Coexistence Compliance—on silicon solution compliant with IEEE 3 wire requirements

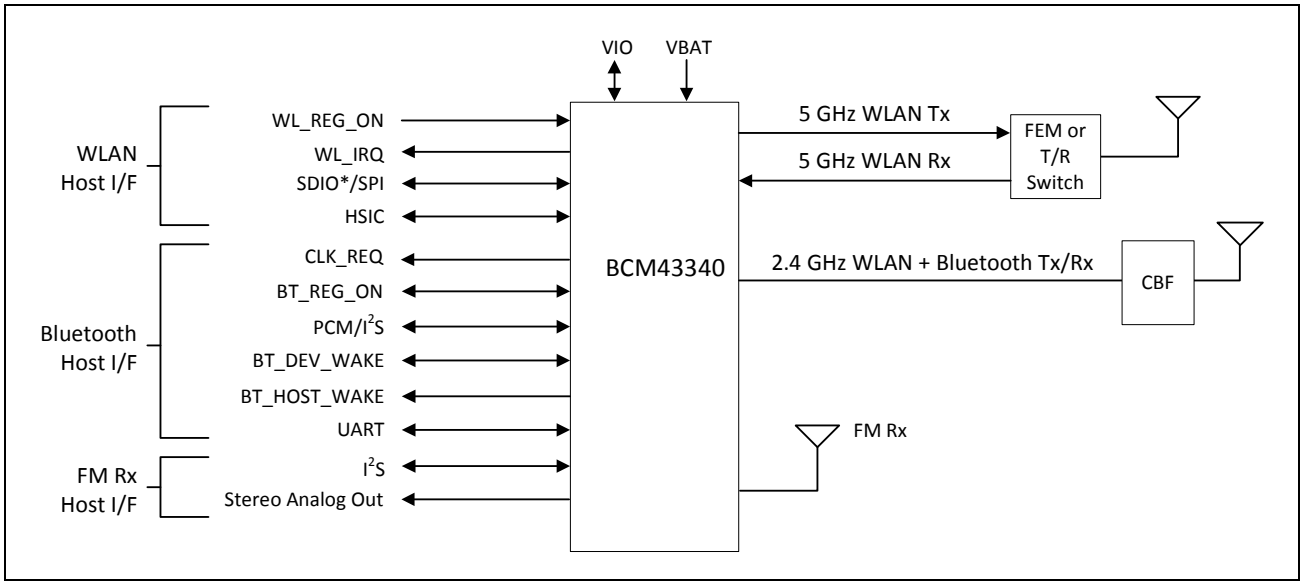
Mobile Phone Usage Model

The BCM43340 incorporates a number of unique features to simplify integration into mobile phone platforms. Its flexible PCM and UART interfaces enable it to transparently connect with the existing circuits. In addition, the TCXO and LPO inputs allow the use of existing handset features to further minimize the size, power, and cost of the complete system.

- The PCM interface provides multiple modes of operation to support both master and slave as well as hybrid interfacing to single or multiple external codec devices.
- The UART interface supports hardware flow control with tight integration to power control sideband signaling to support the lowest power operation.
- The TCXO interface accommodates any of the typical reference frequencies used by cell phones.
- FM digital interfaces can use either I^2S, PCM, or stereo analog output (an analog FM receiver interface is available for legacy systems.)
- The highly linear design of the radio transceiver ensures that the device has the lowest spurious emissions output regardless of the state of operation. It has been fully characterized in the global cellular bands.
- The transceiver design has excellent blocking (eliminating desensitization of the Bluetooth receiver) and intermodulation performance (distortion of the transmitted signal caused by the mixing of the cellular and Bluetooth transmissions) in the presence of a any cellular transmission (GSM®, GPRS, CDMA, WCDMA, or iDEN). Minimal external filtering is required for integration inside the handset.

The BCM43340 is designed to provide direct interface with new and existing handset designs as shown in Figure 3.

Figure 3: Mobile Phone System Block Diagram



Section 2: Power Supplies and Power Management

Power Supply Topology

One Buck regulator, multiple LDO regulators, and a Power Management Unit (PMU) are integrated into the BCM43340. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth, WLAN, and FM in embedded designs.

A single VBAT (2.9–4.8V) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the BCM43340.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO may be turned off/on based on the dynamic demands of the digital baseband.

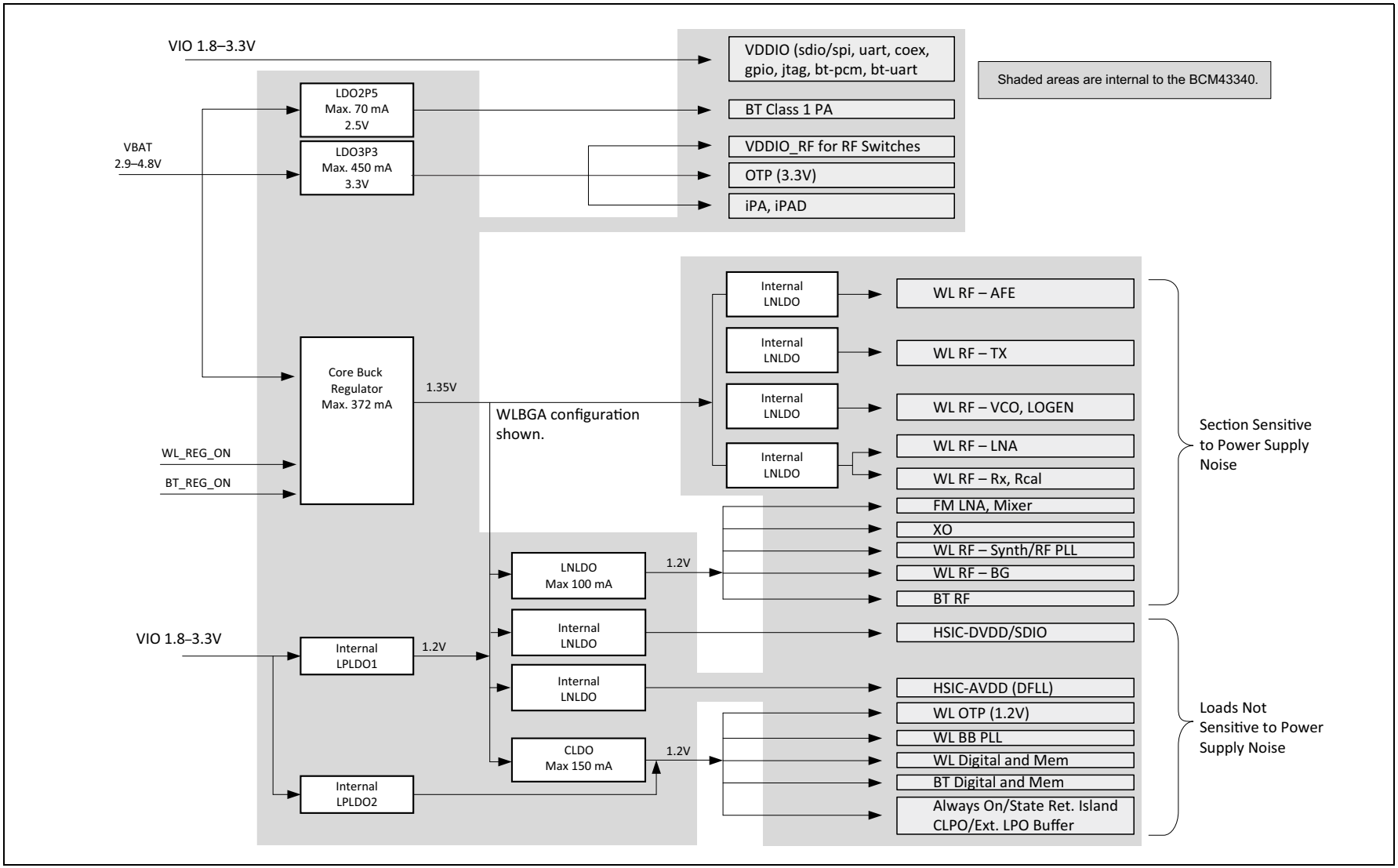
The BCM43340 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNDLO regulators. When in this state, LPLDO1 and LPLDO2 (which are low-power linear regulators that are supplied by the system VIO supply) provide the BCM43340 with all the voltages it requires, further reducing leakage currents.

BCM43340 PMU Features

- VBAT to 1.35Vout (372 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (450 mA maximum) LDO3P3 (external-capacitor)
- VBAT to 2.5Vout (70 mA maximum) LDO2P5 (external-capacitor)
- 1.35V to 1.2Vout (100 mA maximum) LNLDO (external-capacitor)
- 1.35V to 1.2Vout (150 mA maximum) CLDO (external-capacitor)
- 1.35V to 1.2Vout (80 mA maximum) HSICDVDD LDO (external-capacitor)
- Additional internal LDOs (not externally accessible)

Figure 4 on page 22 shows the regulators and a typical power topology.

Figure 4: Typical Power Topology



WLAN Power Management

The BCM43340 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM43340 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the BCM43340 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM43340 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The BCM43340 WLAN power states are described as follows:

- Active mode—All WLAN blocks in the BCM43340 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the BCM43340 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode—Most of the chip including both analog and digital domains and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through the HSIC or SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW re-initialization.
- Power-down mode—The BCM43340 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

1. Computes the required resource set based on requests and the resource dependency table.
2. Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
3. Compares the request with the current resource status and determines which resources must be enabled or disabled.
4. Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
5. Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.