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CYW43362

Single-Chip IEEE 802.11™ b/g/n MAC/Baseband/Radio + SDIO

The Cypress CYW43362 single-chip device provides the highest level of integration for mobile and handheld wireless systems, featuring integrated IEEE 802.11™ b/g and handheld device class IEEE 802.11n. It includes a 2.4 GHz WLAN CMOS power amplifier (PA) that meets the output power requirements of most handheld systems. An optional external low-noise amplifier (LNA) and external PA are also supported.

Along with the integrated power amplifier, the CYW43362 also includes integrated transmit and receive baluns, further reducing the overall solution cost.

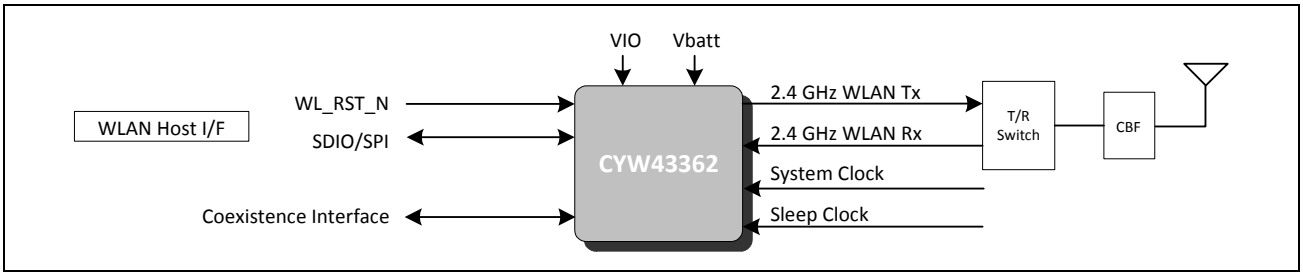
Host interface options include SDIO v2.0 that can operate in 4b or 1b modes, and a generic gSPI mode.

Utilizing advanced design techniques and process technology to reduce active and idle power, the CYW43362 is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It includes a power management unit that simplifies the system power topology and allows for operation directly from a rechargeable mobile platform battery while maximizing battery life.

Features

- Single-band 2.4 GHz IEEE 802.11 b/g/n
- Integrated WLAN CMOS power amplifier with internal power detector and closed-loop power control
- Internal fractional-N PLL enables the use of a wide range of reference clock frequencies
- Supports IEEE 802.15.2 external 3-wire and 4-wire coexistence schemes to optimize bandwidth utilization with other co-located wireless technologies such as Bluetooth, Zigbee, or BT Smart. Also supports sECI coexistence interface.
- Supports standard interfaces SDIO v2.0 (50 MHz, 4-bit and 1-bit) and generic SPI (up to 50 MHz)
- Integrated ARM Cortex™-M3 CPU with on-chip memory enables running IEEE 802.11 firmware that can be field-upgraded with future features.
- Supports WMM®, WMM-PS, and Wi-Fi Voice Personal (upgradable to Voice Enterprise in the future)
- Security:
  - Hardware WAPI acceleration engine
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - WPA™- and WPA2™- (Personal) support for powerful encryption and authentication
- 69-bump WLBGA
  (4.52 mm x 2.92 mm, 0.4 mm pitch)
- Programmable dynamic power management
- Supports battery voltage range from 2.3V to 4.8V supplies with internal switching regulator
- 1 kbit One-Time Programmable (OTP) memory for storing board parameters
- 69-bump WLBGA
  (4.52 mm x 2.92 mm, 0.4 mm pitch)

Figure 1. CYW43362 System Block Diagram



Introduction

This document provides engineering design information for the CYW43362, a single chip with an integrated 2.4 GHz RF transceiver, MAC, and baseband processor that fully supports the IEEE 802.11™ b/g/n standards.

The information provided is intended for hardware design engineers who will be incorporating the CYW43362 into their designs.

Cypress part numbering scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM43362	CYW43362
BCM43362KUBG	CYW43362KUBG

IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

Contents

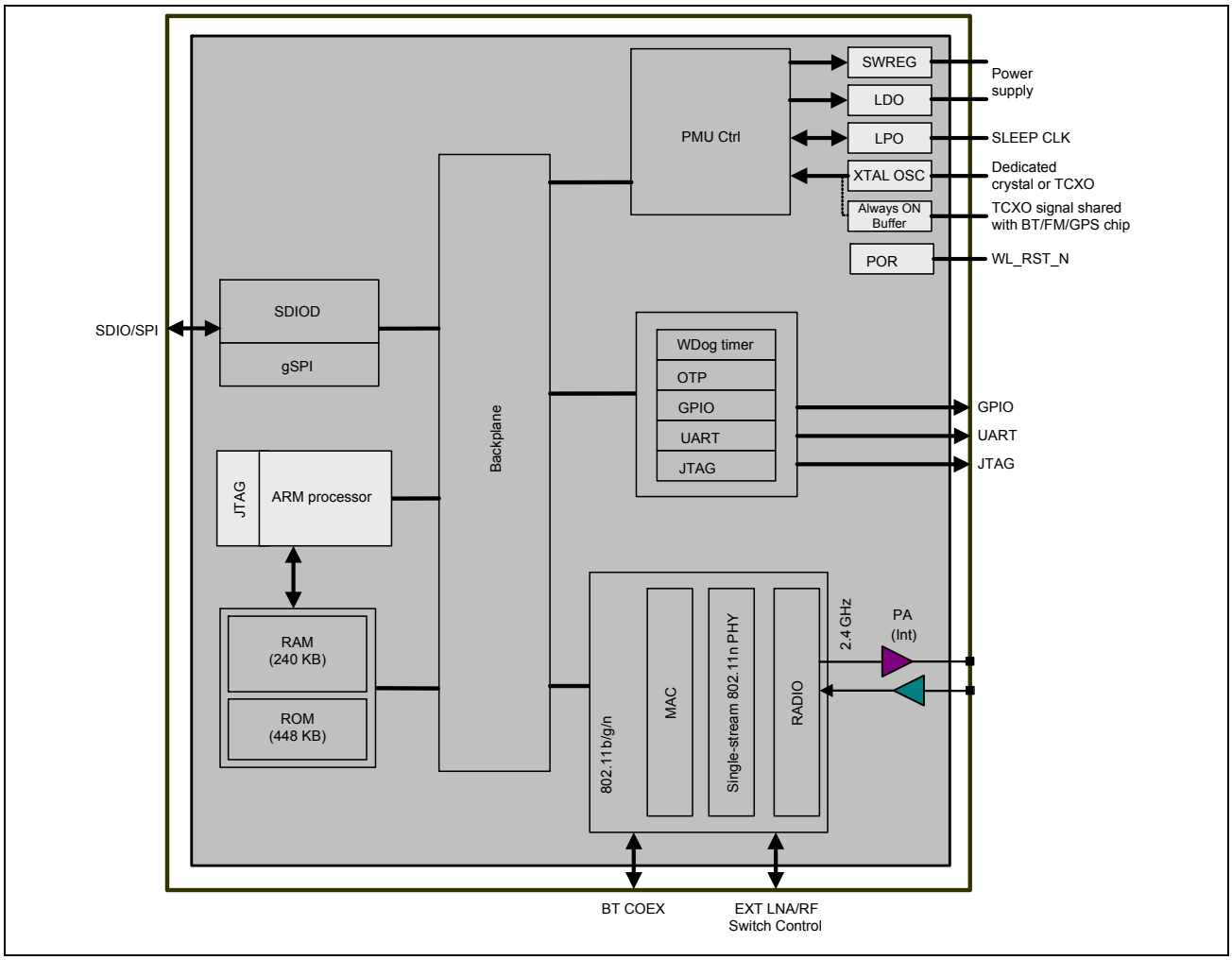
1. Overview

1.1 Overview

The Cypress CYW43362 provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 b/g/n. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. The CYW43362 is designed to address the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the CYW43362 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2. CYW43362 Block Diagram



1.2 Standards Compliance

The CYW43362 supports the following standards:

- IEEE 802.11n
- 802.11b
- 802.11g
- 802.11d

- 802.11h
- 802.11i
- 802.11j

The CYW43362 will support the following future drafts/standards:

- 802.11w—Secure Management Frames
- 802.11 Extensions:
  - WMM®
  - 802.11i MAC Enhancements
  - 802.11r Fast Roaming Support (between APs)
  - 802.11k Radio Resource Measurement
- Security:
  - WEP
  - WAPI
  - WPA™ Personal
  - WPA2™ Personal
  - AES (Hardware Accelerator)
  - TKIP (HW Accelerator)
  - CKIP (SW Support)
- QOS Protocols:
  - WMM
  - WWM-PS (U-APSD)
  - WWM-SA
- Proprietary Protocols:
  - WFAEC
- Coexistence Interfaces:
  - Supports IEEE 802.15.2 external three-wire coexistence scheme to support additional wireless technologies, such as Bluetooth, Zigbee, or BT Smart.

2. Power Supplies and Power Management

2.1 WLAN Power Management

The CYW43362 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW43362 integrated RAM is a low-leakage memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only.

Additionally, the CYW43362 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW43362 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters, which run on the 32.768 kHz low-power oscillator (LPO) sleep clock in the PMU sequencer, are used to turn individual regulators and power switches on and off. Clock speeds are dynamically changed, or gated off, as appropriate for the current mode. Slower clock speeds are used wherever possible.

The CYW43362 power states are described as follows:

- Active mode—All components in the CYW43362 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode (PWM or Burst) based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Sleep mode—The radio, AFE, PLLs, and the crystal oscillator are powered down. The rest of the CYW43362 remains powered up in an IDLE state. All main clocks are shut down. The 32.768-kHz LPO sleep clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Sleep mode, the primary power consumed is due to leakage current.
- Power-down modes—The CYW43362 has a full power-down mode and a low-power shutdown mode. A full power-down occurs when there is no VIO voltage, and WL_RST_N and EXT_SMPRS_REQ are low. A low-power shutdown occurs when VIO is present, and WL_RST_N and EXT_SMPRS_REQ are low. In low-power shutdown, only the band gap and LDO3P3 are on. Both power-down modes are exited when the host asserts either WL_RST_N or EXT_SMPS_REQ high.
- External mode—In this mode, the following are true:
  - The assertion of EXT_SMPS_REQ turns only the Core Buck (CBUCK) regulator on.
  - The WLAN is in reset (WL_RST_N = low).
  - The state of LDO3P3 and the band gap are dependent on VBAT and VIO.

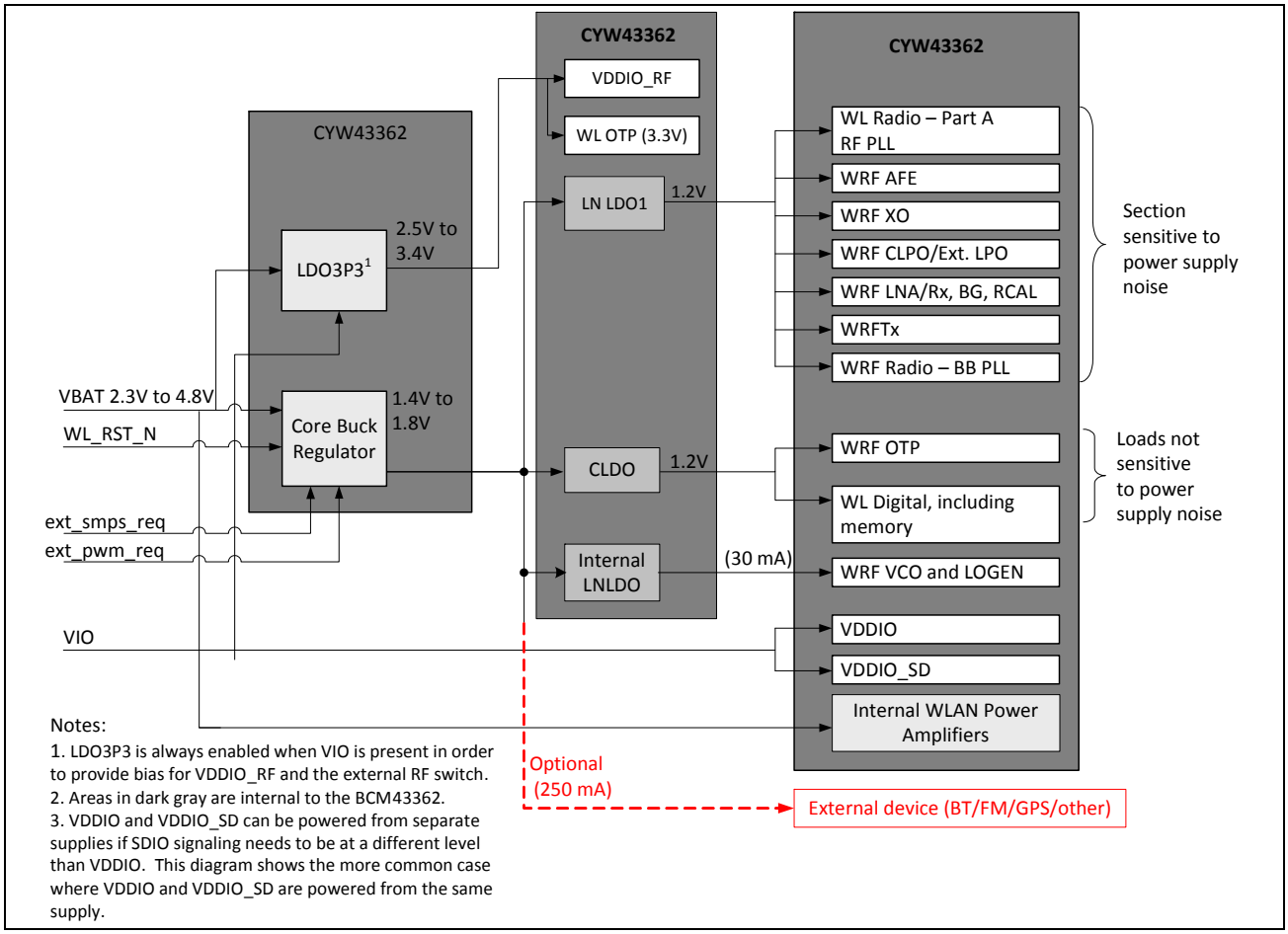
2.2 Power Supply Topology

The CYW43362 contains a Power Management Unit (PMU), a buck-mode switching regulator, and three low noise LDOs. These integrated regulators simplify power supply design in WLAN embedded designs. All regulator inputs and outputs are brought out to pins on the CYW43362, providing system designers with the flexibility to choose which of the CYW43362 integrated regulators to use. One option is to supply the PMU from a single, variable power supply, VBAT, which can range from 2.3V to 4.8V. Using this option, all of the required voltages are provided by CYW43362 regulators except for a low current rail, VIO, which must be provided by the host to power the I/O signal buffers when the chip is out of reset.

Alternately, if specific rails such as 3.3V, 1.8V, and 1.2V already exist in the system, appropriate regulators in the CYW43362 can be bypassed, thereby reducing the cost and board space associated with external regulator components such as inductors and large capacitors.

The CBUCK and CLDO get powered whenever the reset signal is deasserted. The CBUCK regulator can be turned ON by asserting EXT_SMPS_REQ high. Asserting EXT_PWM_REQ high will set CBUCK to PWM mode. Driving EXT_PWM_REQ low will put CBUCK in Burst mode. Optionally, LNLDO may also be powered. All regulators are powered down only when the reset signal is asserted.

Figure 3. Power Topology



2.3 Voltage Regulators

All CYW43362 regulator output voltages are PMU programmable and have the following nominal capabilities. The currents listed below indicate regulator capabilities. See System Power Consumption on page 52 for the actual expected loads.

- Core Buck switching regulator (CBUCK): 2.3–4.8V input, nominal 1.5V output (up to 500 mA).
- LDO3P3: 2.3–4.8V input, nominal 3.3V output (up to 40 mA)
- CLDO (for the core): 1.45–2.0V input, nominal 1.2V output (up to 150 mA)
- Low-noise LNLDO1: 1.45–2.0V input, nominal 1.2V output (up to 150 mA)

See Internal Regulator Electrical Specifications on page 48 for full regulator specifications.

2.4 PMU Sequencing

The WLAN PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Resource requests come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off. Each resource has a timer that contains 0 when the resource is enabled or disabled and a nonzero value in the transition states. The timer is loaded with the resource's time_on or time_off value when the PMU determines that the resource must be enabled or disabled. That timer decrements on each LPO sleep clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can

go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

1. Computes the required resource set based on requests and the resource dependency table.
2. Decrements all timers whose values are nonzero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
3. Compares the request with the current resource status and determines which resources must be enabled or disabled.
4. Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
5. Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Low-Power Shutdown

The CYW43362 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other device in the system, remain operational. When WLAN is not needed, the WLAN core can be put in reset by asserting WL_RST_N (logic LOW). VDDIO_RF and VDDIO remain powered while VIO and VBAT are both present, allowing the CYW43362 to be effectively off while keeping the I/O pins powered. During a low-power shut-down state, provided VIO continues to be supplied to the CYW43362, most outputs are tristated and most inputs are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, enabling the CYW43362 to be a fully integrated embedded device that takes full advantage of the lowest power-saving modes.

Two signals on the CYW43362, the system clock input (OSCIN) and sleep clock input (EXT_SLEEP_CLK), are designed to be high-impedance inputs that do not load down the driving signal even if the CYW43362 does not have VDDIO power applied to it. When the CYW43362 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from before it was powered down.

2.6 CBUCK Regulator Features

The CBUCK regulator has several features that help make the CYW43362 ideal for mobile devices. First, the regulator uses 3.2 MHz as its PWM switching frequency for Buck regulation. This high frequency allows the use of small passive components for the switcher's external circuit, thereby saving PCB space in the design. In addition, the CBUCK regulator has three modes of operation: PWM mode for low-ripple output and for fast transient response and extended load ranges, Burst Mode for lower currents, and Low Power Burst Mode for higher efficiency when the load current is very low (Low Power Burst mode is not available for external devices).

The CBUCK supports external SMPS request to allow flexibility of supplying 1.8V to CYW43362, BCM2076, and other external devices when EXT_SMPS_REQ is asserted high. It also supports low ripple PWM mode (7 mVpp typical) for noise-sensitive applications when EXT_PWM_REQ is asserted high. A 100 µs wait/settling time from the assertion of EXT_PWM_REQ high before increasing the load current allows the internal integrator precharging to complete. This is not a requirement, but is preferred.

Table 2 lists the mode the CBUCK operates in (Burst or PWM), based on various external control signals and internal CBUCK mode register settings.

Table 2. CBUCK Operating Mode Selection

WL_RST_L	EXT_SMPS_REQ	EXT_PWM_REQ	Internal CBUCK Mode Required	CBUCK Mode
0	0	X	X	Off
0	1	0	X	BURST
0	1	1	X	PWM
1	0	X	BURST	BURST
1	0	X	PWM	PWM
1	1	0	BURST	BURST
1	1	0	PWM	PWM
1	1	1	X	PWM

For detailed CBUCK performance specifications, see Core Buck Regulator on page 48.

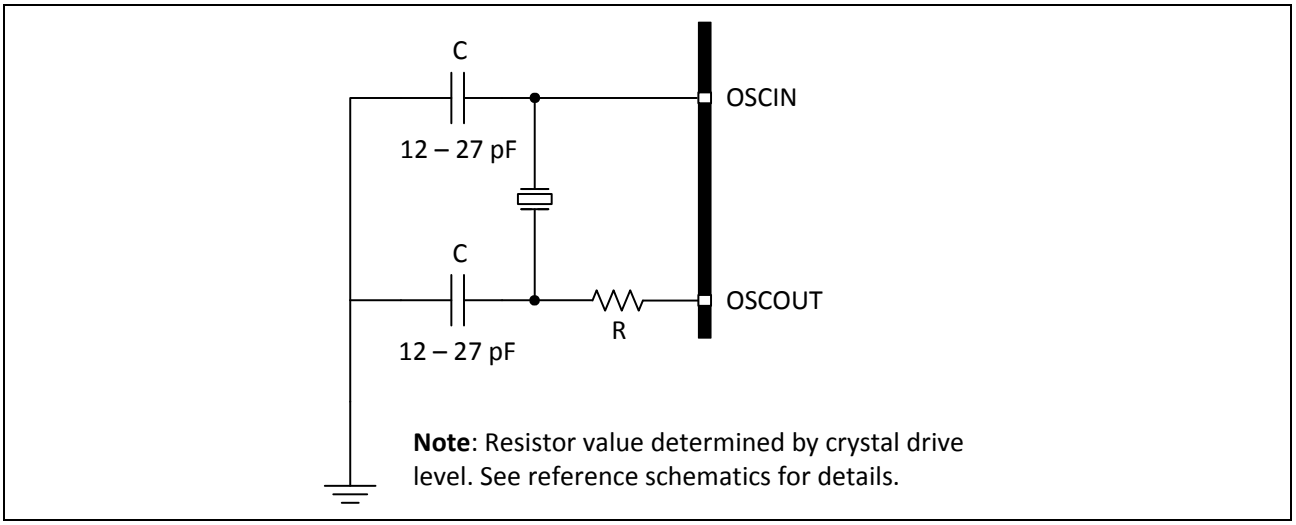
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW43362 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 4. Consult the reference schematics for the latest configuration.

Figure 4. Recommended Oscillator Configuration



The CYW43362 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing. This enables it to operate using numerous frequency references. This may either be an external source such as a TCXO or a crystal interfaced directly to the CYW43362.

The default frequency reference setting is a 26 MHz crystal or TCXO. The signal requirements and characteristics for the crystal interface are shown in Table 3 on page 11.

Note: Although the fractional-N synthesizer can support many reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

3.2 TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the Phase Noise requirements listed in Table 3 on page 11. When the clock is provided by an external TCXO, there are two possible connection methods, as shown in Figure 5 and Figure 6:

1. If the TCXO is dedicated to driving the CYW43362, it should be connected to the OSC_IN pin through an external 1000 pF coupling capacitor, as shown in Figure 5. The internal clock buffer connected to this pin will be turned OFF when the CYW43362 goes into sleep mode. When the clock buffer turns ON and OFF, there will be a small impedance variation up to ±15%. Power must be supplied to the WRF_XTAL_VDD1P2 pin.
2. An alternative is to DC-couple the TCXO to the WRF_TCXO_IN pin, as shown in Figure 6. Use this method when the same TCXO is shared with other devices and a change in the input impedance is not acceptable because it may cause a frequency shift that cannot be tolerated by the other device sharing the TCXO. This pin is connected to a clock buffer powered from WRF_TCXO_VDD3P3. If the power supply to this buffer is always on (even in sleep mode), the clock buffer is always on, thereby ensuring a constant input impedance in all states of the device. The maximum current drawn from WRF_TCXO_VDD3P3 is approximately 500 µA.

Figure 5. Recommended Circuit to Use with an External Dedicated TCXO

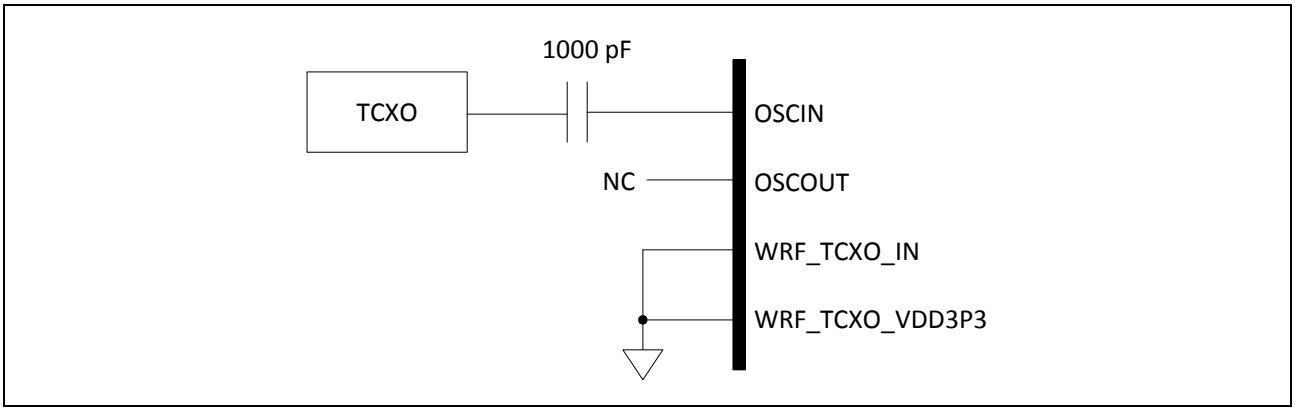


Figure 6. Recommended Circuit to Use with an External Shared TCXO

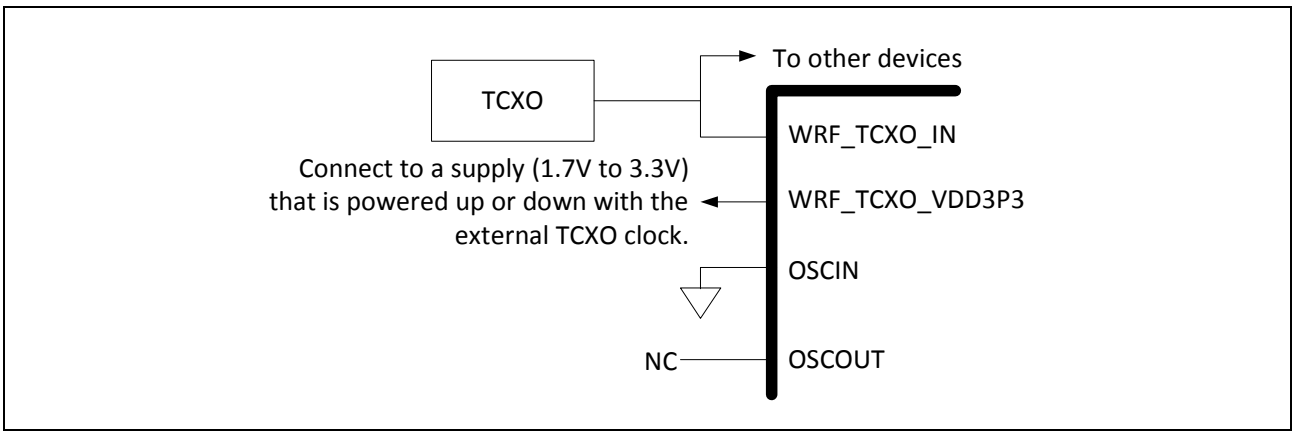


Table 3. Crystal Oscillator and External Clock Requirements and Performance

Parameter	Conditions/Notes	Crystal			External Frequency Reference			Units
		Min	Typ	Max	Min	Typ	Max	
Frequency	–	Between 12 MHz and 52 MHz[a]						
Crystal load capacitance	–	–	12	–				pF
ESR	–	–	–	60				Ω
Input Impedance (OSCIN)[b]	Resistive				30k	100k	–	Ω
	Capacitive				–	–	7.5	pF
Input Impedance (WRF_TCXO_IN)	Resistive				30k	100k	–	Ω
	Capacitive				–	–	4	pF
OSCIN input voltage	AC-coupled analog signal				400	–	1200	mV_{p-p}
OSCIN input low level	DC-coupled digital signal				0	–	0.2	V
OSCIN input high level	DC-coupled digital signal				1.0	–	1.36	V
WRF_TCXO_IN input voltage	DC-coupled analog signal[c]				400	–	TCXO_VDD[d]	mV_{p-p}
Frequency tolerance Initial + over temperature	–	–20	–	20	–20	–	20	ppm

Table 3. Crystal Oscillator and External Clock Requirements and Performance (Cont.)

Parameter	Conditions/Notes	Crystal			External Frequency Reference			
		Min	Typ	Max	Min	Typ	Max	Units
Duty cycle	26 MHz clock				40	50	60	%
Phase Noise[e, f] (IEEE 802.11 b/g)	26 MHz clock at 1 kHz offset				–	–	–119	dBc/Hz
	26 MHz clock at 10 kHz offset				–	–	–129	dBc/Hz
	26 MHz clock at 100 kHz offset				–	–	–134	dBc/Hz
	26 MHz clock at 1 MHz offset				–	–	–139	dBc/Hz
Phase Noise[e, f] (IEEE 802.11n, 2.4 GHz)	26 MHz clock at 1 kHz offset				–	–	–124	dBc/Hz
	26 MHz clock at 10 kHz offset				–	–	–134	dBc/Hz
	26 MHz clock at 100 kHz offset				–	–	–139	dBc/Hz
	26 MHz clock at 1 MHz offset				–	–	–144	dBc/Hz

a. The frequency step size is approximately 80 Hz. The CYW43362 does not auto-detect the reference clock frequency; the frequency is specified in the software/NVRAM file.

b. The internal clock buffer connected to this pin will be turned off when the CYW43362 goes into Sleep mode. When the clock buffer turns on and off, there will be a small impedance variation up to ±15%.

c. This input has an internal DC blocking capacitor, so do not include an external DC blocking capacitor.

d. The maximum allowable voltage swing for the WRF_TCXO_IN input is equal to the WRF_TCX0_VDD3P3 supply voltage range, which is 1.7V to 3.3V.

e. For a clock reference other than 26 MHz, 20 × log10(f/26) dB should be added to the limits, where f = the reference clock frequency in MHz.

f. If the selected clock has a flat phase-noise response above 100 kHz, then it is acceptable to subtract 1 dB from all 1 kHz, 10 kHz, and 100 kHz values shown, and ignore the 1 MHz requirement.

3.3 External 32.768 kHz Low-Power Oscillator

The CYW43362 uses a secondary low-frequency sleep clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 4.

Note: The CYW43362 will auto-detect the LPO clock. If it senses a clock on the EXT_SLEEP_CLK pin, it will use that clock. If it doesn't sense a clock, it will use its own internal LPO.

- To use the internal LPO: Tie EXT_SLEEP_CLK to ground. Do not leave this pin floating. To use an external LPO: Connect the external 32.768 kHz clock to EXT_SLEEP_CLK.

Table 4. External 32.768 kHz Low-Power Oscillator Specifications

Symbol	Parameter	Condition/Notes	Specification			Units
			Minimum	Typical	Maximum	
Fr	Frequency	–	–	32768	–	Hz
Δf/fr	Frequency tolerance	At 25°C	–30	–	+30	ppm
		–20°C <Ta< +70°C	–150	–	+40	
		–30°C <Ta< +85°C	–220	–	+40	
Duty cycle	–	–	30	–	70	%
Vol	Output low voltage	–	0	–	0.2	V
Voh	Output high voltage	–	0.7 Vio	–	Vio	V
Tr/Tf	Rise and fall time	–	–	–	100	ns
–	Signal type	Digital	–	–	–	–
–	Clock jitter	Integrated over 300 Hz to 15 kHz	–	–	30	ns
–	Input impedance	Resistive	10	–	–	MΩ
		Capacitive	–	–	2	pF
–	Input amplitude	Fail safe, 3.3V digital I/O	–	–	3.63	V

4. WLAN System Interfaces

4.1 SDIO v2.0

The CYW43362 WLAN section supports SDIO version 2.0. for both 1-bit (25 Mbps), 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks—200 Mbps). It has the ability to map the interrupt signal on a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided.

SDIO mode is enabled using the strapping option pins. See Table 11 on page 40 for details.

Three functions are supported:

- Function 0 Standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B)

4.1.1 SDIO Pin Descriptions

Table 5. SDIO Pin Descriptions

SD 4-Bit Mode		SD 1-Bit Mode		gSPI Mode	
DATA0	Data line 0	DATA	Data line	DO	Data output
DATA1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data line 2	NC	Not used	NC	Not used
DATA3	Data line 3	NC	Not used	CS	Card select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command line	CMD	Command line	DI	Data input

Figure 7. Signal Connections to SDIO Host (SD 4-Bit Mode)

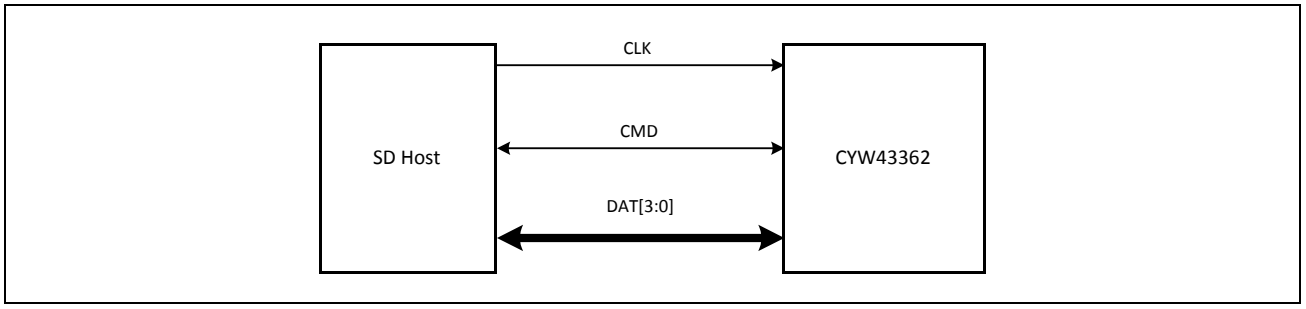
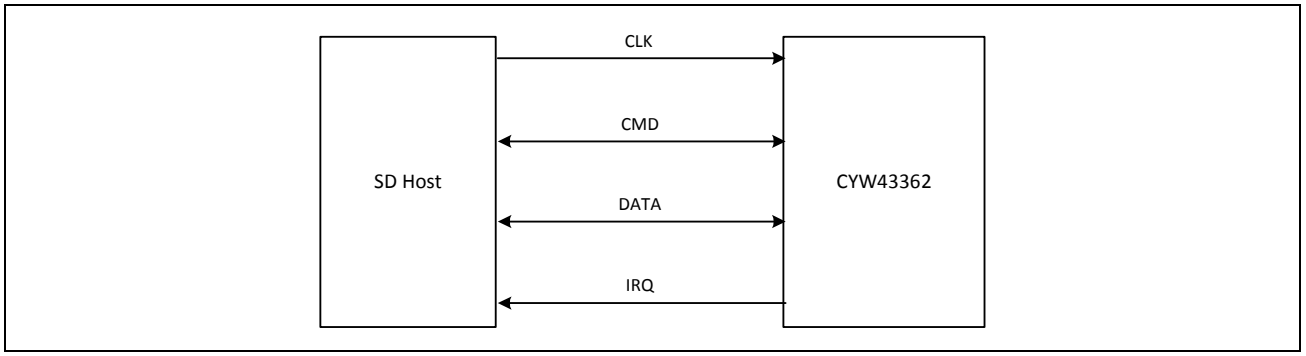


Figure 8. Signal Connections to SDIO Host (SD 1-Bit Mode)



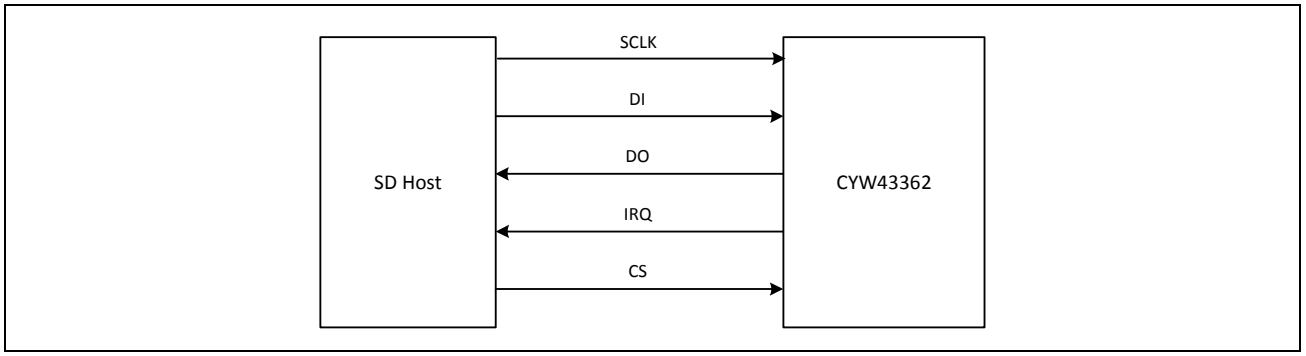
4.2 Generic SPI Mode

In addition to the full SDIO mode, the CYW43362 includes the option of using the simplified generic SPI (gSPI) interface/protocol. Characteristics of the gSPI mode include:

- Supports up to 50 MHz operation
- Supports fixed delays for responses and data from device
- Supports alignment to host gSPI frames (16 or 32 bits)
- Supports up to 2 KB frame size per transfer
- Supports little-endian and big-endian configurations
- Supports configurable active edge for shifting
- Supports packet transfer through DMA for WLAN

gSPI mode is enabled using the strapping option pins. See Table 11 on page 40 for details.

Figure 9. Signal Connections to SDIO Host (gSPI Mode)



4.2.1 SPI Protocol

The SPI protocol supports both 16-bit and 32-bit word operation. Byte endianess is supported in both modes. Figure 10 and Figure 11 show the basic write and write/read commands.

Figure 10. gSPI Write Protocol

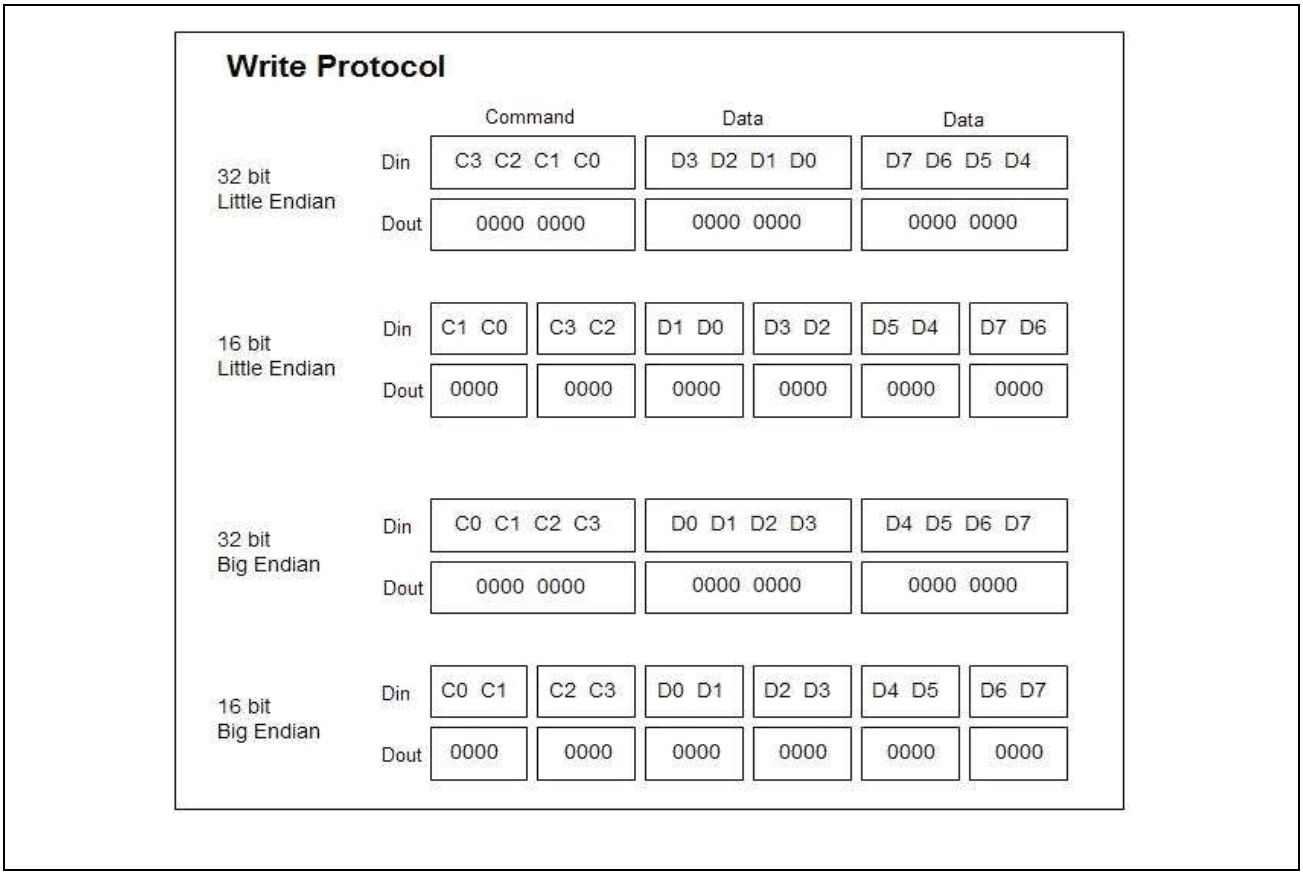
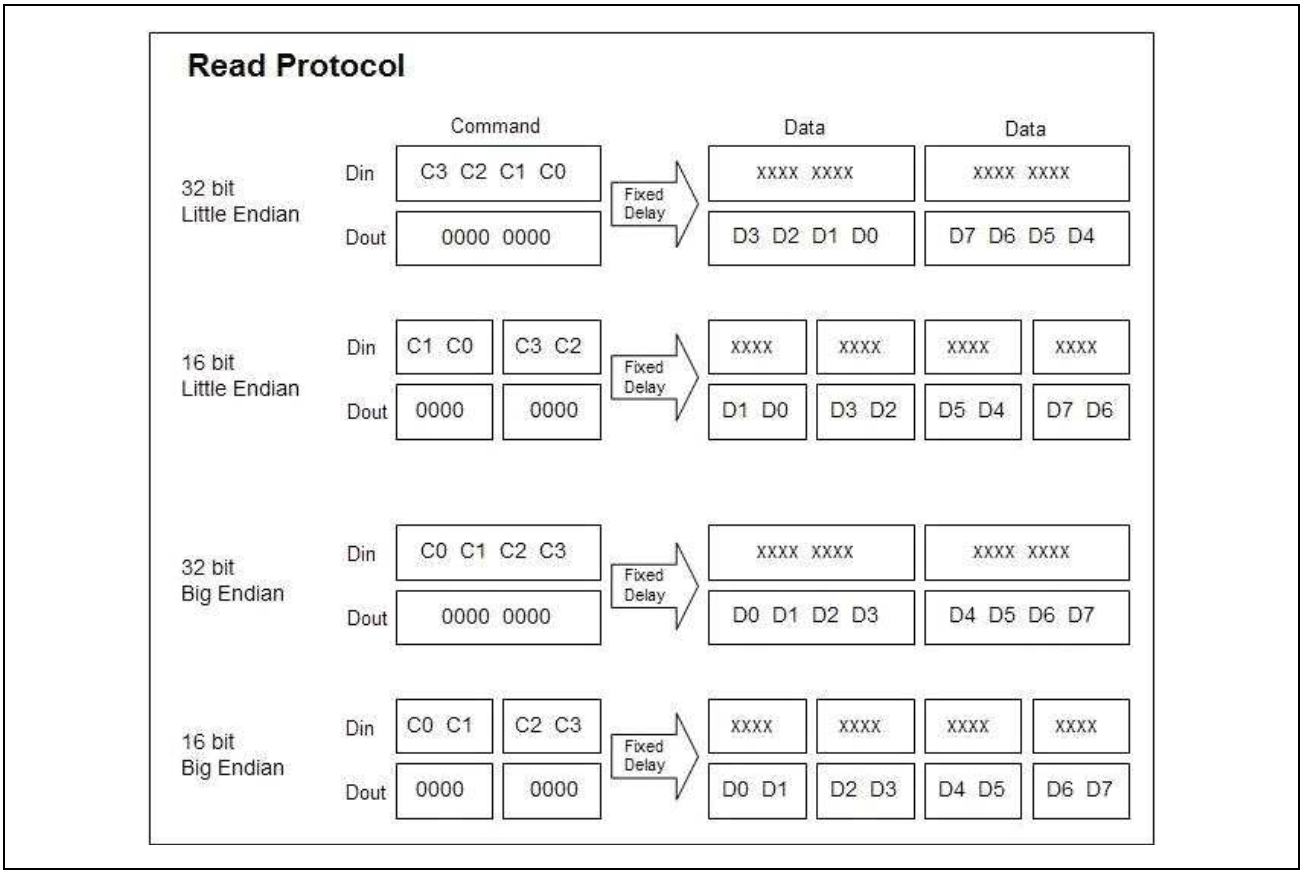


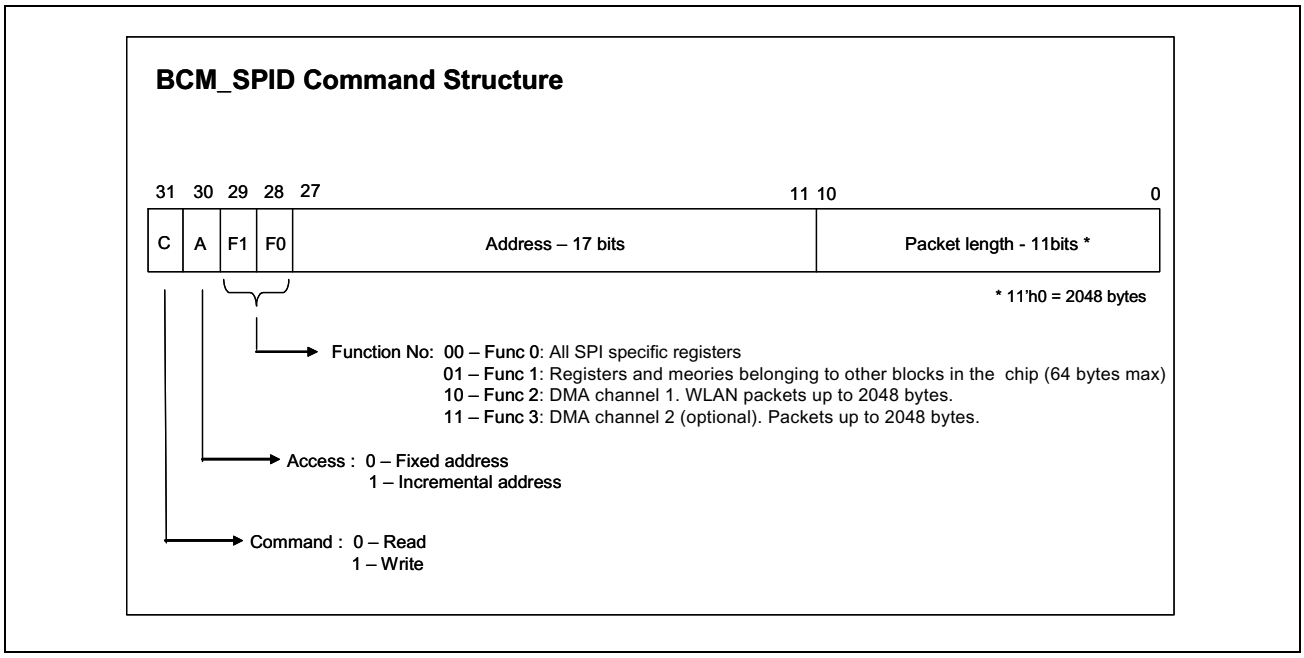
Figure 11. gSPI Read Protocol



4.2.1.1 Command Structure

The gSPI command structure is 32 bits. The bit positions and definitions are as shown in Figure 12.

Figure 12. gSPI Command Structure



4.2.1.2 Write

The host puts the first bit of the data onto the bus half a clock-cycle before the first active edge following the CS going low. The following bits are clocked out on the falling edge of the gSPI clock. The device samples the data on the active edge.

4.2.1.3 Write/Read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising clock edge of the clock burst for the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

4.2.1.4 Read

The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write/read command in the following respects: a) chip selects go high between the command/address and the data and b) the time interval between the command/address is not fixed.

4.2.1.5 Status

The gSPI interface supports status notification to the host after a read/write transaction. This status notification provides information about any packet errors, protocol errors, information about available packet in the RX queue, etc. The status information helps in reducing the number of interrupts to the host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The gSPI bus timing for read/write transactions with and without status notification are as shown in Figure 13 below and Figure 14 on page 19. See Table 6 on page 19 for information on status field details.

Figure 13. gSPI Signal Timing Without Status

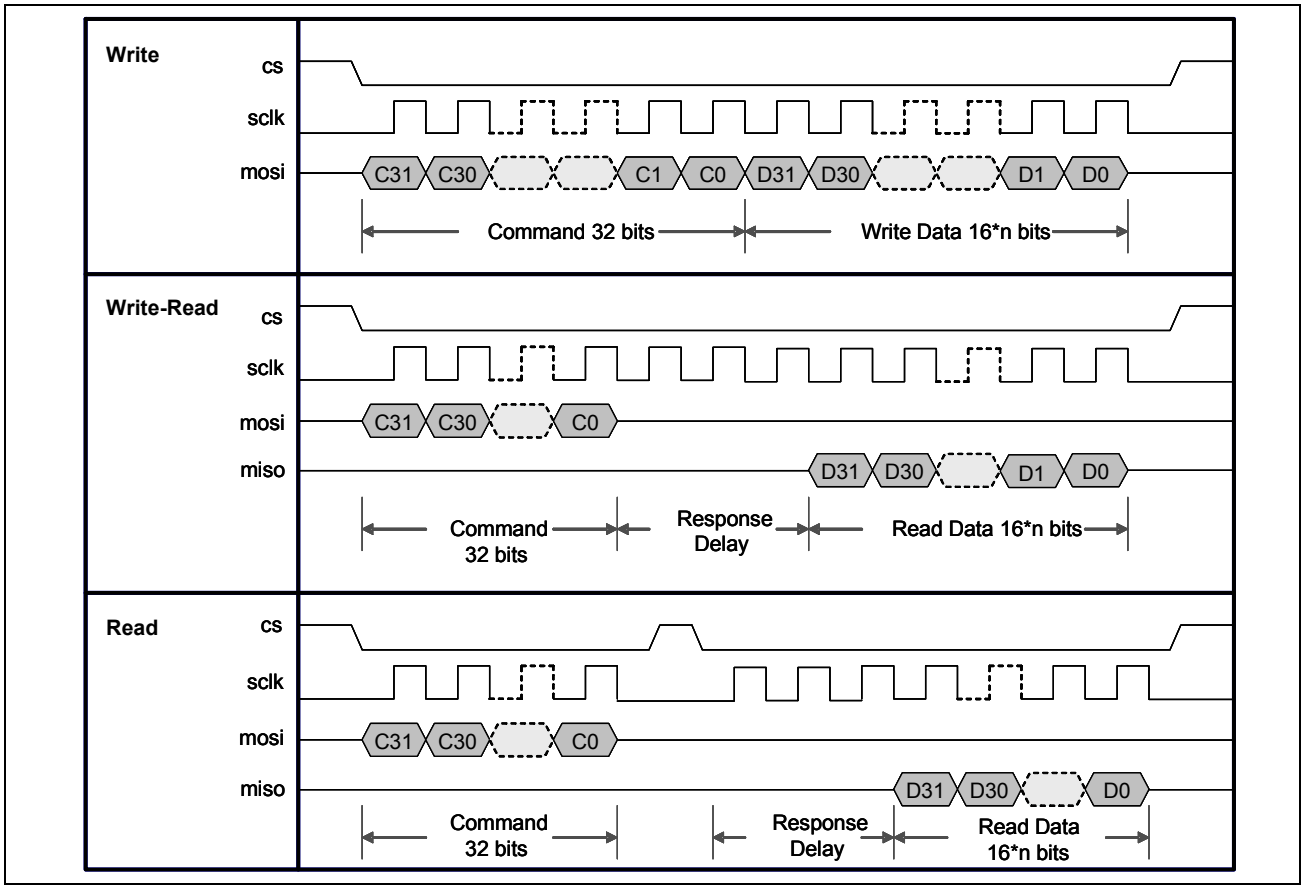


Figure 14. gSPI Signal Timing with Status (Response Delay = 0)

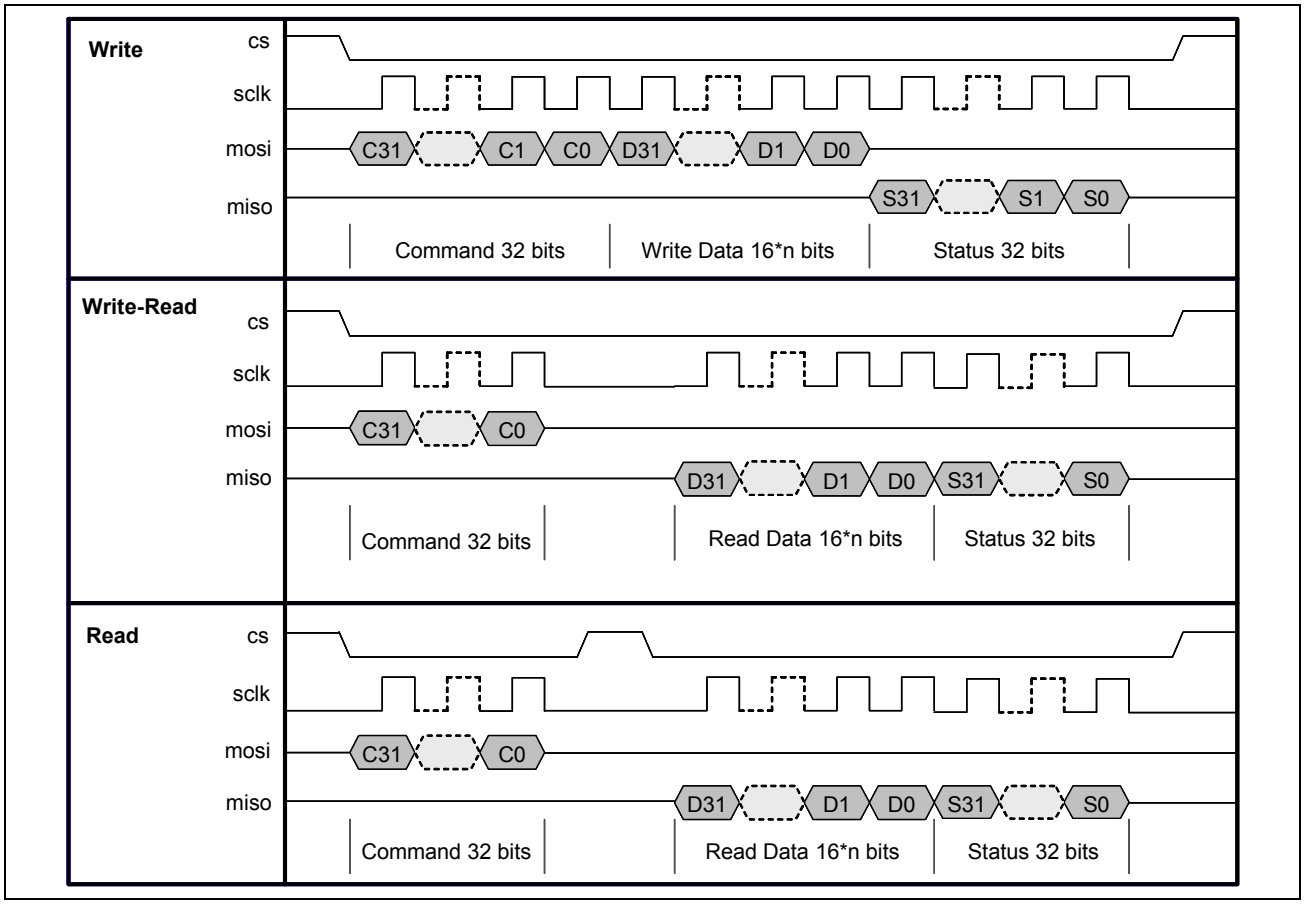


Table 6. gSPI Status Field Details

Bit	Name	Description
0	Data not available	The requested read data is not available.
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command.
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command.
3	F2 interrupt	F2 channel interrupt
5	F2 RX Ready	F2 FIFO is ready to receive data (FIFO empty).
7	Reserved	–
8	F2 Packet Available	Packet is available/ready in F2 TX FIFO.
9:19	F2 Packet Length	Length of packet available in F2 FIFO

4.2.2 gSPI Host-Device Handshake

To initiate communication through the gSPI after power-up, the host needs to bring up the WLAN/Chip by writing to the wake-up WLAN register bit. Writing a 1 to this bit will start up the necessary crystals and PLLs so that the CYW43362 is ready for data transfer. The device can signal an interrupt to the host indicating that the device is awake and ready. This procedure also needs to be followed for waking up the device in sleep mode. The device can interrupt the host using the WLAN IRQ line whenever it has any information to pass to the host. On getting an interrupt, the host needs to read the interrupt and/or status register to determine the cause of interrupt and then take necessary actions.

4.2.3 Boot-Up Sequence

After power-up, the gSPI host needs to wait 50 ms for the device to be out of reset. For this, the host needs to poll with a read command to F0 addr 0x14. Address 0x14 contains a predefined bit pattern. As soon as the host gets a response back with the correct register content, it implies that the device has powered up and is out of reset. After that, the host needs to set the wakeup-WLAN bit (F0 reg 0x00 bit 7). Wakeup-WLAN turns the PLL on; however, the PLL doesn't lock until the host programs the PLL registers to set the crystal frequency.

For the first time after power-up, the host needs to wait for the availability of low-power clock inside the device. Once that is available, the host needs to write to a PMU register to set the crystal frequency. This will turn on the PLL. After the PLL is locked, the chipActive interrupt is issued to the host. This indicates device awake/ready status. See Table 7 for information on gSPI registers.

In Table 7, the following notation is used for register access:

- R: Readable from host and CPU
- W: Writable from host
- U: Writable from CPU

Table 7. gSPI Registers

Address	Register	Bit	Access	Default	Description
x0000	Word length	0	R/W/U	0	0: 16-bit word length 1: 32-bit word length
	Endianess	1	R/W/U	0	0: Little Endian 1: Big Endian
	High-speed mode	4	R/W/U	1	0: Normal mode. Sample on SPICLK rising edge, output on falling edge. 1: High-speed mode. Sample and output on rising edge of SPICLK (default).
	Interrupt polarity	5	R/W/U	1	0: Interrupt active polarity is low. 1: Interrupt active polarity is high (default).
	Wake-up	7	R/W	0	A write of 1 will denote wake-up command from host to device. This will be followed by a F2 Interrupt from gSPI device to host, indicating device awake status.
x0002	Status enable	0	R/W	1	0: no status sent to host after read/write 1: status sent to host after read/write
	Interrupt with status	1	R/W	0	0: do not interrupt if status is sent 1: interrupt host even if status is sent
x0003	Reserved	–	–	–	–
x0004	Interrupt register	0	R/W	0	Requested data not available; Cleared by writing a 1 to this location
		1	R	0	F2/F3 FIFO underflow due to last read
		2	R	0	F2/F3 FIFO overflow due to last write
		5	R	0	F2 packet available
		6	R	0	F3 packet available
		7	R	0	F1 overflow due to last write
x0005	Interrupt register	5	R	0	F1 Interrupt
		6	R	0	F2 Interrupt
		7	R	0	F3 Interrupt
x0006, x0007	Interrupt enable register	15:0	R/W/U	16'hE0E7	Particular Interrupt is enabled if a corresponding bit is set
x0008 to x000B	Status register	31:0	R	32'h0000	Same as status bit definitions
x000C, x000D	F1 info register	0	R	1	F1 enabled
		1	R	0	F1 ready for data transfer
		13:2	R/U	12'h40	F1 max packet size

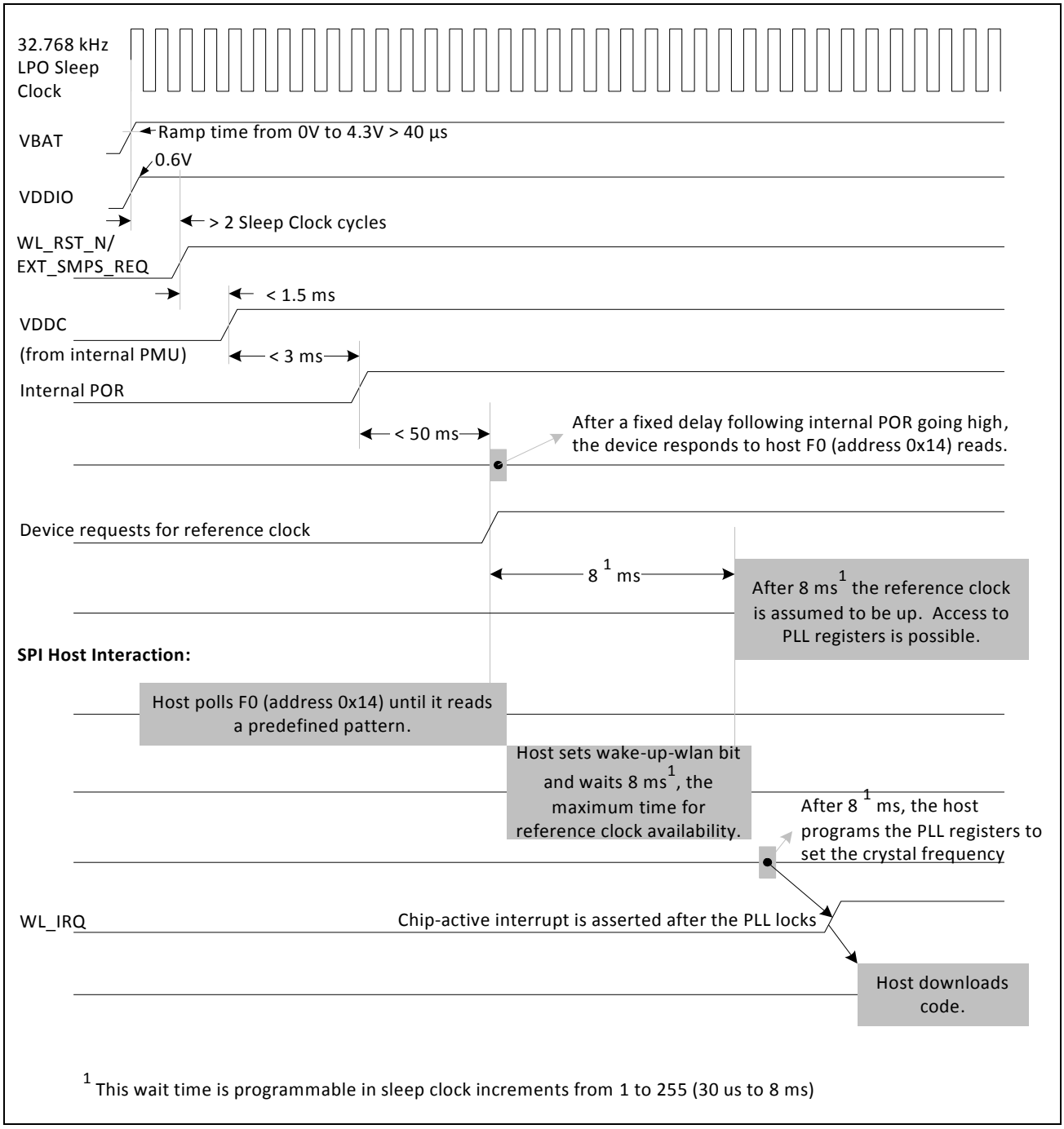
Table 7. gSPI Registers (Cont.)

Address	Register	Bit	Access	Default	Description
x000E, x000F	F2 info register	0	R/U	1	F2 enabled
		1	R	0	F2 ready for data transfer
		15:2	R/U	14'h800	F2 max packet size
x0014 to x0017	Test–Read only register	31:0	R	32'hFEEDBEAD	This register contains a predefined pattern, which the host can read and determine if the gSPI interface is working properly.
x0018 to x001B	Test–R/W register	31:0	R/W/U	32'h00000000	This is a dummy register where the host can write some pattern and read it back to determine if the gSPI interface is working properly.
x001C to x001F	Response delay registers	7:0	R/W	0x1D = 4, other registers = 0	Individual response delays for F0, F1, F2, and F3. The value of the registers is the number of byte delays that are introduced before data is shifted out of the gSPI interface during host reads.

Figure 15 on page 22 shows the WLAN boot-up sequence from power-up to firmware download, including the initial device power-on reset (POR) evoked by the WL_RST_N signal. After initial power-up, the WL_RST_N signal can be held low to disable the CYW43362 or pulsed low to induce a subsequent reset.

Note: The CYW43362 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 3 ms after VDD and VDDIO have both passed the 0.6V threshold.

Figure 15. WLAN Boot-Up Sequence



4.3 External Coexistence Interface

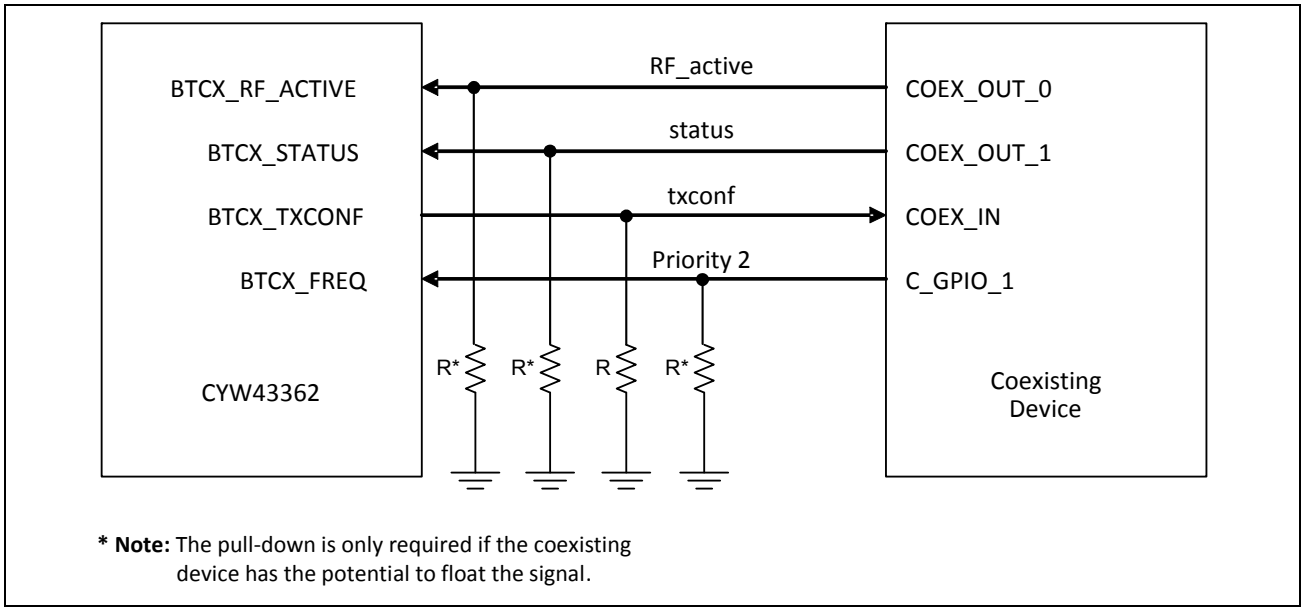
To manage wireless medium sharing for optimal performance, an external coexistence interface is provided that enables signaling between the CYW43362 and one or two external collocated wireless devices such as Bluetooth and/or WiMax. Note that three of the External Coexistence Interface pins are multiplexed with GPIOs. By default, the pins are BT_COEX pins. Through software they can be changed to GPIOs. The fourth BT_COEX signal is also multiplexed with a GPIO, but this one is a GPIO by default and can be changed via software to be BTCX_FREQ. See Pinout and Signal Descriptions on page 32 for more details.

The signals in Table 8 can be enabled by software.

Table 8. Coexistence Signals

Signal	Description
BTCX_STATUS	Coexistence signal indicating Bluetooth priority status and TX/RX direction.
BTCX_RF_ACTIVE	Coexistence signal indicating that Bluetooth is active.
BTCX_FREQ	Indicates that the coexisting Bluetooth is about to transmit on a restricted channel.
BTCX_TXCONF	Coexistence output giving Bluetooth permission to transmit.

Figure 16. 4-Wire Coexistence Wiring



5. Wireless LAN MAC and PHY

5.1 MAC Features

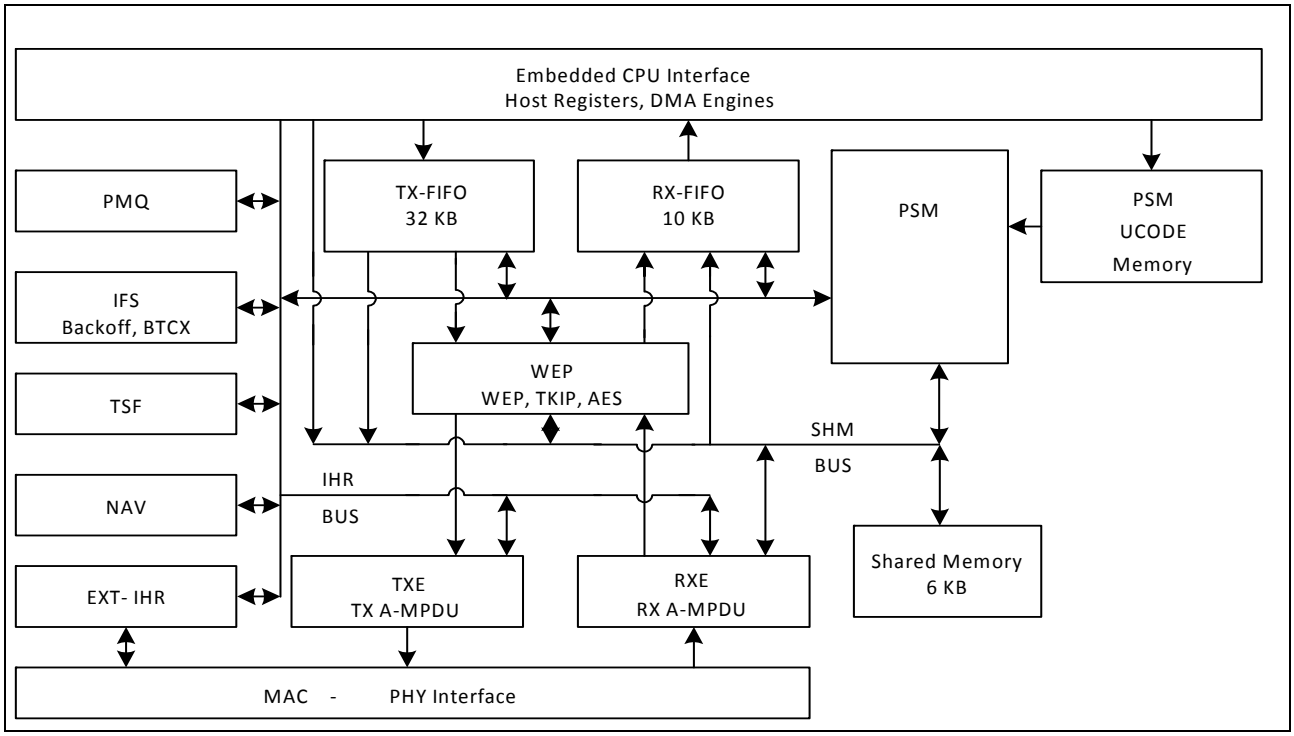
The CYW43362 WLAN MAC supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

- Transmission and reception of aggregated MPDUs (A-MPDU)
- Support for power management schemes, including WMM power-save, power-save multipoll (PSMP) and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware off-load for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

5.1.1 MAC Description

The CYW43362 WLAN MAC is designed to support high throughput operation with low-power consumption. It does so without compromising on Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power-saving modes that have been implemented allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 17 on page 24.

Figure 17. WLAN MAC Architecture



The following sections provide an overview of the important modules in the MAC.

5.1.1.1 PSM

The programmable state machine (PSM) is a microcoded engine that provides most of the low-level control to the hardware to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are collocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations, the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

5.1.1.2 WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, as well as MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

Based on the frame type and association information, the PSM determines the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames. WAPI is also supported.

5.1.1.3 TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

5.1.1.4 RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.