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Single-Chip IEEE 802.11 b/g/n MAC/ Baseband/Radio with Bluetooth 4.1, an FM Receiver, and Wireless Charging

The Cypress CYW4343X is a highly integrated single-chip solution and offers the lowest RBOM in the industry for smartphones smartphones wearables, tablets, and a wide range of other portable devices. The chip includes a 2.4 GHz WLAN IEEE 802.11 b/g/n MAC/baseband/radio, Bluetooth 4.1 support, and an FM receiver. In addition, it integrates a power amplifier (PA) that meets the output power requirements of most handheld systems, a low-noise amplifier (LNA) for best-in-class receiver sensitivity, and an internal transmit/receive (iTR) RF switch, further reducing the overall solution cost and printed circuit board area.

The WLAN host interface supports gSPI and SDIO v2.0 modes, providing a raw data transfer rate up to 200 Mbps when operating in 4-bit mode at a 50 MHz bus frequency. An independent, high-speed UART is provided for the Bluetooth/FM host interface.Using advanced design techniques and process technology to reduce active and idle power, the CYW4343X is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It includes a power management unit that simplifies the system power topology and allows for operation directly from a rechargeable mobile platform battery while maximizing battery life.

The CYW4343X implements the world's most advanced Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative WLAN and Bluetooth coexistence.

Figure 1. CYW4343X System Block Diagram

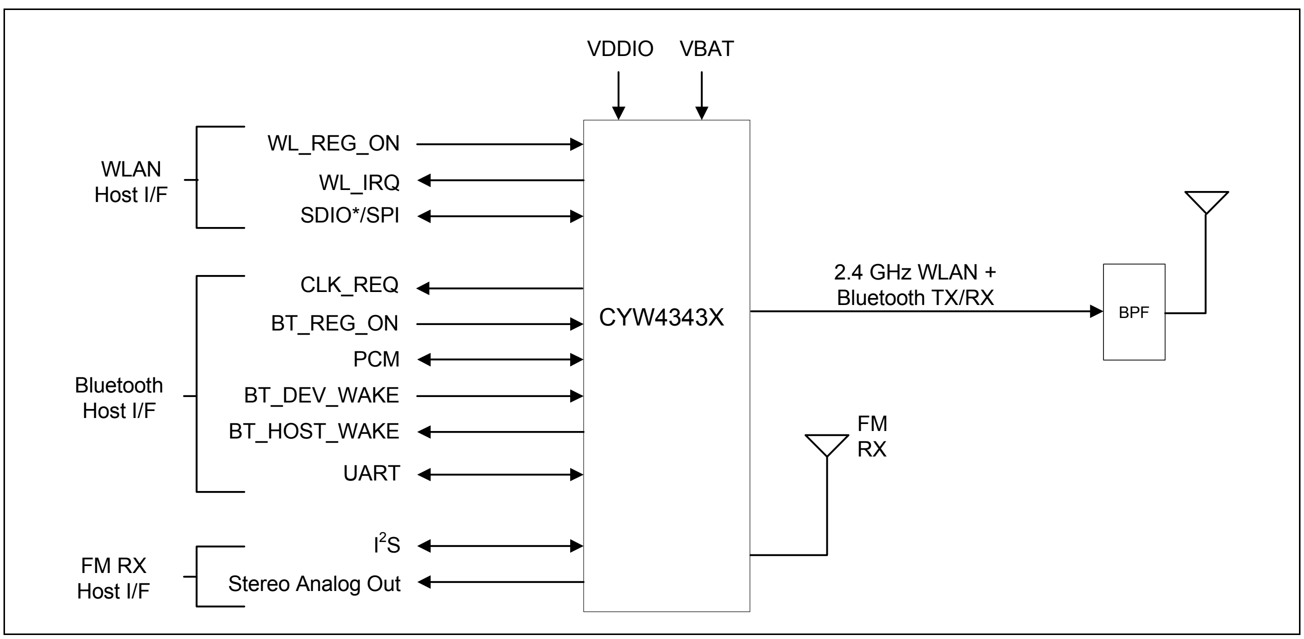
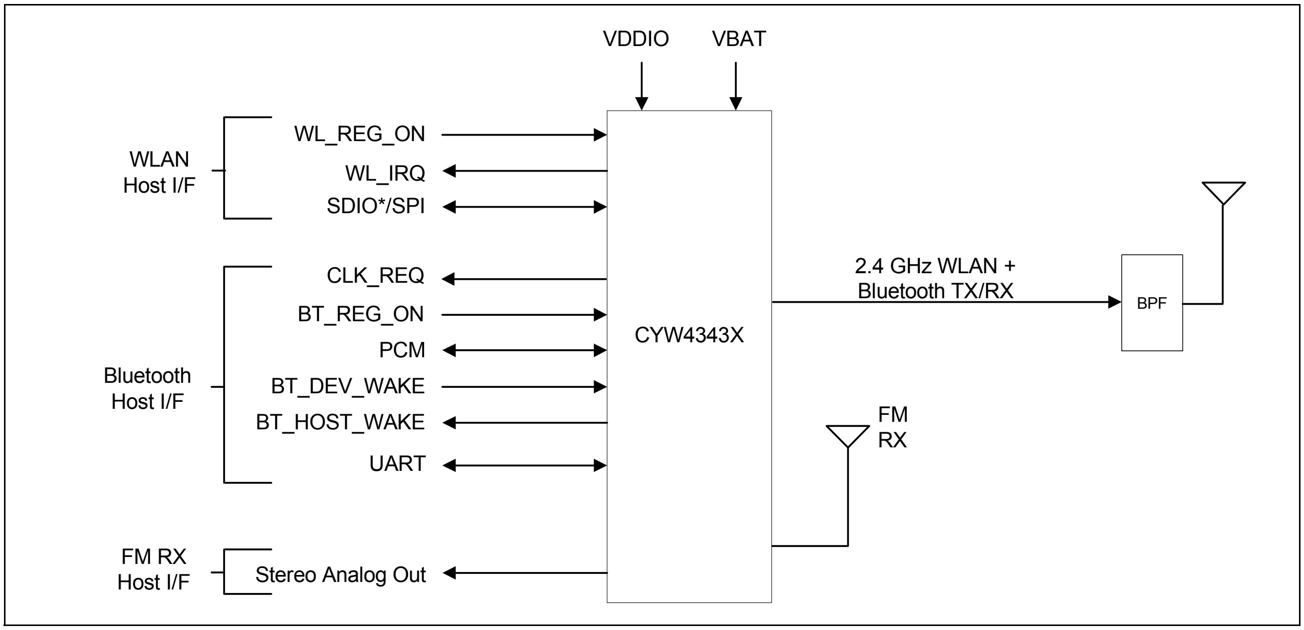


Figure 2. CYW4343X System Block Diagram



Features

IEEE 802.11x Key Features

- Single-band 2.4 GHz IEEE 802.11b/g/n.
- Support for 2.4 GHz Cypress TurboQAM® data rates (256-QAM) and 20 MHz channel bandwidth.
- Integrated iTR switch supports a single 2.4 GHz antenna shared between WLAN and Bluetooth.
- Supports explicit IEEE 802.11n transmit beamforming
- Tx and Rx Low-density Parity Check (LDPC) support for improved range and power efficiency.
- Supports standard SDIO v2.0 and gSPI host interfaces.
- Supports Space-Time Block Coding (STBC) in the receiver.
- Integrated ARM Cortex-M3 processor and on-chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field-upgrade with future features. On-chip memory includes 512 KB SRAM and 640 KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as to future devices.

Bluetooth and FM Key Features

- Complies with Bluetooth Core Specification Version 4.1 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference.
- Interface support — Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data.Bluetooth and FM Key Features (Continued)
- FM receiver unit supports HCI for communication.
- Low-power consumption improves battery life of handheld devices.
- FM receiver: 65 MHz to 108 MHz FM bands; supports the European Radio Data Systems (RDS) and the North American Radio Broadcast Data System (RBDS) standards.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values.

General Features

- Supports a battery voltage range from 3.0V to 4.8V with an internal switching regulator.
- Programmable dynamic power management.
- 4 Kbit One-Time Programmable (OTP) memory for storing board parameters.
- Can be routed on low-cost 1 x 1 PCB stack-ups.
- 74-ball[4343W+43CS4343W1]74-ball 63-ball WLBGA package (4.87 mm × 2.87 mm, 0.4 mm pitch).
- 153-bump WLCSP package (115 µm bump diameter, 180 µm bump pitch).
- Security:
  - WPA and WPA2 (Personal) support for powerful encryption and authentication.
  - AES in WLAN hardware for faster data encryption and IEEE 802.11i compatibility.
  - Reference WLAN subsystem provides Cisco Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0).
  - Reference WLAN subsystem provides Wi–Fi Protected Setup (WPS).
- Worldwide regulatory support: Global products supported with worldwide homologated design.
- Multimode wireless charging support that complies with the Alliance for Wireless Power (A4WP), the Wireless Power Consortium (WPC), and the Power Matters Alliance (PMA).

Introduction

This document provides details of the functional, operational, and electrical characteristics of the Cypress CYW4343X. It is intended for hardware design, application, and OEM engineers.

Cypress part numbering scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4343SKUBG	CYW4343SKUBG
BCM4343WKUBG	CYW4343WKUBG
BCM4343WKWBG	CYW4343WKWBG
BCM4343W1KUBG	CYW4343W1KUBG

IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

Contents

1. Overview

1.1 Overview

The Cypress CYW4343X provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 b/g/n. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. The CYW4343X is designed to address the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 3 on page 7 Figure 4 on page 8 Figure 3 on page 7 shows the interconnection of all the major physical blocks in the CYW4343X and their associated external interfaces, which are described in greater detail in subsequent sections.

Figure 3. CYW4343X Block Diagram

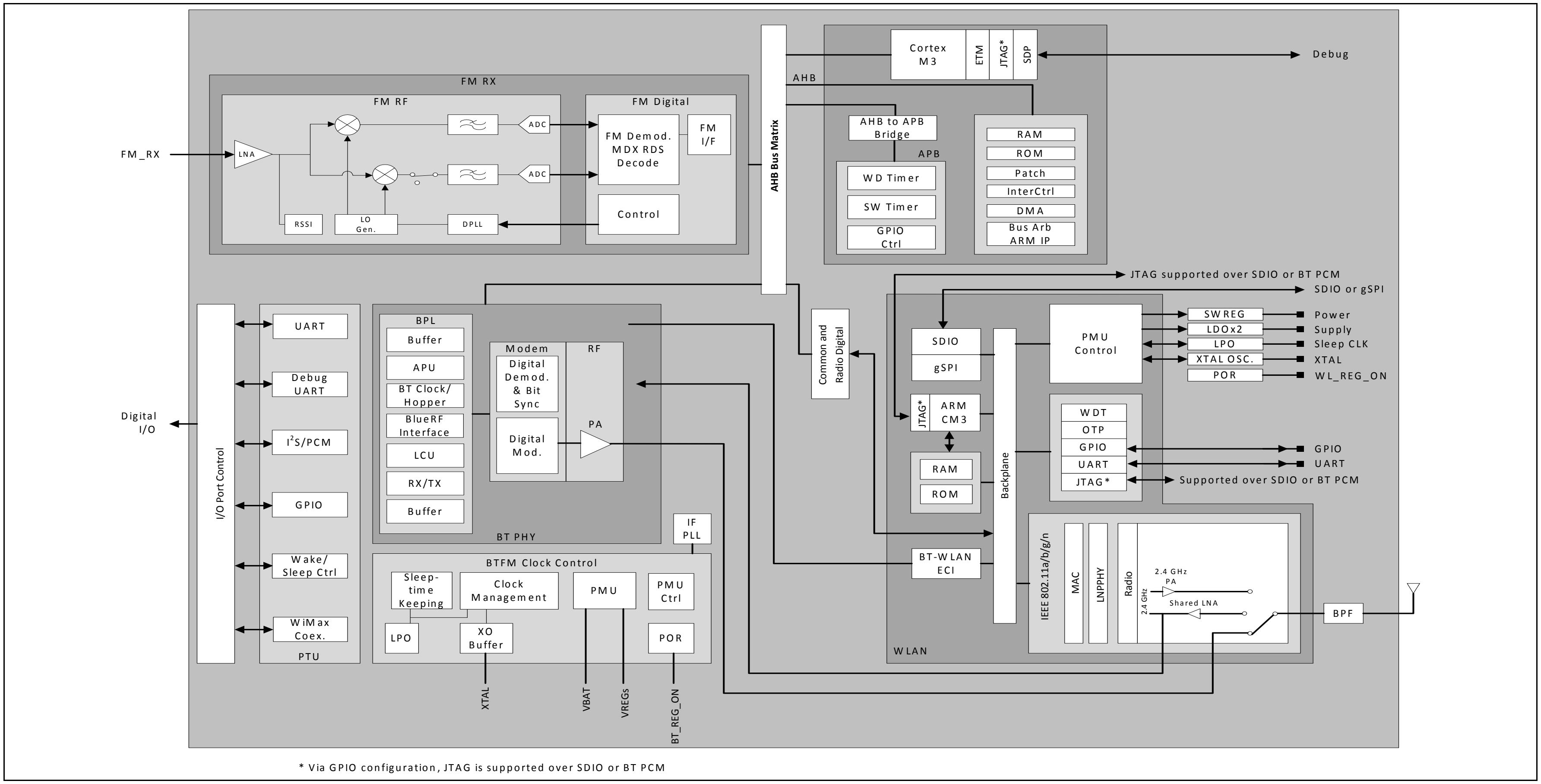
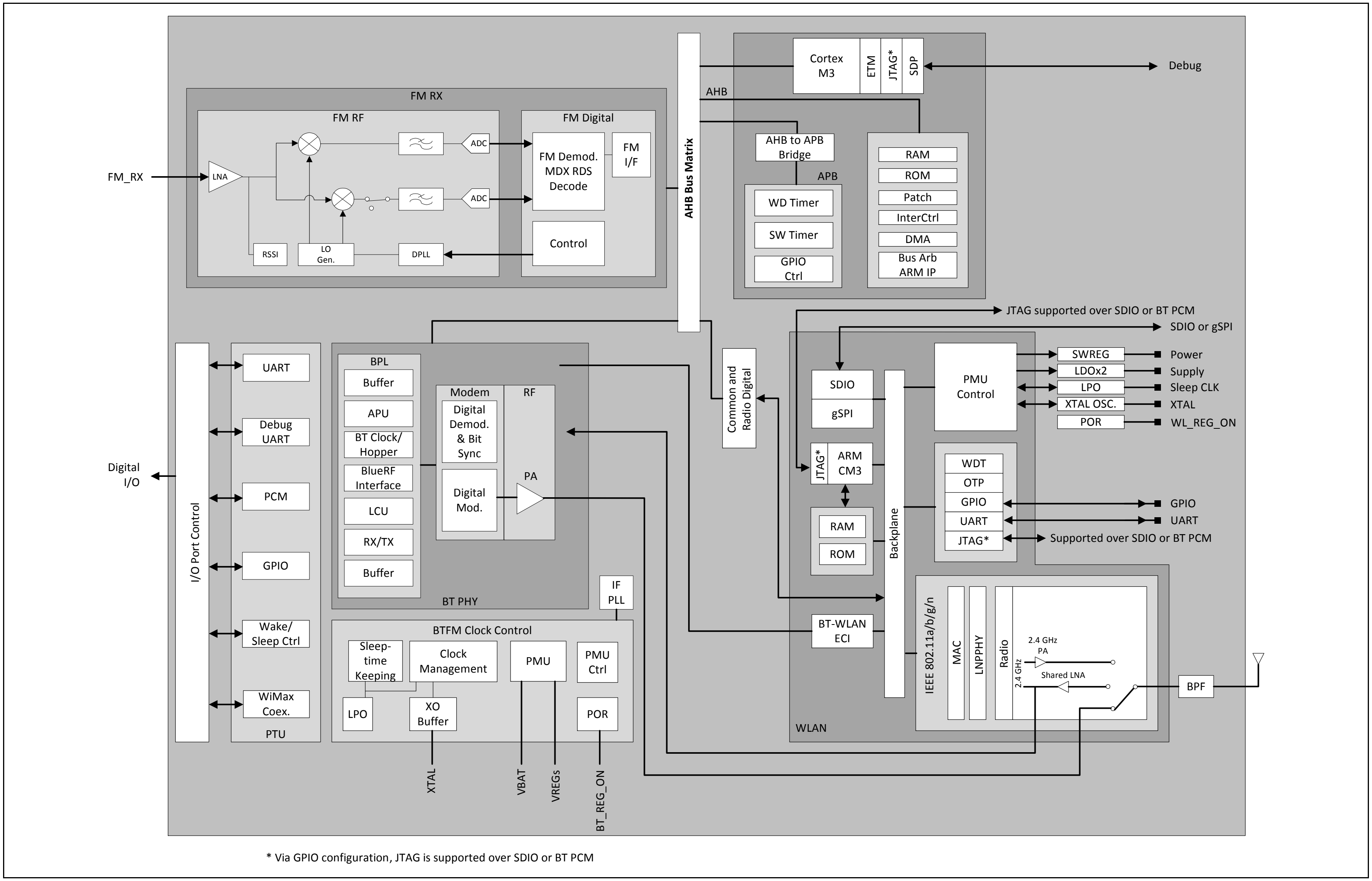


Figure 4. CYW4343X Block Diagram



* Via GPIO configuration, JTAG is supported over SDIO or BT PCM

1.2 Features

The CYW4343X supports the following WLAN, Bluetooth, and FM features:

- IEEE 802.11b/g/n single-band radio with an internal power amplifier, LNA, and T/R switch
- Bluetooth v4.1 with integrated Class 1 PA
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Simultaneous BT/WLAN reception with a single antenna
- WLAN host interface options:
  - SDIO v2.0, including default and high-speed timing.
  - gSPI—up to a 50 MHz clock rate
- BT UART (up to 4 Mbps) host digital interface that can be used concurrently with the above WLAN host interfaces.
- ECI—enhanced coexistence support, which coordinates BT SCO transmissions around WLAN receptions.
- I^2S/PCM for FM/BT audio, HCI for FM block control
- HCI high-speed UART (H4 and H5) transport support
- Wideband speech support (16 bits, 16 kHz sampling PCM, through I^2S and PCM interfaces)
- Bluetooth SmartAudio® technology improves voice and music quality to headsets.
- Bluetooth low power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- FM advanced internal antenna support
- FM auto searching/tuning functions
- FM multiple audio routing options: I^2S, PCM, eSCO, and A2DP
- FM mono-stereo blending and switching, and soft mute support
- FM audio pause detection support
- Multiple simultaneous A2DP audio streams
- FM over Bluetooth operation and on-chip stereo headset emulation

1.3 Standards Compliance

The CYW4343X supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0
- Bluetooth 4.1 (Bluetooth Low Energy)
- 65 MHz to 108 MHz FM bands (US, Europe, and Japan)
- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The CYW4343X will support the following future drafts/standards:

- IEEE 802.11r — Fast Roaming (between APs)
- IEEE 802.11k — Resource Management
- IEEE 802.11w — Secure Management Frames
- IEEE 802.11 Extensions:
- IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
- IEEE 802.11i MAC Enhancements
- IEEE 802.11r Fast Roaming Support
- IEEE 802.11k Radio Resource Measurement

The CYW4343X supports the following security features and proprietary protocols:

- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - WAPI
  - AES (Hardware Accelerator)
  - TKIP (host-computed)
  - CKIP (SW Support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
- IEEE 802.15.2 Coexistence Compliance — on silicon solution compliant with IEEE 3-wire requirements.

2. Power Supplies and Power Management

2.1 Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW4343X. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth, WLAN, and FM functions in embedded designs.

A single VBAT (3.0V to 4.8V DC maximum) and VDDIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the CYW4343X.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power up the regulators and take the respective circuit blocks out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO can be turned on and off based on the dynamic demands of the digital baseband.

The CYW4343X allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, LPLDO1 provides the CYW4343X with all required voltage, further reducing leakage currents.

Note: VBAT should be connected to the LDO_VDDBAT5V and SR_VDDBAT5V pins of the device.

Note: VDDIO should be connected to the SYS_VDDIO and WCC_VDDIO pins WCC_VDDIO pin of the device.

2.2 CYW4343X PMU Features

The PMU supports the following:

- VBAT to 1.35Vout (170 mA nominal, 370 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (250 mA nominal, 450 mA maximum 800 mA peak maximum) LDO3P3
- 1.35V to 1.2Vout (100 mA nominal, 150 mA maximum) LNLDO
- 1.35V to 1.2Vout (80 mA nominal, 200 mA maximum) CLDO with bypass mode for deep sleep
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wake-up timing from extremely low power-consumption mode.
- PMU input supplies automatic sensing and fast switching to support A4WP operations.

Figure 5 on page 12 Figure 6 on page 13 Figure 7 on page 14 and Figure 8 on page 15Figure 9 on page 16 Figure 10 on page 17 show the typical power topology of the CYW4343X.

Figure 5. Typical Power Topology (1 of 2)(4343S)

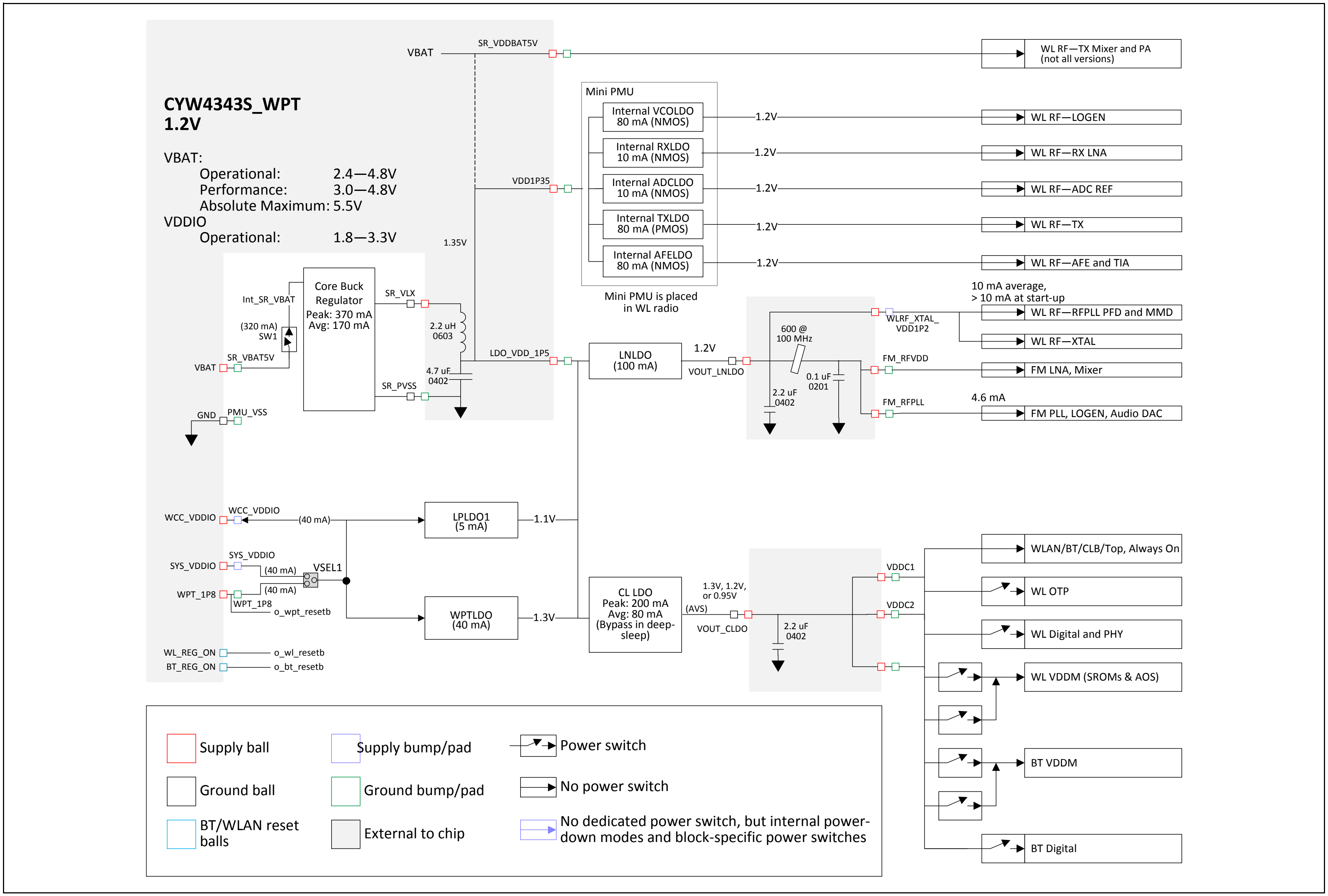


Figure 6. Typical Power Topology (1 of 2)(4343W+43CS4343W1)

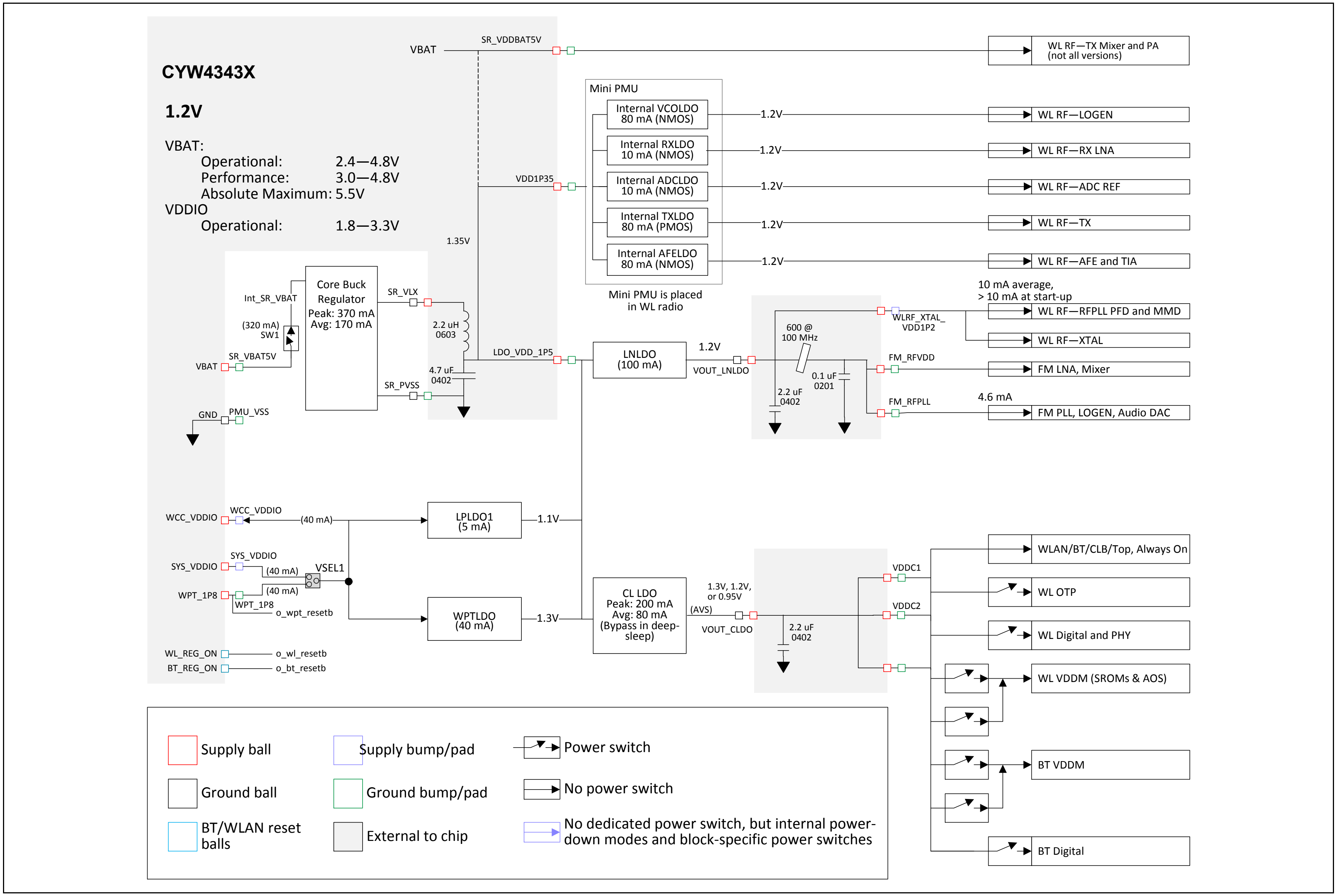


Figure 7. Typical Power Topology (1 of 2)

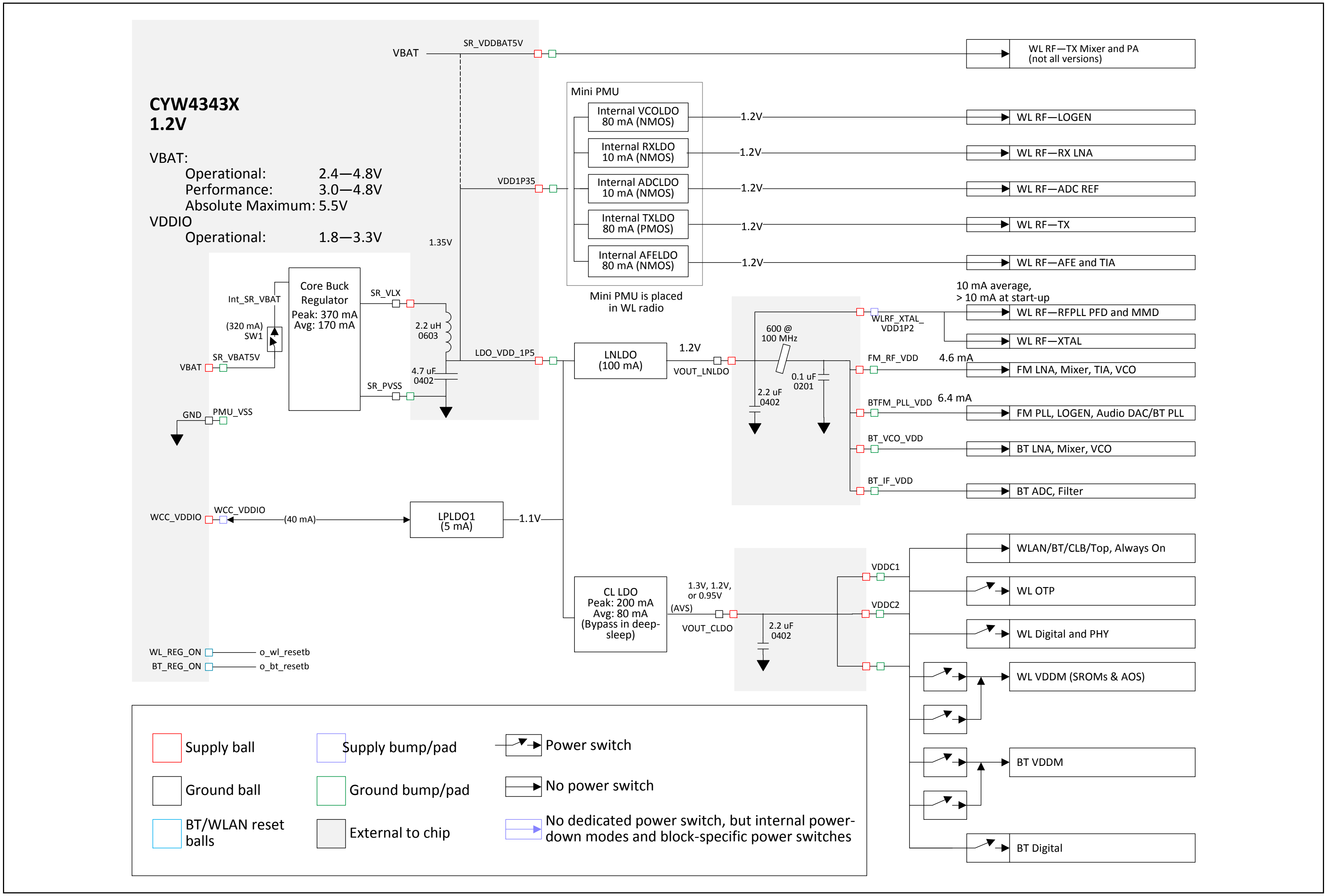


Figure 8. Typical Power Topology (2 of 2)(4343S)

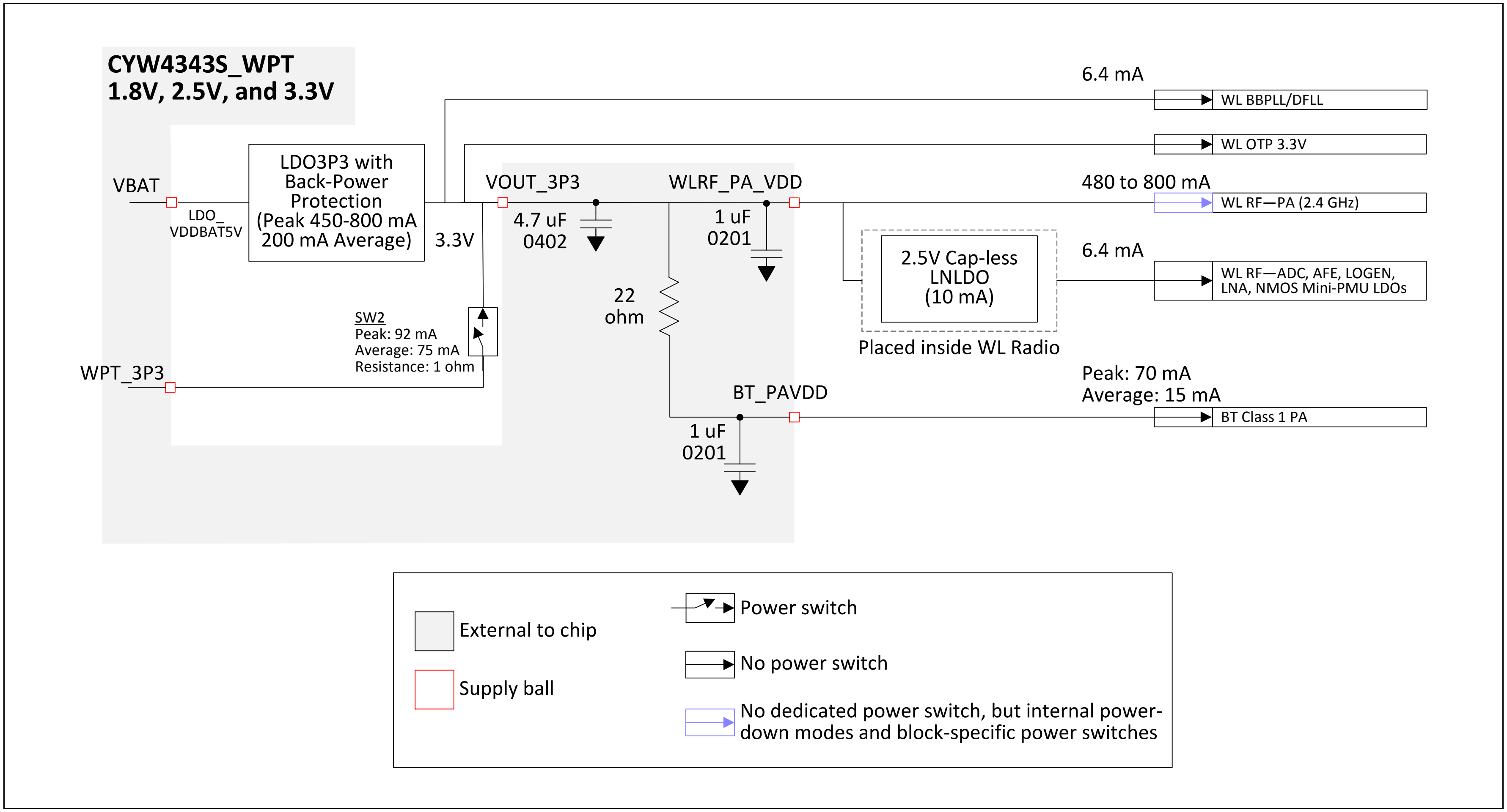


Figure 9. Typical Power Topology (2 of 2)(4343W+43CS4343W1)

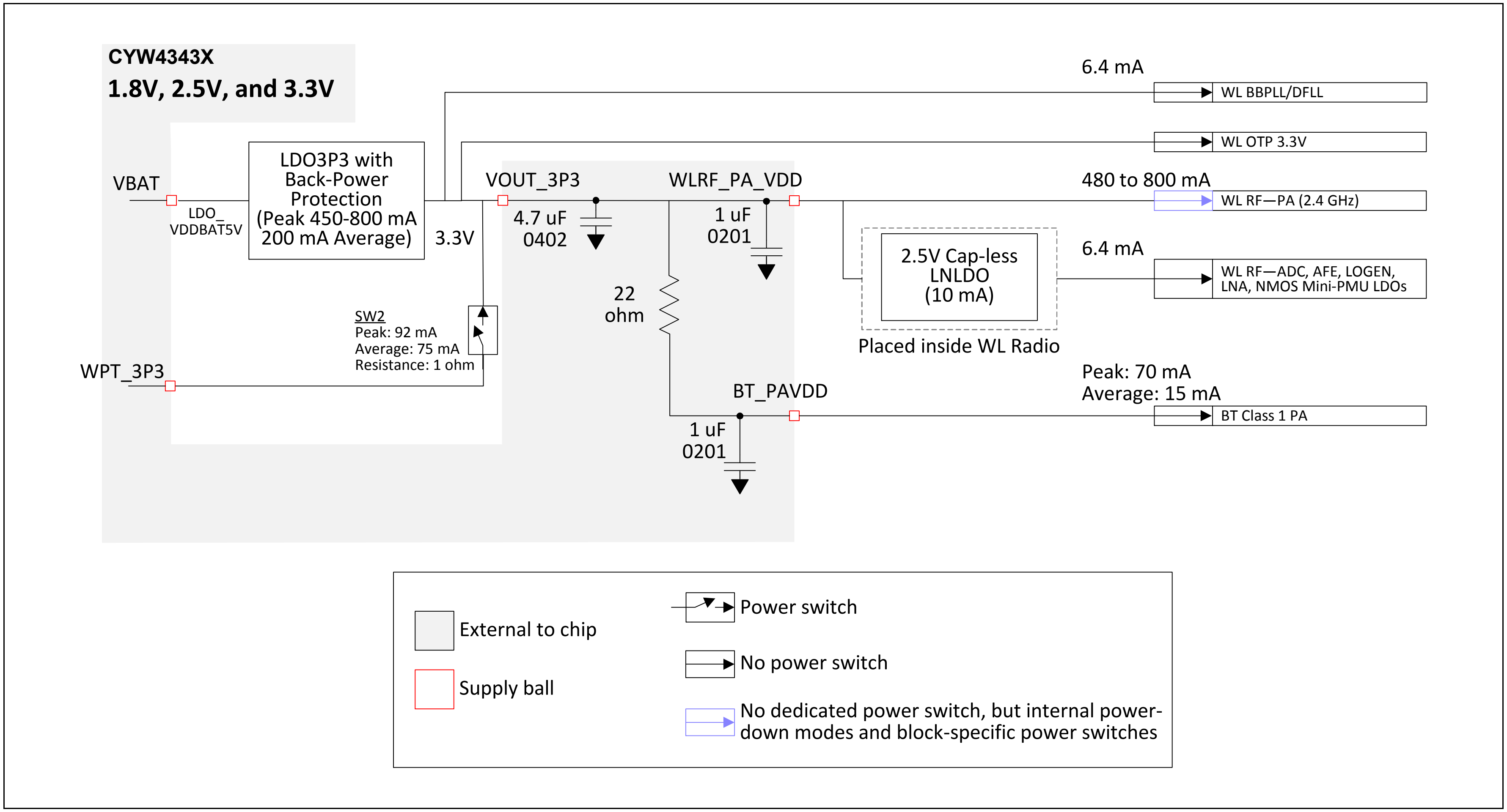
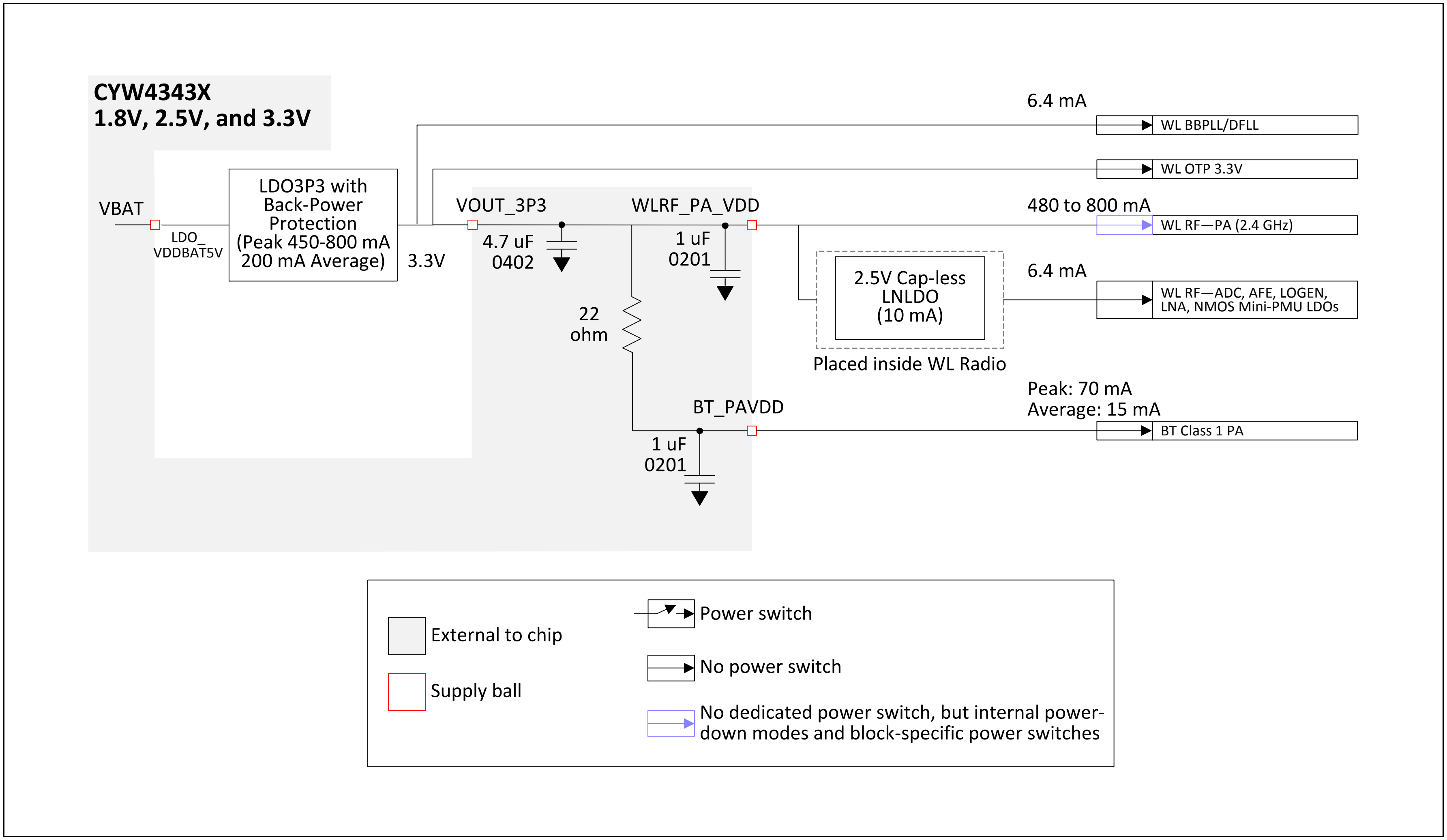


Figure 10. Typical Power Topology (2 of 2)



2.3 WLAN Power Management

The CYW4343X has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW4343X integrated RAM is a high volatile memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW4343X includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW4343X into various power management states appropriate to the operating environment and the activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at the 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW4343X WLAN power states are described as follows:

- Active mode— All WLAN blocks in the CYW4343X are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW4343X remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode—Most of the chip, including analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved to retention memory in the always-on domain before the digital core is powered off. To avoid lengthy hardware reinitialization, the logic states in the digital core are restored to their pre-deep-sleep settings when a wake-up event is triggered by an external interrupt, a host resume through the SDIO bus, or by the PMU timers.
- Power-down mode—The CYW4343X is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is used to minimize system power consumption. It enables and disables various system resources based on a computation of required resources and a table that describes the relationship between resources and the time required to enable and disable them.

Resource requests can derive from several sources: clock requests from cores, the minimum resources defined in the *ResourceMin* register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of the following four states:

- enabled
- disabled
- transition_on
- transition_off

The timer value is 0 when the resource is enabled or disabled and nonzero during state transition. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can transition immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can transition immediately from enabled to disabled. The terms *enable sequence* and *disable sequence* refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are nonzero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.

- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW4343X provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the CYW4343X is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW4343X to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the CYW4343X, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW4343X to be fully integrated in an embedded device and to take full advantage of the lowest power-savings modes.

When the CYW4343X is powered on from this state, it is the same as a normal power-up, and the device does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

The CYW4343X has two signals (see Table 2) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 22.: “Power-Up Sequence and Timing,” on page 116.

Table 2. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power-up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW4343X regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW4343X regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

2.7 Wireless Charging

The CYW4343X, when paired with a Broadcom BCM5935X wireless power transfer (WPT) front-end device, complies with the following three wireless charging standards:

- Alliance for Wireless Power (A4WP)
- Wireless Power Consortium (WPC)
- Power Matters Alliance (PMA)

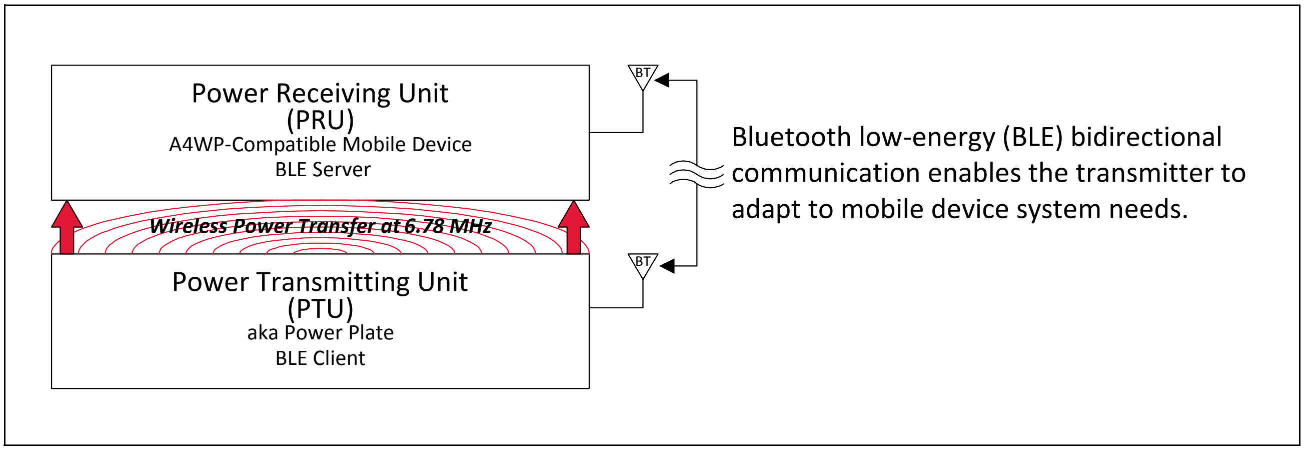
To support the WPC and PMA standards, control-plane signaling is accomplished using in-band signaling between the BCM5935X WPT front-end device (located in the power receiving entity) and the power transmitting wireless charger.

To support the A4WP standard, energy is transferred from a Power Transmitting Unit (PTU) to a Power Receiving Unit (PRU). The energy transferred charges the PRU battery. Bidirectional communication between the PTU and PRU is accomplished using Bluetooth Low Energy (BLE), where the PTU is a BLE client and the PRU is a BLE server. Using a BLE link, the PRU sends performance data to the PTU so that it can adapt its power output to meet the needs of the PRU.

The most common use for wireless charging is to charge a mobile device battery.

Figure 11 shows a simple block diagram of a system that supports the A4WP standard.

Figure 11. A4WP System Block Diagram



Note: A single PTU can be used to charge multiple devices.

Figure 12 shows an example of the magnetic coupling between a single PTU and one or more PRUs.

Figure 12. Magnetic Coupling for Wireless Charging

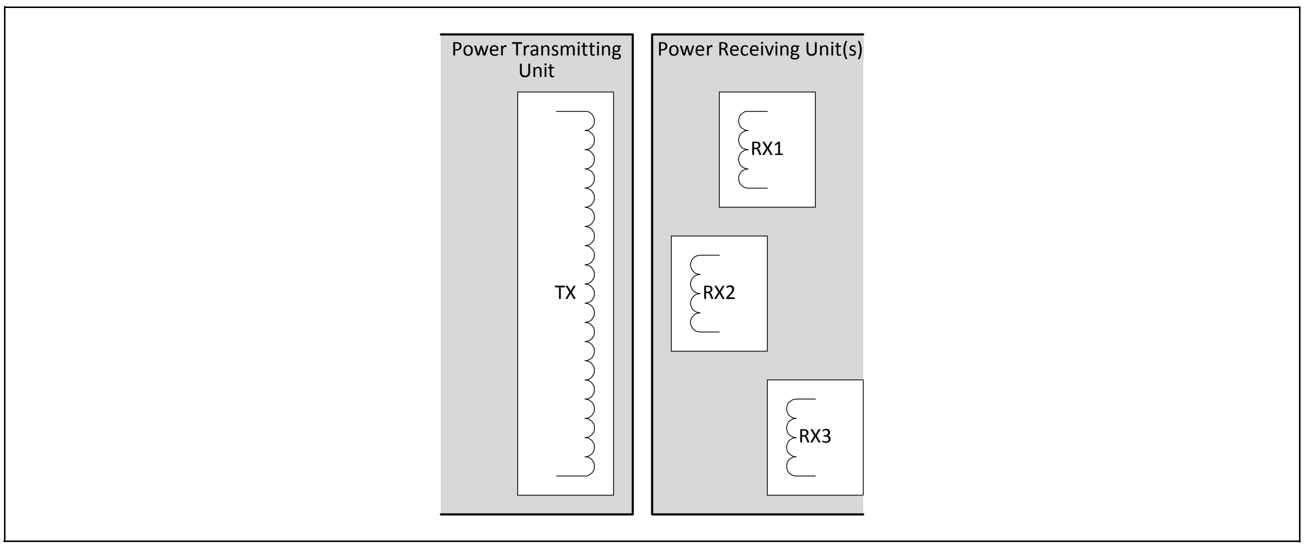


Figure 13 shows an example A4WP-compliant wireless charging implementation.

Figure 13. An Example Multimode Wireless Charging Implementation

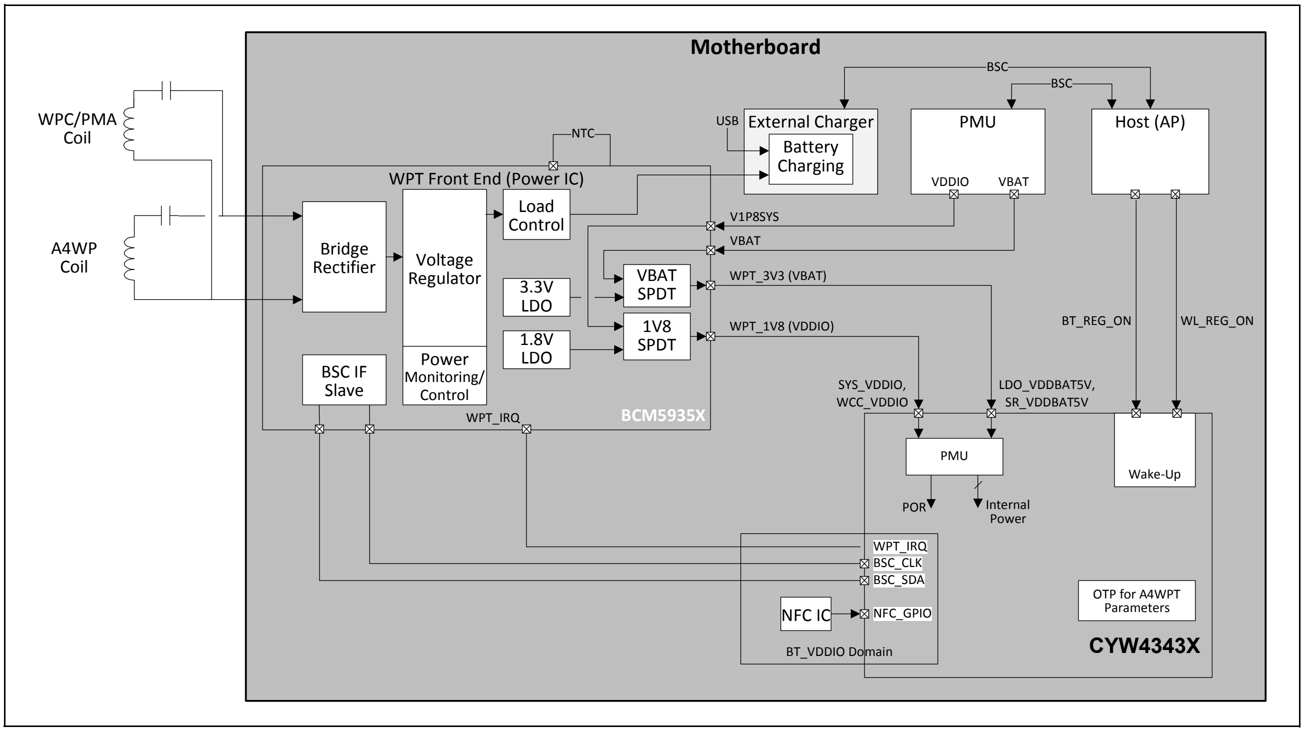
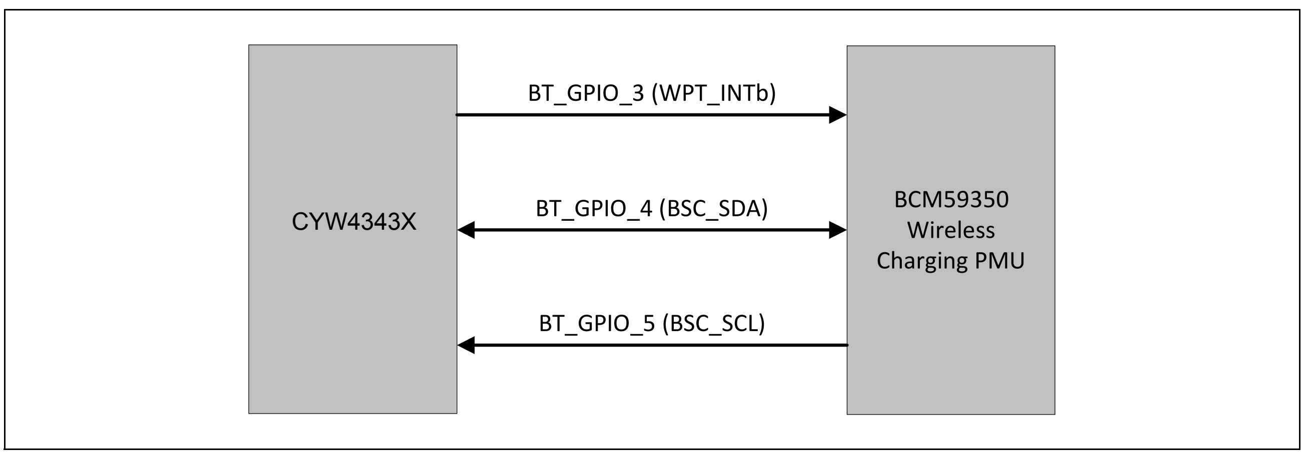


Figure 14 shows the signal interface between a CYW4343X and a CYW59350.

Figure 14. CYW4343X Interface to a BCM59350



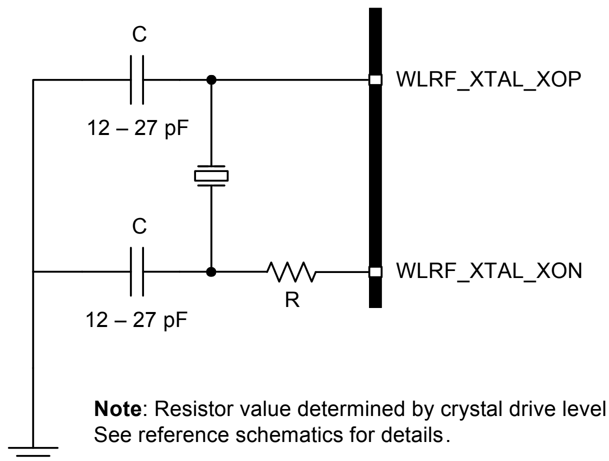
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW4343X can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 15. Consult the reference schematics for the latest configuration.

Figure 15. Recommended Oscillator Configuration



The CYW4343X uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing so that it can operate using numerous frequency references. The frequency reference can be an external source such as a TCXO or a crystal interfaced directly to the CYW4343X.

The default frequency reference setting is a 37.4 MHz crystal or TCXO. The signal requirements and characteristics for the crystal interface are shown in Table 3 on page 23.

Note: Although the fractional-N synthesizer can support many reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Broadcom for further details.

3.2 TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the phase noise requirements listed in Table 3 on page 23.

If the TCXO is dedicated to driving the CYW4343X, it should be connected to the WLRF_XTAL_XOP pin through an external capacitor with value ranges from 200 pF to 1000 pF as shown in Figure 16.

Figure 16. Recommended Circuit to Use with an External Dedicated TCXO

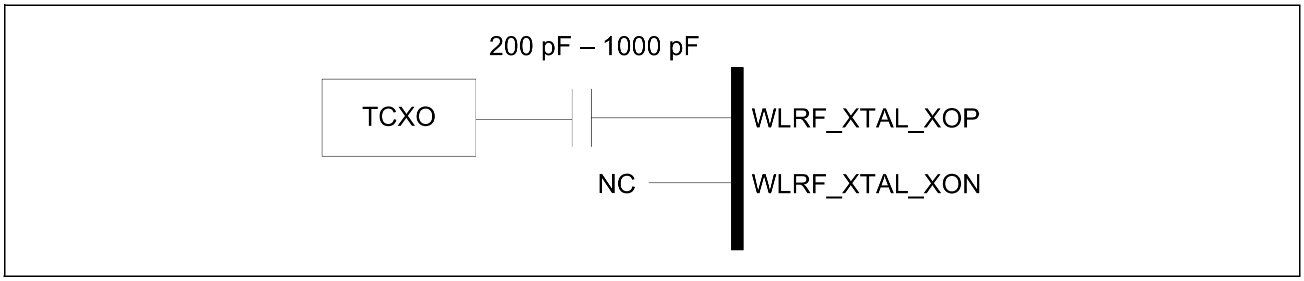


Table 3. Crystal Oscillator and External Clock Requirements and Performance

Parameter	Conditions/Notes	Crystal			External Frequency Reference			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency	–	–	37.4[a]	–	–	–	–	MHz
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	μW
Input Impedance (WLRF_XTAL_XOP)	Resistive	–	–	–	10k	100k	–	Ω
	Capacitive	–	–	–	–	–	7	pF
WLRF_XTAL_XOP input voltage	AC-coupled analog signal	–	–	–	400[b]	–	1260	mV_{p-p}
WLRF_XTAL_XOP input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WLRF_XTAL_XOP input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
Frequency tolerance Initial + over temperature	–	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[c, d, e] (IEEE 802.11 b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase Noise[c, d, e] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
Phase Noise[c, d, e] (256-QAM)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–140	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–147	dBc/Hz

a. The frequency step size is approximately 80 Hz. The CYW4343X does not auto-detect the reference clock frequency; the frequency is specified in the software and/or NVRAM file.

b. To use 256-QAM, a 800 mV minimum voltage is required.

c. For a clock reference other than 37.4 MHz, 20 × log10(f/37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.

d. Phase noise is assumed flat above 100 kHz.

e. The CYW4343X supports a 26 MHz reference clock sharing option. See the phase noise requirement in the table.

3.3 External 32.768 kHz Low-Power Oscillator

The CYW4343X uses a secondary low-frequency sleep clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 4 on page 24.

Note: The CYW4343X will auto-detect the LPO clock. If it senses a clock on the EXT_SLEEP_CLK pin, it will use that clock. If it doesn't sense a clock, it will use its own internal LPO.

- To use the internal LPO: Tie EXT_SLEEP_CLK to ground. Do not leave this pin floating.
- To use an external LPO: Connect the external 32.768 kHz clock to EXT_SLEEP_CLK.

Table 4. External 32.768 kHz Sleep-Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square wave or sine wave	–
Input impedance[a]	>100	kΩ
	<5	pF
Clock jitter	<10,000	ppm

a. When power is applied or switched off.

4. WLAN System Interfaces

4.1 SDIO v2.0

The CYW4343X WLAN section supports SDIO version 2.0. for both 1-bit (25 Mbps) and 4-bit modes (100 Mbps), as well as high speed 4-bit mode (50 MHz clocks—200 Mbps). It has the ability to map the interrupt signal on a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided.

SDIO mode is enabled using the strapping option pins. See Table 24 on page 86 for details.

Three functions are supported:

- Function 0 standard SDIO function. The maximum block size is 32 bytes.
- Function 1 backplane function to access the internal System-on-a-Chip (SoC) address space. The maximum block size is 64 bytes.
- Function 2 WLAN function for efficient WLAN packet transfer through DMA. The maximum block size is 512 bytes.

4.1.1 SDIO Pin Descriptions

Table 5. SDIO Pin Descriptions

SD 4-Bit Mode		SD 1-Bit Mode		gSPI Mode	
DATA0	Data line 0	DATA	Data line	DO	Data output
DATA1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data line 2	NC	Not used	NC	Not used
DATA3	Data line 3	NC	Not used	CS	Card select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command line	CMD	Command line	DI	Data input

Figure 17. Signal Connections to SDIO Host (SD 4-Bit Mode)

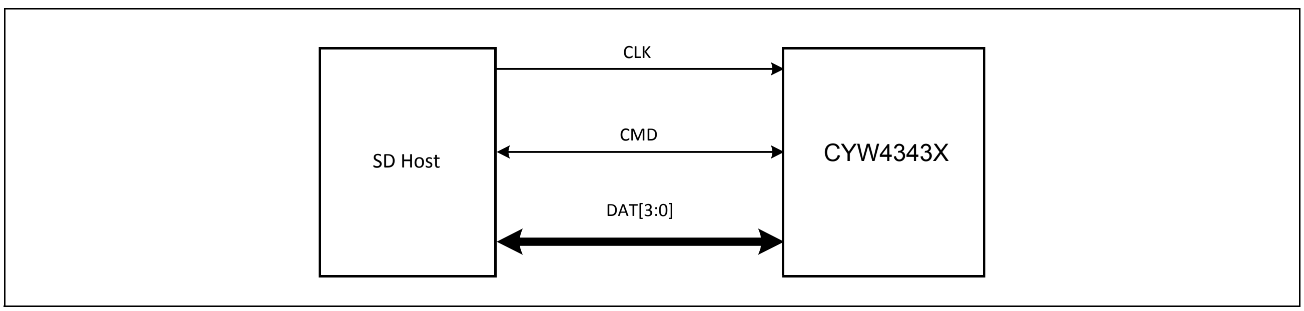


Figure 18. Signal Connections to SDIO Host (SD 1-Bit Mode)