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CYPRESS PERFORM

CYWB022XX Family

West Bridge®: Astoria™ USB and Mass Storage Peripheral Controller

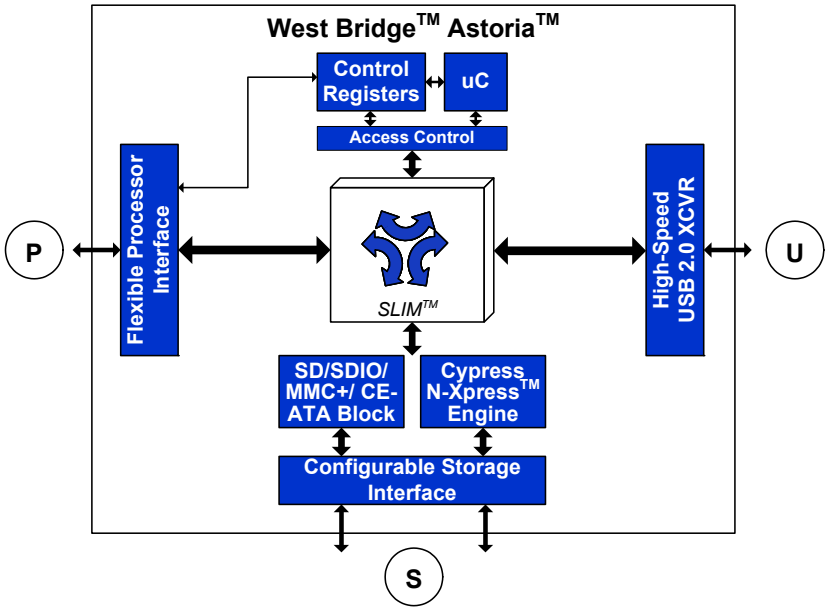
Features

- Multimedia device support
  - Up to two SD, SDIO, MMC, MMC+, and CE-ATA devices
- Supports Microsoft® Media Transfer Protocol (MTP) with optimized data throughput
- Simultaneous Link to Independent Multimedia (SLIM®) architecture, enabling simultaneous and independent data paths between the processor and USB, and between the USB and mass storage
- High-speed USB at 480 Mbps
  - USB 2.0 compliant
  - Integrated USB switch
  - Integrated USB 2.0 transceiver, smart serial interface engine
  - 16 programmable endpoints
- GPIF (General Programmable Interface)
  - Allows direct connection to most parallel interface
  - Programmable waveform descriptors and configuration registers to define waveforms
  - Supports multiple Ready (RDY) inputs and Control (CTL) outputs
- Flexible processor interface that supports:
  - Multiplexing and nonmultiplexing address and data interface
  - SRAM interface
  - Pseudo cellular random access memory (CRAM) interface (Antioch interface)
  - Pseudo NAND flash interface
  - SPI (slave mode) interface
  - Direct memory access (DMA) slave support
- FlexBoot
  - Processor can boot from the processor interface port
- Ultra low power, 1.8-V core operation
- Low power modes
- Small footprint:
  - 3.91 × 3.91 × 0.55 mm 81-ball WLCSP (SP and Lite SP)
  - 6 × 6 × 1.0 mm 100-ball VFBGA
  - 10 × 10 × 1.20 mm 121-ball FBGA
- Supports USB Boot, I^2C Boot and Processor Boot
- Selectable clock input frequencies
  - 19.2 MHz, 24 MHz, 26 MHz, and 48 MHz

Applications

- Cellular phones
- Portable media players
- Personal digital assistants
- Portable navigation devices
- Digital cameras
- POS terminals
- Portable video recorders
- Data cards and wireless dongles

Logic Block Diagram



Contents

Functional Overview

Turbo-MTP Support

Turbo-MTP is an implementation of Microsoft's MTP enabled by West Bridge. In the current generation of MTP-enabled mobile phones, all protocol packets needs to be handled by the main processor. West Bridge Turbo-MTP switches these packet types and sends only control packets to the processor, while data payloads are written directly to mass storage, thereby bringing the high performance of West Bridge to MTP. For more information refer to the application note Optimizing Performance using West Bridge® Controllers with Turbo-MTP.

SLIM Architecture

The SLIM architecture enables three different interfaces (P-port, S-port, and U-port) to connect to one another independently.

With this architecture, connecting a device using Astoria to a PC through USB does not disturb any of the functions of the device. The device can still access mass storage at the same time as the PC synchronizes with the main processor.

The SLIM architecture enables new usage models in which a PC can access a mass storage device independent of the main processor or enumerate access to both the mass storage and the main processor at the same time.

In a handset, this typically enables using the phone as a thumb drive, downloading media files to the phone while still having full functionality available on the phone, or using the same phone as a modem to connect the PC to the web.

8051 Microprocessor

The 8051 microprocessor embedded in Astoria does basic transaction management for all the transactions between P-Port, S-Port, and U-Port. The 8051 does not reside in the data path; it manages the path. The data path is optimized for performance. The 8051 executes firmware that supports SD, SDIO, MMC+, and CE-ATA devices at the S-Port.

Configuration and Status Registers

The West Bridge Astoria device includes configuration and status registers that are accessible as memory mapped registers through the processor interface. The configuration registers allow the system to specify certain Astoria behaviors. For example, it is able to mask certain status registers from raising an interrupt. The status registers convey various status such as the addresses of buffers for read operations.

Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface is configured to support different interface standards. This interface supports multiplexing and nonmultiplexing address or data bus in both synchronous and asynchronous pseudo CRAM-mapped, and nonmultiplexing address or data asynchronous SRAM-mapped memory accesses. The interface also can be configured to a pseudo NAND interface to support the processor's NAND interface. In addition, this interface can be configured to support SPI slave. Asynchronous accesses can reach a bandwidth of up to 66.7 MBps. Synchronous accesses can be performed at 33 MHz across 16 bits for up to 66.7 MBps bandwidth. The P-Port of the WLCSP package only supports PNAND and SPI interface.

The memory address is decoded to access any of the multiple endpoint buffers inside Astoria. These endpoints serve as buffers for data between each pair of ports, for example, between the processor port and the USB port. The processor writes and reads into these buffers through the memory interface.

Access to these buffers is controlled by either using a DMA protocol or using an interrupt to the main processor. These two modes are configurable by the external processor. The 81-ball WLCSP package only supports interrupt.

As a DMA slave, Astoria generates a DMA request signal to signify to the main processor that a specific buffer is ready to be read from or written to. The external processor monitors this signal and polls Astoria for the specific buffers ready for read or write. It then performs the appropriate read or write operations on the buffer through the processor interface. This way, the external processor only deals with the buffers to access a multitude of storage devices connected to Astoria.

In the interrupt mode, Astoria communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Astoria for the specific buffers ready for read or write and it performs the appropriate read or write operations through the processor interface.

FlexBoot

FlexBoot is an optional feature that Astoria emulates a NAND Flash device. In this optional feature, the P-Port is configured as pseudo NAND interface. The processor can download its boot image through the P-Port.

When P-Port is configured to pseudo NAND interface, it supports two operation modes:

- Logic NAND Access (LNA) mode
- Non-Logic NAND Access (non-LNA) mode

LNA refers to the mode of operation where Astoria emulates a NAND flash device. This mode is designed for systems that require booting of the system processor from a NAND Flash device. In this type of application, the system processor can communicate to Astoria using common NAND commands to boot from a NAND Flash connected to Astoria's S-port. In this mode of operation, Astoria mimics a real NAND device and allows the system processor to use its internal boot-ROM to boot from Astoria, as it boots from a NAND Flash.

In the non-LNA mode of operation, the system processor interfaces with Astoria using standard NAND interface, but does not use standard NAND commands. In this mode, Astoria responds to a subset of NAND commands. The system processor uses a set of APIs provided by Cypress to communicate through its NAND controller to Astoria. For details, refer to the application note "Interfacing To West Bridge™ Astoria's™ Pseudo-NAND Processor Port".

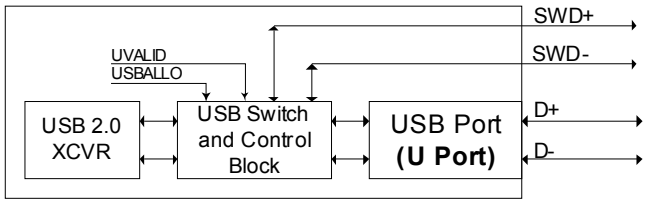
USB Interface (U-Port)

In accordance with the USB 2.0 specification, Astoria can operate in both full speed and high speed USB modes. The USB interface consists of the USB transceiver and can be accessed by both the P-Port and the S-Port.

The Astoria USB interface supports programmable CONTROL/BULK/INTERRUPT/ISOCHRONOUS endpoints.

Astoria also has an integrated USB switch (see Figure 1) that allows interfacing to an external full speed USB PHY.

Figure 1. U-Port With Switch and Control Block



Mass Storage Support (S-Port)

The S-Port is configurable in five different interface modes:

- Simultaneously supporting an SD/SDIO/MMC+/CE-ATA port and an GPIF
- Supporting two SD/SDIO/MMC+/CE-ATA ports
- Supporting SD/SDIO/MMC+/CE-ATA port and GPIO
- Supporting GPIF and GPIO
- Supporting GPIO

These configurations are controlled by the 8051 firmware.

S-Port Configuration Modes

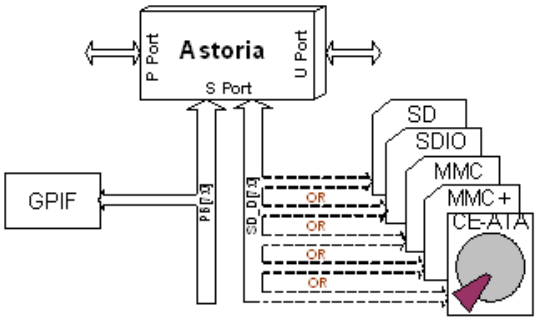
The S Port is configurable in six different interface modes:

- GPIF and SD/SDIO/MMC/CE-ATA interface mode
- Dual SD/SDIO/MMC/CE-ATA interface mode
- SD/SDIO/MMC/CE-ATA and GPIO interlace mode
- GPIF and GPIO interface mode
- GPIO interface mode

GPIF and SD/SDIO/MMC/CE-ATA Interface Mode

This mode configures the S-Port into GPIF and SD/SDIO/MMC/MMC+/CE-ATA ports as shown in Figure 2. The SD/SDIO/MMC/MMC+/CE-ATA port supports either SD, SDIO, MMC, MMC+, or CE-ATA device.

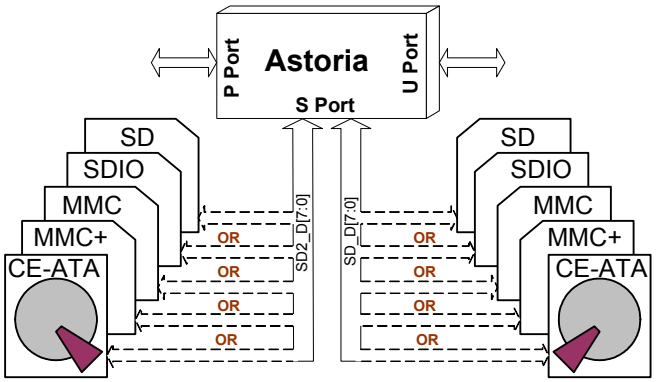
Figure 2. GPIF and SD/SDIO/MMC/CE-ATA Interface Mode



Dual SD/SDIO/MMC/CE-ATA Interface Mode

The dual SD/SDIO/MMC/MMC+/CE-ATA interface mode configures the S-Port for up to two SD/SDIO/MMC/MMC+/CE-ATA port as shown in Figure 3. Each SD/SDIO/MMC/MMC+/CE-ATA port is independent and supports different SD, SDIO, MMC, MMC+, or CE-ATA devices.

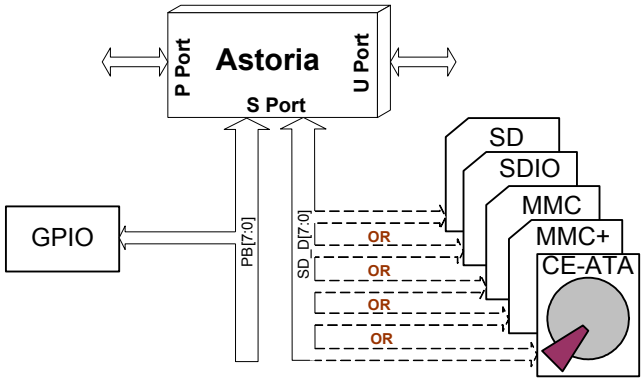
Figure 3. Dual SD/SDIO/MMC/CE-ATA Interface Mode



SD/SDIO/MMC/CE-ATA and GPIO Interface

The SD/SDIO/MMC/MMC+/CE-ATA and GPIO interface mode configures the S-Port to support SD/SDIO/MMC/MMC+/CE-ATA device and GPIOs as shown in Figure 4. Each GPIO is configured as either input or output independently. The processor accesses those GPIO through the P-Port driver's API.

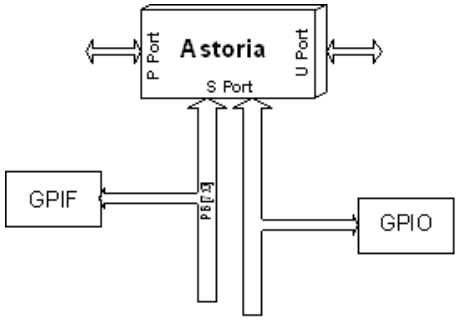
Figure 4. SD/SDIO/MMC/CE-ATA and GPIO Interface Mode



GPIF and GPIO Interface

The GPIF and GPIO interface mode configure the S-Port to support GPIF and GPIO as shown in Figure 5. Each GPIO is configured as either input or output independently. The processor accesses those GPIO through the P-Port driver's API.

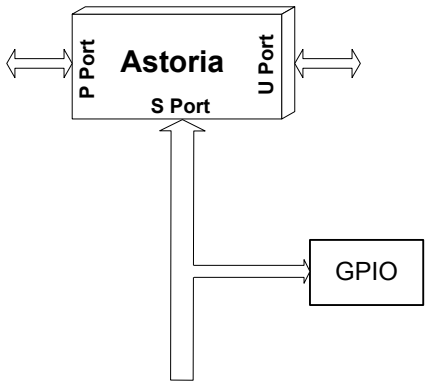
Figure 5. GPIF and GPIO Interface Mode



GPIO Interface Mode

The GPIO interface mode configures the S-Port to all GPIO as shown in Figure 6. Each GPIO is configured as either input or output independently. The processor accesses those GPIO through the P-Port driver's API.

Figure 6. GPIO Interface Mode



SD/SDIO/MMC+/CE-ATA Port (S-Port)

When Astoria is configured with firmware to support SD, SDIO, MMC+, and CE-ATA, this interface supports:

- The Multimedia Card System Specification, MMCA Technical Committee, Version 4.1
- SD Memory Card Specification – Part 1, Physical Layer Specification, SD Group, Version 1.10, October 15, 2004
- SD Memory Card Specification – Part 1, Physical Layer Specification, SD Group, Version 2.0, May 9, 2006
- SD Specifications – Part E1 SDIO Specification, Version 1.10, August 18, 2004
- CE-ATA Specification – CE-ATA Digital Protocol, CE-ATA Committee, Version 1.1, September, 2005

West Bridge Astoria provides support for 1-bit and 4-bit SD; SDIO cards; 1-bit, 4-bit, and 8-bit MMC; MMC+ cards; and CE-ATA drive. For the SD, SDIO, MMC/MMC Plus, and CE-ATA, this block supports one card for one physical bus interface.

Astoria supports SD commands including the multisector program command that are handled by the API.

GPIO Port (S-Port)

The GPIO in S-Port is configurable as either input or output direction independently. The processor accesses the GPIO through the P-Port driver's API.

Clocking

Astoria allows connection of a crystal between the XTALIN and XTALOUT pins or an external clock at the XTALIN pin. The 81-ball WLCSP package only supports the external clock. The power supply level at the crystal supply XVDDQ determines whether a crystal or a clock is provided. If XVDDQ is detected to be 1.8 V, Astoria assumes that a clock input is provided. For a crystal to be connected, XVDDQ must be 3.3 V.

Note Clock inputs at 3.3 V level are not supported.

Astoria's 100-ball VFBGA package supports external crystal and clock inputs at 19.2, 24, and 26 MHz frequencies. At 48 MHz, only clock inputs are supported. The 81-ball SPWLCSP only supports 19.2 and 26 MHz external clock input. The 81-ball Lite SP WLCSP only supports 26 MHz external clock or crystal input. The crystal or clock frequency selection is shown in Table 1 on page 6, Table 2 on page 6, and Table 3 on page 6.

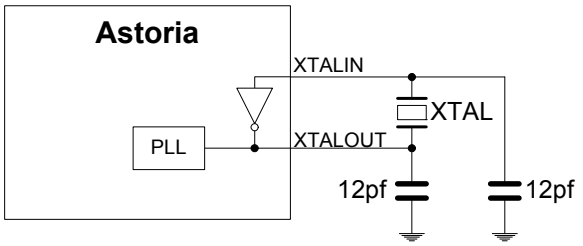
The XTALIN frequency is independent of the clock and data rate of the 8051 microprocessor or any of the device interfaces (including P-Port and S-Port). The internal PLL applies the proper clock multiply option depending on the input frequency.

For applications that use an external clock source to drive XTALIN, the XTALOUT pin must be left floating. The external clock source must also stop high or low and not toggle, to achieve the lowest possible current consumption. The requirements for an external clock source are shown in Table 4 on page 6.

Astoria has an on-chip oscillator circuit that uses an external 19.2, 24, and 26 MHz (±150 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 1 mW drive level
- 12 pF (5% tolerance) load capacitors
- 150 ppm

Figure 7. Crystal Configuration



* 12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four layer FR4 PCA

Table 1. 100-ball FVBGA Clock Selection

XTALSLC[1]	XTALSLC[0]	Freq	Crystal/Clock
0	0	19.2 MHz	Crystal/Clock
0	1	24 MHz	Crystal/Clock
1	0	48 MHz	Clock
1	1	26 MHz	Crystal/Clock

Table 2. 81-ball SP WLCSP Clock Selection

XTALSLC	Freq	Crystal/Clock
0	19.2 MHz	Clock
1	26 MHz	Clock

Table 3. 81-ball Lite SP WLCSP Clock Supports 26 MHz

XTALSLC	Freq	Crystal/Clock
NA	26 MHz	Clock or Crystal

Table 4. External Clock Requirements

Parameter	Description	Specification		Unit
		Min	Max	
Vn (AVDDQ)	Supply voltage noise at frequencies < 50 MHz	–	20	mV p-p
PN_100	Input phase noise at 100 Hz	–	–75	dBc/Hz
PN_1k	Input phase noise at 1 kHz offset	–	–104	dBc/Hz
PN_10k	Input phase noise at 10 kHz offset	–	–120	dBc/Hz
PN_100k	Input phase noise at 100 kHz offset	–	–128	dBc/Hz
PN_1M	Input phase noise at 1 MHz offset	–	–130	dBc/Hz
	Duty cycle	30	70	%
	Maximum frequency deviation	–	150	ppm
	Overshoot	–	3	%
	Undershoot	–	–3	%

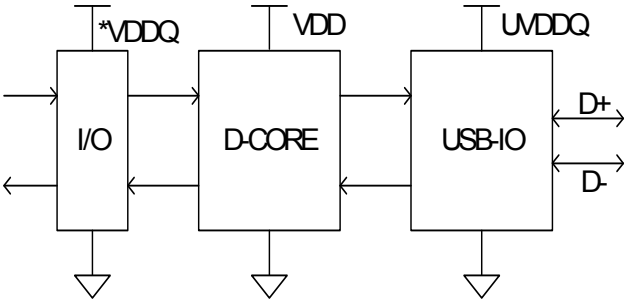
Power Domains

Astoria has multiple power domains that serve different purposes within the chip.

- VDDQ refers to a group of four independent supply domains for the digital I/Os. The nominal voltage level on these supplies are 1.8 V, 2.5 V, or 3.3 V. The three separate I/O power domains are:
  - PVDDQ – P-Port Processor interface I/O
  - SNVDDQ – S-Port GPIF interface I/O
  - SSVDDQ – S-Port SD interface I/O
  - GVDDQ – Other miscellaneous I/O
- UVDDQ is the 3.3-V nominal supply for the USB I/O and some analog circuits. It also supplies power to the USB transceiver
- VDD33 supply is required for the power sequence control circuits. For more details, see Pin Assignments on page 9.
- VDD is the supply voltage for the logic core. The nominal supply voltage level is 1.8 V. This supplies the core logic circuits. The same supply must also be used for AVDDQ
- AVDDQ is the 1.8 V supply for PLL and USB serializer analog components. The same supply must also be used for VDD. The maximum permitted noise on AVDDQ is 20 mV p-p
- XVDDQ is the clock I/O supply; 3.3 V for XTAL or 1.8 V for an external clock

Noise guideline for all supplies except AVDDQ is a maximum of 100 mV p-p. All I/O supplies of Astoria must be ON when a system is active even if Astoria is not in use. The core VDD can also be deactivated at any time to preserve power if there is a minimum impedance of 1 kΩ between the VDD pin and ground. All I/Os tristate when the core is disabled.

Figure 8. Astoria Power Supply Domains



Power Supply Sequence

The power supplies are independently sequenced without damaging the part. All power supplies must be up and stable before the device operates. If the supplies are not stable, the remaining domains are in low power (standby) state.

Power Modes

In addition to the normal operating mode, Astoria contains several low power states when normal operation is not required.

Normal Mode

Normal mode is the mode in which Astoria is fully functional. In this mode, data transfer functions described in this document are performed.

Suspend Mode

This mode is entered internally by 8051 (the external processor only initiates entry into this mode through Mailbox commands). This mode is exited by the D+ bus going low, GPIO[0] going to a pre-determined state or by asserting CE# LOW.

In Astoria's suspend mode:

- The clocks are shut off
- All I/Os maintain their previous state
- Core power supply must be retained
- The states of the configuration registers, endpoint buffers, and the program RAM are maintained. All transactions must be complete before Astoria enters suspend mode (state of outstanding transactions are not preserved)
- The firmware resumes its operation from where it was suspended because the program counter is not reset
- Only inputs that are sensed are RESET#, GPIO[0]/SD_CD, GPIO[1]/SD2_CD, SD_D3, SD2_D3, D+, and CE#. The last three are wake up sources (each can be individually enabled or disabled)
- Hard Reset can be performed by asserting the RESET# input, and Astoria is initialized

Standby Mode

Standby mode is a low-power state. This is the lowest power mode of Astoria while still maintaining external supply levels. This mode is entered through the deassertion of the WAKEUP input pin or through internal register settings. To leave this mode, assert the WAKEUP, CE#, and RESET#; change state of GPIO[0]/SD_CD, GPIO[1]/SD2_CD, SD_D3, and SD2_D3.

In this mode all configuration register settings and program RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed in values. Therefore, the external processor must ensure that the required data is read before placing Astoria in the standby mode.

In the standby mode:

- The program counter is reset on waking up from standby mode
- All outputs are tristated and I/O is placed in input only configuration. Values of I/Os in standby mode are listed in the pin assignments table
- Core power supply must be retained
- Hard Reset can be performed by asserting the RESET# input, and Astoria is initialized
- PLL is disabled
- USB switches the SWD+/SWD– to D+/D–

Core Power Down Mode

The core power supply V_{DD} is powered down in this state. Because AVDDQ is tied to the same supply as V_{DD}, it is also powered down. The endpoint buffers, configuration registers, and program RAM do not maintain state. All VDDQ power supplies (except AVDDQ) must be ON and not power down in this mode. VDD33 must also remain ON. It has an option that the UVDDQ can be powered down or stay ON while V_{DD} is powered down when SWD+/SWD– are not connected. The UVDDQ cannot be powered down when SWD+/SWD– is connected, or V_{DD} is active. When UVDDQ is powered down, D+/D– cannot be driven by an external device.

In the WLCSP package, AVDDQ is internally tied to XVDDQ. Due to this, the clock input at XTALIN must be brought to a steady low level prior to entry into Core Power Down Mode. In the WLCSP package, VDD33 is tied to UVDDQ internally. UVDDQ must be ON during the core power down mode

The core power down mode has two power down options:

- Core only power down – VDD power down
- Core and USB power down – VDD and UVDDQ are both powered down. In this option, SWD+/SWD– are not connected and cannot be driven by an external device

In these power down options, the endpoint buffers, configuration registers, or the program RAM do not maintain state. It is necessary to reload the firmware on exiting from this mode. All VDDQ power supplies must be ON and not powered down in this mode.

In the 82-ball WLCSP package, in the core power down mode, the USB switches the SWD+/SWD– to D+/D–.

Packages and Interface Options

Astoria provides one 100-ball VFBGA, one 100-ball BGA, one 121-ball FBGA and two types of 81-ball WLCSP packages. The two WLCSP packages are SP WLCSP and Lite SP WLCSP. These two packages have different interface options as listed in Table 5. The 100-ball VFBGA/BGA package pin list is listed in Table 6 on page 9, the 81-ball SP CSP package is listed in Table 10 on page 21, and the 81-ball Lite SP CSP package in Table 11 on page 24.

Table 5. Interface Options for 100-ball VFBGA, 81-ball SP, and 81-ball Lite SP

Package	P-Port						S-Port				Clock		
	PCRAM	SRAM	ADM	PNAND	I^2C	SPI	SD1	SD2	GPIF	GPIO	Ext CLK	Crystal	Freq. (MHz)
100-ball BGA / VFBGA	√	√	√	√	√	√	√	√	√	√	√	√	19.2, 24, 26, 48
121-ball FBGA	√	√	√	√	√	√	√	√	√	√	√	√	19.2, 24, 26, 48
81-ball SP WLCSP				√	√	√	√	√	√	√	√		19.2, 26
81-ball Lite SP WLCSP		√	√	√	√		√			√	√	√	26

Pin Assignments

Table 6. Astoria 100-ball VFBGA Package Pin Assignments

	Pin Name											Pin Description	Power Domain
	Ball #	PCRAM Non-Multiplexing	I/O	Address / Data bus Multiplexing (ADM)	I/O	SRAM	I/O	PNAND	I/O	SPI	I/O		
P-Port	J2	CLK (pull low in Asyn mode)	I	CLK (pull low in Async mode)	I	Ext pull low	I	Ext pull low	I	SCK	I	Clock	PVDDQ VGND
	G1	CE#	I	CE#	I	CE#	I	CE#	I	SS#	I	CE# or SPI Slave Select	
	H3	A7	I	Ext pull up	I	A7	I	A7 ≥ 1:SBD A7 ≥ 0:LBD	I	Ext pull up	I	Addr. Bus 7	
	H2	A6	I	SDA	I	A6	I	SDA	I/O	SDA	I/O	A6 or I^2C data	
	H1	A5	I	SCL	I	A5	I	SCL	I/O	SCL	I/O	A5 or I^2C clock	
	J3	A4	I	Ext pull up	I	A4	I	WP#	I	Ext pull up	I	A4 or PNAND WP	
	J1	A3	I	A3 = 0 (Ext pull low)	I	A3	I	A3 = 0 (Ext pull low)	I	A3 = 1 (Ext pull up)	I	A3	
	K3	A2	I	A2 = 1 (Ext pull up)	I	A2	I	A2 = 0 (Ext pull low)	I	A2 = 0 (Ext pull low)	I	A2	
	K2	A1	I	Ext pull up	I	A1	I	RB#	O	Ext pull up	I	A1 or PNAND R/B#	
	K1	A0	I	Ext pull up	I	A0	I	CLE	I	Ext pull up	I	A0 or PNAND CLE	
	G2	DQ[15]	I/O	AD[15]	I/O	DQ[15]	I/O	I/O[15]	I/O	Ext pull up	I	D15, AD15, or I/O15	
	G3	DQ[14]	I/O	AD[14]	I/O	DQ[14]	I/O	I/O[14]	I/O	Ext pull up	I	D14, AD14, or I/O14	
	F1	DQ[13]	I/O	AD[13]	I/O	DQ[13]	I/O	I/O[13]	I/O	Ext pull up	I	D13, AD13, or I/O13	
	F2	DQ[12]	I/O	AD[12]	I/O	DQ[12]	I/O	I/O[12]	I/O	Ext pull up	I	D12, AD12, or I/O12	
	F3	DQ[11]	I/O	AD[11]	I/O	DQ[11]	I/O	I/O[11]	I/O	Ext pull up	I	D11, AD11, or I/O11	
	E1	DQ[10]	I/O	AD[10]	I/O	DQ[10]	I/O	I/O[10]	I/O	Ext pull up	I	D10, AD10, or I/O10	
	E2	DQ[9]	I/O	AD[9]	I/O	DQ[9]	I/O	I/O[9]	I/O	Ext pull up	I	D9, AD9, or I/O9	
	E3	DQ[8]	I/O	AD[8]	I/O	DQ[8]	I/O	I/O[8]	I/O	Ext pull up	I	D8, AD8, or I/O8	
	D1	DQ[7]	I/O	AD[7]	I/O	DQ[7]	I/O	I/O[7]	I/O	Ext pull up	I	D7, AD7, or I/O7	
	D2	DQ[6]	I/O	AD[6]	I/O	DQ[6]	I/O	I/O[6]	I/O	Ext pull up	I	D6, AD6, or I/O6	
	D3	DQ[5]	I/O	AD[5]	I/O	DQ[5]	I/O	I/O[5]	I/O	Ext pull up	I	D5, AD5, or I/O5	
	C1	DQ[4]	I/O	AD[4]	I/O	DQ[4]	I/O	I/O[4]	I/O	Ext pull up	I	D4, AD4, or I/O4	
	C2	DQ[3]	I/O	AD[3]	I/O	DQ[3]	I/O	I/O[3]	I/O	Ext pull up	I	D3, AD3, or I/O3	
	C3	DQ[2]	I/O	AD[2]	I/O	DQ[2]	I/O	I/O[2]	I/O	Ext pull up	I	D2, AD2, or I/O2	
	B1	DQ[1]	I/O	AD[1]	I/O	DQ[1]	I/O	I/O[1]	I/O	SDO	O	SPI SDO, AD1or D1	
	B2	DQ[0]	I/O	AD[0]	I/O	DQ[0]	I/O	I/O[0]	I/O	SDI	I	SPI SDI, AD0, or D0	
	A1	ADV#	I	ADV#	I		I	ALE	I	Ext pull up	I	Address Valid	
	B3	OE#	I	OE#	I	OE#	I	RE#	I	Ext pull up	I	Output Enable	
	A2	WE#	I	WE#	I	WE#	I	WE#	I	Ext pull up	I	WE#	
DRQ & Int	A3	INT#	O	INT#	O	INT#	O	INT#	O	SINT#	O	INT Request	GVDDQ VGND
	A4	DRQ#	O	DRQ#	O	DRQ#	O	DRQ#	O	N/C	O	DMA Request	
	B4	DACK#	I	DACK#	I	DACK#	I	DACK#	I	Ext pull up	I	DMA Acknowledgement	
U-Port	A5	D+									I/O/Z	USB D+	UVDDQ UVSSQ
	A6	D–									I/O/Z	USB D–	
	A7	SWD+									I/O/Z	USB Switch DP	
	C6	SWD–									I/O/Z	USB Switch DM	

Table 6. Astoria 100-ball VFBGA Package Pin Assignments (continued)

	Pin Name											Pin Description	Power Domain
	Ball #	Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GPIF Configuration	I/O	GPIF & GPIO Configuration	I/O		
S-Port	G9	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GPIF_DATA[15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GPIF Data	SSVDDQ VGND
	G10	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GPIF_DATA[14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F9	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GPIF_DATA[13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F10	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GPIF_DATA[12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E9	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GPIF_DATA[11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E10	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GPIF_DATA[10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D9	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GPIF_DATA[9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D10	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GPIF_DATA[8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F8	SD_CLK	O	SD_CLK	O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	SD Clock or GPIO	
	G8	SD_CMD	I/O	SD_CMD	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	SD CMD or GPIO	
	H8	SD_POW		SD_POW		PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	SD Power or GPIO	
	H10	SD_WP	I	SD_WP	I	N/C		N/C		PC[5] (GPIO)		SD Write Protect	
	K7	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GPIF_DATA[7]	I/O	GPIF_DATA[7]	I/O	SD2 Data or GPIO or GPIF Data	SNVDDQ VGND
	K8	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GPIF_DATA[6]	I/O	GPIF_DATA[6]	I/O	SD2 Data or GPIO or GPIF Data	
	J8	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GPIF_DATA[5]	I/O	GPIF_DATA[5]	I/O	SD2 Data or GPIO or GPIF Data	
	K9	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GPIF_DATA[4]	I/O	GPIF_DATA[4]	I/O	SD2 Data or GPIO or GPIF Data	
	J9	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GPIF_DATA[3]	I/O	GPIF_DATA[3]	I/O	SD2 Data or GPIO or GPIF Data	
	H9	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GPIF_DATA[2]	I/O	GPIF_DATA[2]	I/O	SD2 Data or GPIO or GPIF Data	
	K10	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GPIF_DATA[1]	I/O	GPIF_DATA[1]	I/O	SD2 Data or GPIO or GPIF Data	
	J10	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GPIF_DATA[0]	I/O	GPIF_DATA[0]	I/O	SD2 Data or GPIO or GPIF Data	
	K6	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	SD2 Clock or GPIO	
	J6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	SD2 CMD or GPIO	
	J5	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	SD2 Power or GPIO	
	K4	N/C	O	N/C	O	N/C	O	GPIF_CTL[1]	O	GPIF_CTL[1]	O	GPIF Control Signal	
	H6	N/C	O	N/C	O	N/C	O	GPIF_CTL[0]	O	GPIF_CTL[0]	O	GPIF Control Signal	
	J7	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	GPIO	
	J4	N/C	I	N/C	I	N/C	I	GPIF_RDY[0]	O	GPIF_RDY[0]	O	GPIF Ready Signal	
	K5	SD2_WP	O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	SD Write Protect or GPIO	
Other	B10	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT / GPIF_RDY[1]	O	Reset Out	GVDDQ VGND
	C9	SD2_CD	I/O I	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD	
	D8	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD	
	C10	RESET#									I	RESET	
	C7	WAKEUP									I	Wake Up Signal	

Table 6. Astoria 100-ball VFBGA Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	C5	XTALSLC[1]	I	Clock Select 1	GVDDQ VGND
	C4	XTALSLC[0]		Clock Select 0	
	E8	TEST[2]	I	Test Cfg 2	
	C8	TEST[1]		Test Cfg 1	
	D7	TEST[0]		Test Cfg 0	
Clock	A8	XTALIN	I	Crystal/Clock IN	XVDDQ VGND
	B8	XTALOUT	O	Crystal Out	
Power	D4, H4	PVDDQ	Power	Processor I/F VDD	
	H5	SNVDDQ	Power	GPIF VDD	
	B5	UVDDQ	Power	USB VDD	
	H7	SSVDDQ	Power	SDIO VDD	
	D6	GVDDQ	Power	Misc I/O VDD	
	B9	AVDDQ	Power	Analog VDD	
	B7	XVDDQ	Power	Crystal VDD	
	D5, G4, G5, G6, G7, F7	VDD	Power	Core VDD	
	A10	VDD33	Power	Independent 3.3 V	
	B6	UVSSQ	Power	USB GND	
	A9	AVSSQ	Power	Analog GND	
	E4, E5, E6, E7, F4, F5, F6	VGND	Power	Core GND	

Table 7. Astoria CYWB0224ABS 121-ball FBGA Package Pin Assignments

	Pin Name												Pin Description	Power Domain
	Ball #	PCRAM Non Multiplexing	I/O	Addr/Data bus Multiplexing (ADM)	I/O	SRAM	I/O	PNAND	I/O	SPI	I/O		
P-Port	J2	CLK (pull-low in Asyn mode)	I	CLK (pull-low in Async mode)	I	Ext pull-low	I	Ext pull-low	I	SCK	I	Clock	PVDDQ VGND
	G1	CE#	I	CE#	I	CE#	I	CE#	I	SS#	I	CE# or SPI Slave Select	
	H3	A7	I	Ext pull-up	I	A7	I	A7 ≥ 1:SBD A7 ≥ 0: LBD	I	Ext pull-up	I	Addr. Bus 7	
	H2	A6	I	SDA	I	A6	I	SDA	I/O	SDA	I/O	A6 or I^2C data	
	H1	A5	I	SCL	I	A5	I	SCL	I/O	SCL	I/O	A5 or I^2C clock	
	J3	A4	I	Ext pull-up	I	A4	I	WP#	I	Ext pull-up	I	A4 or PNAND WP	
	J1	A3	I	A3 = 0 (Ext pull-low)	I	A3	I	A3 = 0 (Ext pull-low)	I	A3 = 1 (Ext pull-up)	I	A3	
	K3	A2	I	A2 = 1 (Ext pull-up)	I	A2	I	A2 = 0 (Ext pull-low)	I	A2 = 0 (Ext pull-low)	I	A2	
	K2	A1	I	Ext pull-up	I	A1	I	RB#	O	Ext pull-up	I	A1 or PNAND R/B#	
	K1	A0	I	Ext pull-up	I	A0	I	CLE	I	Ext pull-up	I	A0 or PNAND CLE	
	G2	DQ[15]	I/O	AD[15]	I/O	DQ[15]	I/O	I/O[15]	I/O	Ext pull-up	I	D15, AD15, or I/O15	
	G3	DQ[14]	I/O	AD[14]	I/O	DQ[14]	I/O	I/O[14]	I/O	Ext pull-up	I	D14, AD14, or I/O14	
	F1	DQ[13]	I/O	AD[13]	I/O	DQ[13]	I/O	I/O[13]	I/O	Ext pull-up	I	D13, AD13, or I/O13	
	F2	DQ[12]	I/O	AD[12]	I/O	DQ[12]	I/O	I/O[12]	I/O	Ext pull-up	I	D12, AD12, or I/O12	
	F3	DQ[11]	I/O	AD[11]	I/O	DQ[11]	I/O	I/O[11]	I/O	Ext pull-up	I	D11, AD11, or I/O11	
	E1	DQ[10]	I/O	AD[10]	I/O	DQ[10]	I/O	I/O[10]	I/O	Ext pull-up	I	D10, AD10, or I/O10	
	E2	DQ[9]	I/O	AD[9]	I/O	DQ[9]	I/O	I/O[9]	I/O	Ext pull-up	I	D9, AD9, or I/O9	
	E3	DQ[8]	I/O	AD[8]	I/O	DQ[8]	I/O	I/O[8]	I/O	Ext pull-up	I	D8, AD8, or I/O8	
	D1	DQ[7]	I/O	AD[7]	I/O	DQ[7]	I/O	I/O[7]	I/O	Ext pull-up	I	D7, AD7, or I/O7	
	D2	DQ[6]	I/O	AD[6]	I/O	DQ[6]	I/O	I/O[6]	I/O	Ext pull-up	I	D6, AD6, or I/O6	
	D3	DQ[5]	I/O	AD[5]	I/O	DQ[5]	I/O	I/O[5]	I/O	Ext pull-up	I	D5, AD5, or I/O5	
	C1	DQ[4]	I/O	AD[4]	I/O	DQ[4]	I/O	I/O[4]	I/O	Ext pull-up	I	D4, AD4, or I/O4	
	C2	DQ[3]	I/O	AD[3]	I/O	DQ[3]	I/O	I/O[3]	I/O	Ext pull-up	I	D3, AD3, or I/O3	
	C3	DQ[2]	I/O	AD[2]	I/O	DQ[2]	I/O	I/O[2]	I/O	Ext pull-up	I	D2, AD2, or I/O2	
	B1	DQ[1]	I/O	AD[1]	I/O	DQ[1]	I/O	I/O[1]	I/O	SDO	O	SPI SDO, AD1or D1	
	B2	DQ[0]	I/O	AD[0]	I/O	DQ[0]	I/O	I/O[0]	I/O	SDI	I	SPI SDI, AD0, or D0	
	A1	ADV#	I	ADV#	I		I	ALE	I	Ext pull-up	I	Address Valid	
	B3	OE#	I	OE#	I	OE#	I	RE#	I	Ext pull-up	I	Output Enable	
	A2	WE#	I	WE#	I	WE#	I	WE#	I	Ext pull-up	I	WE#	
DRQ & Int	A3	INT#	O	INT#	O	INT#	O	INT#	O	SINT#	O	INT Request	GVDDQ VGND
	A4	DRQ#	O	DRQ#	O	DRQ#	O	DRQ#	O	N/C	O	DMA Request	
	B4	DACK#	I	DACK#	I	DACK#	I	DACK#	I	Ext pull-up	I	DMA Acknowledgement	
U-Port	A5	D+									I/O/Z	USB D+	UVDDQ UVSSQ
	A6	D–									I/O/Z	USB D–	
	A7	SWD+									I/O/Z	USB Switch DP	
	C6	SWD–									I/O/Z	USB Switch DM	

Table 7. Astoria CYWB0224ABS 121-ball FBGA Package Pin Assignments (continued)

	Pin Name											Pin Description	Power Domain
	Ball #	Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GPIF Configuration	I/O	GPIF & GPIO Configuration	I/O		
S-Port	G9	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GPIF_DATA[15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GPIF Data	SSVDDQ VGND
	G10	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GPIF_DATA[14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F9	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GPIF_DATA[13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F10	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GPIF_DATA[12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E9	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GPIF_DATA[11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E10	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GPIF_DATA[10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D9	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GPIF_DATA[9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D10	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GPIF_DATA[8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F8	SD_CLK	O	SD_CLK	O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	SD Clock or GPIO	
	G8	SD_CMD	I/O	SD_CMD	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	SD CMD or GPIO	
	H8	SD_POW		SD_POW		PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	SD Power or GPIO	
	H10	SD_WP	I	SD_WP	I	N/C	I	N/C		PC[5] (GPIO)		SD Write Protect	
	K7	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GPIF_DATA[7]	I/O	GPIF_DATA[7]	I/O	SD2 Data or GPIO or GPIF Data	SNVDDQ VGND
	K8	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GPIF_DATA[6]	I/O	GPIF_DATA[6]	I/O	SD2 Data or GPIO or GPIF Data	
	J8	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GPIF_DATA[5]	I/O	GPIF_DATA[5]	I/O	SD2 Data or GPIO or GPIF Data	
	K9	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GPIF_DATA[4]	I/O	GPIF_DATA[4]	I/O	SD2 Data or GPIO or GPIF Data	
	J9	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GPIF_DATA[3]	I/O	GPIF_DATA[3]	I/O	SD2 Data or GPIO or GPIF Data	
	H9	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GPIF_DATA[2]	I/O	GPIF_DATA[2]	I/O	SD2 Data or GPIO or GPIF Data	
	K10	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GPIF_DATA[1]	I/O	GPIF_DATA[1]	I/O	SD2 Data or GPIO or GPIF Data	
	J10	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GPIF_DATA[0]	I/O	GPIF_DATA[0]	I/O	SD2 Data or GPIO or GPIF Data	
	K6	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	SD2 Clock or GPIO	
	J6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA [7] (GPIO)	I/O	SD2 CMD or GPIO	
	J5	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	SD2 Power or GPIO	
	K4	N/C	O	N/C	O	N/C	O	GPIF_CTL[1]	O	GPIF_CTL[1]	O	GPIF Control Signal	
	H6	N/C	O	N/C	O	N/C	O	GPIF_CTL[0]	O	GPIF_CTL[0]	O	GPIF Control Signal	
	J7	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	GPIO	
	J4	N/C	I	N/C	I	N/C	I	GPIF_RDY[0]	O	GPIF_RDY[0]	O	GPIF Ready Signal	
	K5	SD2_WP	O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	SD Write Protect or GPIO	
Other	B10	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT	GVDDQ VGND
	C9	SD2_CD	I/O I	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD	
	D8	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD	
	C10	RESET#									I	RESET	
	C7	WAKEUP									I	Wake Up Signal	

Table 7. Astoria CYWB0224ABS 121-ball FBGA Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	C5	XTALSLC[1]	I	Clock Select 1	GVDDQ VGND
	C4	XTALSLC[0]		Clock Select 0	
	E8	TEST[2]	I	Test Cfg 2	
	C8	TEST[1]		Test Cfg 1	
	D7	TEST[0]		Test Cfg 0	
Clock	A8	XTALIN	I	Crystal / Clock IN	XVDDQ VGND
	B8	XTALOUT	O	Crystal Out	
Power	D4 H4	PVDDQ	Power	Processor I/F VDD	
	H5	SNVDDQ	Power	GPIF VDD	
	B5	UVDDQ	Power	USB VDD	
	H7	SSVDDQ	Power	SDIO VDD	
	D6	GVDDQ	Power	Misc I/O VDD	
	B9	AVDDQ	Power	Analog VDD	
	B7	XVDDQ	Power	Crystal VDD	
	D5, G4, G5, G6, G7, F7	VDD	Power	Core VDD	
	A10	VDD33	Power	Independent 3.3 V	
	B6	UVSSQ	Power	USB GND	
	A9	AVSSQ	Power	Analog GND	
	E4, E5, E6, E7, F4, F5, F6	VGND	Power	Core GND	

Table 8. Astoria CYWB0220ABS 121-ball FBGA Package Pin Assignments

	Pin Name											Pin Description	Power Domain
	Ball #	PCRAM Non Multiplexing	I/O	Addr/Data bus Multiplexing (ADM)	I/O	SRAM	I/O	PNAND	I/O	SPI	I/O		
P-Port	J2	CLK (pull-low in Asyn mode)	I	CLK (pull-low in Async mode)	I	Ext pull-low	I	Ext pull-low	I	SCK	I	Clock	PVDDQ VGND
	G1	CE#	I	CE#	I	CE#	I	CE#	I	SS#	I	CE# or SPI Slave Select	
	H3	A7	I	Ext pull-up	I	A7	I	A7 ≥ 1:SBD A7 ≥ 0: LBD	I	Ext pull-up	I	Addr. Bus 7	
	H2	A6	I	SDA	I	A6	I	SDA	I/O	SDA	I/O	A6 or I^2C data	
	H1	A5	I	SCL	I	A5	I	SCL	I/O	SCL	I/O	A5 or I^2C clock	
	J3	A4	I	Ext pull-up	I	A4	I	WP#	I	Ext pull-up	I	A4 or PNAND WP	
	J1	A3	I	A3 = 0 (Ext pull-low)	I	A3	I	A3 = 0 (Ext pull-low)	I	A3 = 1 (Ext pull-up)	I	A3	
	K3	A2	I	A2 = 1 (Ext pull-up)	I	A2	I	A2 = 0 (Ext pull-low)	I	A2 = 0 (Ext pull-low)	I	A2	
	K2	A1	I	Ext pull-up	I	A1	I	RB#	O	Ext pull-up	I	A1 or PNAND R/B#	
	K1	A0	I	Ext pull-up	I	A0	I	CLE	I	Ext pull-up	I	A0 or PNAND CLE	
	G2	DQ[15]	I/O	AD[15]	I/O	DQ[15]	I/O	I/O[15]	I/O	Ext pull-up	I	D15, AD15, or I/O15	
	G3	DQ[14]	I/O	AD[14]	I/O	DQ[14]	I/O	I/O[14]	I/O	Ext pull-up	I	D14, AD14, or I/O14	
	F1	DQ[13]	I/O	AD[13]	I/O	DQ[13]	I/O	I/O[13]	I/O	Ext pull-up	I	D13, AD13, or I/O13	
	F2	DQ[12]	I/O	AD[12]	I/O	DQ[12]	I/O	I/O[12]	I/O	Ext pull-up	I	D12, AD12, or I/O12	
	F3	DQ[11]	I/O	AD[11]	I/O	DQ[11]	I/O	I/O[11]	I/O	Ext pull-up	I	D11, AD11, or I/O11	
	E1	DQ[10]	I/O	AD[10]	I/O	DQ[10]	I/O	I/O[10]	I/O	Ext pull-up	I	D10, AD10, or I/O10	
	E2	DQ[9]	I/O	AD[9]	I/O	DQ[9]	I/O	I/O[9]	I/O	Ext pull-up	I	D9, AD9, or I/O9	
	E3	DQ[8]	I/O	AD[8]	I/O	DQ[8]	I/O	I/O[8]	I/O	Ext pull-up	I	D8, AD8, or I/O8	
	D1	DQ[7]	I/O	AD[7]	I/O	DQ[7]	I/O	I/O[7]	I/O	Ext pull-up	I	D7, AD7, or I/O7	
	D2	DQ[6]	I/O	AD[6]	I/O	DQ[6]	I/O	I/O[6]	I/O	Ext pull-up	I	D6, AD6, or I/O6	
	D3	DQ[5]	I/O	AD[5]	I/O	DQ[5]	I/O	I/O[5]	I/O	Ext pull-up	I	D5, AD5, or I/O5	
	C1	DQ[4]	I/O	AD[4]	I/O	DQ[4]	I/O	I/O[4]	I/O	Ext pull-up	I	D4, AD4, or I/O4	
	C2	DQ[3]	I/O	AD[3]	I/O	DQ[3]	I/O	I/O[3]	I/O	Ext pull-up	I	D3, AD3, or I/O3	
	C3	DQ[2]	I/O	AD[2]	I/O	DQ[2]	I/O	I/O[2]	I/O	Ext pull-up	I	D2, AD2, or I/O2	
	B1	DQ[1]	I/O	AD[1]	I/O	DQ[1]	I/O	I/O[1]	I/O	SDO	O	SPI SDO, AD1or D1	
	B2	DQ[0]	I/O	AD[0]	I/O	DQ[0]	I/O	I/O[0]	I/O	SDI	I	SPI SDI, AD0, or D0	
	A1	ADV#	I	ADV#	I		I	ALE	I	Ext pull-up	I	Address Valid	
	B3	OE#	I	OE#	I	OE#	I	RE#	I	Ext pull-up	I	Output Enable	
	A2	WE#	I	WE#	I	WE#	I	WE#	I	Ext pull-up	I	WE#	
DRQ & Int	A3	INT#	O	INT#	O	INT#	O	INT#	O	SINT#	O	INT Request	GVDDQ VGND
	A4	DRQ#	O	DRQ#	O	DRQ#	O	DRQ#	O	N/C	O	DMA Request	
	B4	DACK#	I	DACK#	I	DACK#	I	DACK#	I	Ext pull-up	I	DMA Acknowledgement	

Table 8. Astoria CYWB0220ABS 121-ball FBGA Package Pin Assignments (continued)

	Pin Name											Pin Description	Power Domain
		Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GPIF Configuration	I/O	GPIF & GPIO Configuration	I/O		
S-Port	G9	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GPIF_DATA[15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GPIF Data	SSVDDQ VGND
	G10	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GPIF_DATA[14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F9	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GPIF_DATA[13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F10	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GPIF_DATA[12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E9	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GPIF_DATA[11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E10	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GPIF_DATA[10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D9	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GPIF_DATA[9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D10	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GPIF_DATA[8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F8	SD_CLK	O	SD_CLK	O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	SD Clock or GPIO	
	G8	SD_CMD	I/O	SD_CMD	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	SD CMD or GPIO	
	H8	SD_POW		SD_POW		PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	SD Power or GPIO	
	H10	SD_WP	I	SD_WP	I	N/C		N/C		PC[5] (GPIO)		SD Write Protect	
	K7	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GPIF_DATA[7]	I/O	GPIF_DATA[7]	I/O	SD2 Data or GPIO or GPIF Data	SNVDDQ VGND
	K8	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GPIF_DATA[6]	I/O	GPIF_DATA[6]	I/O	SD2 Data or GPIO or GPIF Data	
	J8	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GPIF_DATA[5]	I/O	GPIF_DATA[5]	I/O	SD2 Data or GPIO or GPIF Data	
	K9	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GPIF_DATA[4]	I/O	GPIF_DATA[4]	I/O	SD2 Data or GPIO or GPIF Data	
	J9	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GPIF_DATA[3]	I/O	GPIF_DATA[3]	I/O	SD2 Data or GPIO or GPIF Data	
	H9	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GPIF_DATA[2]	I/O	GPIF_DATA[2]	I/O	SD2 Data or GPIO or GPIF Data	
	K10	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GPIF_DATA[1]	I/O	GPIF_DATA[1]	I/O	SD2 Data or GPIO or GPIF Data	
	J10	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GPIF_DATA[0]	I/O	GPIF_DATA[0]	I/O	SD2 Data or GPIO or GPIF Data	
	K6	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	SD2 Clock or GPIO	
	J6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	SD2 CMD or GPIO	
	J5	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	SD2 Power or GPIO	
	K4	N/C	O	N/C	O	N/C	O	GPIF_CTL[1]	O	GPIF_CTL[1]	O	GPIF Control Signal	
	H6	N/C	O	N/C	O	N/C	O	GPIF_CTL[0]	O	GPIF_CTL[0]	O	GPIF Control Signal	
	J7	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	GPIO	
	J4	N/C	I	N/C	I	N/C	I	GPIF_RDY[0]	O	GPIF_RDY[0]	O	GPIF Ready Signal	
	K5	SD2_WP	O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	SD Write Protect or GPIO	
Other	B10	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT / GPIF_RDY[1]	O	Reset Out	GVDDQ VGND
	C9	SD2_CD	I/O I	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD	
	D8	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD	
	C10	RESET#									I	RESET	
	C7	WAKEUP									I	Wake Up Signal	

Table 8. Astoria CYWB0220ABS 121-ball FBGA Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	C5	XTALSLC[1]	I	Clock Select 1	GVDDQ VGND
	C4	XTALSLC[0]		Clock Select 0	
	E8	TEST[2]	I	Test Cfg 2	
	C8	TEST[1]		Test Cfg 1	
	D7	TEST[0]		Test Cfg 0	
Clock	A8	XTALIN	I	Crystal / Clock IN	XVDDQ VGND
	B8	XTALOUT	O	Crystal Out	
Power	D4 H4	PVDDQ	Power	Processor I/F VDD	
	H5	SNVDDQ	Power	GPIF VDD	
	B5	UVDDQ	Power	USB VDD	
	H7	SSVDDQ	Power	SDIO VDD	
	D6	GVDDQ	Power	Misc I/O VDD	
	B9	AVDDQ	Power	Analog VDD	
	B7	XVDDQ	Power	Crystal VDD	
	D5, G4, G5, G6, G7, F7	VDD	Power	Core VDD	
	A10	VDD33	Power	Independent 3.3 V	
	B6	UVSSQ	Power	USB GND	
	A9	AVSSQ	Power	Analog GND	
	E4, E5, E6, E7, F4, F5, F6	VGND	Power	Core GND	

Table 9. Astoria CYWB0216ABS 121-ball FBGA Package Pin Assignments

	Pin Name			Pin Description	Power Domain
Unused Pins	Ball #	Pull Direction	I/O		
	J2	P/D	I	Pull-down	PVDDQ VGND
	G1	P/U	I	Pull-up	
	H3	P/U	I	Pull-up	
	J3	P/U	I	Pull-up	
	J1	P/U	I	Pull-up	
	K3	P/D	I	Pull-down	
	K2	P/U	I	Pull-up	
	K1	P/U	I	Pull-up	
	G2	P/U	I	Pull-up	
	G3	P/U	I	Pull-up	
	F1	P/U	I	Pull-up	
	F2	P/U	I	Pull-up	
	F3	P/U	I	Pull-up	
	E1	P/U	I	Pull-up	
	E2	P/U	I	Pull-up	
	E3	P/U	I	Pull-up	
	D1	P/U	I	Pull-up	
	D2	P/U	I	Pull-up	
	D3	P/U	I	Pull-up	
	C1	P/U	I	Pull-up	
	C2	P/U	I	Pull-up	
	C3	P/U	I	Pull-up	
	B1	P/U	O	Pull-up	
	B2	P/U	I	Pull-up	
	A1	P/U	I	Pull-up	
	B3	P/U	I	Pull-up	
	A2	P/U	I	Pull-up	
	A3	N/C	O	No Connect	GVDDQ VGND
	A4	N/C	O	No Connect	
	B4	P/U	I	Pull-up	
I2C Pins		Interface Pins	I/O	Pin Description	
	H2	SDA	I/O	I^2C data	PVDDQ VGND
	H1	SCL	I/O	I^2C clock	
U-Port	A5	D+	I/O/Z	USB D+	UVDDQ UVSSQ
	A6	D–	I/O/Z	USB D–	
	A7	SWD+	I/O/Z	USB Switch DP	
	C6	SWD–	I/O/Z	USB Switch DM	

Table 9. Astoria CYWB0216ABS 121-ball FBGA Package Pin Assignments (continued)

	Pin Name											Pin Description	Power Domain
		Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GPIF Configuration	I/O	GPIF & GPIO Configuration	I/O		
S-Port	G9	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GPIF_DATA[15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GPIF Data	SSVDDQ VGND
	G10	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GPIF_DATA[14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F9	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GPIF_DATA[13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F10	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GPIF_DATA[12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E9	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GPIF_DATA[11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E10	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GPIF_DATA[10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D9	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GPIF_DATA[9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D10	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GPIF_DATA[8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F8	SD_CLK	O	SD_CLK	O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	SD Clock or GPIO	
	G8	SD_CMD	I/O	SD_CMD	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	SD CMD or GPIO	
	H8	SD_POW		SD_POW		PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	SD Power or GPIO	
	H10	SD_WP	I	SD_WP	I	N/C		N/C		PC[5] (GPIO)		SD Write Protect	
	K7	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GPIF_DATA[7]	I/O	GPIF_DATA[7]	I/O	SD2 Data or GPIO or GPIF Data	SNVDDQ VGND
	K8	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GPIF_DATA[6]	I/O	GPIF_DATA[6]	I/O	SD2 Data or GPIO or GPIF Data	
	J8	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GPIF_DATA[5]	I/O	GPIF_DATA[5]	I/O	SD2 Data or GPIO or GPIF Data	
	K9	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GPIF_DATA[4]	I/O	GPIF_DATA[4]	I/O	SD2 Data or GPIO or GPIF Data	
	J9	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GPIF_DATA[3]	I/O	GPIF_DATA[3]	I/O	SD2 Data or GPIO or GPIF Data	
	H9	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GPIF_DATA[2]	I/O	GPIF_DATA[2]	I/O	SD2 Data or GPIO or GPIF Data	
	K10	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GPIF_DATA[1]	I/O	GPIF_DATA[1]	I/O	SD2 Data or GPIO or GPIF Data	
	J10	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GPIF_DATA[0]	I/O	GPIF_DATA[0]	I/O	SD2 Data or GPIO or GPIF Data	
	K6	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	SD2 Clock or GPIO	
	J6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	SD2 CMD or GPIO	
	J5	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	SD2 Power or GPIO	
	K4	N/C	O	N/C	O	N/C	O	GPIF_CTL[1]	O	GPIF_CTL[1]	O	GPIF Control Signal	
	H6	N/C	O	N/C	O	N/C	O	GPIF_CTL[0]	O	GPIF_CTL[0]	O	GPIF Control Signal	
	J7	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	GPIO	
	J4	N/C	I	N/C	I	N/C	I	GPIF_RDY[0]	O	GPIF_RDY[0]	O	GPIF Ready Signal	
	K5	SD2_WP	O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	SD Write Protect or GPIO	
Other	B10	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT / GPIF_RDY[1]	O	Reset Out	GVDDQ VGND
	C9	SD2_CD	I/O I	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD	
	D8	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD	
	C10	RESET#									I	RESET	
	C7	WAKEUP									I	Wake Up Signal	

Table 9. Astoria CYWB0216ABS 121-ball FBGA Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	C5	XTALSLC[1]	I	Clock Select 1	GVDDQ VGND
	C4	XTALSLC[0]		Clock Select 0	
	E8	TEST[2]	I	Test Cfg 2	
	C8	TEST[1]		Test Cfg 1	
	D7	TEST[0]		Test Cfg 0	
Clock	A8	XTALIN	I	Crystal/Clock IN	XVDDQ VGND
	B8	XTALOUT	O	Crystal Out	
Power	D4 H4	PVDDQ	Power	Processor I/F VDD	
	H5	SNVDDQ	Power	NAND VDD	
	B5	UVDDQ	Power	USB VDD	
	H7	SSVDDQ	Power	SDIO VDD	
	D6	GVDDQ	Power	Misc I/O VDD	
	B9	AVDDQ	Power	Analog VDD	
	B7	XVDDQ	Power	Crystal VDD	
	D5, G4, G5, G6, G7, F7	VDD	Power	Core VDD	
	A10	VDD33	Power	Independent 3.3 V	
	B6	UVSSQ	Power	USB GND	
	A9	AVSSQ	Power	Analog GND	
	E4, E5, E6, E7, F4, F5, F6	VGND	Power	Core GND	

Table 10. Astoria 81-ball SP WLCSP Package Pin Assignments

	Pin Name					Pin Description	Power Domain
	Ball #	PNAND	I/O	SPI	I/O		
P-Port	H9	Ext pull low	I	SCK	I	Clock	PVDDQ VGND
	F9	CE#	I	SS#	I	CE# or SPI Slave Select	
	E7	SDA	I/O	SDA	I/O	I2C data	
	H8	SCL	I/O	SCL	I/O	I2C clock	
	J9	WP#	I	Ext pull up	I	PNAND WP	
	G8	A[3]=0; (Ext pull low)	I	A[3]=0; (Ext pull up)	I	A[3]	
	E6	A[2]=0; (Ext pull low)	I	A[2]=0; (Ext pull low)	I	A[2]	
	G9	RB#	O	Ext pull up	I	PNAND R/B#	
	F8	CLE	I	Ext pull up	I	PNAND CLE	
	D9	I/O[7]	I/O	Ext pull up	I	IO7	
	D8	I/O[6]	I/O	Ext pull up	I	IO6	
	C9	I/O[5]	I/O	Ext pull up	I	IO5	
	B9	I/O[4]	I/O	Ext pull up	I	IO4	
	C8	I/O[3]	I/O	Ext pull up	I	IO3	
	C7	I/O[2]	I/O	Ext pull up	I	IO2	
	B8	I/O[1]	I/O	SDO	O	IO1 or SPI SDO	
	A8	I/O[0]	I/O	SDI	I	IO0 or SPI SDI	
	B7	ALE	I	Ext pull up	I	Address Valid	
	B6	RE#	I	Ext pull up	I	Output Enable	
	A7	WE#	I	Ext pull up	I	WE#	
Int	C1	INT#	O	SINT#	O	INT Request	GVDDQ VGND
U-Port	A4	D+			I/O/Z	USB D+	UVDDQ UVSSQ
	A5	D–			I/O/Z	USB D–	
	C4	SWD+			I/O/Z	USB Switch D+	
	C5	SWD–			I/O/Z	USB Switch D–	

Table 10. Astoria 81-ball SP WLCSP Package Pin Assignments (continued)

	Pin Name											Pin Description	Power Domain
	Ball #	Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GPIF Configuration	I/O	GPIF & GPIO Configuration	I/O		
S-Port	H2	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GPIF_DATA [15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GPIF Data	SSVDDQ VGND
	H1	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GPIF_DATA [14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	G3	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GPIF_DATA [13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	G2	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GPIF_DATA [12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F2	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GPIF_DATA [11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F3	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GPIF_DATA [10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E3	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GPIF_DATA [9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E2	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GPIF_DATA [8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	G1	SD_CLK	O	SD_CLK		PC-7 (GPIO)	I/O	PC-7 (GPIO)	I/O	PC-7 (GPIO)	I/O	SD Clock or GPIO	
	F4	SD_CMD	I/O	SD_CMD	I/O	PC-3 (GPIO)	I/O	PC-3 (GPIO)	I/O	PC-3 (GPIO)	I/O	SD CMD or GPIO	
	J1	SD_POW	O	SD_POW	O	PC-6 (GPIO)	I/O	PC-6 (GPIO)	I/O	PC-6 (GPIO)	I/O	SD Power or GPIO	
	E1	SD_WP	I	SD_W	I	N/C	I	N/C	I	PC-5 (GPIO)	I/O	SD Write Protect	
	H5	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GPIF_DATA [7]	I/O	GPIF_DATA [7]	I/O	SD2 Data or GPIO or GPIF Data	SNVDDQ VGND
	J4	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GPIF_DATA [6]	I/O	GPIF_DATA [6]	I/O	SD2 Data or GPIO or GPIF Data	
	G5	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GPIF_DATA [5]	I/O	GPIF_DATA [5]	I/O	SD2 Data or GPIO or GPIF Data	
	H4	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GPIF_DATA [4]	I/O	GPIF_DATA [4]	I/O	SD2 Data or GPIO or GPIF Data	
	J3	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GPIF_DATA [3]	I/O	GPIF_DATA [3]	I/O	SD2 Data or GPIO or GPIF Data	
	G4	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GPIF_DATA [2]	I/O	GPIF_DATA [2]	I/O	SD2 Data or GPIO or GPIF Data	
	H3	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GPIF_DATA [1]	I/O	GPIF_DATA [1]	I/O	SD2 Data or GPIO or GPIF Data	
	J2	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GPIF_DATA [0]	I/O	GPIF_DATA [0]	I/O	SD2 Data or GPIO or GPIF Data	
	F7	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA-6 (GPIO)	I/O	PA-6 (GPIO)	I/O	SD2 Clock or GPIO	
	H6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA-7 (GPIO)	I/O	PA-7 (GPIO)	I/O	SD2 CMD or GPIO	
	G7	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC-0 (GPIO)	I/O	PC-0 (GPIO)	I/O	SD2 Power or GPIO	
	J8	N/C	O	N/C	O	N/C	O	GPIF_CTL[1]	O	GPIF_CTL[1]	O	GPIF Control Signal	
	J5	N/C	O	N/C	O	N/C	O	GPIF_CTL[0]	O	GPIF_CTL[0]	O	GPIF Control Signal	
	G6	PA-5 (GPIO)	I/O	PA-5 (GPIO)	I/O	PA-5 (GPIO)	I/O	PA-5 (GPIO)	I/O	PA-5 (GPIO)	I/O	GPIO	
	H7	N/C	I	N/C	I	N/C	I	GPIF_RDY[0]	O	GPIF_RDY[0]	O	GPIF Ready Signal	
	J7	SD2_WP	O	PC-2 (GPIO)	I/O	PC-2 (GPIO)	I/O	PC-2 (GPIO)	I/O	PC-2 (GPIO)	I/O	SD Write Protect or GPIO	
Other	C2	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT or GPIF	GVDDQ VGND
	D2	PC-5 (GPIO[1]) or SD2_CD	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD	
	D1	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD	
	C3	RESET#									I	RESET	
	D4	WAKEUP									I	Wake Up Signal	

Table 10. Astoria 81-ball SP WLCSP Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	A1	XTALSLC	I	Clock Select	GVDDQ VGND
	B1	TEST[2]	I	Test Cfg 2	
	C6	TEST[1]	I	Test Cfg 1	
	B4	TEST[0]	I	Test Cfg 0	
CLK	A2	XTALIN	I	Crystal / Clock IN	XVDDQ VGND
Power	A9, E8	PVDDQ	Power	Processor I/F VDD	
	J6	SNVDDQ	Power	GPIF VDD	
	B5	UVDDQ	Power	USB VDD	
	F1	SSVDDQ	Power	SDIO VDD	
	D3	GVDDQ	Power	Misc I/O VDD	
	B3	AVDDQ	Power	Analog VDD	
	A6, D6, E5, F6	VDD	Power	Core VDD	
	A3	UVSSQ	Power	USB GND	
	B2	AVSSQ	Power	Analog GND	
	D5, D7, E4, E9, F5	VGND	Power	Core GND	

Table 11. Astoria 81-ball Lite SP WLCSP Package Pin Assignments

	Pin Name							Pin Description	Power Domain
	Ball #	SRAM Interface		ADM (Address/Data Multi-plexing)	I/O	PNAND	I/O		
P-Port	G9	CE#	I	CE#	I	CE#	I	CE#	PVDDQ VGND
	H5	A7	I	External Pull Up	I	A7 ≥ 1:SBD A7 ≥ 0: LBD	I	A7	
	J8	A6	I	SDA	I/O	SDA	I/O	A7 or SDA	
	H6	A5	I	SCL	I/O	SCL	I/O	A6 or SCL	
	H7	A4	I	External Pull Up	I	WP#	I	A4 or WP#	
	J9	A3	I	External Pull Low	I	External Pull Low	I	A3	
	H8	A2	I	External Pull Up	I	External Pull Low	I	A2	
	H9	A1	I	External Pull Up	I	R/B#	I	A1 or R/B#	
	G8	A0	I	External Pull Up	I	CLE	I	A0 or CLE	
	G6	DQ[15]	I/O	AD[15]	I/O	I/O[15]	I/O	D15, AD15, or IO15	
	F9	DQ[14]	I/O	AD[14]	I/O	I/O[14]	I/O	D14, AD14, or IO14	
	F8	DQ[13]	I/O	AD[13]	I/O	I/O[13]	I/O	D13, AD13, or IO13	
	F7	DQ[12]	I/O	AD[12]	I/O	I/O[12]	I/O	D12, AD12, or IO12	
	E9	DQ[11]	I/O	AD[11]	I/O	I/O[11]	I/O	D11, AD11, or IO11	
	E8	DQ[10]	I/O	AD[10]	I/O	I/O[10]	I/O	D10, AD10, or IO10	
	D9	DQ[9]	I/O	AD[9]	I/O	I/O[9]	I/O	D9, AD9, or IO9	
	D7	DQ[8]	I/O	AD[8	I/O	I/O[8]	I/O	D8, AD8, or IO8	
	D8	DQ[7]	I/O	AD[7]	I/O	I/O[7]	I/O	D7, AD7, or IO7	
	C9	DQ[6]	I/O	AD[6]	I/O	I/O[6]	I/O	D6, AD6, or IO6	
	D6	DQ[5]	I/O	AD[5]	I/O	I/O[5]	I/O	D5, AD5, or IO5	
	B9	DQ[4]	I/O	AD[4]	I/O	I/O[4]	I/O	D4, AD4, or IO4	
	C8	DQ[3]	I/O	AD[3]	I/O	I/O[3]	I/O	D3, AD3, or IO3	
	C7	DQ[2]	I/O	AD[2]	I/O	I/O[2]	I/O	D2, AD2, or IO2	
	B8	DQ[1]	I/O	AD[1]	I/O	I/O[1]	I/O	D1, AD1, or IO1	
	A8	DQ[0]	I/O	AD[0]	I/O	I/O[0]	I/O	D0I, AD0, or IO0	
	B7		I	ADV#	I	ALE	I	Address Valid	
	B6	OE#	I	OE#	I	RE#	I	Output Enable	
	A7	WE#	I	WE#	I	WE#	I	WE#	
Int	C1	INT#	O	INT#	O	INT#	O	INT Request	GVDDQ VGND
	D4	DRQ#	O	DRQ#	O	DRQ#	O	DMA Request	
	D3	DACK#	I	DACK#	I	DACK#	I	DMA ACK	
U-Port	A4	D+					I/O/Z	USB D+	UVDDQ UVSSQ
	A5	D–					I/O/Z	USB D–	
	C4	SWD+					I/O/Z	USB Switch DP	
	C5	SWD–					I/O/Z	USB Switch DM	

Table 11. Astoria 81-ball Lite SP WLCSP Package Pin Assignments (continued)

		S-Port Interface	I/O		
S-Port	F3	SD_D[7]	I/O	SD Data or GPIO	SSVDDQ VGND
	H1	SD_D[6]	I/O	SD Data or GPIO	
	G2	SD_D[5]	I/O	SD Data or PIO	
	E3	SD_D[4]	I/O	SD Data or GPIO	
	F2	SD_D[3]	I/O	SD Data or GPIO	
	F1	SD_D[2]	I/O	SD Data or GPIO	
	E2	SD_D[1]	I/O	SD Data or GPIO	
	E1	SD_D[0]	I/O	SD Data or GPIO	
	G1	SD_CLK	I/O	SD Clock or GPIO	
	J1	SD_CMD	I/O	SD CMD or GPIO	
	J5	PB[7] (GPIO)	I/O	GPIOI	
	J4	PB[6] (GPIO)	I/O	GPIOI	
	H4	PB[5] (GPIO)	I/O	GPIOI	
	J3	PB[4] (GPIO)	I/O	GPIOI	
	H3	PB[3] (GPIO)	I/O	GPIOI	
	G4	PB[2] (GPIO)	I/O	GPIOI	
	J2	PB[1] (GPIO)	I/O	GPIOI	
	H2	PB[0] (GPIO)	I/O	GPIOI	
	J7	GPIF_RDY	O	Test Mode	
	J6	GPIF_CTL	I	Test Mode (Ext Pull-High)	
Other	D1	SD_CD	I	SD CD	GVDDQ VGND
	C2	RESET#	I	RESET	
	E5	WAKEUP	I	Wake Up Signal	
Conf	C3	TEST[2]	I	Test Cfg 2	GVDDQ VGND
	D5	TEST[1]	I	Test Cfg 1	
	B1	TEST[0]	I	Test Cfg 0	
CLK	A2	XTALIN	I	Clock IN	XVDDQ VGND
	A1	XTALOUT	O	Clock OUT	
Power	A9, F6	PVDDQ	Power	Processor I/F VDD	
	B5	UVDDQ	Power	USBVDD	
	E4	SSVDDQ	Power	SDIO VDD	
	D2	GVDDQ	Power	Misc I/O VDD	
	B3	AVDDQ	Power	Analog VDD	
	B4	XVDDQ	Power	Crystal VDD	
	E7, A6, C6, F5	VDD	Power	Core VDD	
	A3	UVSSQ	Power	USB GND	
	B2	AVSSQ	Power	Analog GND	
	G7, E6, G5, F4, G3	VGND	Power	Core GND	