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WirelessUSB™ LR 2.4-GHz DSSS Radio SoC

1.0 Features

- **2.4-GHz radio transceiver**
- **Operates in the unlicensed Industrial, Scientific, and Medical (ISM) band (2.4 GHz–2.483 GHz)**
- **–95-dBm receive sensitivity**
- **Up to 0dBm output power**
- **Range of up to 50 meters or more**
- **Data throughput of up to 62.5 kbits/sec**
- **Highly integrated low cost, minimal number of external components required**
- **Dual DSSS reconfigurable baseband correlators**
- **SPI microcontroller interface (up to 2-MHz data rate)**
- **13-MHz input clock operation**
- **Low standby current < 1 µA**
- **Integrated 32-bit Manufacturing ID**
- **Operating voltage from 2.7V to 3.6V**
- **Operating temperature from –40° to 85°C**
- **Offered in a small footprint 48 QFN or cost saving 28 SOIC**

2.0 Functional Description

The CYWUSB6935 transceiver is a single-chip 2.4-GHz Direct Sequence Spread Spectrum (DSSS) Gaussian Frequency Shift Keying (GFSK) baseband modem radio that connects directly to a microcontroller.

The CYWUSB6935 is offered in an industrial temperature range 48-pin QFN, 28-pin SOIC, and a commercial temperature range 48-pin QFN.

3.0 Applications

- Building/Home Automation
  - Climate Control
  - Lighting Control
  - Smart Appliances
  - On-Site Paging Systems
  - Alarm and Security
- Industrial Control
  - Inventory Management
  - Factory Automation
  - Data Acquisition
- Automatic Meter Reading (AMR)
- Transportation
  - Diagnostics
  - Remote Keyless Entry
- Consumer / PC
  - Locator Alarms
  - Presenter Tools
  - Remote Controls
  - Toys

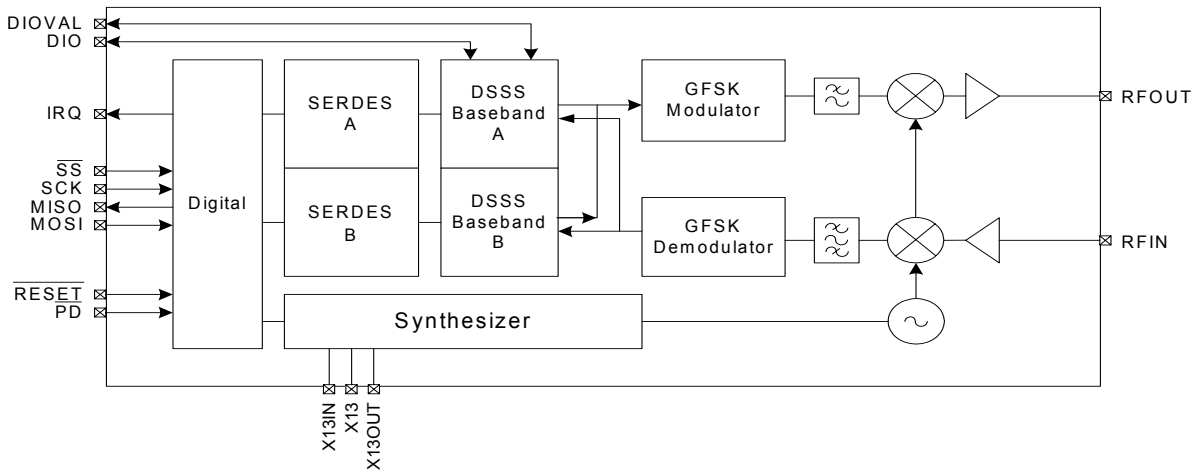

Figure 3-1. CYWUSB6935 Simplified Block Diagram

3.1 Applications Support

The CYWUSB6935 is supported by both the CY3632 WirelessUSB Development Kit and the CY3635 WirelessUSB N:1 Development Kit. The development kit provides all of the materials and documents needed to cut the cord on multipoint to point and point to point low bandwidth high node density applications including four small form-factor sensor boards and a hub board that connect to WirelessUSB LR RF module boards, comprehensive WirelessUSB protocol code examples and all of the associated schematics, gerber files and bill of materials. The WirelessUSB N:1 Development Kit is also supported by the WirelessUSB Listener Tool.

4.0 Functional Overview

The CYWUSB6935 provides a complete WirelessUSB LR SPI to antenna radio modem. The CYWUSB6935 is designed to implement wireless devices operating in the worldwide 2.4-GHz Industrial, Scientific, and Medical (ISM) frequency band (2.400GHz - 2.4835GHz). It is intended for systems compliant with world-wide regulations covered by ETSI EN 301 489-1 V1.4.1, ETSI EN 300 328-1 V1.3.1 (European Countries); FCC CFR 47 Part 15 (USA and Industry Canada) and ARIB STD-T66 (Japan).

The CYWUSB6935 contains a 2.4-GHz radio transceiver, a GFSK modem and a dual DSSS reconfigurable baseband. The radio and baseband are both code- and frequency-agile. Forty-nine spreading codes selected for optimal performance (Gold codes) are supported across 78 1-MHz channels yielding a theoretical spectral capacity of 3822 channels. The CYWUSB6935 supports a range of up to 50 meters or more.

4.1 2.4-GHz Radio

The receiver and transmitter are a single-conversion low-Intermediate Frequency (low-IF) architecture with fully integrated IF channel matched filters to achieve high performance in the presence of interference. An integrated Power Amplifier (PA) provides an output power control range of 30 dB in seven steps.

Both the receiver and transmitter integrated Voltage Controlled Oscillator (VCO) and synthesizer have the agility to cover the complete 2.4-GHz GFSK radio transmitter ISM band. The VCO loop filter is also integrated on-chip.

4.2 GFSK Modem

The transmitter uses a DSP-based vector modulator to convert the 1-MHz chips to an accurate GFSK carrier.

The receiver uses a fully integrated Frequency Modulator (FM) detector with automatic data slicer to demodulate the GFSK signal.

4.3 Dual DSSS Baseband

Data is converted to DSSS chips by a digital spreader. Despreading is performed by an oversampled correlator. The DSSS baseband cancels spurious noise and assembles properly correlated data bytes.

The DSSS baseband has four operating modes: 64 chips/bit Single Channel, 32 chips/bit Dual Channel, 32 chips/bit Single Channel 2x Oversampled, and 32 chips/bit Single Channel Dual Data Rate (DDR).

4.3.1 64 chips/bit Single Channel

The baseband supports a single data stream operating at 15.625 kbits/sec. The advantage of selecting this mode is its ability to tolerate a noisy environment. This is because the 15.625 kbits/sec data stream utilizes the longest PN Code resulting in the highest probability for recovering packets over the air. This mode can also be selected for systems requiring data transmissions over longer ranges.

4.3.2 32 chips/bit Dual Channel

The baseband supports two non-simultaneous data streams each operating at 31.25 kbits/sec.

4.3.3 32 chips/bit Single Channel 2x Oversampled

The baseband supports a single data stream operating at 31.25 kbits/sec that is sampled twice as much as the other modes. The advantage of selecting this mode is its ability to tolerate a noisy environment.

4.3.4 32 chips/bit Single Channel Dual Data Rate (DDR)

The baseband spreads bits in pairs and supports a single data stream operating at 62.5 kbits/sec.

4.4 Serializer/Deserializer (SERDES)

CYWUSB6935 provides a data Serializer/Deserializer (SERDES), which provides byte-level framing of transmit and receive data. Bytes for transmission are loaded into the SERDES and receive bytes are read from the SERDES via the SPI interface. The SERDES provides double buffering of transmit and receive data. While one byte is being transmitted by the radio the next byte can be written to the SERDES data register insuring there are no breaks in transmitted data.

After a receive byte has been received it is loaded into the SERDES data register and can be read at any time until the next byte is received, at which time the old contents of the SERDES data register will be overwritten.

4.5 Application Interfaces

CYWUSB6935 has a fully synchronous SPI slave interface for connectivity to the application MCU. Configuration and byte-oriented data transfer can be performed over this interface. An interrupt is provided to trigger real time events.

An optional SERDES Bypass mode (DIO) is provided for applications that require a synchronous serial bit-oriented data path. This interface is for data only.

4.6 Clocking and Power Management

A 13-MHz crystal is directly connected to X13IN and X13 without the need for external capacitors. The CYWUSB6935 has a programmable trim capability for adjusting the on-chip load capacitance supplied to the crystal. The Radio Frequency (RF) circuitry has on-chip decoupling capacitors. The CYWUSB6935 is powered from a 2.7V to 3.6V DC supply. The CYWUSB6935 can be shutdown to a fully static state using the $\overline{PD}$ pin.

Below are the requirements for the crystal to be directly connected to X13IN and X13:

- Nominal Frequency: 13 MHz
- Operating Mode: Fundamental Mode
- Resonance Mode: Parallel Resonant
- Frequency Stability: ± 30 ppm
- Series Resistance: ≤ 100 ohms
- Load Capacitance: 10 pF
- Drive Level: 10uW–100 uW

4.7 Receive Signal Strength Indicator (RSSI)

The RSSI register (Reg 0x22) returns the relative signal strength of the ON-channel signal power and can be used to: 1) determine the connection quality, 2) determine the value of the noise floor, and 3) check for a quiet channel before transmitting.

The internal RSSI voltage is sampled through a 5-bit analog-to-digital converter (ADC). A state machine controls the conversion process. Under normal conditions, the RSSI state machine initiates a conversion when an ON-channel carrier is detected and remains above the noise floor for over 50uS. The conversion produces a 5-bit value in the RSSI register (Reg 0x22, bits 4:0) along with a valid bit, RSSI register (Reg 0x22, bit 5). The state machine then remains in HALT mode and does not reset for a new conversion until the receive mode is toggled off and on. Once a connection has been established, the RSSI register can be read to determine the relative connection quality of the channel. A RSSI register value lower than 10 indicates that the received signal strength is low, a value greater than 28 indicates a strong signal level.

To check for a quiet channel before transmitting, first set up receive mode properly and read the RSSI register (Reg 0x22). If the valid bit is zero, then force the Carrier Detect register (Reg 0x2F, bit 7=1) to initiate an ADC conversion. Then, wait greater than 50uS and read the RSSI register again. Next, clear the Carrier Detect Register (Reg 0x2F, bit 7=0) and turn the receiver OFF. Measuring the noise floor of a quiet channel is inherently a 'noisy' process so, for best results, this procedure should be repeated several times (~20) to compute an average noise floor level. A RSSI register value of 0-10 indicates a channel that is relatively quiet. A RSSI register value greater than 10 indicates the channel is probably being used. A RSSI register value greater than 28 indicates the presence of a strong signal.

5.0 Application Interfaces

5.1 SPI Interface

The CYWUSB6935 has a four-wire SPI communication interface between an application MCU and one or more slave devices. The SPI interface supports single-byte and multi-byte serial transfers. The four-wire SPI communications interface consists of Master Out-Slave In (MOSI), Master In-Slave Out (MISO), Serial Clock (SCK), and Slave Select ($\overline{SS}$).

The SPI receives SCK from an application MCU on the SCK pin. Data from the application MCU is shifted in on the MOSI pin. Data to the application MCU is shifted out on the MISO pin. The active-low Slave Select ($\overline{SS}$) pin must be asserted to initiate a SPI transfer.

The application MCU can initiate a SPI data transfer via a multi-byte transaction. The first byte is the Command/Address byte, and the following bytes are the data bytes as shown in *Figure 5-1* through *Figure 5-4*. The $\overline{SS}$ signal should not be deasserted between bytes. The SPI communications is as follows:

- Command Direction (bit 7) = “0” Enables SPI read transaction. A “1” enables SPI write transactions.
- Command Increment (bit 6) = “1” Enables SPI auto address increment. When set, the address field automatically increments at the end of each data byte in a burst access, otherwise the same address is accessed.
- Six bits of address.
- Eight bits of data.

The SPI communications interface has a burst mechanism, where the command byte can be followed by as many data bytes as desired. A burst transaction is terminated by deasserting the slave select ($\overline{SS}$ = 1).

The SPI communications interface single read and burst read sequences are shown in *Figure 5-2* and *Figure 5-3*, respectively.

The SPI communications interface single write and burst write sequences are shown in *Figure 5-4* and *Figure 5-5*, respectively.

	Byte 1			Byte 1+N
Bit #	7	6	[5:0]	[7:0]
Bit Name	DIR	INC	Address	Data

Figure 5-1. SPI Transaction Format

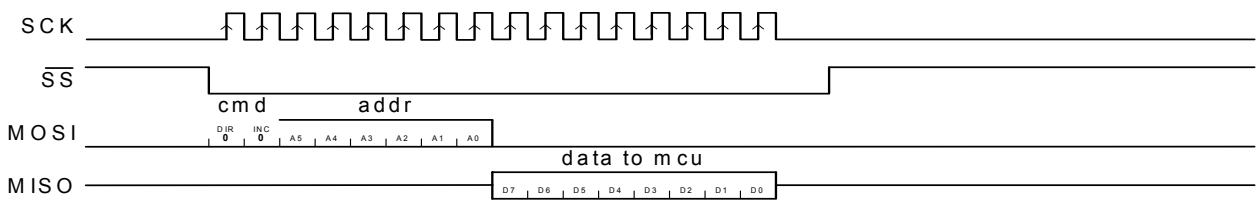

Figure 5-2. SPI Single Read Sequence

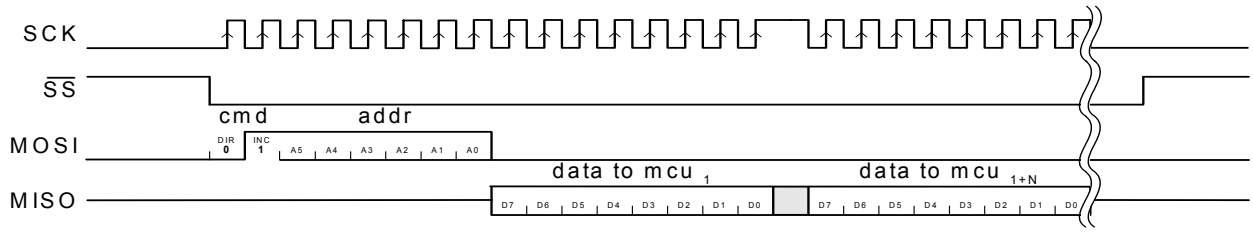

Figure 5-3. SPI Burst Read Sequence

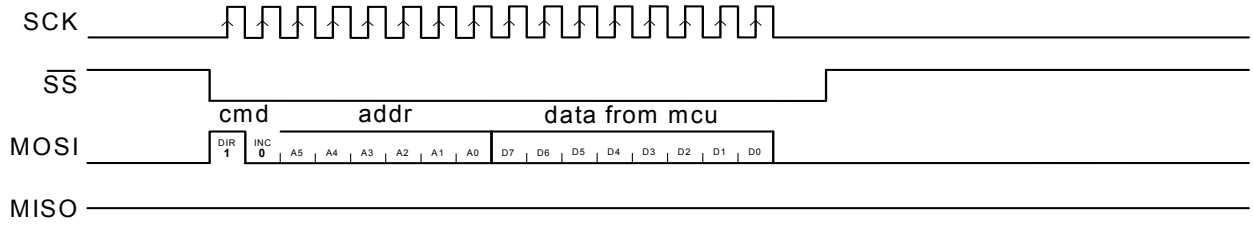

Figure 5-4. SPI Single Write Sequence

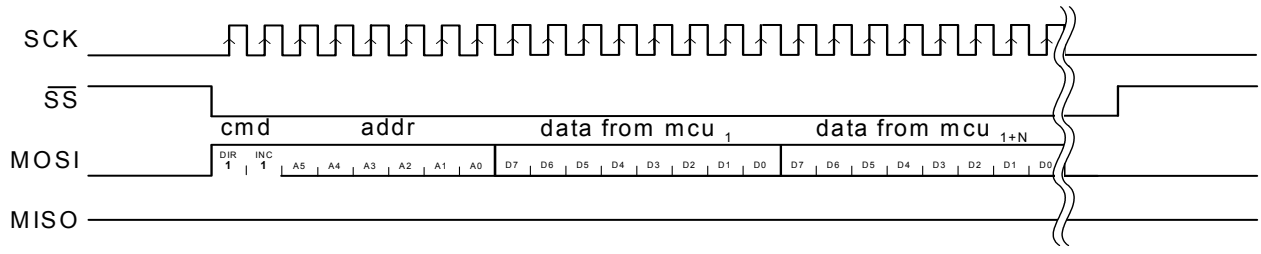

Figure 5-5. SPI Burst Write Sequence

5.2 DIO Interface

The DIO communications interface is an optional SERDES bypass data-only transfer interface. In receive mode, DIO and DIOVAL are valid after the falling edge of IRQ, which clocks the data as shown in *Figure 5-6*. In transmit mode, DIO and DIOVAL are sampled on the falling edge of the IRQ, which clocks the data as shown in *Figure 5-7*. The application MCU samples the DIO and DIOVAL on the rising edge of IRQ.

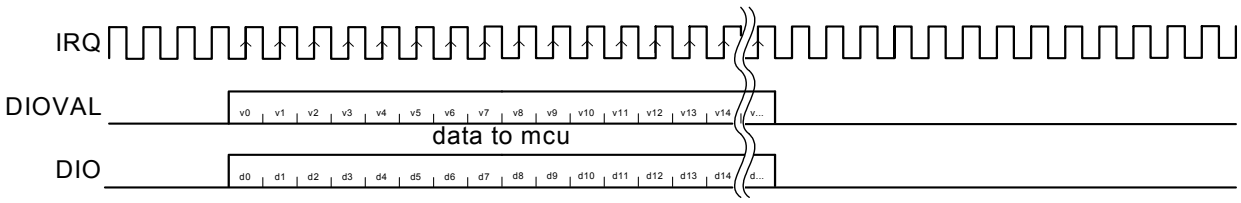

Figure 5-6. DIO Receive Sequence

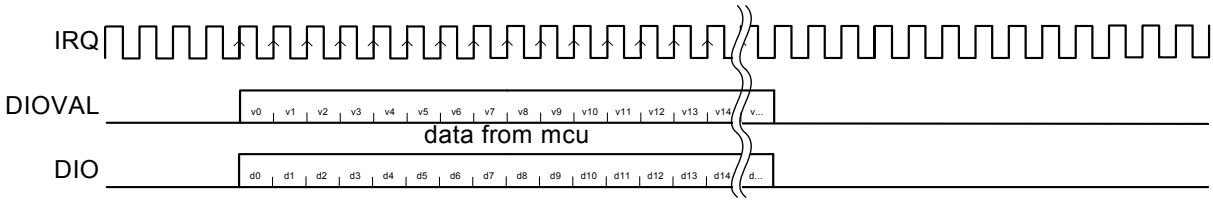

Figure 5-7. DIO Transmit Sequence

5.3 Interrupts

The CYWUSB6935 features three sets of interrupts: transmit, received, and a wake interrupt. These interrupts all share a single pin (IRQ), but can be independently enabled/disabled. In transmit mode, all receive interrupts are automatically disabled, and in transmit mode all receive interrupts are automatically disabled. However, the contents of the enable registers are preserved when switching between transmit and receive modes.

Interrupts are enabled and the status read through 6 registers: Receive Interrupt Enable (Reg 0x07), Receive Interrupt Status (Reg 0x08), Transmit Interrupt Enable (Reg 0x0D), Transmit Interrupt Status (Reg 0x0E), Wake Enable (Reg 0x1C), Wake Status (Reg 0x1D).

If more than 1 interrupt is enabled at any time, it is necessary to read the relevant interrupt status register to determine which event caused the IRQ pin to assert. Even when a given interrupt source is disabled, the status of the condition that would otherwise cause an interrupt can be determined by reading the appropriate interrupt status register. It is therefore possible to use the devices without making use of the IRQ pin at all. Firmware can poll the interrupt status register(s) to wait for an event, rather than using the IRQ pin.

The polarity of all interrupts can be set by writing to the Configuration register (Reg 0x05), and it is possible to configure the IRQ pin to be open drain (if active low) or open source (if active high).

5.3.1 Wake Interrupt

When the $\overline{PD}$ pin is low, the oscillator is stopped. After $\overline{PD}$ is deasserted, the oscillator takes time to start, and until it has done so, it is not safe to use the SPI interface. The wake interrupt indicates that the oscillator has started, and that the device is ready to receive SPI transfers.

The wake interrupt is enabled by setting bit 0 of the Wake Enable register (Reg 0x1C, bit 0=1). Whether or not a wake interrupt is pending is indicated by the state of bit 0 of the Wake Status register (Reg 0x1D, bit 0). Reading the Wake Status register (Reg 0x1D) clears the interrupt.

5.3.2 Transmit Interrupts

Four interrupts are provided to flag the occurrence of transmit events. The interrupts are enabled by writing to the Transmit Interrupt Enable register (Reg 0x0D), and their status may be determined by reading the Transmit Interrupt Status register (Reg 0x0E). If more than 1 interrupt is enabled, it is necessary to read the Transmit Interrupt Status register (Reg 0x0E) to determine which event caused the IRQ pin to assert.

The function and operation of these interrupts are described in detail in *Section 7.0*.

5.3.3 Receive Interrupts

Eight interrupts are provided to flag the occurrence of receive events, four each for SERDES A and B. In 64 chips/bit and 32 chips/bit DDR modes, only the SERDES A interrupts are available, and the SERDES B interrupts will never trigger, even if enabled. The interrupts are enabled by writing to the Receive Interrupt Enable register (Reg 0x07), and their status may be determined by reading the Receive Interrupt Status register (Reg 0x08). If more than one interrupt is enabled, it is necessary to read the Receive Interrupt Status register (Reg 0x08) to determine which event caused the IRQ pin to assert.

The function and operation of these interrupts are described in detail in *Section 7.0*.

6.0 Application Examples

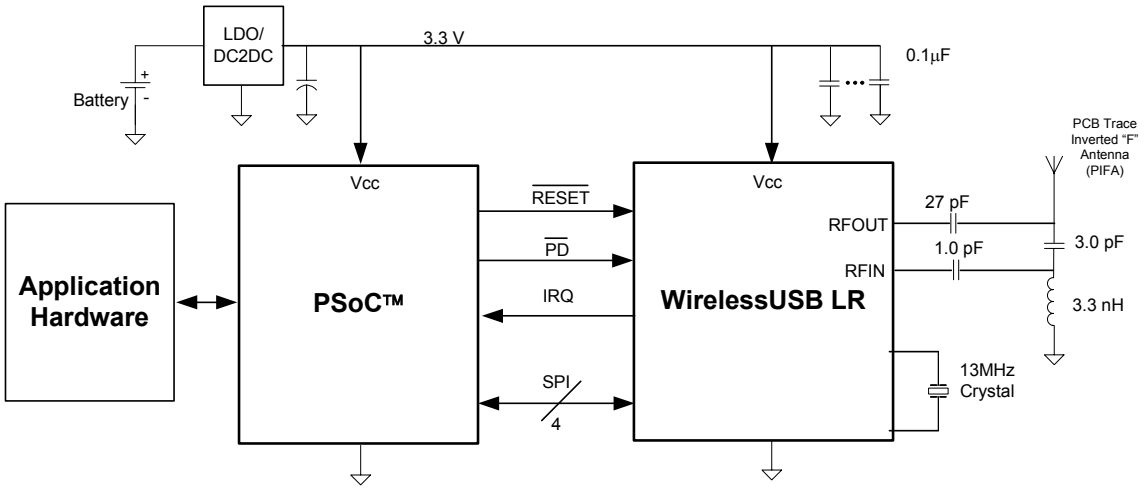

Figure 6-1. CYWUSB6935 Battery Powered Device

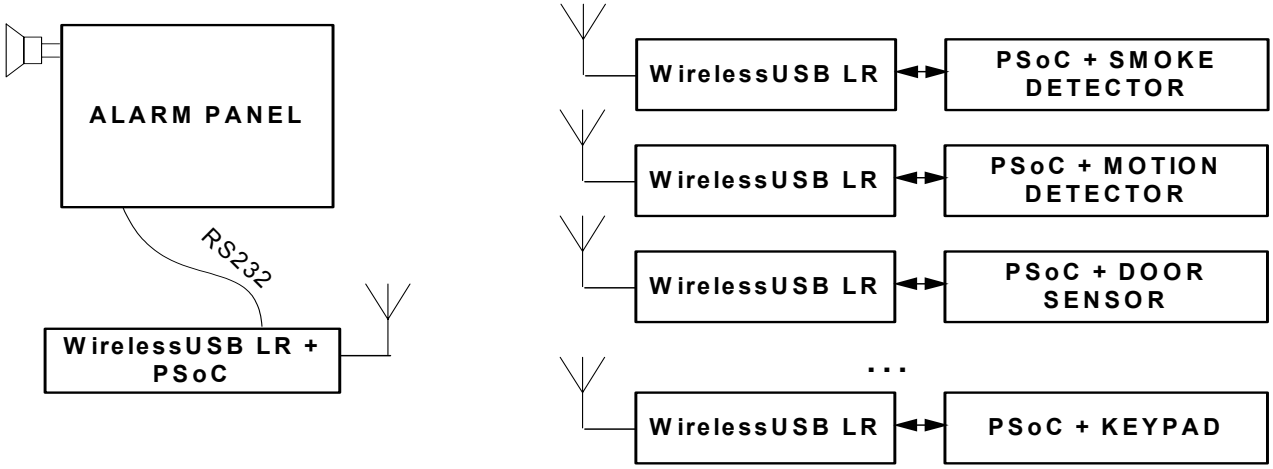

Figure 6-2. WirelessUSB LR Alarm System

7.0 Register Descriptions

Table 7-1 displays the list of registers inside the CYWUSB6935 that are addressable through the SPI interface. All registers are read and writable, except where noted.

Table 7-1. CYWUSB6935 Register Map[1]

Register Name	Mnemonic	CYWUSB6935 Address	Page	Default	Access
Revision ID	REG_ID	0x00	9	0x07	RO
Synthesizer A Counter	REG_SYN_A_CNT	0x01	8	0x00	RW
Synthesizer N Counter	REG_SYN_N_CNT	0x02	8	0x00	RW
Control	REG_CONTROL	0x03	9	0x00	RW
Data Rate	REG_DATA_RATE	0x04	10	0x00	RW
Configuration	REG_CONFIG	0x05	11	0x01	RW

Note:
1. All registers are accessed Little Endian.

Table 7-1. CYWUSB6935 Register Map[1]

Register Name	Mnemonic	CYWUSB6935 Address	Page	Default	Access
SERDES Control	REG_SERDES_CTL	0x06	11	0x03	RW
Receive Interrupt Enable	REG_RX_INT_EN	0x07	12	0x00	RW
Receive Interrupt Status	REG_RX_INT_STAT	0x08	13	0x00	RO
Receive Data A	REG_RX_DATA_A	0x09	14	0x00	RO
Receive Valid A	REG_RX_VALID_A	0x0A	14	0x00	RO
Receive Data B	REG_RX_DATA_B	0x0B	14	0x00	RO
Receive Valid B	REG_RX_VALID_B	0x0C	14	0x00	RO
Transmit Interrupt Enable	REG_TX_INT_EN	0x0D	15	0x00	RW
Transmit Interrupt Status	REG_TX_INT_STAT	0x0E	15	0x00	RO
Transmit Data	REG_TX_DATA	0x0F	16	0x00	RW
Transmit Valid	REG_TX_VALID	0x10	16	0x00	RW
PN Code	REG_PN_CODE	0x11–0x18	16	0x1E8B6A3DE0E9B222	RW
Threshold Low	REG_THRESHOLD_L	0x19	17	0x08	RW
Threshold High	REG_THRESHOLD_H	0x1A	17	0x38	RW
Wake Enable	REG_WAKE_EN	0x1C	18	0x00	RW
Wake Status	REG_WAKE_STAT	0x1D	18	0x01	RO
Analog Control	REG_ANALOG_CTL	0x20	18	0x04	RW
Channel	REG_CHANNEL	0x21	19	0x00	RW
Receive Signal Strength Indicator	REG_RSSI	0x22	19	0x00	RO
Power Control	REG_PA	0x23	19	0x00	RW
Crystal Adjust	REG_CRYSTAL_ADJ	0x24	20	0x00	RW
VCO Calibration	REG_VCO_CAL	0x26	20	0x00	RW
AGC Control	REG_AGC_CTL	0x2E	21	0x00	RW
Carrier Detect	REG_CARRIER_DETECT	0x2F	21	0x00	RW
Clock Manual	REG_CLOCK_MANUAL	0x32	21	0x00	RW
Clock Enable	REG_CLOCK_ENABLE	0x33	21	0x00	RW
Synthesizer Lock Count	REG_SYN_LOCK_CNT	0x38	22	0x64	RW
Manufacturing ID	REG_MID	0x3C–0x3F	22	–	RO

Addr: 0x00			REG_ID				Default: 0x07
7	6	5	4	3	2	1	0
Silicon ID				Product ID			

Figure 7-1. Revision ID Register

Bit	Name	Description
7:4	**Silicon ID**	These are the Silicon ID revision bits. 0000 = Rev A, 0001 = Rev B, etc. These bits are read-only.
3:0	**Product ID**	These are the Product ID revision bits. Fixed at value 0111. These bits are read-only.

Addr: 0x01			REG_SYN_A_CNT				Default: 0x00
7	6	5	4	3	2	1	0
Reserved			Count				

Figure 7-2. Synthesizer A Counter

Bit	Name	Description
7:5	Reserved	These bits are reserved and should be written with zeros.
4:0	Count	The Synthesizer A Counter register is used for diagnostic purposes and is not recommended for normal operation. The Channel register is the recommended method of setting the Synthesizer frequency. The Synthesizer A Count along with the Synthesizer N Count can be used to generate the Synthesizer frequency. The range of valid values of the Synthesizer A Count is 0 through 31. Using the Synthesizer A and N Count register is an alternative to using the Channel register. Selection between the use of the Channel register or the A and N registers is done through the Channel register (Reg 0x21, bit 7). When in Channel mode the A and N Count bits can be used to read the A and N values derived directly from the Channel.

Addr: 0x02			REG_SYN_N_CNT				Default: 0x00
7	6	5	4	3	2	1	0
Reserved	Count						

Figure 7-3. Synthesizer N Counter

Bit	Name	Description
7	Reserved	This bit is reserved and should be written with zero.
6:0	Count	The Synthesizer N Counter register is used for diagnostic purposes and therefore is not recommended for normal operation. The Channel register is the recommended method of setting the Synthesizer frequency. The Synthesizer N Count along with the Synthesizer A Count can be used to generate the Synthesizer frequency. The range of valid values of the Synthesizer N Count is 74 through 76. Using the Synthesizer A and N Count register is an alternative to using the Channel register. Selection between the use of the Channel register or the A and N registers is done through the Channel register (Reg 0x21, bit 7). When in Channel mode the A and N Count bits can be used to read the A and N values derived directly from the Channel.

Addr: 0x03			REG_CONTROL				Default: 0x00
7	6	5	4	3	2	1	0
RX Enable	TX Enable	PN Code Select	Auto Syn Count Select	Auto PA Disable	PA Enable	Auto Syn Disable	Syn Enable

Figure 7-4. Control

Bit	Name	Description
7	RX Enable	The Receive Enable bit is used to place the IC in receive mode. 1 = Receive Enabled 0 = Receive Disabled
6	TX Enable	The Transmit Enable bit is used to place the IC in transmit mode. 1 = Transmit Enabled 0 = Transmit Disabled
5	PN Code Select	The Pseudo-Noise Code Select bit selects between the upper or lower half of the 64 chips/bit PN code. 1 = 32 Most Significant Bits of PN code are used 0 = 32 Least Significant Bits of PN code are used This bit applies only when the Code Width bit is set to 32 chips/bit PN codes (Reg 0x04, bit 2=1).
4	Auto Syn Count Select	The Auto Synthesizer Count Select bit is used to select the method of determining the settle time of the synthesizer. The two options are a programmable settle time based on the value in Syn Lock Count register (Reg 0x38), in units of 2us, or by the auto detection of the synthesizer lock. 1 = Synthesizer settle time is based on a count in Syn Lock Count register (Reg 0x38) 0 = Synthesizer settle time is based on the internal synthesizer lock signal It is recommended that the Auto Syn Count Select bit is set to 1 as that guarantees a consistent settle time for the synthesizer.
3	Auto PA Disable	The Auto Power Amplifier Disable bit is used to determine the method of controlling the Power Amplifier. The two options are automatic control by the baseband or by firmware through register writes. 1 = Register controlled PA Enable. 0 = Auto PA Enable. When this bit is set to 1 the state of PA enable is directly controlled by bit PA Enable (Reg 0x03, bit 2). It is recommended that this bit is set to 0 leaving the PA control to the baseband.
2	PA Enable	The PA Enable bit is used to enable or disable the Power Amplifier. 1 = Power Amplifier Enabled 0 = Power Amplifier Disabled This bit only applies when the Auto PA Disable bit is selected (Reg 0x03, bit 3=1), otherwise this bit is don't care.
1	Auto Syn Disable	The Auto Synthesizer Disable bit is used to determine the method of controlling the Synthesizer. The two options are automatic control by the baseband or by firmware through register writes. 1 = Register controlled Synthesizer Enable. 0 = Auto Synthesizer Enable. When this bit is set to 1 the state of the Synthesizer is directly controlled by bit Syn Enable (Reg 0x03, bit 0). When this bit is set to 0 the state of the Synthesizer is controlled by the Auto Syn Count Select bit (Reg 0x03, bit 4). It is recommended that this bit is set to 0 leaving the Synthesizer control to the baseband.
0	Syn Enable	The Synthesizer Enable bit is used to enable or disable the Synthesizer. 1 = Synthesizer Enabled 0 = Synthesizer Disabled This bit only applies when Auto Syn Disable bit is selected (Reg 0x03, bit 1=1), otherwise this bit is don't care.

Addr: 0x04			REG_DATA_RATE				Default: 0x00
7	6	5	4	3	2	1	0
Reserved					Code Width	Data Rate	Sample Rate

Figure 7-5. Data Rate

Bit	Name	Description
7:3	Reserved	These bits are reserved and should be written with zeros.
2[2]	Code Width	The Code Width bit is used to select between 32 chips/bit and 64 chips/bit PN codes. 1 = 32 chips/bit PN codes 0 = 64 chips/bit PN codes The number of chips/bit used impacts a number of factors such as data throughput, range and robustness to interference. By choosing a 32 chips/bit PN-code, the data throughput can be doubled or even quadrupled (when double data rate is set). A 64 chips/bit PN code offers improved range over its 32 chips/bit counterpart as well as more robustness to interference. By selecting to use a 32 chips/bit PN code a number of other register bits are impacted and need to be addressed. These are PN Code Select (Reg 0x03, bit 5), Data Rate (Reg 0x04, bit 1), and Sample Rate (Reg 0x04, bit 0).
1[2]	Data Rate	The Data Rate bit allows the user to select Double Data Rate mode of operation which delivers a raw data rate of 62.5kbits/sec. 1 = Double Data Rate - 2 bits per PN code (No odd bit transmissions) 0 = Normal Data Rate - 1 bit per PN code This bit is applicable only when using 32 chips/bit PN codes which can be selected by setting the Code Width bit (Reg 0x04, bit 2=1). When using Double Data Rate, the raw data throughput is 62.5 kbits/sec because every 32 chips/bit PN code is interpreted as 2 bits of data. When using this mode a single 64 chips/bit PN code is placed in the PN code register. This 64 chips/bit PN code is then split into two and used by the baseband to offer the Double Data Rate capability. When using Normal Data Rate, the raw data throughput is 32kbits/sec. Additionally, Normal Data Rate enables the user to potentially correlate data using two differing 32 chips/bit PN codes.
0[2]	Sample Rate	The Sample Rate bit allows the use of the 12x sampling when using 32 chips/bit PN codes and Normal Data Rate. 1 = 12x Oversampling 0 = 6x Oversampling Using 12x oversampling improves the correlators receive sensitivity. When using 64 chips/bit PN codes or Double Data Rate this bit is don't care. When in the Normal Data Rate setting and choosing 12x oversampling, eliminates the ability to receive from two different PN codes. Therefore the only time when 12x oversampling is to be selected is when a 32 chips/bit PN code is being used and there is no need to receive data from sources with two different PN codes.

Note:
2. The following Reg 0x04, bits 2:0 values are not valid:
- 001–Not Valid
- 010–Not Valid
- 011–Not Valid

Addr: 0x05			REG_CONFIG			Default: 0x01	
7	6	5	4	3	2	1	0
Reserved			Receive Invert	Transmit Invert	Reserved	IRQ Pin Select	

Figure 7-6. Configuration

Bit	Name	Description
7:5	Reserved	These bits are reserved and should be written with zeros.
4	Receive Invert	The Receive Invert bit is used to invert the received data. 1 = Inverted over-the-air Receive data 0 = Non-inverted over-the-air Receive data
3	Transmit Invert	The Transmit Invert bit is used to invert the data that is to be transmitted. 1 = Inverted Transmit Data. 0 = Non-inverted Transmit Data.
2	Reserved	This bit is reserved and should be written with zero.
1:0	IRQ Pin Select	The Interrupt Request Pin Select bits are used to determine the drive method of the IRQ pin. 11 = Open Drain (asserted = 0, deasserted = Hi-Z) 10 = Open Source (asserted = 1, deasserted = Hi-Z) 01 = CMOS (asserted = 1, deasserted = 0) 00 = CMOS Inverted (asserted = 0, deasserted = 1)

Addr: 0x06			REG_SERDES_CTL			Default: 0x03	
7	6	5	4	3	2	1	0
Reserved				SERDES Enable	EOF Length		

Figure 7-7. SERDES Control

Bit	Name	Description
7:4	Reserved	These bits are reserved and should be written with zeros.
3	SERDES Enable	The SERDES Enable bit is used to switch between bit-serial mode and SERDES mode. 1 = SERDES enabled. 0 = SERDES disabled, bit-serial mode enabled. When the SERDES is enabled data can be written to and read from the IC one byte at a time, through the use of the SERDES Data registers. The bit-serial mode requires bits to be written one bit at a time through the use of the DIO/DIOVAL pins, refer to section 3.2. It is recommended that SERDES mode be used to avoid the need to manage the timing required by the bit-serial mode.
2:0	EOF Length	The End of Frame Length bits are used to set the number of sequential bit times for an inter-frame gap without valid data before an EOF event will be generated. When in receive mode and a valid bit has been received the EOF event can then be identified by the number of bit times that expire without correlating any new data. The EOF event causes data to be moved to the proper SERDES Data Register and can also be used to generate interrupts. If 0 is the EOF length, an EOF condition will occur at the first invalid bit after a valid reception.

Addr: 0x07			REG_RX_INT_EN				Default: 0x00
7	6	5	4	3	2	1	0
Underflow B	Overflow B	EOF B	Full B	Underflow A	Overflow A	EOF A	Full A

Figure 7-8. Receive Interrupt Enable

Bit	Name	Description
7	Underflow B	The Underflow B bit is used to enable the interrupt associated with an underflow condition with the Receive SERDES Data B register (Reg 0x0B) 1 = Underflow B interrupt enabled for Receive SERDES Data B 0 = Underflow B interrupt disabled for Receive SERDES Data B An underflow condition occurs when attempting to read the Receive SERDES Data B register (Reg 0x0B) when it is empty.
6	Overflow B	The Overflow B bit is used to enable the interrupt associated with an overflow condition with the Receive SERDES Data B register (Reg 0x0B) 1 = Overflow B interrupt enabled for Receive SERDES Data B 0 = Overflow B interrupt disabled for Receive SERDES Data B An overflow condition occurs when new received data is written into the Receive SERDES Data B register (Reg 0x0B) before the prior data is read out.
5	EOF B	The End of Frame B bit is used to enable the interrupt associated with the Channel B Receiver EOF condition. 1 = EOF B interrupt enabled for Channel B Receiver. 0 = EOF B interrupt disabled for Channel B Receiver. The EOF IRQ asserts during an End of Frame condition. End of Frame conditions occur after at least one bit has been detected, and then the number of invalid bits in the frame exceeds the number in the EOF length field. If 0 is the EOF length, and EOF condition will occur at the first invalid bit after a valid reception. This IRQ is cleared by reading the receive status register
4	Full B	The Full B bit is used to enable the interrupt associated with the Receive SERDES Data B register (Reg 0x0B) having data placed in it. 1 = Full B interrupt enabled for Receive SERDES Data B 0 = Full B interrupt disabled for Receive SERDES Data B A Full B condition occurs when data is transferred from the Channel B Receiver into the Receive SERDES Data B register (Reg 0x0B). This could occur when a complete byte is received or when an EOF event occurs whether or not a complete byte has been received.
3	Underflow A	The Underflow A bit is used to enable the interrupt associated with an underflow condition with the Receive SERDES Data A register (Reg 0x09) 1 = Underflow A interrupt enabled for Receive SERDES Data A 0 = Underflow A interrupt disabled for Receive SERDES Data A An underflow condition occurs when attempting to read the Receive SERDES Data A register (Reg 0x09) when it is empty.
2	Overflow A	The Overflow A bit is used to enable the interrupt associated with an overflow condition with the Receive SERDES Data A register (0x09) 1 = Overflow A interrupt enabled for Receive SERDES Data A 0 = Overflow A interrupt disabled for Receive SERDES Data A An overflow condition occurs when new receive data is written into the Receive SERDES Data A register (Reg 0x09) before the prior data is read out.
1	EOF A	The End of Frame A bit is used to enable the interrupt associated with an End of Frame condition with the Channel A Receiver. 1 = EOF A interrupt enabled for Channel A Receiver. 0 = EOF A interrupt disabled for Channel A Receiver. The EOF IRQ asserts during an End of Frame condition. End of Frame conditions occur after at least one bit has been detected, and then the number of invalid bits in a frame exceeds the number in the EOF length field. If 0 is the EOF length, an EOF condition will occur at the first invalid bit after a valid reception. This IRQ is cleared by reading the receive status register.
0	Full A	The Full A bit is used to enable the interrupt associated with the Receive SERDES Data A register (0x09) having data written into it. 1 = Full A interrupt enabled for Receive SERDES Data A 0 = Full A interrupt disabled for Receive SERDES Data A A Full A condition occurs when data is transferred from the Channel A Receiver into the Receive SERDES Data A register (Reg 0x09). This could occur when a complete byte is received or when an EOF event occurs whether or not a complete byte has been received.

Addr: 0x08			REG_RX_INT_STAT				Default: 0x00
7	6	5	4	3	2	1	0
Valid B	Flow Violation B	EOF B	Full B	Valid A	Flow Violation A	EOF A	Full A

Figure 7-9. Receive Interrupt Status[3]

Bit	Name	Description
7	Valid B	The Valid B bit is true when all the bits in the Receive SERDES Data B register (Reg 0x0B) are valid. 1 = All bits are valid for Receive SERDES Data B. 0 = Not all bits are valid for Receive SERDES Data B. When data is written into the Receive SERDES Data B register (Reg 0x0B) this bit is set if all of the bits within the byte that has been written are valid. This bit cannot generate an interrupt.
6	Flow Violation B	The Flow Violation B bit is used to signal whether an overflow or underflow condition has occurred for the Receive SERDES Data B register (Reg 0x0B). 1 = Overflow/underflow interrupt pending for Receive SERDES Data B. 0 = No overflow/underflow interrupt pending for Receive SERDES Data B. Overflow conditions occur when the radio loads new data into the Receive SERDES Data B register (Reg 0x0B) before the prior data has been read. Underflow conditions occur when trying to read the Receive SERDES Data B register (Reg 0x0B) when the register is empty. This bit is cleared by reading the Receive Interrupt Status register (Reg 0x08)
5	EOF B	The End of Frame B bit is used to signal whether an EOF event has occurred on the Channel B receive. 1 = EOF interrupt pending for Channel B. 0 = No EOF interrupt pending for Channel B. An EOF condition occurs for the Channel B Receiver when receive has begun and then the number of bit times specified in the SERDES Control register (Reg 0x06) elapse without any valid bits being received. This bit is cleared by reading the Receive Interrupt Status register (Reg 0x08)
4	Full B	The Full B bit is used to signal when the Receive SERDES Data B register (Reg 0x0B) is filled with data. 1 = Receive SERDES Data B full interrupt pending. 0 = No Receive SERDES Data B full interrupt pending. A Full B condition occurs when data is transferred from the Channel B Receiver into the Receive SERDES Data B register (Reg 0x0B). This could occur when a complete byte is received or when an EOF event occurs whether or not a complete byte has been received.
3	Valid A	The Valid A bit is true when all of the bits in the Receive SERDES Data A Register (Reg 0x09) are valid. 1 = All bits are valid for Receive SERDES Data A. 0 = Not all bits are valid for Receive SERDES Data A. When data is written into the Receive SERDES Data A register (Reg 0x09) this bit is set if all of the bits within the byte that has been written are valid. This bit cannot generate an interrupt.
2	Flow Violation A	The Flow Violation A bit is used to signal whether an overflow or underflow condition has occurred for the Receive SERDES Data A register (Reg 0x09). 1 = Overflow/underflow interrupt pending for Receive SERDES Data A. 0 = No overflow/underflow interrupt pending for Receive SERDES Data A. Overflow conditions occur when the radio loads new data into the Receive SERDES Data A register (Reg 0x09) before the prior data has been read. Underflow conditions occur when trying to read the Receive SERDES Data A register (Reg 0x09) when the register is empty. This bit is cleared by reading the Receive Interrupt Status register (Reg 0x08)
1	EOF A	The End of Frame A bit is used to signal whether an EOF event has occurred on the Channel A receive. 1 = EOF interrupt pending for Channel A. 0 = No EOF interrupt pending for Channel A. An EOF condition occurs for the Channel A Receiver when receive has begun and then the number of bit times specified in the SERDES Control register (0x06) elapse without any valid bits being received. This bit is cleared by reading the Receive Interrupt Status register (Reg 0x08).
0	Full A	The Full A bit is used to signal when the Receive SERDES Data A register (Reg 0x09) is filled with data. 1 = Receive SERDES Data A full interrupt pending. 0 = No Receive SERDES Data A full interrupt pending. A Full A condition occurs when data is transferred from the Channel A Receiver into the Receive SERDES Data A Register (Reg 0x09). This could occur when a complete byte is received or when an EOF event occurs whether or not a complete byte has been received.

Note:

3. All status bits are set and readable in the registers regardless of IRQ enable status. This allows a polling scheme to be implemented without enabling IRQs. The status bits are affected by TX Enable and RX Enable (Reg 0x03, bits 7:6). For example, the receive status will read 0 if the IC is not in receive mode. These register are read-only.

Addr: 0x09			REG_RX_DATA_A				Default: 0x00
7	6	5	4	3	2	1	0
Data							

Figure 7-10. Receive SERDES Data A

Bit	Name	Description
7:0	Data	Received Data for Channel A. The over-the-air received order is bit 0 followed by bit 1, followed by bit 2, followed by bit 3, followed by bit 4, followed by bit 5, followed by bit 6, followed by bit 7. This register is read-only.

Addr: 0x0A			REG_RX_VALID_A				Default: 0x00
7	6	5	4	3	2	1	0
Valid							

Figure 7-11. Receive SERDES Valid A

Bit	Name	Description
7:0	Valid	These bits indicate which of the bits in the Receive SERDES Data A register (Reg 0x09) are valid. A “1” indicates that the corresponding data bit is valid for Channel A. If the Valid Data bit is set in the Receive Interrupt Status register (Reg 0x08) all eight bits in the Receive SERDES Data A register (Reg 0x09) are valid. Therefore, it is not necessary to read the Receive SERDES Valid A register (Reg 0x0A). The over-the-air received order is bit 0 followed by bit 1, followed by bit 2, followed by bit 3, followed by bit 4, followed by bit 5, followed by bit 6, followed by bit 7. This register is read-only.

Addr: 0x0B			REG_RX_DATA_B				Default: 0x00
7	6	5	4	3	2	1	0
Data							

Figure 7-12. Receive SERDES Data B

Bit	Name	Description
7:0	Data	Received Data for Channel B. The over-the-air received order is bit 0 followed by bit 1, followed by bit 2, followed by bit 3, followed by bit 4, followed by bit 5, followed by bit 6, followed by bit 7. This register is read-only.

Addr: 0x0C			REG_RX_VALID_B				Default: 0x00
7	6	5	4	3	2	1	0
Valid							

Figure 7-13. Receive SERDES Valid B

Bit	Name	Description
7:0	Valid	These bits indicate which of the bits in the Receive SERDES Data B register (Reg 0x0B) are valid. A “1” indicates that the corresponding data bit is valid for Channel B. If the Valid Data bit is set in the Receive Interrupt Status register (0x08) all eight bits in the Receive SERDES Data B register (Reg 0x0B) are valid. Therefore, it is not necessary to read the Receive SERDES Valid B register (Reg 0x0C).The over-the-air received order is bit 0 followed by bit 1, followed by bit 2, followed by bit 3, followed by bit 4, followed by bit 5, followed by bit 6, followed by bit 7. This register is read-only.

Addr: 0x0D			REG_TX_INT_EN				Default: 0x00
7	6	5	4	3	2	1	0
Reserved				Underflow	Overflow	Done	Empty

Figure 7-14. Transmit Interrupt Enable

Bit	Name	Description
7:4	Reserved	These bits are reserved and should be written with zeros.
3	Underflow	The Underflow bit is used to enable the interrupt associated with an underflow condition associated with the Transmit SERDES Data register (Reg 0x0F) 1 = Underflow interrupt enabled. 0 = Underflow interrupt disabled. An underflow condition occurs when attempting to transmit while the Transmit SERDES Data register (Reg 0x0F) does not have any data.
2	Overflow	The Overflow bit is used to enabled the interrupt associated with an overflow condition with the Transmit SERDES Data register (0x0F). 1 = Overflow interrupt enabled. 0 = Overflow interrupt disabled. An overflow condition occurs when attempting to write new data to the Transmit SERDES Data register (Reg 0x0F) before the preceding data has been transferred to the transmit shift register.
1	Done	The Done bit is used to enable the interrupt that signals the end of the transmission of data. 1 = Done interrupt enabled. 0 = Done interrupt disabled. The Done condition occurs when the Transmit SERDES Data register (Reg 0x0F) has transmitted all of its data and there is no more data for it to transmit.
0	Empty	The Empty bit is used to enable the interrupt that signals when the Transmit SERDES register (Reg 0x0F) is empty. 1 = Empty interrupt enabled. 0 = Empty interrupt disabled. The Empty condition occurs when the Transmit SERDES Data register (Reg 0x0F) is loaded into the transmit buffer and it's safe to load the next byte

Addr: 0x0E			REG_TX_INT_STAT				Default: 0x00
7	6	5	4	3	2	1	0
Reserved				Underflow	Overflow	Done	Empty

Figure 7-15. Transmit Interrupt Status[4]

Bit	Name	Description
7:4	Reserved	These bits are reserved. This register is read-only.
3	Underflow	The Underflow bit is used to signal when an underflow condition associated with the Transmit SERDES Data register (Reg 0x0F) has occurred. 1 = Underflow Interrupt pending. 0 = No Underflow Interrupt pending. This IRQ will assert during an underflow condition to the Transmit SERDES Data register (Reg 0x0F). An underflow occurs when the transmitter is ready to sample transmit data, but there is no data ready in the Transmit SERDES Data register (Reg 0x0F). This will only assert after the transmitter has transmitted at least one bit. This bit is cleared by reading the Transmit Interrupt Status register (Reg 0x0E).
2	Overflow	The Overflow bit is used to signal when an overflow condition associated with the Transmit SERDES Data register (0x0F) has occurred. 1 = Overflow Interrupt pending. 0 = No Overflow Interrupt pending. This IRQ will assert during an overflow condition to the Transmit SERDES Data register (Reg 0x0F). An overflow occurs when the new data is loaded into the Transmit SERDES Data register (Reg 0x0F) before the previous data has been sent. This bit is cleared by reading the Transmit Interrupt Status register (Reg 0x0E).
1	Done	The Done bit is used to signal the end of a data transmission. 1 = Done Interrupt pending. 0 = No Done Interrupt pending. This IRQ will assert when the data is finished sending a byte of data and there is no more data to be sent. This will only assert after the transmitter has transmitted as least one bit. This bit is cleared by reading the Transmit Interrupt Status register (Reg 0x0E)
0	Empty	The Empty bit is used to signal when the Transmit SERDES Data register (Reg 0x0F) has been emptied. 1 = Empty Interrupt pending. 0 = No Empty Interrupt pending. This IRQ will assert when the transmit serdes is empty. When this IRQ is asserted it is ok to write to the Transmit SERDES Data register (Reg 0x0F). Writing the Transmit SERDES Data register (Reg 0x0F) will clear this IRQ. It will be set when the data is loaded into the transmitter, and it is ok to write new data.

Note:

4. All status bits are set and readable in the registers regardless of IRQ enable status. This allows a polling scheme to be implemented without enabling IRQs. The status bits are affected by the TX Enable and RX Enable (Reg 0x03, bits 7:6). For example, the transmit status will read 0 if the IC is not in transmit mode. These registers are read-only.

Addr: 0x0F			REG_TX_DATA				Default: 0x00
7	6	5	4	3	2	1	0
Data							

Figure 7-16. Transmit SERDES Data

Bit	Name	Description
7:0	Data	Transmit Data. The over-the-air transmitted order is bit 0 followed by bit 1, followed by bit 2, followed by bit 3, followed by bit 4, followed by bit 5, followed by bit 6, followed by bit 7.

Addr: 0x10			REG_TX_VALID				Default: 0x00
7	6	5	4	3	2	1	0
Valid							

Figure 7-17. Transmit SERDES Valid

Bit	Name	Description
7:0	Valid[5]	The Valid bits are used to determine which of the bits in the Transmit SERDES Data register (reg 0x0F) are valid. 1 = Valid transmit bit. 0 = Invalid transmit bit.

Addr: 0x11-18								REG_PN_CODE																Default: 0x1E8B6A3DE0E9B222							
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Address 0x18								Address 0x17								Address 0x16								Address 0x15							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address 0x14								Address 0x13								Address 0x12								Address 0x11							

Figure 7-18. PN Code

Bit	Name	Description
63:0	PN Codes	The value inside the 8 byte PN code register is used as the spreading code for DSSS communication. All 8 bytes can be used together for 64 chips/bit PN code communication, or the registers can be split into two sets of 32 chips/bit PN codes and these can be used alone or with each other to accomplish faster data rates. Not any 64 chips/bit value can be used as a PN code as there are certain characteristics that are needed to minimize the possibility of multiple PN codes interfering with each other or the possibility of invalid correlation. The over-the-air order is bit 0 followed by bit 1... followed by bit 62, followed by bit 63.

Note:

5. Note: The Valid bit in the Transmit SERDES Valid register (Reg 0x10) is used to mark whether the radio will send data or preamble during that bit time of the data byte. Data is sent LSB first. The SERDES will continue to send data until there are no more VALID bits in the shifter. For example, writing 0x0F to the Transmit SERDES Valid register (Reg 0x10) will send half a byte.

Addr: 0x19			REG_THRESHOLD_L				Default: 0x08
7	6	5	4	3	2	1	0
Reserved	Threshold Low						

Figure 7-19. Threshold Low

Bit	Name	Description
7	Reserved	This bit is reserved and should be written with zero.
6:0	Threshold Low	The Threshold Low value is used to determine the number of missed chips allowed when attempting to correlate a single data bit of value ‘0’. A perfect reception of a data bit of ‘0’ with a 64 chips/bit PN code would result in zero correlation matches, meaning the exact inverse of the PN code has been received. By setting the Threshold Low value to 0x08 for example, up to eight chips can be erroneous while still identifying the value of the received data bit. This value along with the Threshold High value determine the correlator count values for logic ‘1’ and logic ‘0’. The threshold values used determine the sensitivity of the receiver to interference and the dependability of the received data. By allowing a minimal number of erroneous chips the dependability of the received data increases while the robustness to interference decreases. On the other hand increasing the maximum number of missed chips means reduced data integrity but increased robustness to interference and increased range.

Addr: 0x1A			REG_THRESHOLD_H				Default: 0x38
7	6	5	4	3	2	1	0
Reserved	Threshold High						

Figure 7-20. Threshold High

Bit	Name	Description
7	Reserved	This bit is reserved and should be written with zero.
6:0	Threshold High	The Threshold High value is used to determine the number of matched chips allowed when attempting to correlate a single data bit of value ‘1’. A perfect reception of a data bit of ‘1’ with a 64 chips/bit or a 32 chips/bit PN code would result in 64 chips/bit or 32 chips/bit correlation matches, respectively, meaning every bit was received perfectly. By setting the Threshold High value to 0x38 (64-8) for example, up to eight chips can be erroneous while still identifying the value of the received data bit. This value along with the Threshold Low value determine the correlator count values for logic ‘1’ and logic ‘0’. The threshold values used determine the sensitivity of the receiver to interference and the dependability of the received data. By allowing a minimal number of erroneous chips the dependability of the received data increases while the robustness to interference decreases. On the other hand increasing the maximum number of missed chips means reduced data integrity but increased robustness to interference and increased range.

Addr: 0x1C			REG_WAKE_EN				Default: 0x00
7	6	5	4	3	2	1	0
Reserved							Wakeup Enable

Figure 7-21. Wake Enable

Bit	Name	Description
7:1	Reserved	These bits are reserved and should be written with zeros.
0	Wakeup Enable	Wakeup interrupt enable. 0 = disabled 1 = enabled A wakeup event is triggered when the $\overline{PD}$ pin is deasserted and once the IC is ready to receive SPI communications.

Addr: 0x1D			REG_WAKE_STAT				Default: 0x01
7	6	5	4	3	2	1	0
Reserved							Wakeup Status

Figure 7-22. Wake Status

Bit	Name	Description
7:1	Reserved	These bits are reserved. This register is read-only.
0	Wakeup Status	Wakeup status. 0 = Wake interrupt not pending 1 = Wake interrupt pending This IRQ will assert when a wakeup condition occurs. This bit is cleared by reading the Wake Status register (Reg 0x1D). This register is read-only.

Addr: 0x20			REG_ANALOG_CTL				Default: 0x00
7	6	5	4	3	2	1	0
Reserved	AGC Disable	MID Read Enable	Reserved	Reserved	PA Output Enable	PaInv	Rst

Figure 7-23. Analog Control

Bit	Name	Description
7	Reserved	This bit is reserved and should be written with zero.
6	AGC RSSI Control	Enables AGC/RSSI control via Reg 0x2E and Reg 0x2F.
5	MID Read Enable	The MID Read Enable bit must be set to read the contents of the Manufacturing ID register (Reg 0x3C-0x3F). Enabling the Manufacturing ID register (Reg 0x3C-0x3F) consumes power. This bit should only be set when reading the contents of the Manufacturing ID register (Reg 0x3C-0x3F).
4:3	Reserved	These bits are reserved and should be written with zeros.
2	PA Output Enable	The Power Amplifier Output Enable bit is used to enable the PACTL pin for control of an external power amplifier. 1 = PA Control Output Enabled on PACTL pin. 0 = PA Control Output Disabled on PACTL pin.
1	PA Invert	The Power Amplifier Invert bit is used to specify the polarity of the PACTL signal when the PaOe bit is set high. PA Output Enable and PA Invert cannot be simultaneously changed. 1 = PACTL active low 0 = PACTL active high
0	Reset	The Reset bit is used to generate a self clearing device reset. 1 = Device Reset. All registers are restored to their default values. 0 = No Device Reset.

Addr: 0x21			REG_CHANNEL				Default: 0x00
7	6	5	4	3	2	1	0
A+N	Channel						

Figure 7-24. Channel

Bit	Name	Description
7	A+N	The A+N bit is used to specify whether the Synthesizer frequency is generated through the use of the Channel register (Reg 0x21) or through the use of the Synthesizer A Counter register (Reg 0x01) and the Synthesizer N Counter register (Reg 0x02). 1 = Synthesizer A Counter register (Reg 0x01) and the Synthesizer N Counter register (Reg 0x02) registers used to generate Synthesizer frequency. 0 = Channel register (Reg 0x21) is used to generate Synthesizer frequency. When set to 1 the channel value is ignored and the values written in the Synthesizer A Counter register (Reg 0x01) and the Synthesizer N Counter register (Reg 0x02) are used. When set to 0 the values written to the Synthesizer A Counter register (Reg 0x01) and the Synthesizer N Counter register (Reg 0x02) are ignored and the channel value is used by the synthesizer. It is recommended that the Channel register (Reg 0x21) is used as opposed to the Synthesizer A Counter register (Reg 0x01) and the Synthesizer N Counter register (Reg 0x02) method.
6:0	Channel	The Channel register (Reg 0x21) is used to determine the Synthesizer frequency when the A+N bit is set to 0. Use of other channels may be restricted by certain regulatory agencies. A value of 1 corresponds to a communication frequency of 2.402 GHz, while a value of 79 corresponds to a frequency of 2.479GHz. The channels are separated from each other by 1 MHz intervals.

Addr: 0x22			REG_RSSI				Default: 0x00
7	6	5	4	3	2	1	0
Reserved		Valid	RSSI				

Figure 7-25. Receive Signal Strength Indicator (RSSI)[6]

Bit	Name	Description
7:6	Reserved	These bits are reserved. This register is read-only.
5	Valid	The Valid bit indicates whether the RSSI value in bits [4:0] are valid. This register is Read Only. 1 = RSSI value is valid 0 = RSSI value is invalid
4:0	RSSI	The Receive Strength Signal Indicator (RSSI) value indicates the strength of the received signal. This is a read only value with the higher values indicating stronger received signals meaning more reliable transmissions.

Addr: 0x23			REG_PA				Default: 0x00
7	6	5	4	3	2	1	0
Reserved					PA Bias		

Figure 7-26. Power Control

Bit	Name	Description
7:3	Reserved	These bits are reserved and should be written with zeros.
2:0	PA Bias	The Power Amplifier Bias (PA Bias) bits are used to set the transmit power of the IC through increasing (values up to 7) or decreasing (values down to 0) the gain of the on-chip Power Amplifier. The higher the register value the higher the transmit power. By changing the PA Bias value signal strength management functions can be accomplished. For general purpose communication a value of 7 is recommended.

Note:
6. The RSSI will collect a single value each time the part is put into receive mode via Control register (Reg 0x03, bit 7=1).

Addr: 0x24		REG_CRYSTAL_ADJ					Default: 0x00
7	6	5	4	3	2	1	0
Reserved	Clock Output Disable	Crystal Adjust					

Figure 7-27. Crystal Adjust

Bit	Name	Description
7	Reserved	This bit is reserved and should be written with zero.
6	Clock Output Disable	The Clock Output Disable bit disables the 13 MHz clock driven on the X13OUT pin. 1 = No 13 MHz clock driven externally. 0 = 13 MHz clock driven externally. If the 13 MHz clock is driven on the X13OUT pin then receive sensitivity will be reduced by -4 dBm on channels 5+13*n*. By default the 13 MHz clock output pin is enabled. This pin is useful for adjusting the 13 MHz clock, but it interfere with every 13th channel beginning with 2.405GHz channel. Therefore, it is recommended that the 13 MHz clock output pin be disabled when not in use.
5:0	Crystal Adjust	The Crystal Adjust value is used to calibrate the on-chip load capacitance supplied to the crystal. The Crystal Adjust value will depend on the parameters of the crystal being used. Refer to the appropriate reference material for information about choosing the optimum Crystal Adjust value.

Addr: 0x26		REG_VCO_CAL					Default: 0x00
7	6	5	4	3	2	1	0
VCO Slope Enable		Reserved					

Figure 7-28. VCO Calibration

Bit	Name	Description
7:6	VCO Slope Enable (Write-Only)	The Voltage Controlled Oscillator (VCO) Slope Enable bits are used to specify the amount of variance automatically added to the VCO. 11 = -5/+5 VCO adjust. The application MCU must configure this option during initialization. 10 = -2/+3 VCO adjust. 01 = Reserved. 00 = No VCO adjust. These bits are undefined for read operations.
5:0	Reserved	These bits are reserved and should be written with zeros.

Addr: 0x2E			REG_AGC_CTL				Default: 0x00
7	6	5	4	3	2	1	0
AGC Lock	Reserved						

Figure 7-29. AGC Control

Bit	Name	Description
7	AGC Lock	When set, this bit disables the on-chip LNA AGC system, powers down unused circuitry, and locks the LNA to maximum gain. The user must set Reg 20, bit 6=1 to enable writes to Reg 0x2E. It is recommended to set this bit during initialization to save power.
6:0	Reserved	These bits are reserved and should be written with zeros.

Addr: 0x2F			REG_CARRIER_DETECT				Default: 0x00
7	6	5	4	3	2	1	0
Carrier Detect Override	Reserved						

Figure 7-30. Carrier Detect

Bit	Name	Description
7	Carrier Detect Override	When set, this bit overrides carrier detect. The user must set Reg 20, bit 6=1 to enable writes to Reg 0x2F.
6:0	Reserved	These bits are reserved and should be written with zeros.

Addr: 0x32			REG_CLOCK_MANUAL				Default: 0x00
7	6	5	4	3	2	1	0
Manual Clock Overrides							

Figure 7-31. Clock Manual

Bit	Name	Description
7:0	Manual Clock Overrides	This register must be written with 0x41 after reset for correct operation

Addr: 0x33			REG_CLOCK_ENABLE				Default: 0x00
7	6	5	4	3	2	1	0
Manual Clock Enables							

Figure 7-32. Clock Enable

Bit	Name	Description
7:0	Manual Clock Enables	This register must be written with 0x41 after reset for correct operation

Addr: 0x38			REG_SYN_LOCK_CNT				Default: 0x64
7	6	5	4	3	2	1	0
Count							

Figure 7-33. Synthesizer Lock Count

Bit	Name	Description
7:0	Count	Determines the length of delay in 2µs increments for the synthesizer to lock when auto synthesizer is enabled via Control register (0x03, bit 1=0) and not using the PLL lock signal.

Addr: 0x3C-3F								REG_MID																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address 0x3F								Address 0x3E								Address 0x3D								Address 0x3C							

Figure 7-34. Manufacturing ID

Bit	Name	Description
31:0	Address[31:0]	These bits are the Manufacturing ID (MID) for each IC. The contents of these bits cannot be read unless the MID Read Enable bit (bit 5) is set in the Analog Control register (Reg 0x20). Enabling the Manufacturing ID register (Reg 0x3C-0x3F) consumes power. The MID Read Enable bit in the Analog Control register (Reg 0x20, bit 5) should only be set when reading the contents of the Manufacturing ID register (Reg 0x3C-0x3F). This register is read-only.

8.0 Pin Descriptions

Table 8-1. Pin Description Table

Pin SOIC	Pin QFN	Name	Type	Default	Description
Analog RF					
3	46	RFIN	Input	Input	**RF Input**. Modulated RF signal received.
6	5	RFOUT	Output	N/A	**RF Output**. Modulated RF signal to be transmitted.
Crystal / Power Control					
26	38	X13	Input	N/A	**Crystal Input**. (refer to *Section 4.6*).
25	35	X13IN	Input	N/A	**Crystal Input**. (refer to *Section 4.6*).
19	26	X13OUT	Output /Hi-Z	Output	**System Clock**. Buffered 13-MHz system clock.
23	33	$\overline{PD}$	Input	N/A	**Power Down**. Asserting this input (low), will put the IC in the Suspend Mode (X13OUT is 0 when $\overline{PD}$ is Low).
10	14	$\overline{RESET}$	Input	N/A	**Active LOW Reset**. Device reset.
24	34	PACTL	I/O	Input	**PACTL**. External Power Amplifier control. Pull-down or make output.
SERDES Bypass Mode Communications/Interrupt					
13	20	DIO	I/O	Input	**Data Input/Output.** SERDES Bypass Mode Data Transmit/Receive.
12	19	DIOVAL	I/O	Input	**Data I/O Valid**. SERDES Bypass Mode Data Transmit/Receive Valid.
14	21	IRQ	Output /Hi-Z	Output	**IRQ**. Interrupt and SERDES Bypass Mode DIOCLK.
SPI Communications					
16	23	MOSI	Input	N/A	**Master-Output-Slave-Input Data**. SPI data input pin.
17	24	MISO	Output /Hi-Z	Hi-Z	**Master-Input-Slave-Output Data**. SPI data output pin.
18	25	SCK	Input	N/A	**SPI Input Clock**. SPI clock.
15	22	$\overline{SS}$	Input	N/A	**Slave Select Enable**. SPI enable.
Power and Ground					
2, 7, 8, 11, 20, 21, 22, 27, 28	6, 9, 16, 28, 29, 32, 41, 42, 45	VCC	VCC	H	V_{CC} = 2.7V to 3.6V.
1	44	AVCC	AVCC	H	Vcc = 2.7V to 3.6V. (Decouple separately from VCC pins)
9	13	GND	GND	L	**Ground = 0V**.
4, 5	1, 2, 3, 4, 7, 8, 10, 11, 12, 15, 17, 18, 27, 30, 31, 36, 37, 39, 40, 43, 47, 48	NC	N/A	N/A	Tie to Ground.
Exposed paddle		GND	GND	L	Must be tied to Ground.

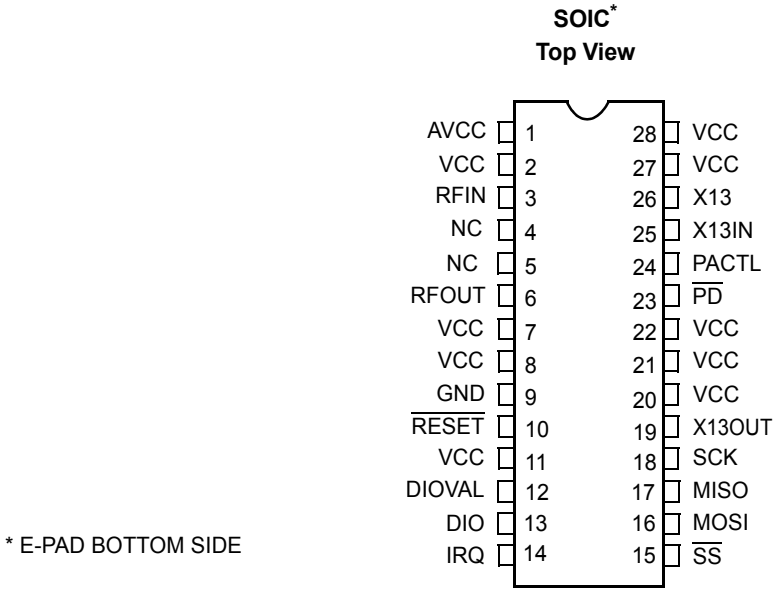

Figure 8-1. CYWUSB6935, 28 SOIC – Top View

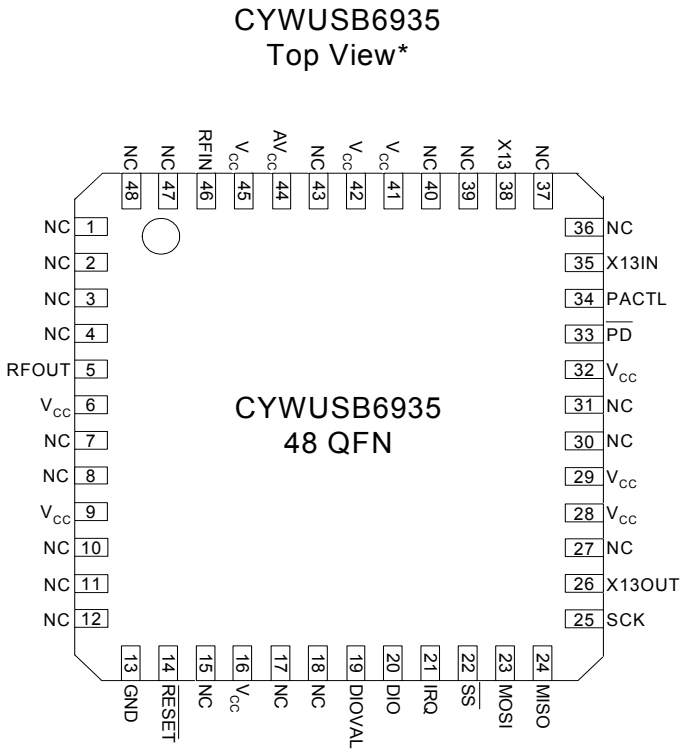

Figure 8-2. CYWUSB6935, 48 QFN – Top View

9.0 Absolute Maximum Ratings

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied .. –55°C to +125°C
Supply Voltage on V_{CC} relative to VSS..... –0.3V to +3.9V
DC Voltage to Logic Inputs[7] ..... –0.3V to V_{CC} +0.3V
DC Voltage applied to Outputs in High-Z State..... –0.3V to V_{CC} +0.3V
Static Discharge Voltage (Digital).....>2000V
Static Discharge Voltage (RF)[8]..... 500V
Latch-up Current..... +200 mA, –200 mA

10.0 Operating Conditions

V_{CC} (Supply Voltage).....2.7V to 3.6V
T_A (Ambient Temperature Under Bias)..... -40°C to +85°C
Ground Voltage 0V
F_{OSC} (Oscillator or Crystal Frequency) ..... 13 MHz

11.0 DC Characteristics (over the operating range)

Table 11-1. DC Parameters

Parameter	Description	Conditions	Min.	Typ.[10]	Max.	Unit
V_{CC}	Supply Voltage		2.7	3.0	3.6	V
V_{OH1}	Output High Voltage condition 1	At I_{OH} = –100.0µA	V_{CC}–0.1	V_{CC}		V
V_{OH2}	Output High Voltage condition 2	At I_{OH} = –2.0 mA	2.4	3.0		V
V_{OL}	Output Low Voltage	At I_{OL} = 2.0 mA		0.0	0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}[9]	V
V_{IL}	Input Low Voltage		–0.3		0.8	V
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CC}$	–1	0.26	+1	µA
C_{IN}	Pin Input Capacitance (except X13, X13IN, RFIN)			3.5	10	pF
I_{Sleep}	Current consumption during power-down mode	$\overline{PD}$ = LOW		0.24	10	µA
IDLE I_{CC}	Current consumption without synthesizer	$\overline{PD}$ = HIGH		3		mA
STARTUP I_{CC}	ICC from $\overline{PD}$ high to oscillator stable.			1.8		mA
TX AVG I_{CC1}	Average transmitter current consumption[11]	no handshake		5.9		mA
TX AVG I_{CC2}	Average transmitter current consumption[12]	with handshaking		8.1		mA
RX $I_{CC\ (PEAK)}$	Current consumption during receive			57.7		mA
TX $I_{CC\ (PEAK)}$	Current consumption during transmit			69.1		mA
SYNTH SETTLE I_{CC}	Current consumption with Synthesizer on, No Transmit or Receive			28.7		mA

Notes:
7. It is permissible to connect voltages above Vcc to inputs through a series resistor limiting input current to 1 mA. This can't be done during power down mode. AC timing not guaranteed.
8. Human Body Model (HBM).
9. It is permissible to connect voltages above Vcc to inputs through a series resistor limiting input current to 1 mA.
10. Typ. values measured with Vcc = 3.0V @ 25°C
11. Average Icc when transmitting a 5-byte packet (3 data bytes + 2 bytes of protocol) every 10ms using the WirelessUSB 1-way protocol.
12. Average Icc when transmitting a 5-byte packet (3 data bytes + 2 bytes of protocol) every 10ms using the WirelessUSB 2-way protocol.