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Intelligent Digital Amplifier and Sound Processor

D2-926xx

The D2-926xx family of the DAE-3™ and DAE-3HT™ Digital Audio Engine™ devices are complete System-on Chip (SoC) multi-channel digital sound processors and Class-D amplifier controllers.

The integrated DSP provides efficient and configurable audio signal path processing including equalization, dynamic range compression, mixing, and filtering that is completely configurable via the Audio Canvas™ III high level programming interface. The integrated PWM engine supports programmable and dynamic control of audio output, enabling a variety of multi-channel output configurations and output power capacity. Internal noise shaping, an embedded asynchronous sample rate converter, dynamic level-dependent timing, and high resolution operation supports power stage audio performances with SNR >110dB and THD+N < 0.01%.

The D2-926xx devices are provided in two package and feature configurations which include the 128-pin DAE-3, and the72-pin DAE-3HT. Both the DAE-3 and DAE-3HT provide identical performance and enable an extremely flexible platform for feature rich and cost-affordable quality audio solutions, which benefit from the addition of Class-D amplifiers and DSP audio processing.

The 12 integrated digital PWM controllers can be used in a variety of multi-channel audio system configurations, supporting powered as well as line outputs. Fully protected amplifier control provides efficient and clean Class-D power output support.

Applications

- DTV and Blu-ray Soundbar
- DVD and Blu-ray Home Theater Systems
- Home Theater in a Box (HTiB)
- Audio Video Receiver (AVR)
- Multi-Channel Multi-Media (MM) Systems
- Multi-Room Distributed Audio (MRDA)
- Powered Speaker Systems
- Automotive Trunk/Amplified Solutions

Features

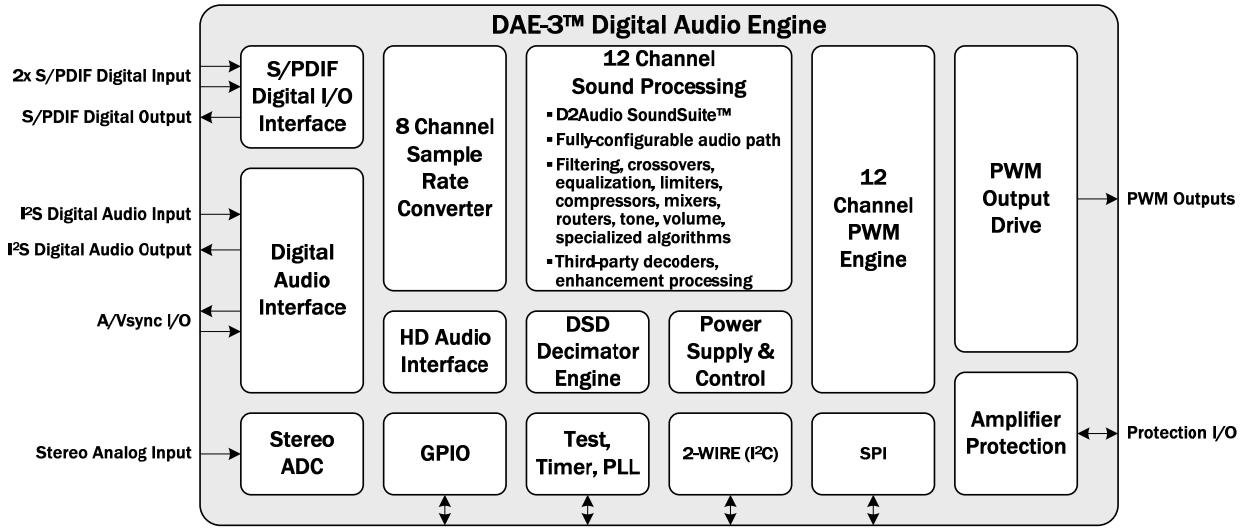
- Advanced DAE-3™ Digital Audio Engine™ IC Family
  - DAE-3™ Pin Compatible and Function/Feature Compatible with the D2Audio™ DAE-6™ Device Family
  - DAE-3HT™ - Identical DAE-3 performance, in 72-QFN package
- Integrated DSP Digital Sound Processing
  - Customizable audio path sound processing
  - Fully configurable and routable audio signal paths and hardware function assignment
  - Fully Supported with Audio Canvas™ III Design Tool
- Flexible Audio Input and Output Configurations
  - 12 Independent PWM Engine Channels
  - 4 Independent Asynchronous I^2S Digital Inputs
  - Integrated high-performance stereo ADC (DAE-3 only)
  - S/PDIF™ Digital Audio Inputs supporting Linear IEC-61958 PCM or Compressed IEC-61937 Audio
  - S/PDIF Digital Audio PCM Output
- Embedded 8-Channel Sample Rate Converter
- Real-Time Amplifier Control and Monitoring
  - Supports Bridged, Half-Bridged, and Bridge-Tied Load (BTL) Topologies, Using Discrete or Integrated Power Stages
  - Complete Fault Protection with Automatic Recovery
- D2Audio™ SoundSuite™ Enhancement and Virtualization
- Enhanced Audio Processing Decoders And Virtualization
  - Dolby® Digital/AC3
  - Dolby® Pro Logic IIx
  - Dolby® Virtual Speaker
  - DTS®(SRS) TruSurround HD4™ , DTS®(SRS) WOW HD™, DTS®(SRS) TruVolume™

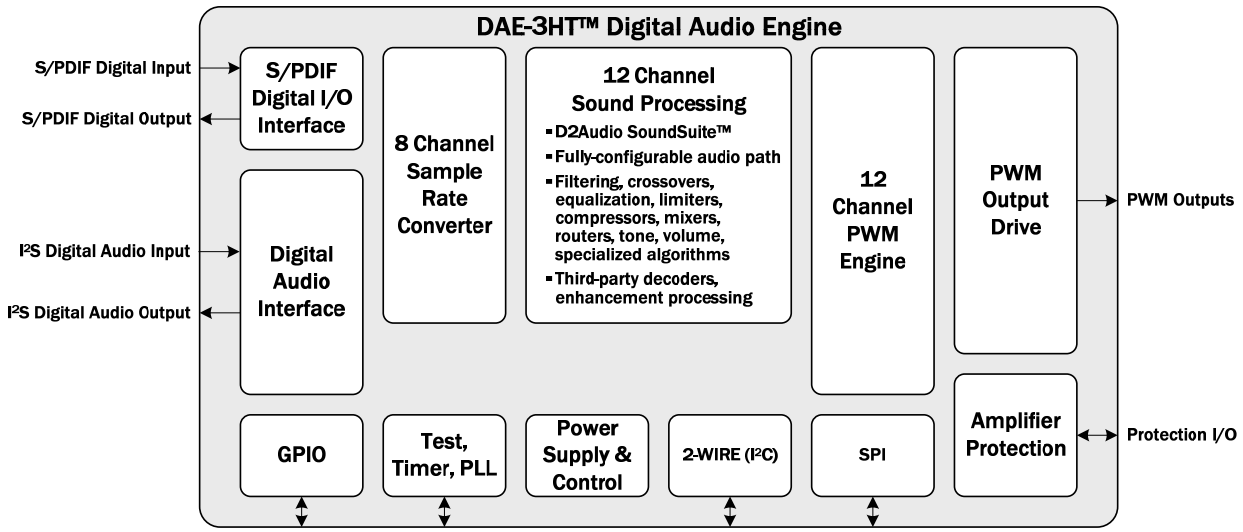
Ordering Information

PART NUMBER (Notes 3, 4)	DAE DEVICE FAMILY	PART MARKING	AUDIO PROCESSING FEATURE SET SUPPORT (Note 1)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
D2-92633-LR	DAE-3	D2-92633-LR	Refer to Table 1	-10 to +85	128 Ld LQFP	Q128.14x14
D2-92634-LR	DAE-3	D2-92634-LR	Refer to Table 1	-10 to +85	128 Ld LQFP	Q128.14x14
D2-92683-QR (Note 2)	DAE-3HT	D2-92683-QR	Refer to Table 1	-10 to +85	72 Ld QFN	L72.10x10F
D2-92684-QR (Note 2)	DAE-3HT	D2-92684-QR	Refer to Table 1	-10 to +85	72 Ld QFN	L72.10x10F

NOTES:

1. The D2-926xx devices support multiple audio processing algorithms and decoders, and support is device-dependent. Refer to Table 1 on page 3 for the supported features for each device part number.
2. Add "-T" suffix for 3k unit Tape and Reel option. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see product information page for D2-92633, D2-92634, D2-92683, D2-92684. For more information on MSL, please see tech brief TB363.





DAE-3 Device Feature Set Offering

The D2-926xx family has specific part numbers to specify the features and algorithms supported in the device. All devices of the DAE-3 family include 8 audio input processing channels, up to 12 PWM output channels, an embedded 8-channel Sample Rate Converter (SRC), and are fully supported with the Audio Canvas III™ design tool software. Additional features within each DAE-3 family part number are shown in Table 1.

TABLE 1. DAE-3 DEVICE PART NUMBERS AND FEATURES

PART NUMBER	DAE FAMILY	FEATURES	LICENSED ALGORITHM SUPPORT (Note 5)
D2-92633-LR	DAE-3 128-Pin Package	8 Channels of I^2S or Left Justified Serial Digital Audio Inputs 8 Channels of I^2S or Left Justified Serial Digital Audio Outputs 2 S/PDIF Digital Inputs 1 S/PDIF Digital Output 2 ADC Analog Audio Inputs	D2Audio™ SoundSuite™ DTS®(SRS) TruSurround HD4™ DTS®(SRS) WOWHD4™ DTS®(SRS) TruVolume™
D2-92634-LR	DAE-3 128-Pin Package	8 Channels of I^2S or Left Justified Serial Digital Audio Inputs 8 Channels of I^2S or Left Justified Serial Digital Audio Outputs 2 S/PDIF Digital Inputs 1 S/PDIF Digital Output 2 ADC Analog Audio Inputs	D2Audio™ SoundSuite™ Dolby® Digital/AC3 Decoder Dolby® Pro Logic IIx Surround
D2-92683-QR	DAE-3HT 72-Pin Package	8 Channels of I^2S or Left Justified Serial Digital Audio Inputs, or 6 Channels of I^2S or Left Justified Serial Digital Audio Inputs plus 2 Channels of I^2S or Left Justified Serial Digital Audio Outputs 1 S/PDIF Digital Input 1 S/PDIF Digital Output	D2Audio™ SoundSuite™ DTS®(SRS) TruSurround HD4™ DTS®(SRS) WOWHD4™ DTS®(SRS) TruVolume™
D2-92684-QR	DAE-3HT 72-Pin Package	8 Channels of I^2S or Left Justified Serial Digital Audio Inputs, or 6 Channels of I^2S or Left Justified Serial Digital Audio Inputs plus 2 Channels of I^2S or Left Justified Serial Digital Audio Outputs 1 S/PDIF Digital Input 1 S/PDIF Digital Output	D2Audio™ SoundSuite™ Dolby® Digital/AC3 Decoder Dolby® Pro Logic IIx Surround

NOTE:

5. All DAE-3 family devices support D2Audio™ SoundSuite™ Audio Processing algorithms, and with license agreements executed with DTS®(SRS) Labs, also support DTS®(SRS) TruSurround HD4™, DTS®(SRS) WOW HD™, and DTS®(SRS) TruVolume™

Device Designations

This datasheet applies to all of the DAE-3 device family, which includes both the DAE-3 and DAE-3HT. Functional specifications apply to both designations of this family unless otherwise indicated.

Throughout this document the device names apply to all part numbers of their respective names as follows:

DAE DEVICE NAME	DAE DEVICE PART NUMBERS	PACKAGE PINS
DAE-3	D2-92633-LR, D2-92634-LR	128-Pin Package
DAE-3HT	D2-92683-QR, D2-92684-QR	72-Pin Package

Table of Contents

Ordering Information 2
Device Designations 3
Absolute Maximum Ratings 5
Thermal Information 5
Recommended Operating Conditions 5
Electrical Specifications 5
Serial Audio Interface Port Timing 7
Two-Wire (I^2C) Interface Port Timing 8
SPI™ Interface Port Timing 9
Pin Configuration DAE-3 (128-Pin Package) 10
Pin Configuration DAE-3HT (72-Pin Package) 11
Pin Description, DAE-3 (128-Pin) 12
Pin Description DAE-3HT (72-Pin) 17
Functional Block Diagram - DAE-3 21
Functional Block Diagram - DAE-3HT 22
Functional Description 23
Introduction 23
Sample Rate Converters (SRC) 23
Serial Digital Audio Interface 23
S/PDIF Digital Audio Interface 25
ADC input (DAE-3 Devices Only) 25
PWM Audio Amplifier Outputs 25
Amplifier Protection 26
Hardware I/O Features 26
Clocks And PLL 26
Reset and Initialization 26
Power Sequencing 26
Reset 27
Booting and Boot Modes 27
Control Interfaces 27
Reading and Writing Control Registers 28
Audio Processing Algorithms 29
SoundSuite™ Processing 30
Third Party Virtualization and Enhancements 30
Audio Processing Block Controls 30
Dynamic Register Addressing Architecture 31
Hardware Feature Functions 31
DAE-3 And DAE-3HT Differences 32
Pin Function Mapping Between Devices 32
I/O Pin Function Assignment Comparison 33
Revision History 34
About Intersil 34
Disclaimer for DTS®(SRS) Technology License Required Notice: 35
Package Outline Drawing 36
L72.10x10F 36
Q128.14x14 37

Absolute Maximum Ratings (Note 10)

Supply Voltage
- RVDD, PWMVDD, ADCVDD ..... -0.3V to 4.0V
- CVDD, PLLVDD ..... -0.3V to 2.4V

Input Voltage
- Any Input but XTALI .....-0.3V to RVDD +0.3V
- XTALI .....-0.3V to PLLVDD +0.3V

Input Current, Any Pin but Supplies ..... ±10mA

ESD Rating
- Human Body Model (Tested per JESD22-A114F).....2000V
- Machine Model (Tested per JESD22-A115C) 200V
- Charged Device Model (Tested per JESD22-C101E)..... 750V

Latch-Up
- (Pins 2, 4, 6, 7, 8, 9, 37 (72 Ld Package only) Tested per JESD78D Class II, Level B) 50mA
- (All Other pins Tested per JESD78D Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
128 Ld LQFP Package (Notes 6, 8)	39	6.5
72 Ld QFN Package (Notes 7, 9)	22	0.80

Maximum Storage Temperature..... -55°C to +150°C

Pb-Free Reflow Profile ..... see TB493

Recommended Operating Conditions

Temperature Range .....-10°C to +85°C

Digital I/O Supply Voltage, PWMVDD 3.3V

Core Supply Voltage, CVDD 1.8V

Analog Supply Voltage, PLLVDD 1.8V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board with direct attach of exposed pad to PCB.
8. For θ_{JC}, the “case temp” location is taken at the package top center.
9. For θ_{JC}, the “case temp” is measured on bottom of exposed pad.
10. Absolute Maximum parameters are not tested in production.

Electrical Specifications

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
V_{IH}	Digital Input High Logic Level (Note 11)	Relative to RVDD	2.0	-	-	V
V_{IL}	Digital Input Low Logic Level (Note 11)	Relative to RVDD	-	-	0.8	V
V_{OH}	High Level Output Drive Voltage I_{OUT} at - Pin Drive Strength Current. See “Pin Description, DAE-3 (128-Pin)” on page 12, and “Pin Description DAE-3HT (72-Pin)” on page 17		RVDD - 0.4	-	-	V
V_{OL}	Low Level Output Drive Voltage I_{OUT} at + Pin Drive Strength Current. See “Pin Description, DAE-3 (128-Pin)” on page 12, and “Pin Description DAE-3HT (72-Pin)” on page 17		-	-	0.4	V
VIHX	High Level Input Drive Voltage XTALI Pin		0.7	-	PLLVDD	V
VILX	Low Level Input Drive Voltage XTALI Pin		-	-	0.3	V
I_{IN}	Input Leakage Current (Note 12)		-	-	±10	µA
C_{IN}	Input Capacitance		-	9	-	pF
VOHO	High Level Output Drive Voltage OSCOUT Pin		PLLVDD - 0.3	-	-	V
VOLO	Low Level Output Drive Voltage OSCOUT Pin		-	-	0.3	V
C_{OUT}	Output Capacitance		-	9	-	pF
t_{RST}	nRESET Pulse Width		-	10	-	ns
R_{VDD}	Typical Digital I/O Pad Ring Supply (Voltage)		3.0	3.3	3.6	V
	(Current, Active)		-	10	-	mA
	(Current, Power-Down)		-	<1	-	mA
PWM_{VDD}	Typical PWM I/O Pad Ring Supply (Voltage)		3.0	3.3	3.6	V
	(Current, Active)		-	5	-	mA
	(Current, Power-Down)		-	<1	-	mA

Electrical Specifications T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
CVDD	Typical Core Supply (Voltage)		1.7	1.8	1.9	V
	(Current, Active)		-	300	-	mA
	(Current, Power-Down)		-	15	-	mA
PLLVDD	Typical PLL Analog Supply (Voltage)		1.7	1.8	1.9	V
	(Current, Active)		-	25	-	mA
	(Current, Power-Down)		-	10	-	mA
ADCVDD	Typical ADC Analog Supply (Voltage)		3.0	3.3	3.6	V
	(Current, Active, Power-Down)		-	12	-	mA
CRYSTAL OSCILLATOR						
Xo	Crystal Frequency (Fundamental Mode Crystal)		20	24.576	24.822 (24.576 + 1%)	MHz
Dt	Duty Cycle		40	-	60	%
t_{START}	Start-Up Time (Start-Up Time is Oscillator Enabled (with Valid Supply) to Stable Oscillation)		-	5	20	ms
PLL						
F_{VCO}	VCO Frequency		80.00	294.912	297.86	MHz
F_{IN}	Input Reference Frequency		20	-	24.822 (24.576 + 1%)	MHz
	Feedback Dividers (Integer)		4	12	15	
	PLL Lock Time from any Input Change		-	2	-	ms
1.8V POWER-ON RESET						
V_{EN}	Reset Enabled Voltage Level		0.9	1.1	1.4	V
t_{REJ}	POR Pulse Width Rejection (Note 14)		-	150	500	µs
t_{DIS}	POR Minimum Output Pulse Width		-	5	-	µs
1.8V BROWNOUT DETECTION						
	Detect Level		1.4	1.5	1.6	V
t_{BOD1}	Pulse Width Rejection			100	-	ns
t_{O1}	Minimum Output Pulse Width		20	-	-	ns
3.3V BROWNOUT DETECTION						
	Detect Level		2.5	2.7	2.9	V
t_{BOD3}	Pulse Width Rejection			100	-	ns
t_{O3}	Minimum Output Pulse Width		20	-	-	ns
ADC PERFORMANCE SPECIFICATIONS (DAE-3 only)						
V_{REF}	ADCREF DC Level		1.3	1.4	1.5	V
I_{REF}	ADCREF Load Current		-	-	±20	µA
V_{AIN}	Analog Input Level		V_{REF} - 0.6	-	V_{REF} + 0.6	V
	ADC Dynamic Range and SNR (Note 15) (ADC + ADC Decimator performance only, DSP inactive, no digital audio processing, PWM outputs off, no pPWM switching)	1.0 V_{P-P} 1kHz sine wave input reference level, using firmware from Audio Canvas III™ rev 3.1.4 or newer.	-	94	-	dB
	ADC Dynamic Range and SNR (Note 15) (DSP active and processing audio data, PWM active and driving audio outputs, measurements using typical system-level amplifier equivalent as measurement environment)		-	83	-	dB

Electrical Specifications

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
	THD+N		-	-80	-	dB
	Gain Mismatch		-	0.1	-	dB
	Crosstalk		-	-80	-	dB
	Power Supply Rejection		-	-70	-	dB

NOTES:

11. All input pins except XTALI.
12. Input leakage applies to all pins except XTALO.
13. Power-down is with device in reset and clocks stopped.
14. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
15. Analog performance is system-design dependent and is affected by factors that include PCB layout, shielding and routing of analog traces, additional components within the analog input path, and power supply isolation.

Serial Audio Interface Port Timing

(Figure 1) T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
tc_{SCLK}	SCKRx Frequency - SCKR0, SCKR1			12.5	MHz
tw_{SCLK}	SCKRx Pulse Width (High and Low) - SCKR0, SCKR1	40			ns
ts_{LRCLK}	LRCKRx Set-Up to SCLK Rising - LRCKR0, LRCKR1	20			ns
th_{LRCLK}	LRCKRx Hold from SCLK Rising - LRCKR0, LRCKR1	20			ns
ts_{SDI}	SDINx Set-Up to SCLK Rising - SDIN0, SDIN1	20			ns
th_{SDI}	SDINx Hold from SCLK Rising - SDIN0, SDIN1	20			ns
t_{dSDO}	SDOUTx Delay from SCLK Falling			20	ns

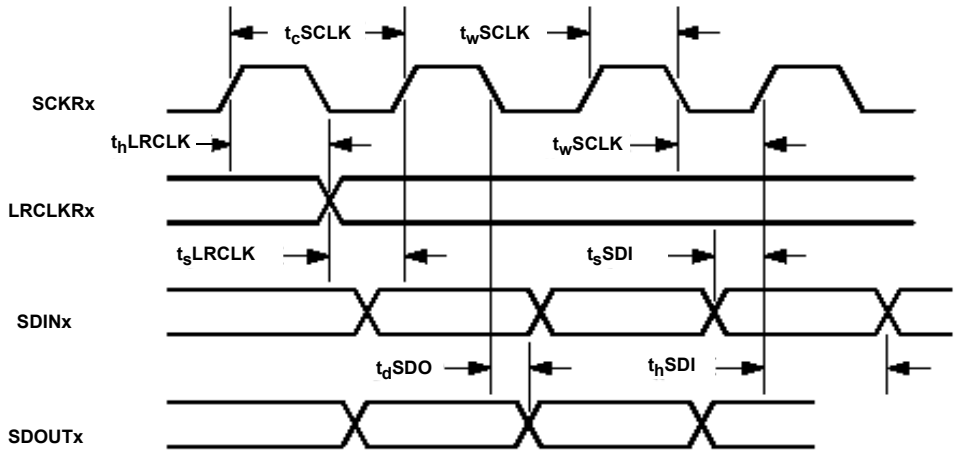


FIGURE 1. SERIAL AUDIO INTERFACE PORT TIMING

Two-Wire (I^2C) Interface Port Timing

(Figure 2) T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN (Note 14)	MAX (Note 14)	UNIT
f_{SCL}	SCL Frequency		100	kHz
t_{buf}	Bus Free Time Between Transmissions	4.7		µs
$tw_{lowSCLx}$	SCL Clock Low	4.7		µs
$tw_{highSCLx}$	SCL Clock High	4.0		µs
ts_{STA}	Set-Up Time For a (Repeated) Start	4.7		µs
th_{STA}	Start Condition Hold Time	4.0		µs
th_{SDAx}	SDA Hold From SCL Falling (Note 16)	0		µs
ts_{SDAx}	SDA Set-Up Time to SCL Rising	250		ns
td_{SDAx}	SDA Output Delay Time From SCL Falling		3.5	µs
t_r	Rise Time of Both SDA and SCL		1	µs
t_f	Fall Time of Both SDA and SCL		300	ns
ts_{STO}	Set-Up Time For a Stop Condition	4.7		µs

NOTE:

16. Data must be held sufficient time to bridge the 300ns transition time of SCL.

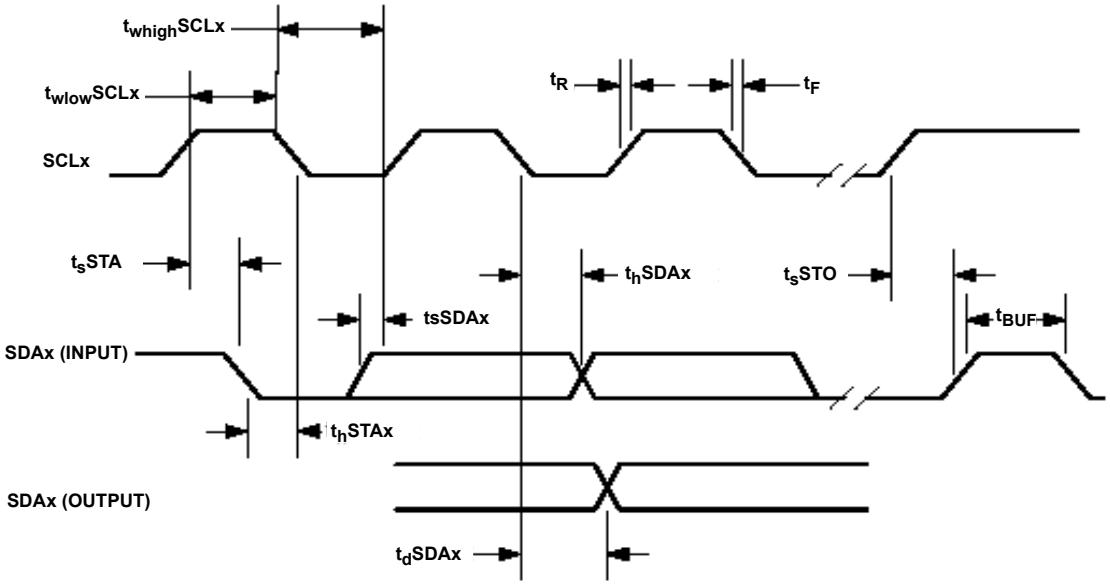


FIGURE 2. I^2C INTERFACE TIMING

SPI™ Interface Port Timing (Figure 3) T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN (Note 14)	MAX (Note 14)	UNIT
SPI MASTER MODE TIMING				
t_V	MOSI Valid From Clock Edge		8	ns
t_S	MISO Set-Up to Clock Edge	2		ns
t_H	MISO Hold From Clock Edge	2		ns
t_{WI}	nCS Minimum Width	3		3 system clocks + 2ns
SPI SLAVE MODE TIMING				
t_V	MISO Valid From Clock Edge		8	ns
t_S	MOSI Set-Up to Clock Edge	2		ns
t_H	MOSI Hold From Clock Edge	2		ns
t_{WI}	nCS Minimum Width	3		3 system clocks + 2ns

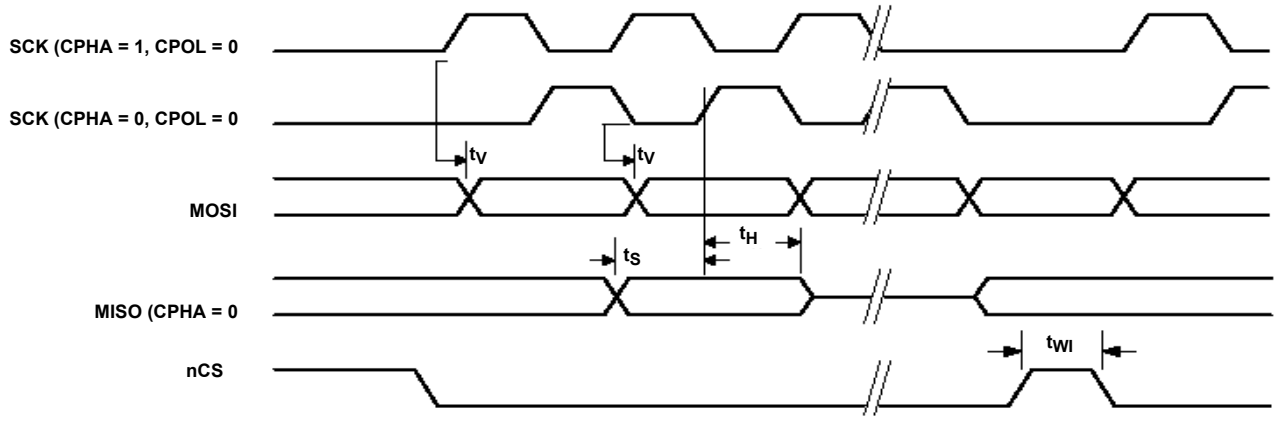
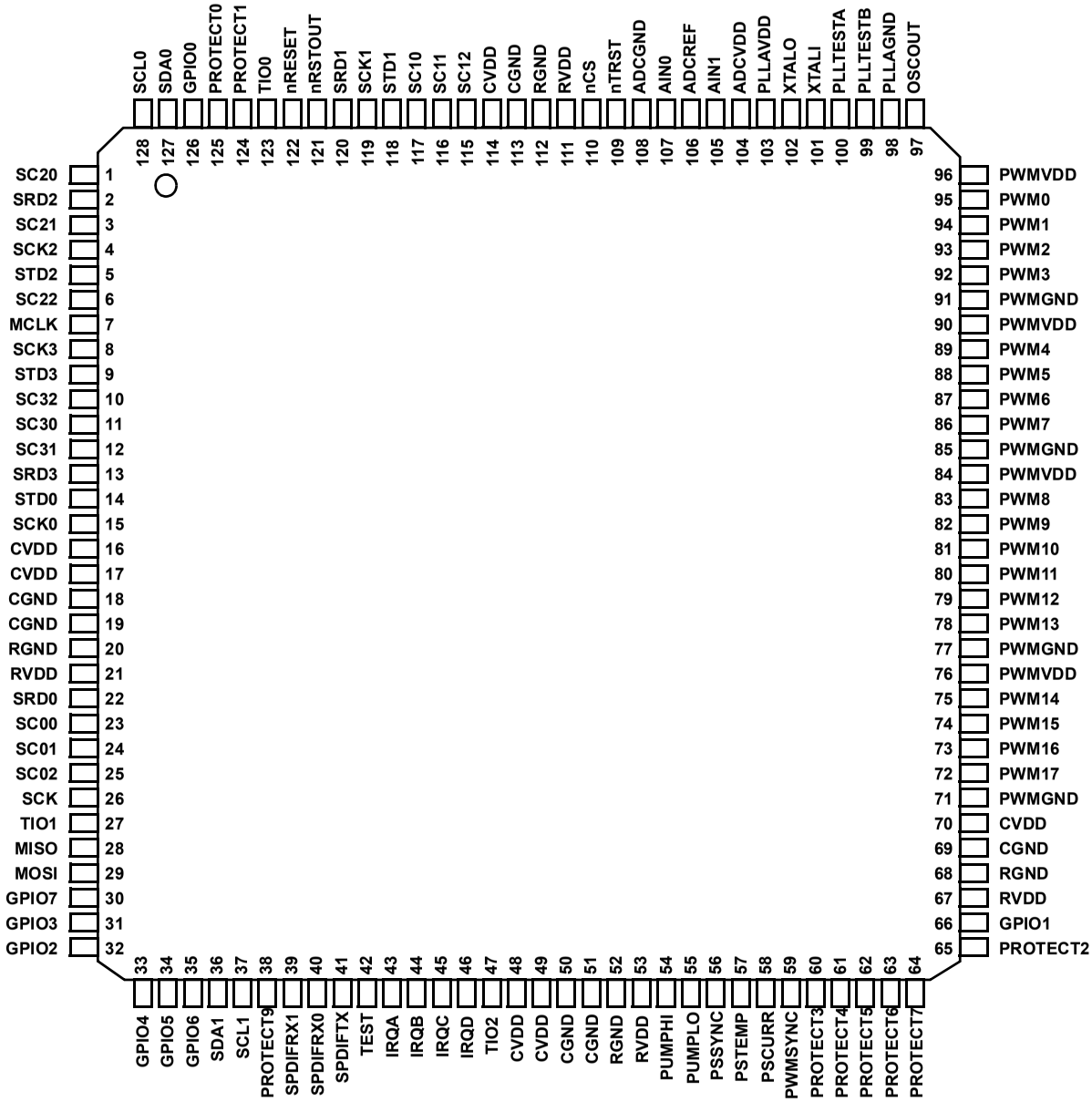


FIGURE 3. SPI TIMING

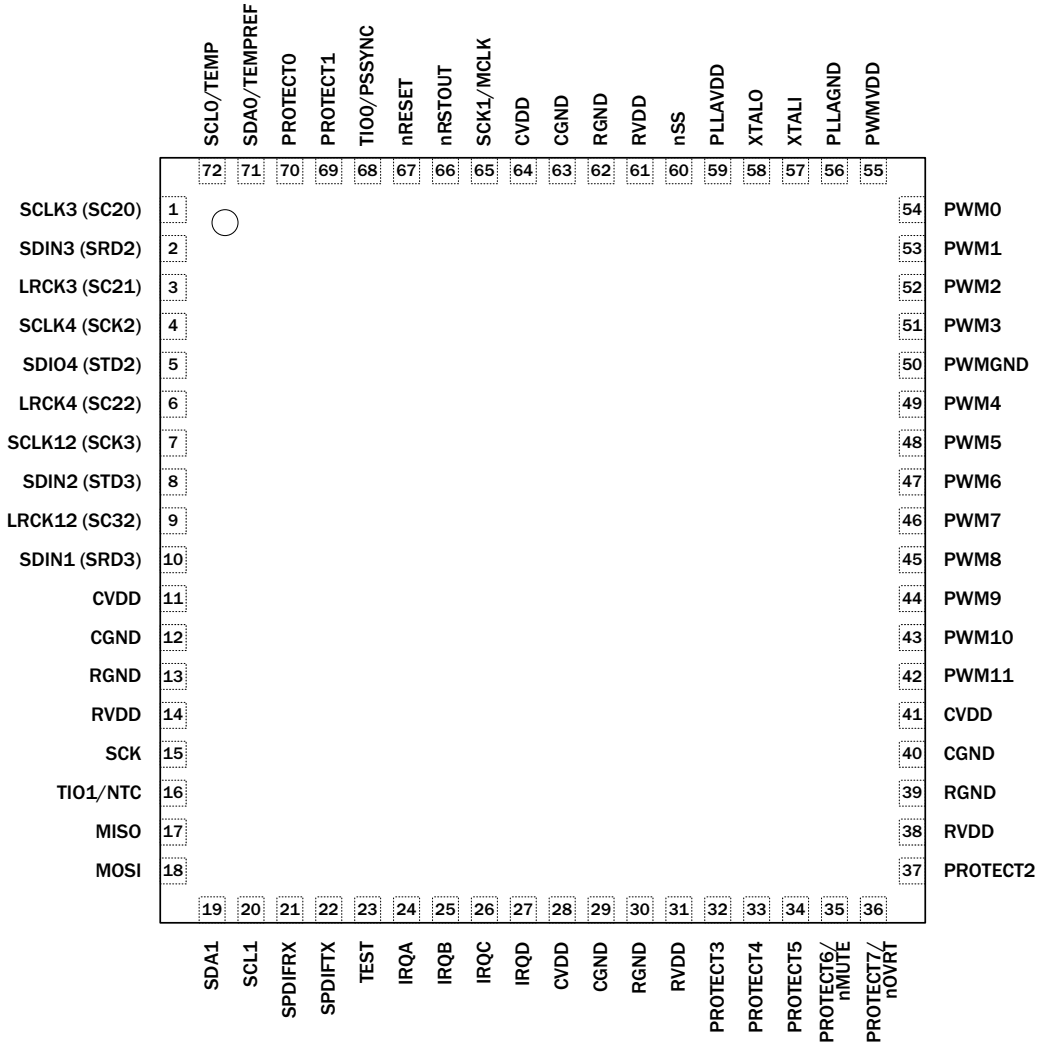
Pin Configuration DAE-3 (128-Pin Package)

D2-92633, D2-92634
(128 LD LQFP)
TOP VIEW



Pin Configuration DAE-3HT (72-Pin Package)

D2-92683, D2-92684
(72 LD QFN)
TOP VIEW



NOTE:

17. All pins pass Jedec II 100mA at +85°C, with exception of pins 2, 4, 6, 7, 8, 9, 37, which pass 50mA at +85°C

Pin Description, DAE-3 (128-Pin)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
1	SC20	I/O	3.3	8	Serial Audio Interface 2, I^2S0 SCLK
2	SRD2	I/O	3.3	4	Serial Audio Interface 2, I^2S0 SDIN
3	SC21	I/O	3.3	8	Serial Audio Interface 2, I^2S0 LRCK
4	SCK2	I/O	3.3	8	Serial Audio Interface 2, I^2S1 SCLK
5	STD2	I/O	3.3	8	Serial Audio Interface 2, I^2S1 SDIN
6	SC22	I/O	3.3	4	Serial Audio Interface 2, I^2S1 LRCK
7	MCLK	O	3.3	16	I^2S Serial Audio Master Clock output for external ADC/DAC components, drives low on reset and is enabled by firmware assignment.
8	SCK3	I/O	3.3	8	Serial Audio Interface 3, I^2S3 SCLK
9	STD3	I/O	3.3	8	Serial Audio Interface 3, I^2S3 SDIN
10	SC32	I/O	3.3	8	Serial Audio Interface 3, I^2S3 LRCK
11	SC30	I/O	3.3	8	Serial Audio Interface 3, I^2S2 SCLK
12	SC31	I/O	3.3	8	Serial Audio Interface 3, I^2S2 LRCK
13	SRD3	I/O	3.3	4	Serial Audio Interface 3, I^2S2 SDIN
14	STD0	I/O	3.3	8	Serial Audio Interface 0, I^2S SDAT0
15	SCK0	I/O	3.3	8	Serial Audio Interface 0, I^2S LRCK0
16	CVDD	P	3.3		Core power, 1.8V
17	CVDD	P	3.3		Core power, 1.8V
18	CGND	P	3.3		Core ground
19	CGND	P	3.3		Core ground
20	RGND	P	3.3		Digital pad ring ground. Internally connected to PWMGND.
21	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
22	SRD0	I/O	3.3	4	Serial Audio Interface 0, SDIO, Defaults to input, and may be configured as GPIO by firmware.
23	SC00	I/O	3.3	8	Serial Audio Interface 0, SDIO, Defaults to input, and may be configured as GPIO by firmware.
24	SC01	I/O	3.3	8	Serial Audio Interface 0, I^2S SDAT1
25	SC02	I/O	3.3	8	Serial Audio Interface 0, I^2S LRCK1
26	SCK	I/O	3.3	4	SPI clock I/O with hysteresis input.
27	TIO1	I/O	3.3	16	Timer I/O Port 1. Operation and assignment is controlled by firmware. Leave unconnected when not in use.
28	MISO	I/O	3.3	4	SPI master input, slave output data signal.
29	MOSI	I/O	3.3	4	SPI master output, slave input data signal.
30	GPIO7	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
31	GPIO3	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
32	GPIO2	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
33	GPIO4	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)

Pin Description, DAE-3 (128-Pin) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
34	GPIO5	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
35	GPIO6	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
36	SDA1	I/O	3.3	8 - OD	Two-Wire Serial data Port 1. Bidirectional signal used by both the master and slave controllers for data transport.
37	SCL1	I/O	3.3	8 - OD	Two-Wire Serial clock Port 1. Bidirectional signal is used by both the master and slave controllers for clock signaling.
38	PROTECT9	I/O	3.3	4	PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.)
39	SPDIFRX1	I	3.3		S/PDIF Digital audio data input 1
40	SPDIFRX0	I	3.3		S/PDIF Digital audio data input 0
41	SPDIFTX	O	3.3	4	S/PDIF Digital audio output. (Audio content and audio processing signal flow is dependent upon firmware, driving stereo output up to 192kHz.)
42	TEST	I	3.3		Factory test use only. Must be tied low.
43	IRQA	I	3.3		Interrupt request Port A, Boot Mode Select. One of 4 IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle.
44	IRQB	I	3.3		Interrupt request Port B, Boot Mode Select. One of 4 IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle.
45	IRQC	I	3.3		Interrupt request Port C, Boot Mode Select. One of 4 IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle.
46	IRQD	I	3.3		Interrupt request Port D, Boot Mode Select. One of 4 IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle.
47	TIO2	I/O	3.3	16	Timer I/O Port 2. Operation and assignment is controlled by firmware. Leave unconnected when not in use.
48	CVDD	P	3.3		Core power, 1.8V
49	CVDD	P	3.3		Core power, 1.8V
50	CGND	P	3.3		Core ground
51	CGND	P	3.3		Core ground
52	RGND	P	3.3		Digital pad ring ground. Internally connected to PWMGND.
53	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
54	PUMPHI	I/O	3.3	16	Assignable I/O. Function and operation defined by firmware.
55	PUMPLO	I/O	3.3	16	Assignable I/O. Function and operation defined by firmware.
56	PSSYNC	I/O	3.3	16	Synchronizing output signal to switching power supply. (Operates under specification of firmware and resets to high impedance inactive state when not used.)
57	PSTEMP	I/O	3.3	4	Assignable I/O. Function and operation defined by firmware.
58	PSCURR	I/O	3.3	4	Assignable I/O. Function and operation defined by firmware.
59	PWMSYNC	I/O	3.3	16	PWM synchronization port. (Function and operation is defined by firmware.)
60	PROTECT3	I/O	3.3	4	PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.)

Pin Description, DAE-3 (128-Pin) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
61	PROTECT4	I/O	3.3	4	PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.)
62	PROTECT5	I/O	3.3	4	PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.)
63	PROTECT6	I/O	3.3	4	PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.)
64	PROTECT7	I/O	3.3	4	PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.)
65	PROTECT2	I/O	3.3	4	PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.)
66	GPIO1	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
67	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
68	RGND	P	3.3		Digital pad ring ground. Internally connected to PWMGND.
69	CGND	P	3.3		Core ground
70	CVDD	P	3.3		Core power, 1.8V
71	PWMGND	P	3.3		PWM output pin ground. Internally connected to RGND.
72	PWM17	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
73	PWM16	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
74	PWM15	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
75	PWM14	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
76	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
77	PWMGND	P	3.3		PWM output pin ground. Internally connected to RGND.
78	PWM13	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
79	PWM12	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
80	PWM11	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
81	PWM10	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
82	PWM9	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
83	PWM8	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
84	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
85	PWMGND	P	3.3		PWM output pin ground. Internally connected to RGND.
86	PWM7	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)

Pin Description, DAE-3 (128-Pin) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
87	PWM6	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
88	PWM5	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
89	PWM4	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
90	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
91	PWMGND	P	3.3		PWM output pin ground. Internally connected to RGND.
92	PWM3	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
93	PWM2	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
94	PWM1	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
95	PWM0	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
96	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
97	OSCOUT	P	1.8		Analog oscillator output to slave D2-926xx devices. OSCOUT drives a buffered version of the crystal oscillator signal from the XTALI pin.
98	PLLAGND	P	1.8		PLL Analog ground
99	PLLTESTB	O	1.8		Factory test use only. Must be tied low.
100	PLLTESTA	O	1.8		Factory test use only. Must be tied low.
101	XTALI	P	1.8		Crystal oscillator analog input port. An external clock source would be driven into the this port. In multi-D2-926xx systems, the OSCOUT from the master D2-926xx would drive the XTALI pin.
102	XTALO	P	1.8		Crystal oscillator analog output port. When using an external clock source, this pin must be open. XTALO does not have a drive strength specification.
103	PLLAVDD	P	1.8		PLL Analog power, 1.8V
104	ADCVDD	P	3.3		Analog power for internal ADC, 3.3V
105	AIN1	I	3.3		Analog input 1 to internal ADC
106	ADCREF	O	3.3		Analog voltage reference output. Must be de-coupled to analog ground with 1µF capacitor.
107	AIN0	I	3.3		Analog input 0 to internal ADC
108	ADCGND	P	3.3		Analog ground for internal ADC
109	nTRST	I	3.3		Factory test only. Must be tied high at all times.
110	nCS	I/O	3.3	4	SPI slave select I/O.
111	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
112	RGND	P	3.3		Digital pad ring ground. Internally connected to PWMGND.
113	CGND	P	3.3		Core ground
114	CVDD	P	3.3		Core power, 1.8V
115	SC12	I/O	3.3	8	Serial Audio Interface 1, LRCK
116	SC11	I/O	3.3	8	Serial Audio Interface 1, SDAT3

Pin Description, DAE-3 (128-Pin) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
117	SC10	I/O	3.3	8	Serial Audio Interface 1, data (Assignment by firmware control.)
118	STD1	I/O	3.3	8	Serial Audio Interface 1, SDAT2
119	SCK1	I/O	3.3	8	Serial Audio Interface 1, SCK
120	SRD1	I/O	3.3	4	Serial Audio Interface 1, data (Assignment by firmware control.)
121	nRSTOUT	O	3.3	16 - OD	Active low open-drain reset output. Pin drives low from POR generator, 3.3V brownout detector going active, or from 1.8V brownout detector going active. This output should be used to initiate a system reset to the nRESET pin upon brownout event detection.
122	nRESET	I	3.3		Active low reset input with hysteresis. Activates system level reset when pulled low, initializing all internal logic and program operations. System latches boot mode selection of the IRQ input pins on the rising edge.
123	TIO0	I/O	3.3	16	Timer I/O Port 0. Operation and assignment is controlled by firmware. Leave unconnected when not in use.
124	PROTECT1	I/O	3.3	4	PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.)
125	PROTECT0	I/O	3.3	4	PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.)
126	GPIO0	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
127	SDA0	I/O	3.3	8 - OD	Two-Wire Serial data Port 0. Bidirectional signal used by both the master and slave controllers for data transport.
128	SCL0	I/O	3.3	8 - OD	Two-Wire Serial clock Port 0. Bidirectional signal is used by both the master and slave controllers for clock signaling.

NOTES:

18. Unless otherwise specified, all pin names are active high. Those that are active low have an “n” prefix.
19. All power and ground pins of same names are to be tied together to all other pins of their same name. (i.e., CVDD pins to be tied together, CGND pins to be tied together, RVDD pins to be tied together, and RGND pins to be tied together.) CGND and RGND are to be tied together on board. RGND and PWMGND pins are also internally connected and are to be tied together.

Pin Description DAE-3HT (72-Pin)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
1	SCLK3 (SC20)	In	3.3	8	Bit clock, I^2S Port 3, audio input channels 5-6. (I^2S Port 3 is 1 of 3 input-only ports, providing channels 5-6 input audio content.)
2	SDIN3 (SRD2)	In	3.3	4	Audio data, I^2S Port 3, audio input channels 5-6 (I^2S Port 3 is 1 of 3 input-only ports, providing channels 5-6 input audio content.)
3	LRCK3 (SC21)	In	3.3	8	L/R clock, I^2S Port 3, audio input channels 5-6 (I^2S Port 3 is 1 of 3 input-only ports, providing channels 5-6 input audio content.)
4	SCLK4 (SCK2)	In	3.3	8	Bit clock, I^2S Port 4, audio input channels 7-8, or audio output channels 1-2. (I^2S Port 4 is either an I^2S input port, or and I^2S output port. Selection of input or output is defined by firmware. When used as input, Port 4 provides channel 7-8 input audio content. When used as an output, Port 4 provides the 2 channels of I^2S output audio.)
5	SDIO4 (STD2)	I/O	3.3	8	Audio data, I^2S Port 4, input channels 7-8, or output channels 1-2. (I^2S Port 4 is either an I^2S input port, or and I^2S output port. Selection of input or output is defined by firmware. When used as input, Port 4 provides channel 7-8 input audio content. When used as an output, Port 4 provides the 2 channels of I^2S output audio.)
6	LRCK4 (SC22)	In	3.3	4	L/R clock, I^2S Port 4, audio input channels 7-8, or audio output channels 1-2. (I^2S Port 4 is either an I^2S input port, or and I^2S output port. Selection of input or output is defined by firmware. When used as input, Port 4 provides channel 7-8 input audio content. When used as an output, Port 4 provides the 2 channels of I^2S output audio.)
7	SCLK12 (SCK3)	In	3.3	8	Bit clock, I^2S ports 1 and 2, audio input channels 1-4 (I^2S ports 1 and 2 are 2 of the 3 input-only ports, providing channels 1-4 input audio content.)
8	SDIN2 (STD3)	In	3.3	8	Audio data, I^2S Port 2, audio input channels 3-4 (I^2S ports 1 and 2 are 2 of the 3 input-only ports, providing channels 1-4 input audio content.)
9	LRCK12 (SC32)	In	3.3	8	L/R clock, I^2S ports 1 and 2, audio input channels 1-4 (I^2S ports 1 and 2 are 2 of the 3 input-only ports, providing channels 1-4 input audio content.)
10	SDIN1 (SRD3)	In	3.3	8	Audio data, I^2S Port 1, audio input channels 1-2 (I^2S ports 1 and 2 are 2 of the 3 input-only ports, providing channels 1-4 input audio content.)
11	CVDD	P	3.3		Core power, 1.8V
12	CGND	G	3.3		Core ground
13	RGND	G	3.3		Digital pad ring ground. Internally connected to PWMGND.
14	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
15	SCK	I/O	3.3	4	SPI clock I/O with hysteresis input.
16	TIO1/NTC	I/O	3.3	16	Timer I/O Port 1, or assignable NTC temperature sensing common I/O. Operation and assignment is controlled by firmware. Leave unconnected when not in use.
17	MISO	I/O	3.3	4	SPI master input, slave output data signal.
18	MOSI	I/O	3.3	4	SPI master output, slave input data signal.
19	SDA1	I/O	3.3	8 - OD	Two-Wire Serial (I^2C) data Port 1. Primary control interface data signal used for device boot and control. Bidirectional port for both master and slave controllers operation.
20	SCL1	I/O	3.3	8 - OD	Two-Wire Serial (I^2C) clock Port 1. Primary control interface clock signal used for device boot and control. Bidirectional port for both master and slave controllers operation.
21	SPDIFRX	In	3.3		S/PDIF Digital audio data input
22	SPDIFTX	O	3.3		S/PDIF Digital audio output. (Audio content and audio processing signal flow is dependent upon firmware, driving stereo output up to 192kHz.)
23	TEST	In	3.3		Factory test use only. Must be tied low.
24	IRQA	In	3.3		Interrupt request Port A, Boot Mode Select. One of 4 IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle.

Pin Description DAE-3HT (72-Pin) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
25	IRQB	In	3.3		Interrupt request Port B, Boot Mode Select. One of 4 IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle.
26	IRQC	In	3.3		Interrupt request Port C, Boot Mode Select. One of 4 IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle.
27	IRQD	In	3.3		Interrupt request Port D, Boot Mode Select. One of 4 IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle.
28	CVDD	P	3.3		Core power, 1.8V
29	CGND	G	3.3		Core ground
30	RGND	G	3.3		Digital pad ring ground. Internally connected to PWMGND.
31	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers. Internally connected to PWMVDD.
32	PROTECT3	In	3.3	4	PWM protection input with hysteresis. (One of 8 protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
33	PROTECT4	In	3.3	4	PWM protection input with hysteresis. (One of 8 protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
34	PROTECT5	In	3.3	4	PWM protection input with hysteresis. (One of 8 protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
35	PROTECT6 /nMUTE	I/O	3.3	4	PWM protection input with hysteresis, or optional mute output. (One of 8 protection inputs. Specific function, channel assignment, and/or optional GPIO is defined by firmware.)
36	PROTECT7 /nOVRT	In	3.3	4	PWM protection input with hysteresis, or optional over-temperature monitor input. (One of 8 protection inputs. Specific function, channel assignment, and/or optional GPIO is defined by firmware.)
37	PROTECT2	In	3.3	4	PWM protection input with hysteresis. (One of 8 protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
38	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers. Internally connected to PWMVDD.
39	RGND	G	3.3		Digital pad ring ground. Internally connected to PWMGND.
40	CGND	G	3.3		Core ground
41	CVDD	P	3.3		Core power, 1.8V
42	PWM11	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
43	PWM10	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
44	PWM9	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
45	PWM8	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
46	PWM7	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)

Pin Description DAE-3HT (72-Pin) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
47	PWM6	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
48	PWM5	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
49	PWM4	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
50	PWMGND	O	3.3		PWM output pin power ground
51	PWM3	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
52	PWM2	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
53	PWM1	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
54	PWM0	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
55	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
56	PLLAGND	G	1.8		PLL Analog ground
57	XTALI	In	1.8		Crystal oscillator analog input port. When using an external clock source, the external clock is driven into the this port.
58	XTALO	O	1.8		Crystal oscillator analog output port. When using an external clock source, this pin must be open. XTALO does not have a drive strength specification.
59	PLLAVDD	P	1.8		PLL Analog power, 1.8V
60	nSS	O	3.3	4	SPI slave select I/O.
61	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers. Internally connected to PWMVDD.
62	RGND	G	3.3		Digital pad ring ground. Internally connected to PWMGND.
63	CGND	G	3.3		Core ground
64	CVDD	P	3.3		Core power, 1.8V
65	SCK1 /MCLK	I/O	3.3	8	Assignable general purpose I/O, or MCLK output. Operation and assignment is controlled by firmware. Assigns as default output for MCLK when enabled through firmware.
66	nRSTOUT	O	3.3	16 - OD	Active low open drain reset output. Pin drives low from POR generator, 3.3V brownout detector going active, or from 1.8V brownout detector going active. This output should be used to initiate a system reset to the nRESET pin upon brownout event detection.
67	nRESET	In	3.3		Active low reset input with hysteresis. Activates system level reset when pulled low, initializing all internal logic and program operations. System latches boot mode selection of the IRQ input pins on the rising edge.
68	TIO0 /PSSYNC	I/O	3.3	16	Timer I/O Port 0, or power supply sync output. Operation and assignment is controlled by firmware. Leave unconnected when not in use.

Pin Description DAE-3HT (72-Pin) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
69	PROTECT1	In	3.3	4	PWM protection input with hysteresis. (One of 8 protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
70	PROTECT0	In	3.3	4	PWM protection input with hysteresis. (One of 8 protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
71	SDA0 /TEMPREF	I/O	3.3	8 - OD	Two-Wire Serial data Port 0, or assignable I/O. Available for NTC temperature sensing reference as assignable I/O. Function is assigned by firmware.
72	SCL0 /TEMPNTC	I/O	3.3	8 - OD	Two-Wire Serial clock Port 0, assignable I/O. Available for NTC temperature sensing reference as assignable I/O. Function is assigned by firmware.

NOTES:

20. Unless otherwise specified, all pin names are active high. Those that are active low have an “n” prefix.
21. All power and ground pins of same names are to be tied together to all other pins of their same name. (i.e., CVDD pins to be tied together, CGND pins to be tied together, RVDD pins to be tied together, and RGND pins to be tied together.) CGND and RGND are to be tied together on board. RGND and PWMGND pins are also internally connected and are to be tied together.

Functional Block Diagram - DAE-3

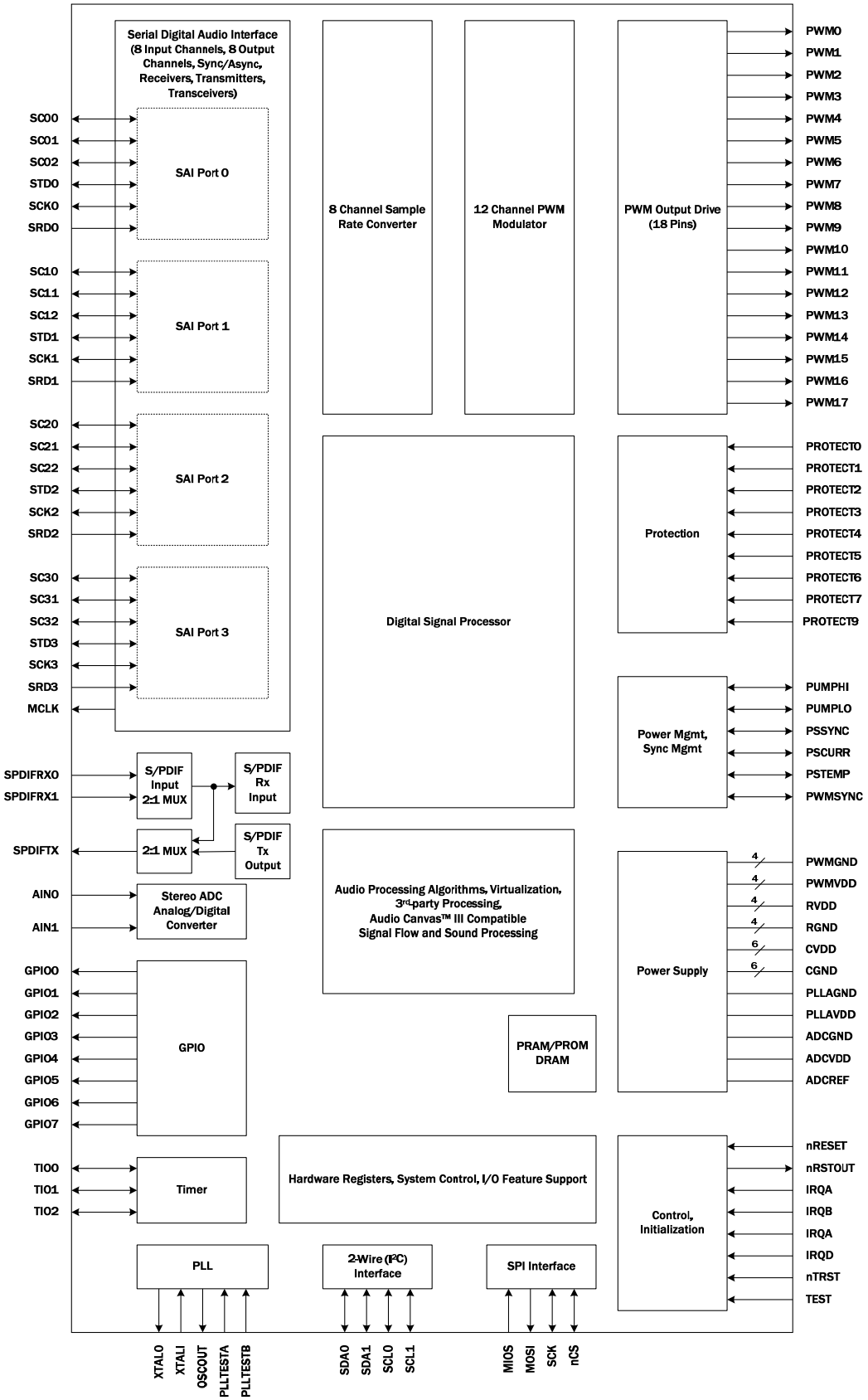


FIGURE 4. DAE-3 IC FUNCTIONAL BLOCK DIAGRAM

Functional Block Diagram - DAE-3HT

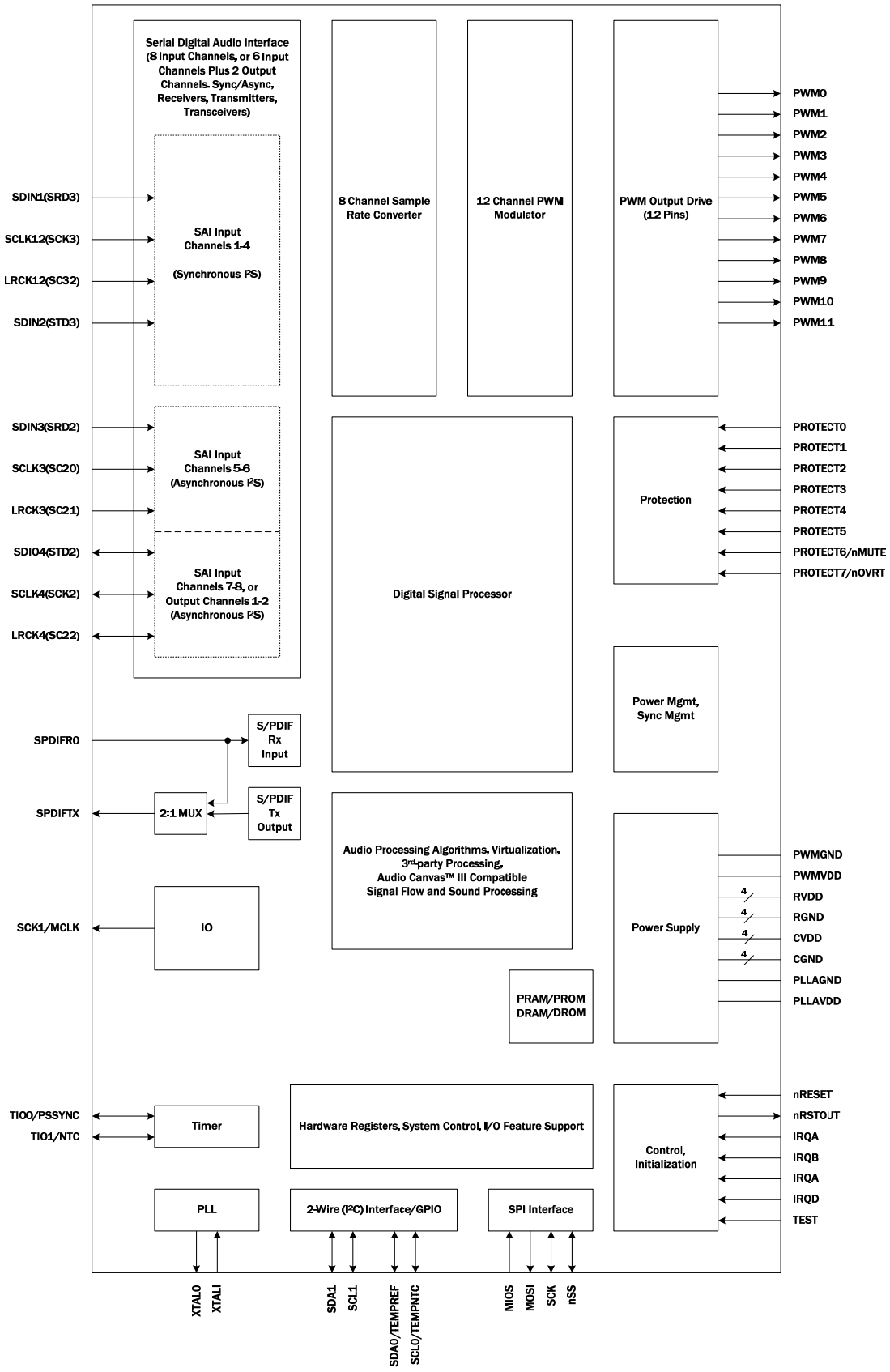


FIGURE 5. DAE-3HT IC FUNCTIONAL BLOCK DIAGRAM

Functional Description

Introduction

The DAE-3 family of ICs provide the core functionality, amplifier control, and complete audio signal processing for D2Audio Class-D amplifier solutions. The devices are highly programmable with all system features and functionality totally defined by firmware, that includes complete definition of audio processing, signal flow, digital audio I/O, and amplifier hardware interface control.

The Audio Canvas III software design tool supports building of the firmware for the DAE-3 family devices. Using Audio Canvas III, the designer is able to fully define audio processing and hardware function features with I/O assignments, and build complete production-ready firmware for the DAE-3 devices.

DAE-3 DEVICE DESIGNATIONS

The DAE-3 device family includes both the DAE-3 and DAE-3HT ICs. Functional specifications are identical to both designations of this family unless otherwise indicated.

The family device names apply to these part numbers:

DAE FAMILY DEVICE NAME	DAE PART NUMBERS	PACKAGE PINS
DAE-3	D2-92633-LR D2-92634-LR	128-Pin Package
DAE-3HT	D2-92683-QR D2-92684-QR	72-Pin Package

The DAE-3 devices are completely pin-compatible with the DAE-6 devices, allowing full flexibility for function vs cost trade-off, providing cost-effective solutions for applications of varying end-user features and capabilities.

The DAE-3HT devices are identical to the DAE-3 but are provided in a smaller 72-pin package with features and I/O mapped to pins supported in that package.

AUDIO CANVAS III SUPPORT

Audio Canvas III is a powerful design tool that lets the designer define audio processing and build a signal flow customized to the user's specifications. It fully supports the DAE-3 family including configuring the DAE family hardware I/O features and pin assignments. The designer can define the entire audio signal flow and architecture without signal flow limitations to any specific system. Capabilities include drag-and-drop of individual audio processing blocks that can be inserted into the signal flow, ability to connect and re-route signal flow, and live update capability to build and download the new audio architecture directly into the operating amplifier.

The DAE-3 family of ICs supports a wide variety of signal flows and audio processing options that are fully programmable and are completely defined by the system firmware and system architecture.

The firmware is built by the Audio Canvas III software, enabling full audio processing and amplifier hardware feature definition by the designer.

The DAE-3 supports a Class-D amplifier system built around internal audio processing blocks and amplifier system hardware functions.

In addition to audio processing blocks and signal flow that are user-selectable, system functions of hardware are configurable that include PWM timing control, channel configuration and assignment, protection and monitoring features, clock configurations, and other audio system features. Choices and settings are defined using the Audio Canvas III design tool software which builds the unique DAE firmware for each particular system design.

DSP

The majority of the audio processing functions and hardware feature implementations operate through firmware running within the DSP core. The core is a 24-bit fixed-point Digital Signal Processor, with its own DMA, interrupt control, memory spaces, and control interfaces.

Sample Rate Converters (SRC)

DAE-3 family supports internal asynchronous sample rate conversion to align input audio streams to a single rate compatible with the DSP processing rate and PWM switch rate. The family has 4 independent rate estimators, allowing up to 4 asynchronous stereo inputs (8 channels) to be sample rate converted and processed simultaneously. The sample rate converter has a measured SNR that exceeds 140dB and a THD+N that exceeds -125dB.

Serial Digital Audio Interface

SERIAL DIGITAL AUDIO INPUTS

The DAE-3 families include 4 Serial Audio Interface (SAI) digital audio input ports supporting up to 8 audio channels.

- The DAE-3 supports four independent SAI ports. All 4 ports operate asynchronously to receive audio from 4 independent audio sources, and each of the 4 ports has its own clock and frame inputs. SAI Port 3 (the 4th port) of the DAE-3 has multiplexed inputs to select that port's audio from the SAI input or from the on-chip ADC.
- The DAE-3HT devices support either 4 SAI input ports, or when its fourth port is used as an audio output, support 3 SAI input ports.

Each SAI port supports the digital audio industry I^2S standard which is capable of carrying up to 24-bit Linear PCM audio words per subframe IEC60958, or compressed digital audio (Dolby® Digital, AAC, MPEG, etc.) packing per the IEC61937 specification. The SAI port also supports Left-Justified formatted Linear PCM or compressed digital audio. These ports support sample rates from 32kHz to 192kHz.

SAI data formats are shown in Figure 6 on page 24. For I2S format, the left channel data is read when LRCK is low. For the Left-Justified format, the left channel data is read when LRCK is high. Either format requires data to be valid on the rising edge of SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs runs asynchronously to the others and may accept different sample rates and formats.

Input audio may be received from the S/PDIF input for 2 audio input channels, concurrent with and asynchronous from audio that is also being presented to SAI inputs for other audio input channels. Routing through the SRC synchronizes this audio from multiple sources for synchronous audio processing within the DAE audio processing paths.

SERIAL DIGITAL AUDIO OUTPUTS

Up to 4 SAI ports (up to 8 channels) are supported in the DAE-3 families.

- The DAE-3 supports 4 independent I^2S output ports for a total of 8 channels of audio.
- the DAE-3HT supports 1 I^2S output port (2 channels) and that port is configured to operate as either an input port or as an output port.

Use and channel assignment to the SAI outputs is configured using the Audio Canvas III software. Any of the DAE device's 12 audio processing channels may be assigned to any of the available SAI output channels. Audio Canvas III also assigns use of the 4th SAI port as in input or output for the DAE-3HT.

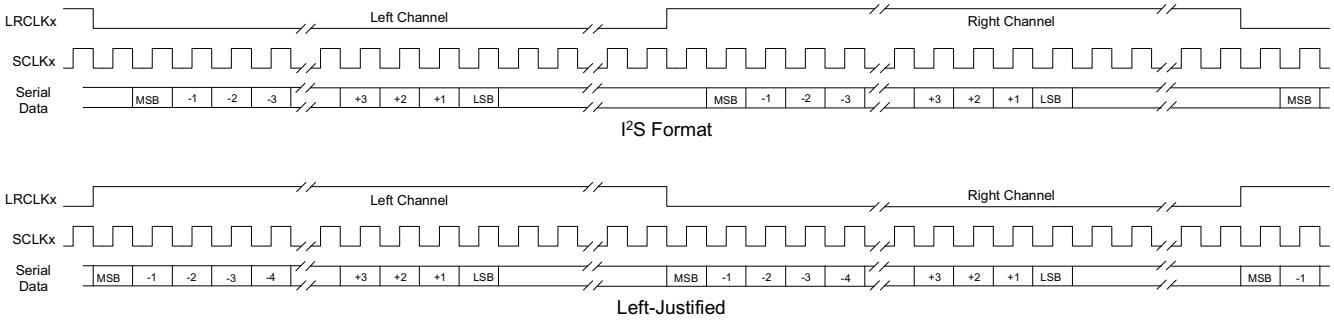


FIGURE 6. SAI PORT SUPPORTED DATA FORMATS FOR DELIVERY OF LINEAR PCM OR COMPRESSED AUDIO DATA

S/PDIF Digital Audio Interface

The device families include a S/PDIF Digital receiver and transmitter.

- The DAE-3 devices (128 pin packaged devices) include an on-chip multiplexer supporting switching of input from 2 different S/PDIF input pins. Input selection determines which pin routes to the S/PDIF receiver.
- The DAE-3HT devices (72 pin packaged devices) support one input pin only and do not use multiplex switching.

All of the devices in the family include a S/PDIF Digital transmitter.

S/PDIF RECEIVER

The S/PDIF receiver input pins are 3.3V CMOS input level compatible, requiring external circuitry to condition the serial input. The receiver contains an input transition detector, digital PLL clock recovery, and a decoder to separate audio, channel status, and user data. Only the first 24-Channel status bits are supported. The receiver constantly monitors the incoming data stream to detect the IEC61937-1 packet headers, and if found, captures the Pc and Pd data words into registers. The receiver meets the jitter tolerance specified in IEC60958-4.

S/PDIF is typically used for receiving compressed (IEC61937-compliant) as well as stereo PCM (IEC60958-compliant) audio data. This interface also supports receipt of compressed audio data that is not compliant with the IEC61937 specification, but instead meets the IEC60958 specification.

S/PDIF receive data is routed through the SRC, providing a time synchronized audio input stream for use within any of the DAE audio processing channels. Audio may be presented on the S/PDIF input asynchronous to audio also being presented to the I^2S Serial Digital inputs such that after routing through the SRC, are synchronous time aligned for internal DAE audio processing.

S/PDIF TRANSMITTER

The transmitter complies with the consumer applications defined in IEC60958-3. The transmitter supports 24-bit audio data, 24-bit user data, and 30-bit channel status data. S/PDIF output is linear PCM only and is non-compressed. Routing of compressed audio that is presented to the DAE inputs must be decoded by the DAE and its firmware before the selected channels may be routed to the S/PDIF outputs.

Audio routing to the S/PDIF transmitter is defined by the signal flow built by the Audio Canvas III software. That software supports assigning any of the audio processing channels to the 2 (L/R) channels of the S/PDIF output. Because all timing of the internal audio processing is synchronous to the internal DSP and processing channels, the S/PDIF audio output is also synchronous to that internal timing.

ADC input (DAE-3 Devices Only)

The DAE-3 devices contains a high-performance Analog-to-Digital Converter (ADC) that connects to input analog sources with a minimum of interface circuitry. The ADC is included in the DAE-3 devices only. It is not supported in the DAE-3HT devices.

At a bandwidth of 20kHz at nominal voltage and temperature, the ADC input of the DAE-3 provides a typical THD+N (unweighted) value of -81dB and a typical SNR/Dynamic Range of 83dB. These typical performances are based on a $1.0V_{P-P}$ 1 kHz sine wave input reference level, using a representative system-level amplifier environment processing digital audio data and producing PWM amplifier outputs.

Analog performance is affected by factors that include PCB layout, shielding and routing of analog traces, additional components within the analog input path, and proper power supply isolation techniques.

The ADC master clock is supplied from the low jitter PLL of the D2-926xx. The ADC operates synchronous to the DSP processing which minimizes noise pickup.

PWM Audio Amplifier Outputs

The DAE-3 family devices include an integrated 12-channel PWM engine. Each engine is independently programmable for timing, output pin assignment and audio processing path source.

PWM operation is defined by firmware. The Audio Canvas III design tool provides the selection for audio channel assignment routing, protection enabling, timing, and PWM output pin mapping, then uses these selections to build the firmware that controls the PWM outputs. Some features such as dead-band timing are also adjustable in real-time through the control interface.

Programmability enable use of multiple PWM output topologies, which supporting system designs of a broad range of output stages. Output topologies include integrated power stages, or discrete implementations using N+N or P+N for half-bridge, full-bridge or bridged-tied-load power stages. The PWM outputs may be used for powered outputs, and may also be used for driving line-level or headphone outputs.

The 12 PWM channels are mapped to the PWM output pins by firmware register assignment. Both DAE-3 and DAE-3HT include 12 PWM engines, and their available pins are:

- DAE-3 - 18 assignable and mappable pins
- DAE-3HT- 12 assignable and mappable pins