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## General description

The DA7210 is a high fidelity audio codec with integrated true-ground capless headphone driver suitable for a variety of low power, digital portable audio products.

Featuring a high efficiency headphone amplifier and supporting economic single supply voltages down to 1.8 V, the ultra-low 2.5 mW power consumption extends music playback time for battery operated equipment.

Eight analogue input pins allow multiple audio sources to be internally mixed, eliminating the need for external switches. Both single-ended and fully-differential line and microphone inputs are supported with built-in variable gain amplifiers to optimise dynamic range prior to digitisation.

DA7210 provides simultaneous connection to stereo headphone, stereo line outputs, and a mono differential output. Stereo line outputs can be differential or single-ended. Both stereo outputs have volume control from -54 dB to +15 dB.

Filtering and gain control is performed digitally including 5-band EQ and a digital input AGC with programmable attack and decay parameters. A configurable signal processing engine allows various enhancements and effects on the digital audio signal like acoustic filtering, wind noise suppression and 3D sound.

The multi-slot I2S/PCM interface supports all common sample rates between 8 and 96 kHz in master or slave mode operation.

## Key features

- Stereo multi-bit Delta Sigma DAC with SNR 100 dB ('A' weighted @ 48 kHz)
- Stereo multi-bit Delta Sigma ADC with SNR 96 dB ('A' weighted @ 48 kHz)
- Ultra low-power stereo headphone driver with
  - Stereo DAC to HP playback power: 2.5 mW
  - 2x58 mW output power (16 Ω)
  - 'Capless' output via GND centred signals
  - Four level charge pump with continuous tracking of audio signal (Class G)
  - Short circuit protection
- Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 and 96 kHz sample rates
- On-chip PLL with signal shaper and audio Sample Rate Matching
- Wide range of external clocks including industry standard 256xFs, system clock 12, 13, 24, 26 or 27 MHz and low power 32 kHz mode
- Audio serial data bus supports I2S, left/right justified, DSP and TDM modes
- Stereo or mono differential microphone interface
- Programmable ultra-low noise bias supply for electret microphones
- Volume controlled stereo auxiliary inputs and outputs supporting FM Radio and fixed gain speaker amplifiers
- Multi-mode audio routing and mixers
- Pop & click suppression circuitry
- ASSP DSP filter engine for digital audio enhancements (acoustic filtering, wind noise suppression, 5-band equaliser, 3D sound, automatic gain control)
- Supports supply from single voltage (1.8/2.5 V)
- Extensive modular power control
- Package: 49 bump WL-CSP – 0.4 mm pitch

## Applications

- Personal media players
- Portable consumer devices
- Music handsets
- Personal navigation devices

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# 1 Terms and definitions

| | |
|---|---|
| ADC | Analogue to Digital Converter |
| ALC | Automatic Level Control |
| ASSP | Application Specific Standard Product |
| DAC | Digital to Analogue Converter |
| DAI | Digital Audio Interface |
| DMIC | Digital microphone |
| DSP | Digital Signal Processor or Digital Signal Processing |
| FIR | Finite Impulse Response (Filter) |
| I2C | Inter-Integrated Circuit interface |
| I2S | Inter-IC Sound |
| IIR | Infinite Impulse Response (Filter) |
| GP | General Purpose (Filter) |
| LDO | Low Dropout regulator |
| MCLK | Master Clock |
| PCM | Pulse Code Modulation |
| PGA | Programmable Gain Amplifier |
| PLL | Phase Locked Loop |
| PSRR | Power Supply Rejection Ratio |
| RDL | Redistribution Layer |
| RC | Resistance-Capacitance |
| SC | System Controller |
| SDM | Sigma Delta Modulator |
| SNR | Signal to Noise Ratio |
| SRM | Sample Rate Matching |
| TDM | Time Division Multiplexing |
| THD+N | Total Harmonic Distortion plus Noise |
| VCO | Voltage-Controlled Oscillator |
| WL-CSP | Wafer Level-Chip Scale Packaging |

# 2 Block diagram

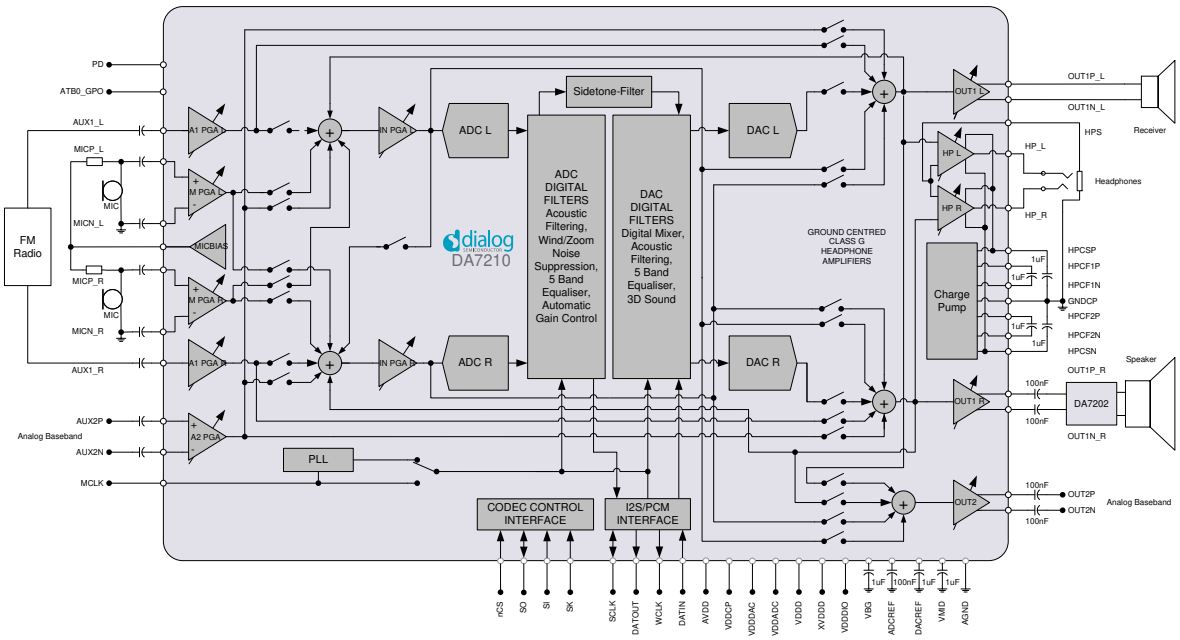


**Figure 1: DA7210 block diagram**

# 3 Pinout

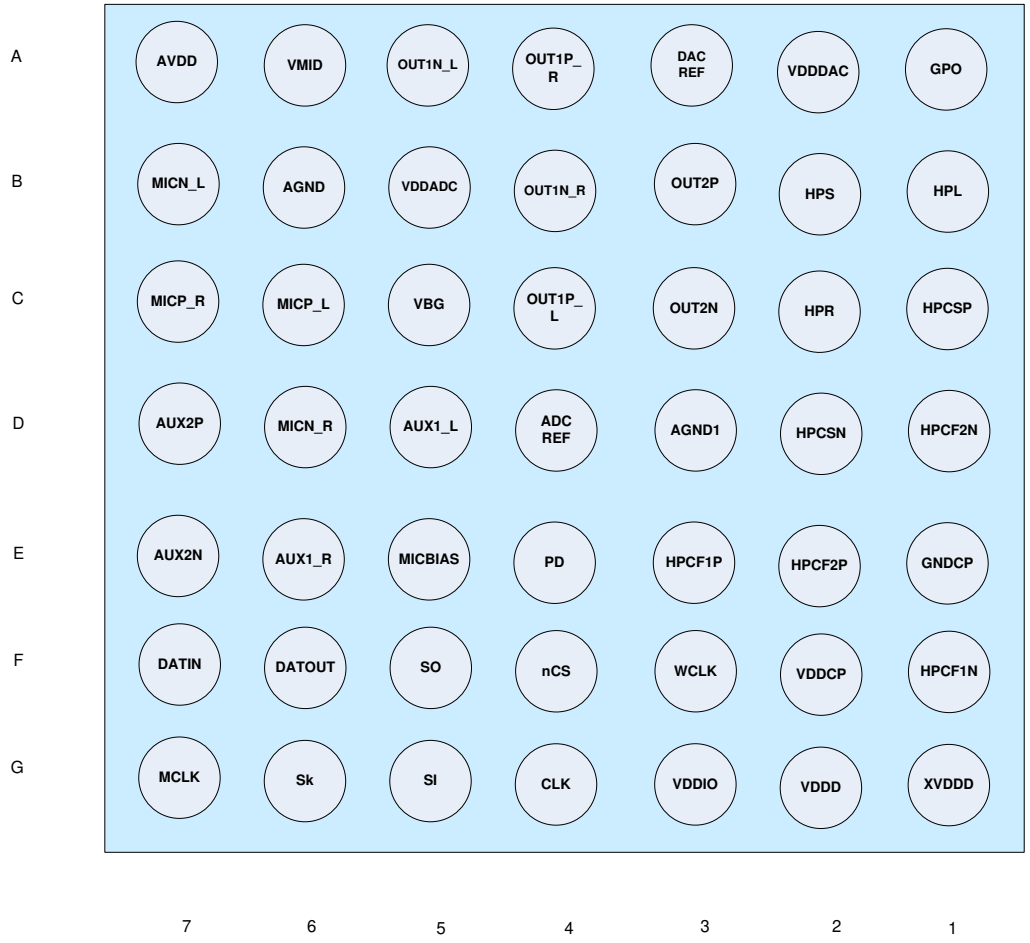


**Figure 2: DA7210 pad arrangement (bottom view ball side up)**

**Table 1: Pin description**

| Pin no. | Pin name | Type (Table 2) | Description |
|---|---|---|---|
| **Supplies and references** | | | |
| 7A | AVDD | PS | Analogue supply (PLL, bias, etc) |
| 2A | VDDDAC | PS | DAC and line output supplies |
| 5B | VDDADC | PS | Mic input and ADC supplies |
| 2F | VDDCP | PS | Charge pump supply |
| 1G | XVDDD | PS | Digital supply (regulator input) |
| 2G | VDDD | PS | Digital supply (1.5 V, if on-chip regulator is active) |
| 3G | VDDDIO | PS | Digital supply for I/O |
| 3A | DACREF | AI | Decoupling capacitor for DAC |
| 4D | ADCREF | AI | Decoupling capacitor for ADC |
| 6A | VMID | AI | Decoupling capacitor for VMID |
| 5C | VBG | AI | Decoupling capacitor for VBG |
| 5E | MICBIAS | AO | Current supply for microphone (2mA max) |

| Pin no. | Pin name | Type (Table 2) | Description |
|---|---|---|---|
| 1A | GPO | AIO | General Purpose Output |
| 6B | AGND | VSS | Analogue GND |
| 3D | AGND1 | VSS | Analogue GND |
| 1E | GNDCP | VSS | Digital and charge pump ground, attached to paddle |
| **Control** | | | |
| 5F | SO | DO | 4-WIRE Data output |
| 5G | SI | DIO | 4-WIRE Data input/2-WIRE bidirectional Data |
| 6G | SK | DI | 4-WIRE/2-WIRE Clock |
| 4F | nCS | DI | 4-wire Chip select |
| 4E | PD | DI | Power down signal (power down when high) |
| 2B | HPS | AIO | Headphone Ground Sense |
| **Digital Audio Interface** | | | |
| 4G | CLK | DIO | Digital Audio bit clock |
| 3F | WCLK | DIO | Digital Audio left/right clock |
| 7F | DATIN | DI | Digital Audio Data input |
| 6F | DATOUT | DO | Digital Audio Data output |
| 7G | MCLK | DI | Master clock input |
| **Audio inputs/outputs** | | | |
| 6C | MICP_L | AI | Left channel differential microphone +ve input |
| 7B | MICN_L | AI | Left channel differential microphone –ve input |
| 7C | MICP_R | AI | Right channel differential microphone +ve input |
| 6D | MICN_R | AI | Right channel differential microphone –ve input |
| 5D | AUX1_L | AI | Left channel single-ended auxiliary input |
| 6E | AUX1_R | AI | Right channel single-ended auxiliary input |
| 7D | AUX2P | AI | 2nd channel differential auxiliary +ve input |
| 7E | AUX2N | AI | 2nd channel differential auxiliary –ve input |
| 4C | OUT1P_L | AO | Differential or single ended +ve line out left |
| 5A | OUT1N_L | AO | Differential –ve line out left |
| 4A | OUT1P_R | AO | Differential or single ended +ve line out right |
| 4B | OUT1N_R | AO | Differential –ve line out right |
| 3C | OUT2N | AO | 2nd channel differential auxiliary -ve output |
| 3B | OUT2P | AO | 2nd channel differential auxiliary +ve output |
| 1B | HP_L | AO | Left head phone amp output |
| 2C | HP_R | AO | Right head phone amp output |
| **Charge pump** | | | |
| 3E | HPCF1P | PS | Head phone amp charge pump floating cap1 +ve |
| 1F | HPCF1N | PS | Head phone amp charge pump floating cap1 –ve |
| 2E | HPCF2P | PS | Head phone amp charge pump floating cap2 +ve |

| Pin no. | Pin name | Type (Table 2) | Description |
|---|---|---|---|
| 1D | HPCF2N | PS | Head phone amp charge pump floating cap2 –ve |
| 1C | HPCSP | PS | Head phone amp charge pump storage cap +ve |
| 2D | HPCSN | PS | Head phone amp charge pump storage cap –ve |

**Table 2: Pin type definition**

| Pin type | Description |
|---|---|
| AI | Analogue Input |
| AO | Analogue Output |
| AIO | Analogue Input/Output |
| DI | Digital Input |
| DO | Digital Output |
| DIO | Digital Input/Output |
| PS | Power Supply |
| VSS | Power Supply |

## 3.1 The 49-ball DA7210 device

On the DA7210, all supplies are accessible as external pins. The VDD pin is only required for capacitive decoupling. If the LDO is not required to supply the digital core voltage, the VDD supply should still be applied to the XVDD pin and the LDO should be disabled.

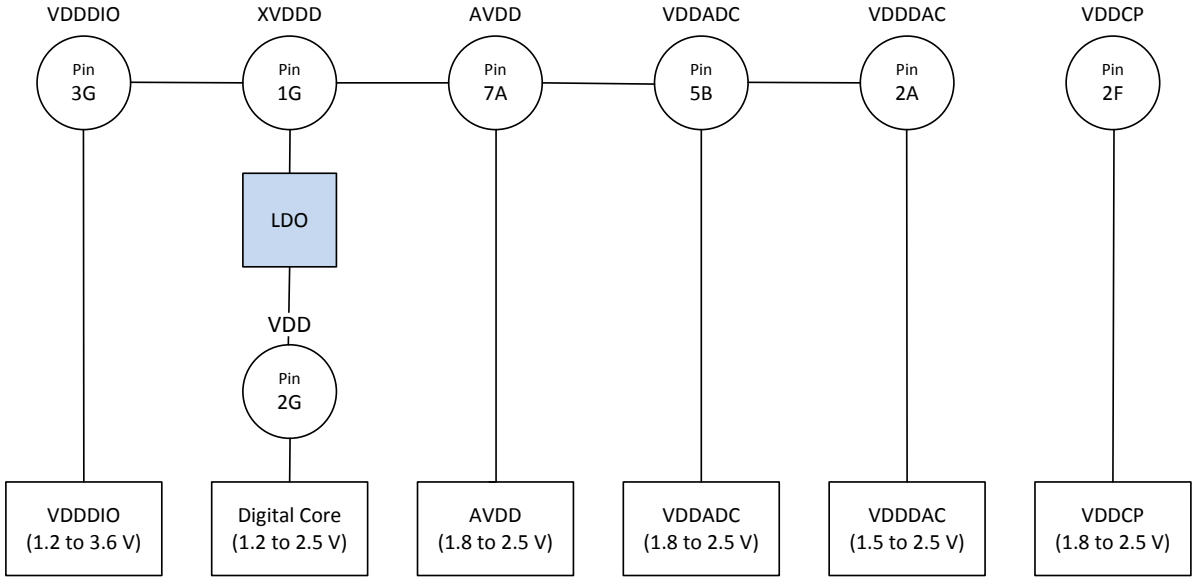


**Figure 3: DA7210 power supply topology**

# 4 Absolute maximum ratings

**Table 3: Absolute maximum ratings**

| Parameter | Description | Conditions (Note 1) | Min | Max | Unit |
|---|---|---|---|---|---|
| | Storage temperature | | -40 | +95 | °C |
| Ta | Operating temperature | | -40 | +85 | °C |
| AVDD, VDDDAC, VDDADC, VDDD, VDDDIO | Power Supply Input | | -0.3 | 2.75 | V |
| VDDDIO | | 3.6 V mode | -0.3 | 3.6 | V |
| | Supply voltage all input pins except power | | -0.3 | AVDD+ 0.3 | V |
| | Maximum power dissipation | | | 200 | mW |
| | Package thermal resistance | | | 40 | k/W |
| | ESD susceptibility | Human body model | | 2 | kV |

**Note 1** Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# 5 Recommended operating conditions

**Table 4: Recommended operating conditions**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Operating temperature | | -40 | | +85 | °C |
| VDDD | Supply voltage digital | Min and max values can accept +/-5% tolerances | 1.2 | | 2.5 | V |
| VDDDIO | Supply voltage I/O | Min and max values can accept +/-5% tolerances | 1.2 | | 2.5 | V |
| | | 3.6 V mode | 2.65 | | 3.6 | V |
| AVDD, VDDADC, VDDDAC | Supply voltage analogue | Min and max values can accept +/-5% tolerances | 1.8 | | 2.5 | V |
| VDDCP | Supply voltage headphone | Max value can accept +/-5% tolerances | 1.8 | | 2.5 | V |

# 6 Electrical characteristics

**Table 5: Power dissipation table**

| Parameter | Description | Conditions (Note 2) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | All registers at default values | Powerdown | | 6 | | µA |
| | Digital playback to lineout | DACL/R to OUT1L/R | | 3.15 | | mW |
| | Digital playback to HP no load | DACL/R to HPL/R quiescent | | 2.54 | | mW |
| | Digital playback to HP with load | DACL/R to HPL/R 16 Ω load 0.1 mW | | 4.66 | | mW |
| | Analogue bypass to lineout | AUX1L/R to OUT1L/R | | 2.87 | | mW |
| | Analogue bypass to HP no load | AUX1L/R to HPL/R quiescent | | 2.43 | | mW |
| | Analogue bypass to HP with load | AUX1L/R to HPL/R 16 Ω load 0.1 mW | | 4.57 | | mW |
| | Microphone stereo record | MICL/R to ADCL/R | | 2.38 | | mW |
| | Mic one channel record and digital playback to lineout | MICR to ADCR and DACR to OUT2 | | 3.10 | | mW |
| | Mic stereo record and digital playback to HP no load | MICL/R to ADCL/R and DACL/R to HPL/R quiescent | | 4.35 | | mW |
| | Mic stereo record and digital playback to HP with load | MICL/R to ADCL/R and DACL/R to HPL/R 16 Ω load 0.1 mW | | 6.49 | | mW |

**Note 2** SC_CLK_DIS, 0x03[7] = 1 for all measurements
VMID_BUFF_EN, 0x96[2:0] = 000 for all modes not using DAC

Test conditions: VDD=2.5 V, Ta=25°C, fs=48 kHz, 24-bit audio data unless specified otherwise

**Table 6: Electrical characteristics: Microphone bias**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BIAS}$ | Bias Voltage | No load, AVDD = 2.5 V<br>No load, AVDD = 1.8 V | 2.2<br>1.5 | Pro-grammable | 2.3<br>1.6 | V |
| $I_{BIAS}$ | Maximum Current | Voltage drop < 50 mV | | 2 | | mA |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz<br>2 kHz - 20 kHz | 70<br>50 | | | dB |
| $V_N$ | Output Noise Voltage | | | 5 | | $\mu V_{RMS}$ |
| | Capacitive Load | $I_{BIAS}$ < 100 µA,<br>100 µA < $I_{BIAS}$ < 2 mA | | 100<br>200 | | pF |

**Table 7: Electrical characteristics: Input mixing units**

(MICP_L, MICN_L, AUX_L, MICP_R, MICN_R, AUX1_R, AUX2P, AUX2N)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{MAX}$ | Full-scale Input Signal | single-ended<br>differential<br>MIC-PGA=0 dB<br>IN-PGA=0 dB | | 0.8*AVDD<br>1.6*AVDD | | $V_{PP}$ |
| $R_{IN}$ | Input resistance | Mic, meas. single ended<br>AUX1<br>AUX2 | 12<br>6<br>24 | 15<br>variable<br>30 | 18<br>40<br>36 | kΩ |
| | Frequency Response | +/- 0.5 dB | 20 | | 20k | Hz |
| | Amplitude Ripple | 20 Hz – 20 kHz | -0.5 | | 0.5 | dB |
| | Programmable Gain<br>Note 3 | M-PGA<br>AUX1-PGA<br>AUX2-PGA<br>IN-PGA | -6<br>-48<br>-6<br>-4.5 | | 24<br>21<br>12<br>18 | dB |
| | Programmable Gain Step Size | M-PGA, AUX2-PGA<br>AUX1-PGA, IN-PGA | | 6<br>1.5 | | dB |
| | Absolute Gain Accuracy | 0 dB @ 1 kHz | -1.0 | | 1.0 | dB |
| | Input Gain L/R-Mismatch | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| | Input Gain Step Error | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| $V_{NOISE}$ | Input Noise Level | Inputs connected to GND<br>A-weighting input referred, measured @ ADC output<br>Mic (Gain = 42 dB)<br>AUX1 (Gain = 21 dB)<br>AUX2 (Gain = 18 dB) | | 5<br>6.5<br>8.8 | | $\mu V_{RMS}$ |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz<br>2 kHz - 20 kHz,<br>single ended input | 80<br>70 | | | dB |

**Note 3** The gain describes the ratio of input and output signal level at the related amplifier stage (independent of whether the connection is single ended or differential).

**Table 8: Electrical characteristics: Analogue to digital converter (ADC)**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{MAX}$ | Full-scale Input Signal | Corresponding digital level 0 dBFS | | 1.6* AVDD | | $V_{PP}$ |
| SNR | Signal to Noise Ratio | A-weighting, no input selected | | 96 | | dB |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS | | -89 | | dB |
| | Channel separation | | | 90 | | dB |
| $B_{PASS}$ | Pass band | | | | 0.45*fs | kHz |
| $B_{STOP}$ | Stop band | fs ≤ 48 kHz<br>fs = 88.2/96 kHz | 0.56*fs | | 7*fs<br>3.5*fs | kHz |
| | Pass band Ripple | Voice Mode<br>Music Mode | | | +/-0.3<br>+/-0.1 | dB |
| | Stop band Attenuation | Voice Mode<br>Music Mode | 70<br>55 | | | dB |
| | Group delay | Voice Mode<br>Music Mode (Note 4)<br>fs= 88.2/96 kHz | | 4.3/fs<br>18/fs<br>9/fs | 600 | µs |
| | Group delay mismatch | Between left and right channel | | | 2 | µs |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz<br>2 kHz - 20 kHz | 80<br>70 | | | dB |

**Note 4** 5-band-equaliser disabled.

**Table 9: Electrical characteristics: Digital to analogue converter (DAC)**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{MAX}$ | Full-scale Output Signal | Corresponding digital level 0 dBFS | | 1.6* VDDDAC | | $V_{PP}$ |
| SNR | Signal to Noise Ratio | A weighting | | 102 | | dB |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS | | -90 | | dB |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS, 32 kHz PLL mode | | -80 | | dB |
| | Channel separation | | | 90 | | dB |
| $B_{PASS}$ | Pass band | | | | 0.45*fs | kHz |
| $B_{STOP}$ | Stop band | fs ≤ 48 kHz<br>fs = 88.2/96 kHz | 0.56*fs | | 7.5*fs<br>3.5*fs | kHz |
| | Pass band Ripple | Voice Mode<br>Music Mode | | | ±0.15<br>±0.1 | dB |
| | Stop band Attenuation | Voice Mode<br>Music Mode | 70<br>55 | | | dB |
| | Group delay | Voice Mode<br>Music Mode<br>fs = 88.2/96 kHz | | 4.8/fs<br>18.5/fs<br>9/fs | 650 | µs |
| | Group delay variation | 20 Hz to 20 kHz | | | 1 | µs |
| | Group delay mismatch | Between left and right channel | | | 2 | µs |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz<br>2 kHz - 20 kHz | 70<br>60 | | | dB |

**Table 10: Electrical characteristics: Line out and receiver amplifier**

(OUT1P_L, OUT1N_L, OUT1P_R, OUT1N_R)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{MAX}$ | Full-scale Input Signal | No load, single-ended<br>No load, differential | | 0.8*AVDD<br>1.6 *AVDD | | $V_{PP}$ |
| | Load Impedance | single-ended output mode | 500 | 2k | <br>1<br>200 | Ω<br>µH<br>pF |
| | | differential output mode | 25 | 32 | <br>1<br>200 | Ω<br>µH<br>pF |
| | Frequency Response | +/- 0.5 dB | 20 | | 20k | Hz |
| | Amplitude Ripple | 20 Hz – 20 kHz | -0.5 | | 0.5 | dB |
| | Programmable Gain | | -54 | | 15 | dB |
| | Mute Attenuation | | | 100 | | dB |
| | Programmable Gain Step Size | | | 1.5 | | dB |
| | Absolute Gain Accuracy | 0 dB @ 1 kHz | -0.8 | | 0.8 | dB |
| | Input Gain L/R-Mismatch | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| | Input Gain Step Error | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| SNR | Signal to Noise Ratio | A weighting | | 102 | | dB |
| $V_{NOISE}$ | Output Noise Level | 20 - 20 kHz, unweighted<br>gain < -15 dB<br>single-ended<br>differential | | <br><br><5.5<br><4.5 | | µV |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS, 44.1 kHz slave mode non A-weighting | | -90 | | |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz<br>2 kHz - 20 kHz<br>single-ended output | 70<br>47 | | | dB |
| | | 20 Hz - 2 kHz<br>2 kHz - 20 kHz<br>differential output | 90<br>70 | | | dB |

**Table 11: Electrical characteristics: Line out amplifier**

(OUT2P, OUT2N)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{MAX}$ | Full-scale Input Signal | No load | | 1.6*AVDD | | $V_{PP}$ |
| | Load Impedance | | 25 | 32 | <br>1<br>200 | Ω<br>µH<br>pF |
| | Frequency Response | +/- 0.5 dB | 20 | | 20k | Hz |
| | Amplitude Ripple | 20 Hz – 20 kHz | -0.5 | | 0.5 | dB |
| | Programmable Gain | | -18 | | 6 | dB |
| | Programmable Gain Step Size | | | 6 | | dB |
| | Input Gain L/R-Mismatch | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| | Input Gain Step Error | 20 Hz – 20 kHz | -0.2 | | 0.2 | dB |
| SNR | Signal to Noise Ratio | A-weighting, gain = 0 dB | | 102 | | dB |
| $V_{NOISE}$ | Output Noise Level | 20 -20 kHz, unweighed<br>Gain < -15 dB, gain ≤ -12 dB | | <5 | | µV |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS , A-weighting | | -90 | | |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz<br>2 kHz - 20 kHz | 90<br>70 | | | dB |

**Table 12: Electrical characteristics: Dynamic charge pump**

(HPCSP, HPCSN)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDDCSP | Positive dynamic supply voltage | VDDCP/3/4 can optionally be enabled if two flying caps are available | | VDDCP<br>VDDCP/2<br>(VDDCP/3, VDDCP/4) | | |
| VDDCSN | Negative dynamic supply voltage | -VDDCP/3/4 can optionally be enabled if two flying caps are available | | -VDDCP<br>-VDDCP/2<br>(-VDDCP/3, -VDDCP/4) | | |
| | Floating capacitors | | | 1.0 | | µF |
| | Storage capacitors | | | 1.0 | | µF |

**Table 13: Electrical characteristics: Headphone amplifier**

(HPL, HPR)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{MAX}$ | Full-scale Output Signal | No load | | 1.6*VDD CP | | $V_{PP}$ |
| | DC output offset | | | 100 | | µV |
| $P_{MAX}$ | Output Power per channel | VDDCP = 1.8 V, THD < 0.1%, $R_L$=16 Ω 1 kHz | | 28 | | $mW_{RMS}$ |
| | | VDDCP = 2.5 V, THD < 0.1%, $R_L$=16 Ω 1 kHz | | 58 | | $mW_{RMS}$ |
| | Dynamic internal supply voltages | VDD/3 or VDD/4 can optionally be selected if two flying caps are available | | ±VDD<br>±VDD/2<br>(±VDD/3<br>(±VDD/4) | | |
| IQ | Quiescent current per channel | from VDDCP | | 100 | | uA |
| | Load Impedance | 13 < $R_L$ < ∞ | 13 | 16 | <br>400<br>500 | Ω<br>µH<br>pF |
| | Frequency Response | +/- 0.5 dB | 20 | | 20k | |
| | Amplitude Ripple | 20 Hz – 20 kHz | -0.5 | | 0.5 | dB |
| | Programmable Gain | | -54 | | 15 | dB |
| | Mute Attenuation | | | 100 | | dB |
| | Programmable Gain Step Size | | | 1.5 | | dB |
| | Absolute Gain Accuracy | 0 dB @ 1 kHz | -0.8 | | 0.8 | dB |
| | Input Gain L/R-Mismatch | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| | Input Gain Step Error | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| SNR | Signal to Noise Ratio | A weighting, gain = 0 dB | | 100 | | dB |
| $V_{NOISE}$ | Output Noise Level | 20 to 20 kHz, unweighted, gain < -15 dB | | <4.5 | | $µV_{rms}$ |
| THD+N | Total Harmonic Distortion Plus Noise | VDDCP = 1.8 V, -5 dBFS, $R_L$=16 Ω | | -80 | | dB |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz<br>2 kHz - 20 kHz | 70<br>50 | | | dB |
| | Output power per channel | VDDCP=2.5 V, THD<1%, $R_L$=16 Ω, 1 kHz | | 72 | | mW |

**Table 14: Electrical characteristics: Phase locked loop (MCLK)**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Input Jitter | cycle to cycle | | | 35 | ps |
| | | rms | | | 100 | ps |
| | Input Impedance | DC impedance > 10 MΩ | 300<br>0.5 | <br>1 | <br>2 | Ω<br>pF |
| **Interface mode (MCLK is 256 Fs, PLL off)** | | | | | | |
| $F_{in}$ | Input frequency | 256 Fs<br>128 Fs (96 kHz) | 11.289 | | 12.288 | MHz |
| **Oscillator mode (MCLK from standard oscillator, PLL on)** | | | | | | |
| $F_{in}$ | Input frequency | 12.0, 13.0, 13.5, 14.4, 19.2, 19.68 MHz (x 1, 2 or 4), 32 kHz mode | 10 | <br>32.768 | 80 | MHz<br>kHz |
| | I2S tracking range (SRM) | Maximum mismatch of I2S word-clock | | | 4 | % |
| | I2S clock drift | Maximum frequency drift of I2S word clock | | | 50 | ppm/s |
| $V_{IN\ AC}$ | MCLK Shaper range | For AC coupling with internal clock shaping | 300 | 500 | 1000 | $mV_{PP}$ |

**Table 15: Electrical characteristics: Digital I/O**

(Ta = -40 to +85ºC)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VIH | CLK, WCLK, DATIN, SK, nCS, SI, PD, MCLK,<br>Input High Voltage | | 0.7*VDDDIO | | VDDDIO | V |
| VIL | CLK, WCLK, DATIN, SK, nCS, SI, PD, MCLK,<br>Input Low Voltage | | -0.3 | | 0.3*VDDDIO | V |
| VOH @ 1 mA | CLK, WCLK, DATOUT<br>Output High Voltage | | 0.8*VDDDIO | | VDDDIO | V |
| VOH | SO<br>(open drain mode)<br>Output High Voltage | | | OPEN DRAIN | 3.6 | V |
| VOL @ 1 mA | CLK, WCLK, DATOUT<br>Output Low Voltage | | 0 | | 0.3 | V |
| | MCLK<br>Input High Voltage | DC-coupled TTL signal | 0.7*VDDDIO | | VDDDIO | V |
| | MCLK<br>Input Low Voltage | | -0.3 | | 0.3*VDDDIO | V |

# 7 Timing characteristics

## 7.1 Digital audio interface timing - I2S/DSP (in master/slave mode)

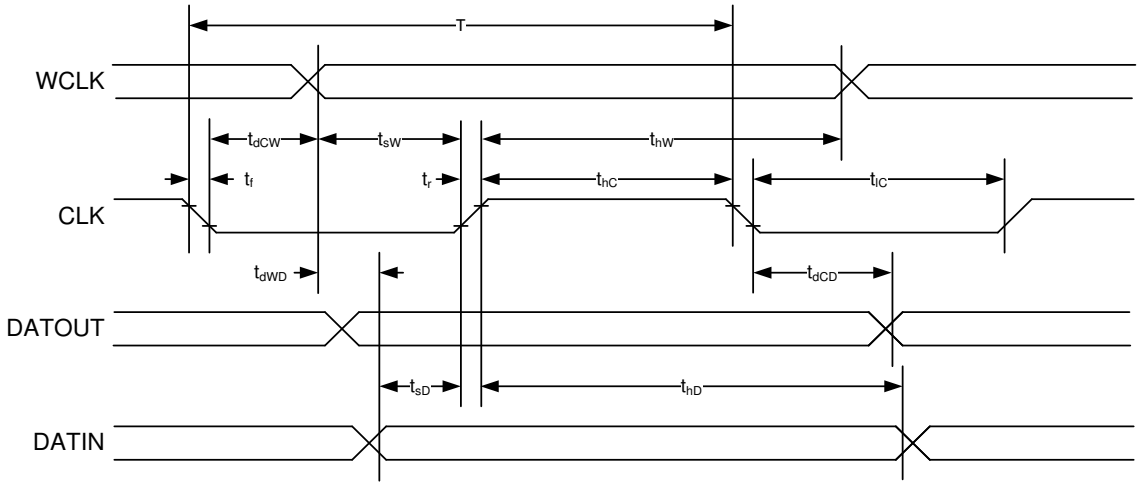


**Figure 4: I2S/DSP timing diagram**

**Table 16: I2S/DSP timing characteristics**

(Ta = -40 to +85ºC)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Input impedance | DC impedance > 10 MΩ | 300<br>1.0 | | <br>2.5 | Ω<br>pF |
| T | CLK period | | 75 | | | ns |
| $t_r$ | CLK rise time | | | | 8 | ns |
| $t_f$ | CLK fall time | | | | 8 | ns |
| $t_{hC}$ | CLK high period | | 40% | | 60% | T |
| $t_{lC}$ | CLK low period | | 40% | | 60% | T |
| $t_{dCW}$ | CLK to WCLK delay | | -30% | | +30% | T |
| $t_{dCD}$ | CLK to DATOUT delay | | -30% | | +30% | T |
| $t_{hW}$ | WCLK high time | DSP mode | 100% | | | T |
| | | Non-DSP mode | Word length | | | T |
| $t_{lW}$ | WCLK low time | DSP mode | 100% | | | T |
| | | Non-DSP mode | Word length | | | T |
| $t_{sW}$ | WCLK setup time | Slave mode | 7 | | | ns |
| $t_{hW}$ | WCLK hold time | Slave mode | 2 | | | ns |
| $t_{sD}$ | DATIN setup time | | 7 | | | ns |
| $t_{hD}$ | DATIN hold time | | 2 | | | ns |
| $t_{dWD}$ | DATOUT to WCLK delay | | DATOUT is synchronised to CLK | | | |

## 7.2 Digital audio control timing - 2-wire control timing

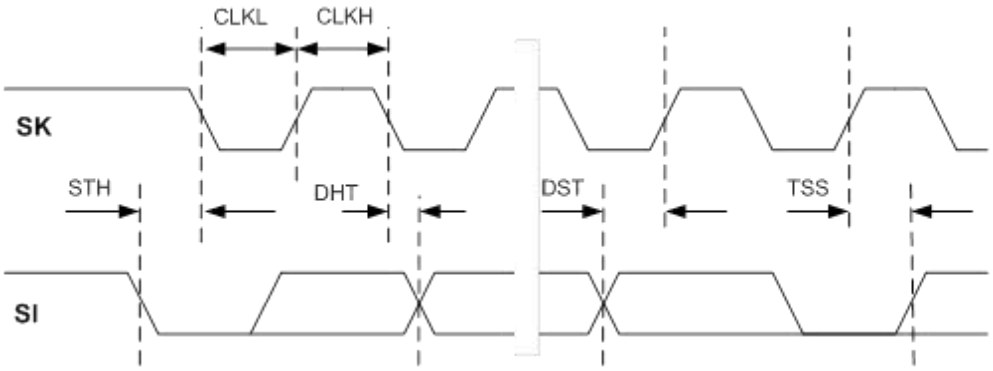


**Figure 5: 2-wire control timing diagram**

**Table 17: 2-wire control timing characteristics**

(Ta = -40 to +85ºC)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Bus free time STOP to START | | 1.3 | | | µs |
| | Bus Line Capacitive load | | | | 100 | pF |
| **Standard/Fast Mode** | | | | | | |
| | SK clock frequency | | 1 | | 400 | kHz |
| | Bus free time STOP to START | | 1.3 | | | µs |
| | Start condition set-up time | | 0.6 | | | µs |
| STH | Start condition hold time | | 0.6 | | | µs |
| CLKL | SK low time | | 1.3 | | | µs |
| CLKH | SK high time | | 0.6 | | | µs |
| | 2-wire SK and SI rise/fall time | | | | 300 | ns |
| DST | SI set-up time | | 100 | | | ns |
| DHT | SI hold-time | | 0 | | | ns |
| TSS | Stop condition set-up time | | 0.6 | | | µs |
| **High Speed Mode** | | | | | | |
| | SK clock frequency | | 1 | | 1700 | kHz |
| | Start condition set-up time | | 160 | | | ns |
| STH | Start condition hold time | | 160 | | | ns |
| CLKL | SK low time | | 160 | | | ns |
| CLKH | SK high time | | 60 | | | ns |
| | HS-2-wire SK rise/fall time | | | | 40 | ns |
| | HS-2-wire SI rise/fall time | | | | 80 | ns |
| DST | SI set-up time | | 10 | | | ns |
| | SI hold-time | | 0 | | | ns |
| TSS | Stop condition set-up time | | 16 | | | ns |

## 7.3 Digital audio interface timing - 4-wire control timing

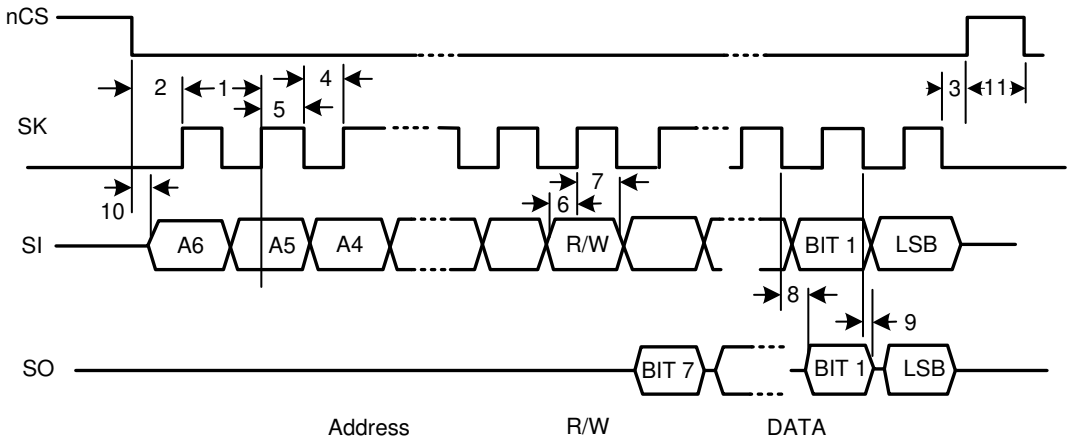


**Figure 6: 4-wire control timing diagram**

Timing shown is valid for active low and active high CS.

**Table 18: 4-wire control timing characteristics**

(Ta = -40 to +85ºC)

| Parameter | Description | Label in plot | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_C$ | Cycle time | 1 | 70 | | | ns |
| $t_{CSS}$ | Enable lead time | 2, from CS active to first SK edge | 20 | | | ns |
| $t_{SCS}$ | Enable lag time | 3, from last SK edge to CS idle | 20 | | | ns |
| $t_{CL}$ | Clock low time | 4 | 0.4 x $t_C$ | | | ns |
| $t_{CH}$ | Clock high time | 5 | 0.4 x $t_C$ | | | ns |
| $t_{SIS}$ | Data In setup time | 6 | 5 | | | ns |
| $t_{SIH}$ | Data In hold time | 7 | 5 | | | ns |
| $t_{SOV}$ | Data Out valid time | 8 | | | 22 | ns |
| $t_{SOH}$ | Data Out hold time | 9 | 6 | | | ns |
| $t_H$ | Data access time | 10 | | | 22 | ns |
| $t_{WCS}$ | CS inactive time | 11 | 20 | | | ns |

**Table 19: Start-up times after setting SC_MST_EN = 1**

| Source | Output | Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | VBG | VBG voltage >90% with 1 µF VBG capacitor | | 25 | | ms |
| All analogue inputs and DACL/R | HPL/R | Slave mode; 200 ms added delay required | 200 | 200 | | ms |
| All analogue inputs and DACL/R | HPL/R | 32 kHz PLL master mode; 200 ms added delay required | | 500 | | ms |
| All analogue inputs and DACL/R | OUT1L/R | Slave mode | | 250 | | ms |
| All analogue inputs | ADCL/R | Slave mode | | 200 | | ms |
| All analogue inputs | ADCL/R | 32 kHz PLL master mode | | 600 | | ms |