



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



General description

The DA7210 is a high fidelity audio codec with integrated true-ground capless headphone driver suitable for a variety of low power, digital portable audio products.

Featuring a high efficiency headphone amplifier and supporting economic single supply voltages down to 1.8 V, the ultra-low 2.5 mW power consumption extends music playback time for battery operated equipment.

Eight analogue input pins allow multiple audio sources to be internally mixed, eliminating the need for external switches. Both single-ended and fully-differential line and microphone inputs are supported with built-in variable gain amplifiers to optimise dynamic range prior to digitisation.

DA7210 provides simultaneous connection to stereo headphone, stereo line outputs, and a mono differential output. Stereo line outputs can be differential or single-ended. Both stereo outputs have volume control from -54 dB to +15 dB.

Filtering and gain control is performed digitally including 5-band EQ and a digital input AGC with programmable attack and decay parameters. A configurable signal processing engine allows various enhancements and effects on the digital audio signal like acoustic filtering, wind noise suppression and 3D sound.

The multi-slot I2S/PCM interface supports all common sample rates between 8 and 96 kHz in master or slave mode operation.

Key features

- Stereo multi-bit Delta Sigma DAC with SNR 100 dB ('A' weighted @ 48 kHz)
- Stereo multi-bit Delta Sigma ADC with SNR 96 dB ('A' weighted @ 48 kHz)
- Ultra low-power stereo headphone driver with
 - Stereo DAC to HP playback power: 2.5 mW
 - 2x58 mW output power (16 Ω)
 - 'Capless' output via GND centred signals
 - Four level charge pump with continuous tracking of audio signal (Class G)
 - Short circuit protection
- Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 and 96 kHz sample rates
- On-chip PLL with signal shaper and audio Sample Rate Matching
- Wide range of external clocks including industry standard 256xFs, system clock 12, 13, 24, 26 or 27 MHz and low power 32 kHz mode
- Audio serial data bus supports I2S, left/right justified, DSP and TDM modes
- Stereo or mono differential microphone interface
- Programmable ultra-low noise bias supply for electret microphones
- Volume controlled stereo auxiliary inputs and outputs supporting FM Radio and fixed gain speaker amplifiers
- Multi-mode audio routing and mixers
- Pop & click suppression circuitry
- ASSP DSP filter engine for digital audio enhancements (acoustic filtering, wind noise suppression, 5-band equaliser, 3D sound, automatic gain control)
- Supports supply from single voltage (1.8/2.5 V)
- Extensive modular power control
- Package: 49 bump WL-CSP – 0.4 mm pitch

Applications

- Personal media players
- Portable consumer devices
- Music handsets
- Personal navigation devices

Contents

General description	1
Key features	1
Applications	1
Contents	2
Figures	3
Tables	4
1 Terms and definitions	8
2 Block diagram	9
3 Pinout	10
3.1 The 49-ball DA7210 device.....	13
4 Absolute maximum ratings	14
5 Recommended operating conditions	14
6 Electrical characteristics	15
7 Timing characteristics	23
7.1 Digital audio interface timing - I2S/DSP (in master/slave mode).....	23
7.2 Digital audio control timing - 2-wire control timing	24
7.3 Digital audio interface timing - 4-wire control timing	25
8 Functional description	26
8.1 Stereo codec	26
8.1.1 Input signal chain	26
8.1.2 Microphone inputs	27
8.1.3 Auxiliary inputs.....	27
8.1.4 Stereo audio ADC.....	28
8.1.5 Automatic level control (ALC)	30
8.1.6 Noise gate.....	32
8.2 Output signal chain	32
8.2.1 Stereo audio DAC.....	32
8.2.2 Soft mute	33
8.2.3 Output mixer and line-out amplifier.....	34
8.2.4 Headphone amplifier.....	37
8.2.5 Ambient noise suppression	38
8.2.6 Digital signal processing engine	38
8.3 Programming the general purpose filter.....	40
8.4 Hi-Fi recording.....	41
8.4.1 5-band equaliser for recording path.....	41
8.4.2 Digital audio processing for the record path	44
8.5 Hi-Fi playback	45
8.5.1 5-band equaliser for playback path	45
8.5.2 Digital audio processing for playback path	45
8.6 Telephone/Bluetooth voice recording/playback at low sample rates	47
8.6.1 Voice filtering for recording at low sample rates.....	47
8.6.2 Voice filtering for playback at low sample rates	48
8.6.3 Digital audio processing for phone applications	50

9	INTERFACES	51
9.1	Digital audio interface (DAI)	51
9.1.1	Operation modes DAI interface	51
9.1.2	Right justified mode	52
9.1.3	Left justified mode.....	52
9.1.4	I2S mode	52
9.1.5	DSP mode	53
9.1.6	TDM mode	53
9.1.7	Clocking schemes.....	53
9.1.8	Master mode.....	55
9.1.9	Programming master and 32 kHz mode – PLL enabled	57
9.2	Slave mode	59
9.2.1	Conditions:.....	59
9.2.2	Programming slave mode – PLL not enabled	59
9.2.3	Programming slave mode – PLL enabled	61
9.2.4	32 kHz master or slave mode	63
9.2.5	Phase locked loop (PLL).....	63
9.2.6	Control interface	64
9.2.7	4-wire communication.....	65
9.2.8	2-wire communication.....	66
9.2.9	Details of the 2-wire control bus protocol	67
10	Register definitions	69
10.1	Register map.....	69
10.2	Control and status registers	72
10.3	Codec registers	74
10.4	GP filter engine	96
10.5	ALC level controls	107
11	Package information	110
11.1	Package outlines.....	110
11.2	Soldering information	110
12	Ordering information	110
13	Applications information	111
13.1	Supporting information.....	111
13.2	Minimum component recommendations	111
13.3	General component suggestions	112

Figures

Figure 1:	DA7210 block diagram	9
Figure 2:	DA7210 pad arrangement (bottom view ball side up).....	10
Figure 3:	DA7210 power supply topology	13
Figure 4:	I2S/DSP timing diagram	23
Figure 5:	2-wire control timing diagram	24
Figure 6:	4-wire control timing diagram	25
Figure 7:	Typical microphone applications	27
Figure 8:	ADC and DAC DC blocking (cut-off frequency setting '00' to '11', 16 kHz).....	29
Figure 9:	ADC pass band attenuation (audio mode, 48 kHz).....	29

Figure 10: ADC pass band suppression (audio mode, 48 kHz)	30
Figure 11: Operation of ALC.....	30
Figure 12: DAC DC blocking (cut-off frequency setting '00' to '11', 48 kHz).....	33
Figure 13: DAC pass band attenuation (audio mode, 48 kHz).....	34
Figure 14: DAC pass band suppression (audio mode, 48 kHz)	34
Figure 15: DA7210 audio signal paths	36
Figure 16: Digital signal processing engine (simplified block diagram)	39
Figure 17: Direct form I implementation of a second order IIR filter	39
Figure 18: Band 5 (LP 50 Hz) frequency response at FS = 48 kHz.....	42
Figure 19: Band 5 (BP 150 Hz) frequency response at FS = 48 kHz	42
Figure 20: Band 5 (BP 500 Hz) frequency response at FS = 48 kHz	43
Figure 21: Band 5 (BP 2500 Hz) frequency response at FS = 48 kHz	43
Figure 22: Band 5 (HP 5000 Hz) frequency response at FS = 48 kHz	43
Figure 23: Record only	44
Figure 24: Record with sound monitor	44
Figure 25: Stereo playback (for example, freefield headphone equalisation).....	45
Figure 26: Sound spatialiser for stereo speaker	46
Figure 27: Voice mode recording high-pass filter (cut-off frequency setting '000' to '111', 8 kHz)	47
Figure 28: Voice mode recording frequency response (setting '001', 8 kHz)	48
Figure 29: Voice mode recording stop band suppression (8 kHz)	48
Figure 30: Voice mode playback high-pass filter (cut-off frequency setting '000' to '111', 16 kHz)...	49
Figure 31: Voice mode playback frequency response (setting '001', 8 kHz)	49
Figure 32: Voice mode playback stop band suppression (8 kHz)	50
Figure 33: Transmit (red), receive (green) and sidetone (blue) sound filtering for phone applications	50
Figure 34: Right justified format	52
Figure 35: Left justified format.....	52
Figure 36: I2S format.....	52
Figure 37: DSP format.....	53
Figure 38: TDM left justified format	53
Figure 39: TDM DSP format.....	53
Figure 40: PLL master mode start up sequence	58
Figure 41: Non-PLL mode start-up sequence	61
Figure 42: PLL Slave mode start-up sequence	63
Figure 43: PLL block diagram.....	64
Figure 44: Schematic of a 4-wire and a 2-wire control bus.....	64
Figure 45: 4-wire host write and read timing (nCS_POL = '0', CPOL = '0', CPHA = '1')	66
Figure 46: 2-wire byte write (SI/DATA line).....	67
Figure 47: Examples of 2-wire byte read (SI/DATA line)	67
Figure 48: Examples of 2-wire page read (SI/DATA line)	68
Figure 49: 2-wire page write (SI/DATA line).....	68
Figure 50: 2-wire repeated write (SI/DATA line)	68
Figure 51: 49 bump WL-CSP 0.4mm pitch package outline drawing	110

Tables

Table 1: Pin description	10
Table 2: Pin type definition	12
Table 3: Absolute maximum ratings	14
Table 4: Recommended operating conditions	14
Table 5: Power dissipation table	15
Table 6: Electrical characteristics: Microphone bias	16
Table 7: Electrical characteristics: Input mixing units.....	16
Table 8: Electrical characteristics: Analogue to digital converter (ADC)	17
Table 9: Electrical characteristics: Digital to analogue converter (DAC).....	18
Table 10: Electrical characteristics: Line out and receiver amplifier	19
Table 11: Electrical characteristics: Line out amplifier	20
Table 12: Electrical characteristics: Dynamic charge pump.....	20

Table 13: Electrical characteristics: Headphone amplifier	21
Table 14: Electrical characteristics: Phase locked loop (MCLK)	22
Table 15: Electrical characteristics: Digital I/O	22
Table 16: I2S/DSP timing characteristics	23
Table 17: 2-wire control timing characteristics	24
Table 18: 4-wire control timing characteristics	25
Table 19: Start-up times after setting SC_MST_EN = 1	25
Table 20: ADC digital high pass filter specifications	28
Table 21: Permitted register values for ALC_NOIS (0x85 [5:0])	31
Table 22: DAC digital high pass filter specifications	33
Table 23: Headphone/OUT1 amplifier gain settings	37
Table 24: GP filter section enable bits	41
Table 25: Band-equaliser corner frequencies	41
Table 26: 5-band-equaliser turn-over/centre frequencies	41
Table 27: Voice mode recording high-pass filter specifications	47
Table 28: Voice mode playback high-pass filter specifications	49
Table 29: Internal system clock frequency	54
Table 30: Block enable and system standby bits	54
Table 31: ADC and DAC clock frequencies	55
Table 32: Master mode PLL-DIV look up table	56
Table 33: SRM mode PLL-DIV look up table	56
Table 34: PLL master mode register setting recommendations	57
Table 35: MCLK frequencies in non-PLL slave mode	59
Table 36: Non-PLL slave mode and PLL master mode sample rate settings	60
Table 37: SRM mode PLL division ratio settings	62
Table 38: Slave mode PLL-enabled register setting recommendations	62
Table 39: 4 wire interface	65
Table 40: 4 wire clock configurations	66
Table 41: Register map	69
Table 42: PAGE0 0x00	72
Table 43: CONTROL 0x01	72
Table 44: STATUS 0x02	72
Table 45: STARTUP 1 0x03	73
Table 46: STARTUP 2 0x04	73
Table 47: STARTUP 3 0x05	74
Table 48: MIC_L 0x07	74
Table 49: MIC_R 0x08	75
Table 50: AUX1_L 0x09	75
Table 51: AUX1_R 0x0A	75
Table 52: AUX2 0x0B	76
Table 53: IN_GAIN 0x0C	77
Table 54: INMIX_L 0x0D	78
Table 55: INMIX_R 0x0E	78
Table 56: ADC_HPF 0x0F	79
Table 57: ADC 0x10	79
Table 58: ADC_EQ1_2 0x11	80
Table 59: ADC_EQ3_4 0x12	81
Table 60: ADC_EQ5 0x13	82
Table 61: DAC_HPF 0x14	83
Table 62: DAC_L 0x15	83
Table 63: DAC_R 0x16	84
Table 64: DAC_SEL 0x17	84
Table 65: SOFTMUTE 0x18	85
Table 66: DAC_EQ1_2 0x19	86
Table 67: DAC_EQ3_4 0x1A	87
Table 68: DAC_EQ5 0x1B	88
Table 69: OUTMIX_L 0x1C	88
Table 70: OUTMIX_R 0x1D	89
Table 71: OUT1_L 0x1E	89

Table 72: OUT1_R 0x1F	90
Table 73: OUT2 0x20	90
Table 74: HP_L_VOL 0x21	91
Table 75: HP_R_VOL 0x22	91
Table 76: HP_CFG 0x23	92
Table 77: ZEROX 0x24	92
Table 78: DAI_SRC_SEL 0x25	93
Table 79: DAI_CFG1 0x26	93
Table 80: DAI_CFG2 0x27	94
Table 81: DAI_CFG3 0x28	94
Table 82: PLL_DIV1 0x29	94
Table 83: PLL_DIV2 0x2A	94
Table 84: PLL_DIV3 0x2B	95
Table 85: PLL 0x2C	96
Table 86: GP1A A0L 0x2D	96
Table 87: GP1A A0H 0x2E	96
Table 88: GP1B A0L 0x2F	97
Table 89: GP1B A0H 0x30	97
Table 90: GP2A A0L 0x31	97
Table 91: GP2A A0H 0x32	97
Table 92: GP2B_A0L 0x33	97
Table 93: GP2B_A0H 0x34	97
Table 94: GP1C_A0L 0x35	97
Table 95: GP1C_A0H 0x36	97
Table 96: GP1D_A0L 0x37	97
Table 97: GP1D_A0H 0x38	97
Table 98: GP2C_A0L 0x39	97
Table 99: GP2C_A0H 0x3A	98
Table 100: GP2D_A0L 0x3B	98
Table 101: GP2D_A0H 0x3C	98
Table 102: GP1A_A1L 0x3D	98
Table 103: GP1A_A1H 0x3E	98
Table 104: GP1B_A1L 0x3F	98
Table 105: GP1B_A1H 0x40	98
Table 106: GP2A_A1L 0x41	98
Table 107: GP2A_A1H 0x42	98
Table 108: GP2B_A1L 0x43	98
Table 109: GP2B_A1H 0x44	98
Table 110: GP1C_A1L 0x45	99
Table 111: GP1C_A1H 0x46	99
Table 112: GP1D_A1L 0x47	99
Table 113: GP1D_A1H 0x48	99
Table 114: GP2C_A1L 0x49	99
Table 115: GP2C_A1H 0x4A	99
Table 116: GP2D_A1L 0x4B	99
Table 117: GP2D_A1H 0x4C	99
Table 118: GP1A_A2L 0x4D	99
Table 119: GP1A_A2H 0x4E	99
Table 120: GP1B_A2L 0x4F	99
Table 121: GP1B_A2H 0x50	100
Table 122: GP2A_A2L 0x51	100
Table 123: GP2A_A2H 0x52	100
Table 124: GP2B_A2L 0x53	100
Table 125: GP2B_A2H 0x54	100
Table 126: GP1C_A2L 0x55	100
Table 127: GP1C_A2H 0x56	100
Table 128: GP1D_A2L 0x57	100
Table 129: GP1D_A2H 0x58	100
Table 130: GP2C_A2L 0x59	100

Table 131: GP2C_A2H 0x5A	100
Table 132: GP2D_A2L 0x5B	101
Table 133: GP2D_A2H 0x5C	101
Table 134: GP1A_B1L 0x5D	101
Table 135: GP1A_B1H 0x5E	101
Table 136: GP1B_B1L 0x5F	101
Table 137: GP1B_B1H 0x60	101
Table 138: GP2A_B1L 0x61	101
Table 139: GP2A_B1H 0x62	101
Table 140: GP2B_B1L 0x63	101
Table 141: GP2B_B1H 0x64	101
Table 142: GP1C_B1L 0x65	101
Table 143: GP1C_B1H 0x66	102
Table 144: GP1D_B1L 0x67	102
Table 145: GP1D_B1H 0x68	102
Table 146: GP2C_B1L 0x69	102
Table 147: GP2C_B1H 0x6A	102
Table 148: GP2D_B1L 0x6B	102
Table 149: GP2D_B1H 0x6C	102
Table 150: GP1A_B2L 0x6D	102
Table 151: GP1A_B2H 0x6E	102
Table 152: GP1B_B2L 0x6F	102
Table 153: GP1B_B2H 0x70	102
Table 154: GP2A_B2L 0x71	103
Table 155: GP2A_B2H 0x72	103
Table 156: GP2B_B2L 0x73	103
Table 157: GP2B_B2H 0x74	103
Table 158: GP1C_B2L 0x75	103
Table 159: GP1C_B2H 0x76	103
Table 160: GP1D_B2L 0x77	103
Table 161: GP1D_B2H 0x78	103
Table 162: GP2C_B2L 0x79	103
Table 163: GP2C_B2H 0x7A	103
Table 164: GP2D_B2L 0x7B	103
Table 165: GP2D_B2H 0x7C	104
Table 166: GPF_SRC1 0x7D	104
Table 167: GPF_SRC2 0x7E	105
Table 168: DSP_CFG 0x7F	105
Table 169: PAGE1 0x80	106
Table 170: CHIP_ID 0x81	106
Table 171: INTERFACE 0x82	106
Table 172: ALC_MAX 0x83	107
Table 173: ALC_MIN 0x84	107
Table 174: ALC_NOIS 0x85	107
Table 175: ALC_ATT 0x86	107
Table 176: ALC_REL 0x87	107
Table 177: ALC_DEL 0x88	107
Table 178: A_HID_UNLOCK 0x8A	108
Table 179: A_TST_UNLOCK 0x8B	108
Table 180: A_PLL0 0x8F	108
Table 181: A_PLL1 0x90	108
Table 182: A_ADC0 0x95	108
Table 183: A_DAC0 0x96	109
Table 184: A_CPHP6 0xA2	109
Table 185: A_CP_MODE 0xA7	109
Table 186: Ordering information	110

1 Terms and definitions

ADC	Analogue to Digital Converter
ALC	Automatic Level Control
ASSP	Application Specific Standard Product
DAC	Digital to Analogue Converter
DAI	Digital Audio Interface
DMIC	Digital microphone
DSP	Digital Signal Processor or Digital Signal Processing
FIR	Finite Impulse Response (Filter)
I2C	Inter-Integrated Circuit interface
I2S	Inter-IC Sound
IIR	Infinite Impulse Response (Filter)
GP	General Purpose (Filter)
LDO	Low Dropout regulator
MCLK	Master Clock
PCM	Pulse Code Modulation
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio
RDL	Redistribution Layer
RC	Resistance-Capacitance
SC	System Controller
SDM	Sigma Delta Modulator
SNR	Signal to Noise Ratio
SRM	Sample Rate Matching
TDM	Time Division Multiplexing
THD+N	Total Harmonic Distortion plus Noise
VCO	Voltage-Controlled Oscillator
WL-CSP	Wafer Level-Chip Scale Packaging

2 Block diagram

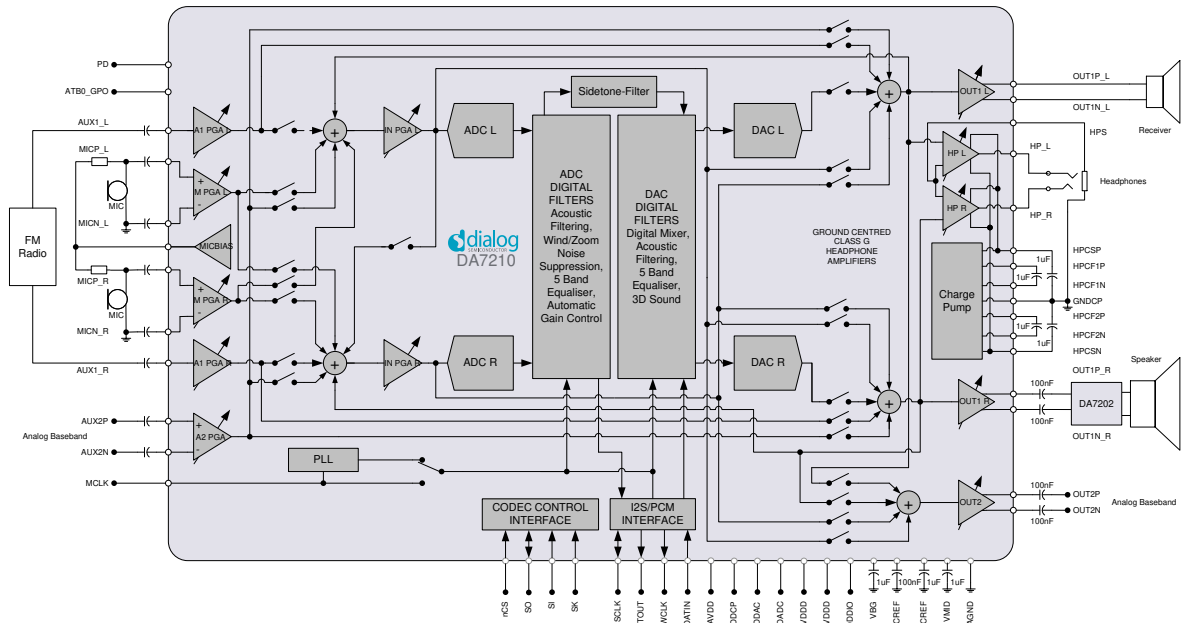


Figure 1: DA7210 block diagram

3 Pinout



Figure 2: DA7210 pad arrangement (bottom view ball side up)

Table 1: Pin description

Pin no.	Pin name	Type (Table 2)	Description
Supplies and references			
7A	AVDD	PS	Analogue supply (PLL, bias, etc)
2A	VDDDAC	PS	DAC and line output supplies
5B	VDDADC	PS	Mic input and ADC supplies
2F	VDDCP	PS	Charge pump supply
1G	XVDDD	PS	Digital supply (regulator input)
2G	VDDD	PS	Digital supply (1.5 V, if on-chip regulator is active)
3G	VDDDIO	PS	Digital supply for I/O
3A	DACREF	AI	Decoupling capacitor for DAC
4D	ADCREF	AI	Decoupling capacitor for ADC
6A	VMID	AI	Decoupling capacitor for VMID
5C	VBG	AI	Decoupling capacitor for VBG
5E	MICBIAS	AO	Current supply for microphone (2mA max)

Pin no.	Pin name	Type (Table 2)	Description
1A	GPO	AIO	General Purpose Output
6B	AGND	VSS	Analogue GND
3D	AGND1	VSS	Analogue GND
1E	GNDCP	VSS	Digital and charge pump ground, attached to paddle
Control			
5F	SO	DO	4-WIRE Data output
5G	SI	DIO	4-WIRE Data input/2-WIRE bidirectional Data
6G	SK	DI	4-WIRE/2-WIRE Clock
4F	nCS	DI	4-wire Chip select
4E	PD	DI	Power down signal (power down when high)
2B	HPS	AIO	Headphone Ground Sense
Digital Audio Interface			
4G	CLK	DIO	Digital Audio bit clock
3F	WCLK	DIO	Digital Audio left/right clock
7F	DATIN	DI	Digital Audio Data input
6F	DATOUT	DO	Digital Audio Data output
7G	MCLK	DI	Master clock input
Audio inputs/outputs			
6C	MICP_L	AI	Left channel differential microphone +ve input
7B	MICN_L	AI	Left channel differential microphone -ve input
7C	MICP_R	AI	Right channel differential microphone +ve input
6D	MICN_R	AI	Right channel differential microphone -ve input
5D	AUX1_L	AI	Left channel single-ended auxiliary input
6E	AUX1_R	AI	Right channel single-ended auxiliary input
7D	AUX2P	AI	2nd channel differential auxiliary +ve input
7E	AUX2N	AI	2nd channel differential auxiliary -ve input
4C	OUT1P_L	AO	Differential or single ended +ve line out left
5A	OUT1N_L	AO	Differential -ve line out left
4A	OUT1P_R	AO	Differential or single ended +ve line out right
4B	OUT1N_R	AO	Differential -ve line out right
3C	OUT2N	AO	2nd channel differential auxiliary -ve output
3B	OUT2P	AO	2nd channel differential auxiliary +ve output
1B	HP_L	AO	Left head phone amp output
2C	HP_R	AO	Right head phone amp output
Charge pump			
3E	HPCF1P	PS	Head phone amp charge pump floating cap1 +ve
1F	HPCF1N	PS	Head phone amp charge pump floating cap1 -ve
2E	HPCF2P	PS	Head phone amp charge pump floating cap2 +ve

Pin no.	Pin name	Type (Table 2)	Description
1D	HPCF2N	PS	Head phone amp charge pump floating cap2 -ve
1C	HPCSP	PS	Head phone amp charge pump storage cap +ve
2D	HPCSN	PS	Head phone amp charge pump storage cap -ve

Table 2: Pin type definition

Pin type	Description
AI	Analogue Input
AO	Analogue Output
AIO	Analogue Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PS	Power Supply
VSS	Power Supply

3.1 The 49-ball DA7210 device

On the DA7210, all supplies are accessible as external pins. The VDD pin is only required for capacitive decoupling. If the LDO is not required to supply the digital core voltage, the VDD supply should still be applied to the XVDD pin and the LDO should be disabled.

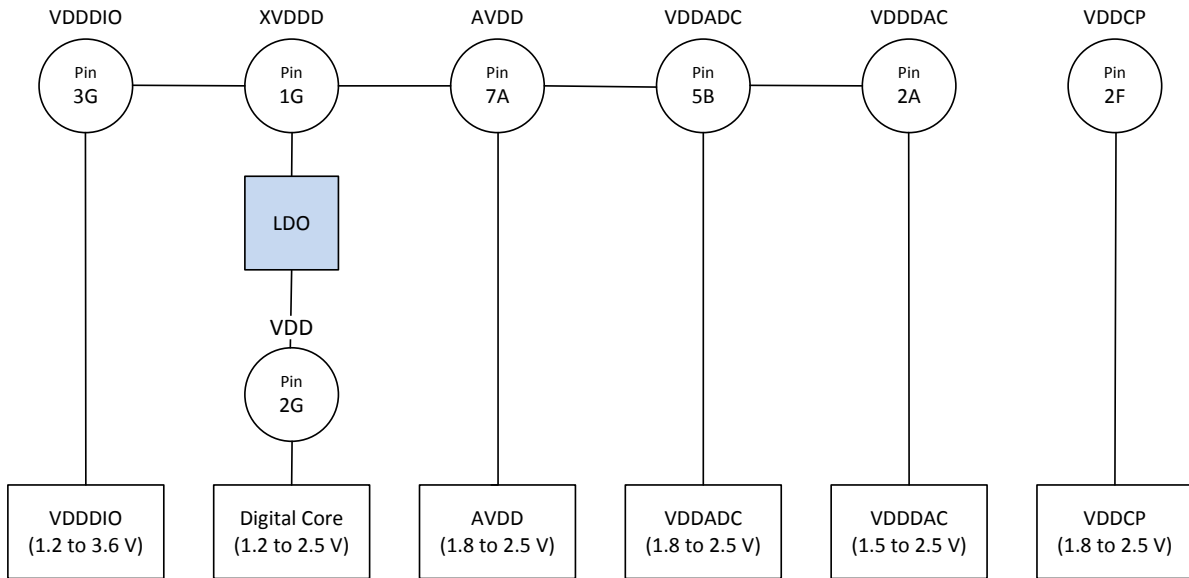


Figure 3: DA7210 power supply topology

4 Absolute maximum ratings

Table 3: Absolute maximum ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
	Storage temperature		-40	+95	°C
Ta	Operating temperature		-40	+85	°C
AVDD, VDDDAC, VDDADC, VDDD, VDDDIO	Power Supply Input		-0.3	2.75	V
VDDDIO		3.6 V mode	-0.3	3.6	V
	Supply voltage all input pins except power		-0.3	AVDD+ 0.3	V
	Maximum power dissipation			200	mW
	Package thermal resistance			40	k/W
	ESD susceptibility	Human body model		2	kV

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5 Recommended operating conditions

Table 4: Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Operating temperature		-40		+85	°C
VDDD	Supply voltage digital	Min and max values can accept +/-5% tolerances	1.2		2.5	V
VDDDIO	Supply voltage I/O	Min and max values can accept +/-5% tolerances	1.2		2.5	V
		3.6 V mode	2.65		3.6	V
AVDD, VDDADC, VDDDAC	Supply voltage analogue	Min and max values can accept +/-5% tolerances	1.8		2.5	V
VDDCP	Supply voltage headphone	Max value can accept +/-5% tolerances	1.8		2.5	V

6 Electrical characteristics

Table 5: Power dissipation table

Parameter	Description	Conditions (Note 2)	Min	Typ	Max	Unit
	All registers at default values	Powerdown		6		μA
	Digital playback to lineout	DACL/R to OUT1L/R		3.15		mW
	Digital playback to HP no load	DACL/R to HPL/R quiescent		2.54		mW
	Digital playback to HP with load	DACL/R to HPL/R 16 Ω load 0.1 mW		4.66		mW
	Analogue bypass to lineout	AUX1L/R to OUT1L/R		2.87		mW
	Analogue bypass to HP no load	AUX1L/R to HPL/R quiescent		2.43		mW
	Analogue bypass to HP with load	AUX1L/R to HPL/R 16 Ω load 0.1 mW		4.57		mW
	Microphone stereo record	MICL/R to ADCL/R		2.38		mW
	Mic one channel record and digital playback to lineout	MICR to ADCR and DACR to OUT2		3.10		mW
	Mic stereo record and digital playback to HP no load	MICL/R to ADCL/R and DACL/R to HPL/R quiescent		4.35		mW
	Mic stereo record and digital playback to HP with load	MICL/R to ADCL/R and DACL/R to HPL/R 16 Ω load 0.1 mW		6.49		mW

Note 2 SC_CLK_DIS, 0x03[7] = 1 for all measurements
VMID_BUFF_EN, 0x96[2:0] = 000 for all modes not using DAC

Test conditions: VDD=2.5 V, Ta=25°C, fs=48 kHz, 24-bit audio data unless specified otherwise

Table 6: Electrical characteristics: Microphone bias

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{BIAS}	Bias Voltage	No load, AVDD = 2.5 V No load, AVDD = 1.8 V	2.2 1.5	Pro-grammable	2.3 1.6	V
I _{BIAS}	Maximum Current	Voltage drop < 50 mV		2		mA
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	70 50			dB
V _N	Output Noise Voltage			5		μV _{RMS}
	Capacitive Load	I _{BIAS} < 100 μA, 100 μA < I _{BIAS} < 2 mA		100 200		pF

Table 7: Electrical characteristics: Input mixing units

(MICP_L, MICN_L, AUX_L, MICP_R, MICN_R, AUX1_R, AUX2P, AUX2N)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{MAX}	Full-scale Input Signal	single-ended differential MIC-PGA=0 dB IN-PGA=0 dB		0.8*AVDD 1.6*AVDD		V _{PP}
R _{IN}	Input resistance	Mic, meas. single ended AUX1 AUX2	12 6 24	15 variable 30	18 40 36	kΩ
	Frequency Response	+/- 0.5 dB	20		20k	Hz
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain Note 3	M-PGA AUX1-PGA AUX2-PGA IN-PGA	-6 -48 -6 -4.5		24 21 12 18	dB
	Programmable Gain Step Size	M-PGA, AUX2-PGA AUX1-PGA, IN-PGA		6 1.5		dB
	Absolute Gain Accuracy	0 dB @ 1 kHz	-1.0		1.0	dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.1		0.1	dB
V _{NOISE}	Input Noise Level	Inputs connected to GND A-weighting input referred, measured @ ADC output Mic (Gain = 42 dB) AUX1 (Gain = 21 dB) AUX2 (Gain = 18 dB)		5 6.5 8.8		μV _{RMS}
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz, single ended input	80 70			dB

Note 3 The gain describes the ratio of input and output signal level at the related amplifier stage (independent of whether the connection is single ended or differential).

Table 8: Electrical characteristics: Analogue to digital converter (ADC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{MAX}	Full-scale Input Signal	Corresponding digital level 0 dBFS		1.6* AVDD		V _{PP}
SNR	Signal to Noise Ratio	A-weighting, no input selected		96		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS		-89		dB
	Channel separation			90		dB
B _{PASS}	Pass band				0.45*fs	kHz
B _{STOP}	Stop band	fs ≤ 48 kHz fs = 88.2/96 kHz	0.56*fs		7*fs 3.5*fs	kHz
	Pass band Ripple	Voice Mode Music Mode			+/-0.3 +/-0.1	dB
	Stop band Attenuation	Voice Mode Music Mode	70 55			dB
	Group delay	Voice Mode Music Mode (Note 4) fs = 88.2/96 kHz		4.3/fs 18/fs 9/fs	600	µs
	Group delay mismatch	Between left and right channel			2	µs
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	80 70			dB

Note 4 5-band-equaliser disabled.

Table 9: Electrical characteristics: Digital to analogue converter (DAC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{MAX}	Full-scale Output Signal	Corresponding digital level 0 dBFS		1.6* V _{DDDAC}		V _{PP}
SNR	Signal to Noise Ratio	A weighting		102		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS		-90		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS, 32 kHz PLL mode		-80		dB
	Channel separation			90		dB
B _{PASS}	Pass band				0.45*fs	kHz
B _{STOP}	Stop band	fs ≤ 48 kHz fs = 88.2/96 kHz	0.56*fs		7.5*fs 3.5*fs	kHz
	Pass band Ripple	Voice Mode Music Mode			±0.15 ±0.1	dB
	Stop band Attenuation	Voice Mode Music Mode	70 55			dB
	Group delay	Voice Mode Music Mode fs = 88.2/96 kHz		4.8/fs 18.5/fs 9/fs	650	µs
	Group delay variation	20 Hz to 20 kHz			1	µs
	Group delay mismatch	Between left and right channel			2	µs
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	70 60			dB

Table 10: Electrical characteristics: Line out and receiver amplifier

(OUT1P_L, OUT1N_L, OUT1P_R, OUT1N_R)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{MAX}	Full-scale Input Signal	No load, single-ended No load, differential		0.8*AVDD 1.6 *AVDD		V _{PP}
	Load Impedance	single-ended output mode	500	2k	1 200	Ω μH pF
		differential output mode	25	32	1 200	Ω μH pF
	Frequency Response	+/- 0.5 dB	20		20k	Hz
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain		-54		15	dB
	Mute Attenuation			100		dB
	Programmable Gain Step Size			1.5		dB
	Absolute Gain Accuracy	0 dB @ 1 kHz	-0.8		0.8	dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.1		0.1	dB
SNR	Signal to Noise Ratio	A weighting		102		dB
V _{NOISE}	Output Noise Level	20 - 20 kHz, unweighted gain < -15 dB single-ended differential		<5.5 <4.5		μV
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS, 44.1 kHz slave mode non A-weighting		-90		
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz single-ended output	70 47			dB
		20 Hz - 2 kHz 2 kHz - 20 kHz differential output	90 70			dB

Table 11: Electrical characteristics: Line out amplifier

(OUT2P, OUT2N)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{MAX}	Full-scale Input Signal	No load		1.6*AVDD		V _{PP}
	Load Impedance		25	32	1 200	Ω μH pF
	Frequency Response	+/- 0.5 dB	20		20k	Hz
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain		-18		6	dB
	Programmable Gain Step Size			6		dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.2		0.2	dB
SNR	Signal to Noise Ratio	A-weighting, gain = 0 dB		102		dB
V _{NOISE}	Output Noise Level	20 -20 kHz, unweighed Gain < -15 dB, gain ≤ -12 dB		<5		μV
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS , A-weighting		-90		
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	90 70			dB

Table 12: Electrical characteristics: Dynamic charge pump

(HPCSP, HPCSN)

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDDCSP	Positive dynamic supply voltage	VDDCP/3/4 can optionally be enabled if two flying caps are available		VDDCP VDDCP/2 (VDDCP/3, VDDCP/4)		
VDDCSN	Negative dynamic supply voltage	-VDDCP/3/4 can optionally be enabled if two flying caps are available		-VDDCP -VDDCP/2 (-VDDCP/3, -VDDCP/4)		
	Floating capacitors			1.0		μF
	Storage capacitors			1.0		μF

Table 13: Electrical characteristics: Headphone amplifier
(HPL, HPR)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{MAX}	Full-scale Output Signal	No load		1.6*VDD CP		V _{PP}
	DC output offset			100		μV
P _{MAX}	Output Power per channel	VDDCP = 1.8 V, THD < 0.1%, R _L =16 Ω 1 kHz		28		mW _{RMS}
		VDDCP = 2.5 V, THD < 0.1%, R _L =16 Ω 1 kHz		58		mW _{RMS}
	Dynamic internal supply voltages	VDD/3 or VDD/4 can optionally be selected if two flying caps are available		±VDD ±VDD/2 (±VDD/3 (±VDD/4)		
IQ	Quiescent current per channel	from VDDCP		100		uA
	Load Impedance	13 < R _L < ∞	13	16	400 500	Ω μH pF
	Frequency Response	+/- 0.5 dB	20		20k	
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain		-54		15	dB
	Mute Attenuation			100		dB
	Programmable Gain Step Size			1.5		dB
	Absolute Gain Accuracy	0 dB @ 1 kHz	-0.8		0.8	dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.1		0.1	dB
SNR	Signal to Noise Ratio	A weighting, gain = 0 dB		100		dB
V _{NOISE}	Output Noise Level	20 to 20 kHz, unweighted, gain < -15 dB		<4.5		μV _{rms}
THD+N	Total Harmonic Distortion Plus Noise	VDDCP = 1.8 V, -5 dBFS, R _L =16 Ω		-80		dB
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz	70			dB
		2 kHz - 20 kHz	50			
	Output power per channel	VDDCP=2.5 V, THD<1%, R _L =16 Ω, 1 kHz		72		mW

Table 14: Electrical characteristics: Phase locked loop (MCLK)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Input Jitter	cycle to cycle			35	ps
		rms			100	ps
	Input Impedance	DC impedance > 10 MΩ	300	1	2	Ω
			0.5			pF
Interface mode (MCLK is 256 Fs, PLL off)						
F _{in}	Input frequency	256 Fs 128 Fs (96 kHz)	11.289		12.288	MHz
Oscillator mode (MCLK from standard oscillator, PLL on)						
F _{in}	Input frequency	12.0, 13.0, 13.5, 14.4, 19.2, 19.68 MHz (x 1, 2 or 4), 32 kHz mode	10	32.768	80	MHz
					kHz	
	I2S tracking range (SRM)	Maximum mismatch of I2S word-clock			4	%
	I2S clock drift	Maximum frequency drift of I2S word clock			50	ppm/s
V _{IN AC}	MCLK Shaper range	For AC coupling with internal clock shaping	300	500	1000	mV _{PP}

Table 15: Electrical characteristics: Digital I/O

(T_a = -40 to +85°C)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{IH}	CLK, WCLK, DATIN, SK, nCS, SI, PD, MCLK, Input High Voltage		0.7*V _{DDIO}		V _{DDIO}	V
V _{IL}	CLK, WCLK, DATIN, SK, nCS, SI, PD, MCLK, Input Low Voltage		-0.3		0.3*V _{DDIO}	V
V _{OH @} 1 mA	CLK, WCLK, DATOUT Output High Voltage		0.8*V _{DDIO}		V _{DDIO}	V
V _{OH}	SO (open drain mode) Output High Voltage			OPEN DRAIN	3.6	V
V _{OL @} 1 mA	CLK, WCLK, DATOUT Output Low Voltage		0		0.3	V
	MCLK Input High Voltage	DC-coupled TTL signal	0.7*V _{DDIO}		V _{DDIO}	V
	MCLK Input Low Voltage		-0.3		0.3*V _{DDIO}	V

7 Timing characteristics

7.1 Digital audio interface timing - I2S/DSP (in master/slave mode)

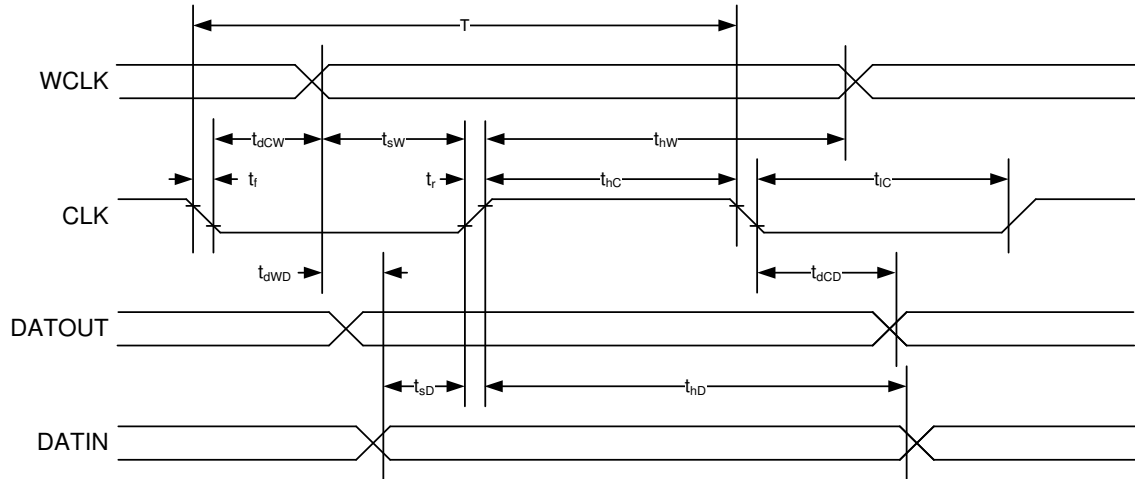


Figure 4: I2S/DSP timing diagram

Table 16: I2S/DSP timing characteristics

($T_a = -40$ to $+85^\circ\text{C}$)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Input impedance	DC impedance > 10 M Ω	300 1.0		2.5	Ω pF
T	CLK period		75			ns
t_r	CLK rise time				8	ns
t_f	CLK fall time				8	ns
t_{hC}	CLK high period		40%		60%	T
t_{lC}	CLK low period		40%		60%	T
t_{dCW}	CLK to WCLK delay		-30%		+30%	T
t_{dCD}	CLK to DATOUT delay		-30%		+30%	T
t_{hW}	WCLK high time	DSP mode	100%			T
		Non-DSP mode	Word length			T
t_{lW}	WCLK low time	DSP mode	100%			T
		Non-DSP mode	Word length			T
t_{sW}	WCLK setup time	Slave mode	7			ns
t_{hW}	WCLK hold time	Slave mode	2			ns
t_{sD}	DATIN setup time		7			ns
t_{hD}	DATIN hold time		2			ns
t_{dWD}	DATOUT to WCLK delay		DATOUT is synchronised to CLK			

7.2 Digital audio control timing - 2-wire control timing

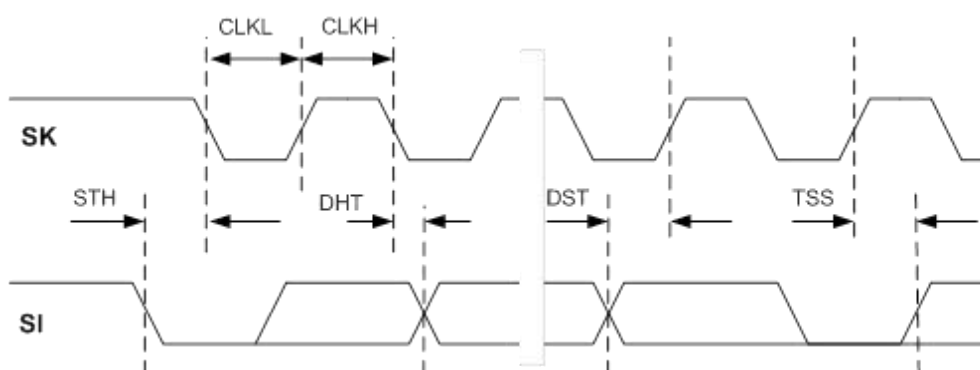


Figure 5: 2-wire control timing diagram

Table 17: 2-wire control timing characteristics

(Ta = -40 to +85°C)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Bus free time STOP to START		1.3			µs
	Bus Line Capacitive load				100	pF
Standard/Fast Mode						
	SK clock frequency		1		400	kHz
	Bus free time STOP to START		1.3			µs
	Start condition set-up time		0.6			µs
STH	Start condition hold time		0.6			µs
CLKL	SK low time		1.3			µs
CLKH	SK high time		0.6			µs
	2-wire SK and SI rise/fall time				300	ns
DST	SI set-up time		100			ns
DHT	SI hold-time		0			ns
TSS	Stop condition set-up time		0.6			µs
High Speed Mode						
	SK clock frequency		1		1700	kHz
	Start condition set-up time		160			ns
STH	Start condition hold time		160			ns
CLKL	SK low time		160			ns
CLKH	SK high time		60			ns
	HS-2-wire SK rise/fall time				40	ns
	HS-2-wire SI rise/fall time				80	ns
DST	SI set-up time		10			ns
	SI hold-time		0			ns
TSS	Stop condition set-up time		16			ns

7.3 Digital audio interface timing - 4-wire control timing

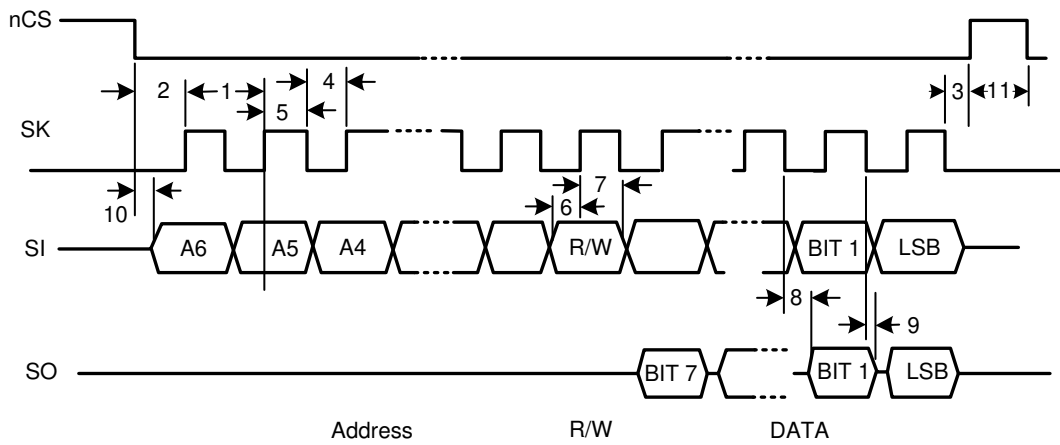


Figure 6: 4-wire control timing diagram

Timing shown is valid for active low and active high CS.

Table 18: 4-wire control timing characteristics

(Ta = -40 to +85°C)

Parameter	Description	Label in plot	Min	Typ	Max	Unit
t _c	Cycle time	1	70			ns
t _{css}	Enable lead time	2, from CS active to first SK edge	20			ns
t _{scs}	Enable lag time	3, from last SK edge to CS idle	20			ns
t _{CL}	Clock low time	4	0.4 x t _c			ns
t _{CH}	Clock high time	5	0.4 x t _c			ns
t _{sis}	Data In setup time	6	5			ns
t _{sih}	Data In hold time	7	5			ns
t _{sov}	Data Out valid time	8			22	ns
t _{soh}	Data Out hold time	9	6			ns
t _H	Data access time	10			22	ns
t _{wcs}	CS inactive time	11	20			ns

Table 19: Start-up times after setting SC_MST_EN = 1

Source	Output	Comment	Min	Typ	Max	Unit
	VBG	VBG voltage >90% with 1 μF VBG capacitor		25		ms
All analogue inputs and DACL/R	HPL/R	Slave mode; 200 ms added delay required	200	200		ms
All analogue inputs and DACL/R	HPL/R	32 kHz PLL master mode; 200 ms added delay required		500		ms
All analogue inputs and DACL/R	OUT1L/R	Slave mode		250		ms
All analogue inputs	ADCL/R	Slave mode		200		ms
All analogue inputs	ADCL/R	32 kHz PLL master mode		600		ms