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General description

DA7211 features a high fidelity and powerful 72 mW per channel headphone amplifier. The device may be operated from a single 1.8 V supply. Total device consumption is only 2.5 mW which helps extend music playback time for battery operated equipment.

The fully integrated fractional PLL has been designed to use minimal power while supporting a wide range of input and output frequencies. Internal suppression circuits help maintain audio synchronisation in the presence of system noise on the external clock.

Six analogue input pins allow multiple audio sources to be internally mixed, eliminating the need for external switches. Both single-ended and fully-differential line and microphone inputs are supported with built-in variable gain amplifiers to optimise the dynamic range prior to digitisation. This provides hardware support for ambient noise cancellation.

The DA7211 provides two volume-controlled differential/single-ended stereo line-out drivers and ground-centred stereo amplifiers to directly drive standard 3-wire 16 Ω headphones. For example the dc coupled, dedicated pop-free drivers may be connected simultaneously to stereo headphones, stereo speakers and a mono line out without external switches.

All filtering functions are performed digitally including 5-band EQ and a digital input AGC with programmable attack and decay parameters. A configurable signal processing engine allows various audio enhancements and effects such as acoustic filtering, transducer equalisation, wind noise suppression and 3D sound

The multi-slot I2S/PCM interface supports all common sample rates between 8 and 96 kHz in master or slave mode operation.

Key features

- Stereo multi-bit Delta Sigma DAC with SNR 100 dB ('A' weighted @ 48 kHz)
- Stereo multi-bit Delta Sigma ADC with SNR 96 dB ('A' weighted @ 48 kHz)
- Ultra low-power stereo headphone driver with
  - Stereo DAC to HP playback power: 2.5 mW
  - 2x58 mW output power (16 Ω)
  - 'Capless' output via GND centred signals
  - Four level charge pump with continuous tracking of audio signal (Class G)
  - Short circuit protection
- Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 and 96 kHz sample rates
- On-chip PLL with signal shaper and audio Sample Rate Matching
- 2-wire software control interface
- Audio serial data bus supports I2S, left/right justified, DSP and TDM modes
- Stereo or mono differential microphone interface
- Programmable ultra-low noise bias supply for electret microphones
- Volume controlled stereo auxiliary inputs and outputs supporting FM Radio and fixed gain speaker amplifiers
- Multi-mode audio routing and mixers
- Pop & click suppression circuitry
- ASSP DSP filter engine for digital audio enhancements (acoustic filtering, wind noise suppression, 5-band equaliser, 3D sound, automatic gain control)
- Supports supply from single voltage (1.8/2.5 V)
- Extensive modular power control
- Package: 36 bump WL-CSP 3x3 – 0.5 mm pitch

Applications

- Personal media players
- Portable consumer devices
- Music handsets
- Personal navigation devices

Contents

Figures

Tables

1 Terms and definitions

ADC	Analogue to Digital Converter
ALC	Automatic Level Control
ASSP	Application Specific Standard Product
DAC	Digital to Analogue Converter
DAI	Digital Audio Interface
DMIC	Digital microphone
DSP	Digital Signal Processor or Digital Signal Processing
FIR	Finite Impulse Response (Filter)
I2C	Inter-Integrated Circuit interface
I2S	Inter-IC Sound
IIR	Infinite Impulse Response (Filter)
GP	General Purpose (Filter)
LDO	Low Dropout regulator
MCLK	Master Clock
PCM	Pulse Code Modulation
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio
RDL	Redistribution Layer
RC	Resistance-Capacitance
SC	System Controller
SDM	Sigma Delta Modulator
SNR	Signal to Noise Ratio
SRM	Sample Rate Matching
TDM	Time Division Multiplexing
THD+N	Total Harmonic Distortion plus Noise
VCO	Voltage-Controlled Oscillator
WL-CSP	Wafer Level-Chip Scale Packaging

2 Block diagram

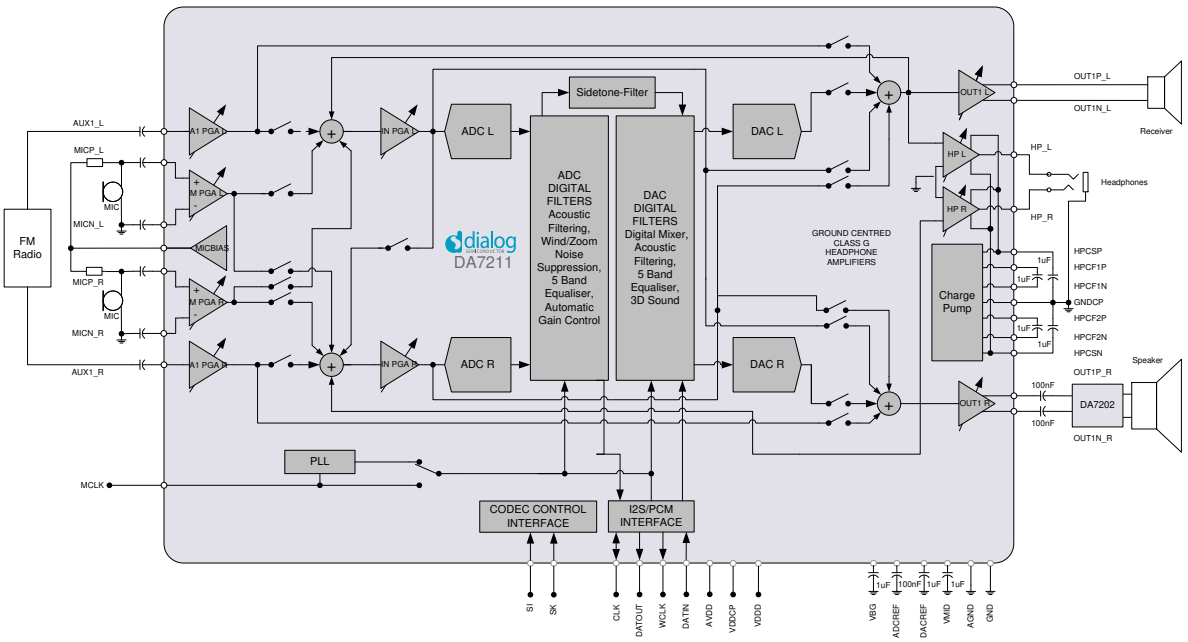

Figure 1: DA7211 block diagram

3 Pinout

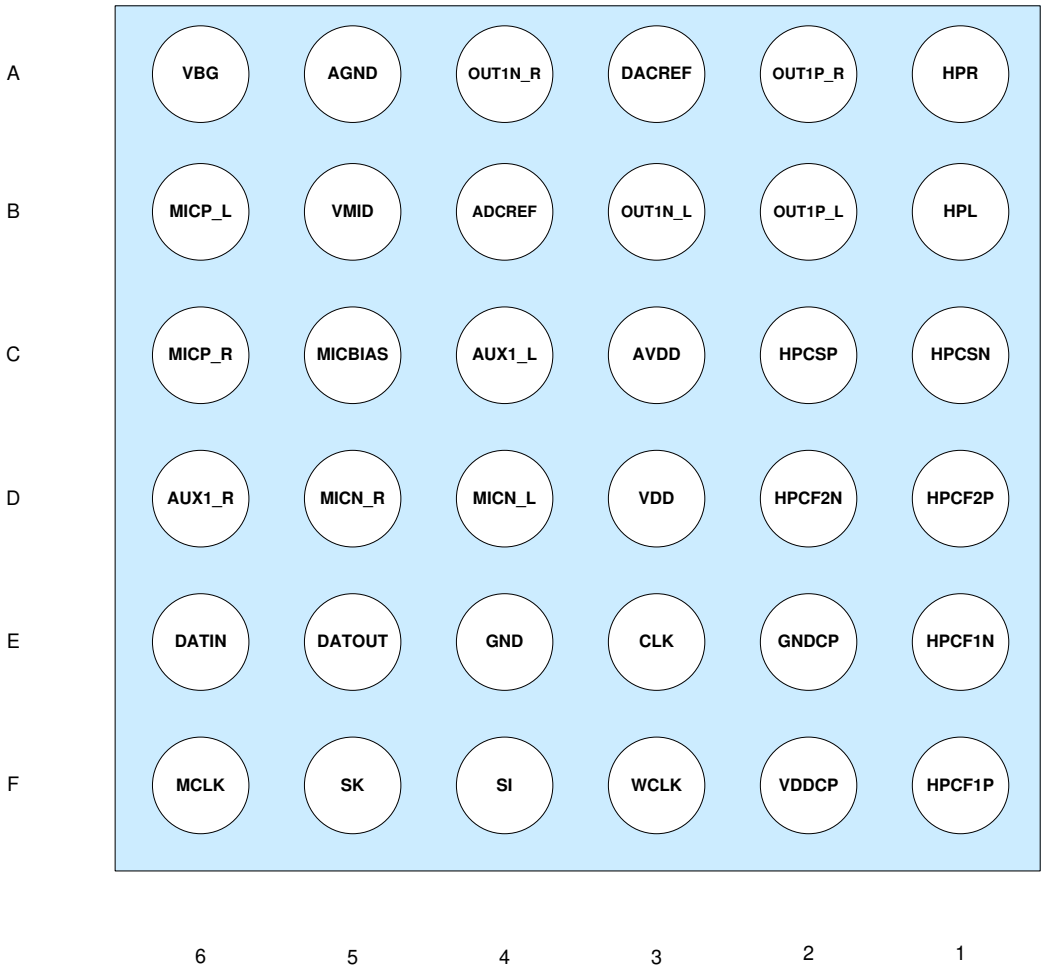

Figure 2: DA7211 pad arrangement (bottom view ball side up)

Table 1: Pin description

Pin no.	Pin name	Description
5A	AGND	Analogue ground
3C	AVDD	Analogue supply
3D	VDD	Digital and input supply
4C	AUX1_L	Left channel single-ended auxiliary input
6B	MICP_L	Left channel differential microphone +ve input
4D	MICN_L	Left channel differential microphone –ve input
5C	MICBIAS	Current supply for microphone
6C	MICP_R	Right channel differential microphone +ve input
5D	MICN_R	Right channel differential microphone -ve input
6D	AUX1_R	Right channel single-ended auxiliary input
6F	MCLK	Master clock input (reference to PLL)
6E	DATIN	I2S digital data input

Pin no.	Pin name	Description
5E	DATOUT	I2S digital data output
5F	SK	Digital clock for 2-wire
4F	SI	2-wire input and open drain output
3E	CLK	Digital bit clock for I2S
3F	WCLK	Digital word clock for I2S
2F	VDDCP	Headphone charge pump supply
1F	HPCF1P	Head phone amp charge pump floating cap1 +ve
1E	HPCF1N	Head phone amp charge pump floating cap1 –ve
2E	GNDCP	Headphone and digital ground
1D	HPCF2P	Head phone amp charge pump floating cap2 +ve
2D	HPCF2N	Head phone amp charge pump floating cap2 –ve
1C	HPCSN	Head phone amp charge pump storage cap –ve
2C	HPCSP	Head phone amp charge pump storage cap +ve
1B	HPL	Left head phone amp output
1A	HPR	Right head phone amp output
4E	GND	Ground bump
3A	DACREF	Decoupling capacitor for DAC
2A	OUT1P_R	Differential or single ended +ve line out right
4A	OUT1N_R	Differential –ve line out right
2B	OUT1P_L	Differential or single ended +ve line out left
3B	OUT1N_L	Differential –ve line out left
4B	ADCREF	Decoupling capacitor for ADC
5B	VMID	Decoupling capacitor for VMID
6A	VBG	Decoupling capacitor for VBG

3.1 The 36-ball DA7211 device

The VDDIO and the digital core supplies are joined in the RDL layer, so the internal LDO is unusable and should remain disabled. Separating the digital supply voltages from the AVDD allows a digital supply as low as 1.2 V to be used.

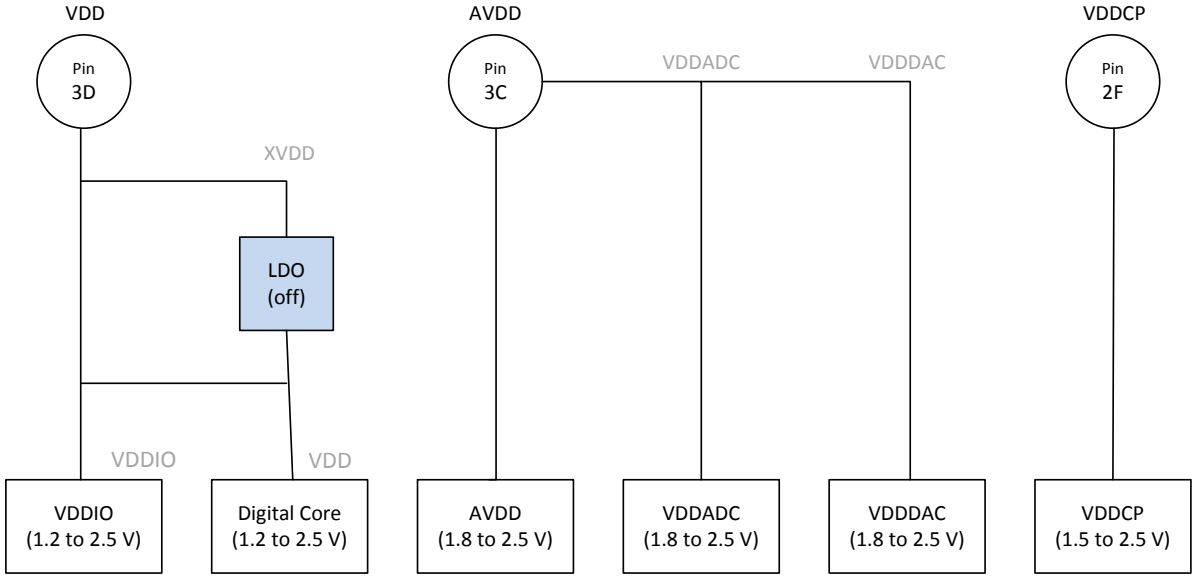

Figure 3: DA7211 power supply topology

4 Absolute maximum ratings

Table 2: Absolute maximum ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
	Storage temperature		-40	+95	°C
Ta	Operating temperature		-40	+85	°C
AVDD VDDCP	Power Supply Input		-0.3	2.75	V
	Supply voltage all input pins except power		-0.3	AVDD+ 0.3	V
	Maximum power dissipation			200	mW
	Package thermal resistance			40	k/W
	ESD susceptibility	Human body model		2	kV

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5 Recommended operating conditions

Table 3: Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Operating temperature		-40		+85	°C
VDD	Supply voltage digital and I/O	Min and max values can accept +/-5% tolerances	1.2		2.5	V
AVDD	Supply voltage analogue	Min and max values can accept +/-5% tolerances	1.8		2.5	V
VDDCP	Supply voltage headphone	Max value can accept +/-5% tolerances	1.8		2.5	V

6 Electrical characteristics

Table 4: Power dissipation table

Parameter	Description	Conditions (Note 2)	Min	Typ	Max	Unit
	All registers at default values	Powerdown		6		µA
	Digital playback to lineout	DACL/R to OUT1L/R		3.15		mW
	Digital playback to HP no load	DACL/R to HPL/R quiescent		2.54		mW
	Digital playback to HP with load	DACL/R to HPL/R 16 Ω load 0.1 mW		4.66		mW
	Analogue bypass to lineout	AUX1L/R to OUT1L/R		2.87		mW
	Analogue bypass to HP no load	AUX1L/R to HPL/R quiescent		2.43		mW
	Analogue bypass to HP with load	AUX1L/R to HPL/R 16 Ω load 0.1 mW		4.57		mW
	Microphone stereo record	MICL/R to ADCL/R		2.38		mW
	Mic one channel record and digital playback to lineout	MICR to ADCR		3.10		mW
	Mic stereo record and digital playback to HP no load	MICL/R to ADCL/R and DACL/R to HPL/R quiescent		4.35		mW
	Mic stereo record and digital playback to HP with load	MICL/R to ADCL/R and DACL/R to HPL/R 16 Ω load 0.1 mW		6.49		mW

Note 2 SC_CLK_DIS, 0x03[7] = 1 for all measurements
VMID_BUFF_EN, 0x96[2:0] = 000 for all modes not using DAC
AVDD and VDDCP = 1.8 V. Internal regulator configured for 1.2 V, 0xB7 [5:4] = 11

Table 5: Power consumption figures 1:

AVDD and VDDCP = 1.8 V (Note 3)

DA7211	Current (mA)			Power (mW)			
	AVDD 1.8 V	VDDCP 1.8 V	VDD 1.2 V	AVDD	VDDCP	VDD	Total
Powerdown	0.005	0	0.006	0.009	0	0.007	0.016
DACL/R to HPL/R quiescent no load Class G On	0.303	0.191	0.686	0.545	0.344	0.823	1.712
DACL/R to HPL/R 16 Ω load 0.1 mW Class G On	0.336	1.357	0.726	0.605	2.443	0.871	3.918
DACL/R to HPL/R "Love Comes Around" 16 Ω	0.298	0.279	0.731	0.536	0.503	0.877	1.915
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC	0.331	0.365	0.84	0.595	0.657	1.008	2.26
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC & PLL	0.762	0.365	1.13	1.372	0.657	1.356	3.385
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC & MICBIAS (2 k load,1.5 V) & PLL	0.776	0.365	1.13	1.397	0.657	1.356	3.41

Table 6: Power consumption figures 2:

AVDD and VDDCP = 2.5 V (Note 3)

DA7211	Current (mA)			Power (mW)			
	AVDD 2.5 V	VDDCP 2.5 V	VDD 1.2 V	AVDD	VDDCP	VDD	Total
Powerdown	0.303	0.204	0.685	0.758	0.509	0.822	2.089
DACL/R to HPL/R quiescent no load Class G On	0.336	1.416	0.724	0.839	3.54	0.869	5.248
DACL/R to HPL/R 16 Ω load 0.1 mW Class G On	0.306	0.306	0.728	0.765	0.764	0.874	2.403
DACL/R to HPL/R "Love Comes Around" 16 Ω	0.311	0.3	0.833	0.777	0.75	1	2.527
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC	0.824	0.298	1.01	2.06	0.745	1.212	4.017
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC & PLL	0.832	0.298	1.003	2.08	0.745	1.204	4.029
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC & MICBIAS (2 k load,1.5 V) & PLL	0.303	0.204	0.685	0.758	0.509	0.822	2.089

Note 3 Corinne Bailey Rae, 'Love Comes Around' 44.1 kHz, volume referenced to a 0.1 mW sine wave. The gain from a pure sine wave input is adjusted to give 0.1 mW output. Power consumption measurements are then made while playing the music track played at the same volume.

Test conditions: VDD=2.5 V, Ta=25°C, fs=48 kHz, 24-bit audio data unless specified otherwise

Table 7: Electrical characteristics: Microphone bias

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BIAS}	Bias Voltage	No load, AVDD = 2.5 V No load, AVDD = 1.8 V	2.2 1.5	Pro-grammable	2.3 1.6	V
I_{BIAS}	Maximum Current	Voltage drop < 50 mV		2		mA
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	70 50			dB
V_N	Output Noise Voltage			5		μV_{RMS}
	Capacitive Load	I_{BIAS} < 100 µA, 100 µA < I_{BIAS} < 2 mA		100 200		pF

Table 8: Electrical characteristics: Input mixing units

(MICP_L, MICN_L, AUX_L, MICP_R, MICN_R, AUX1_R)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Input Signal	single-ended differential MIC-PGA=0 dB IN-PGA=0 dB		0.8*AVDD 1.6*AVDD		V_{PP}
R_{IN}	Input resistance	Mic, single-ended AUX1	12 6	15 variable	18 40	kΩ
	Frequency Response	+/- 0.5 dB	20		20k	Hz
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain Note 4	MIC-PGA AUX1-PGA IN-PGA	-6 -48 -4.5		24 21 18	dB
	Programmable Gain Step Size	MIC-PGA AUX1-PGA, IN-PGA		6 1.5		dB
	Absolute Gain Accuracy	0 dB @ 1 kHz	-1.0		1.0	dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.1		0.1	dB
V_{NOISE}	Input Noise Level	Inputs connected to GND A-weighting input referred, measured @ ADC output Mic (Gain = 42 dB) AUX1 (Gain = 21 dB)		 5 6.5		μV_{RMS}
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz, single-ended input	80 70			dB

Note 4 The gain describes the ratio of input and output signal level at the related amplifier stage (independent of whether the connection is single ended or differential).

Table 9: Electrical characteristics: Analogue to digital converter (ADC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Input Signal	Corresponding digital level 0 dBFS		1.6* AVDD		V_{PP}
SNR	Signal to Noise Ratio	A-weighting, no input selected		96		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS		-89		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS, 32 kHz PLL mode		-80		dB
	Channel separation			90		dB
B_{PASS}	Pass band				0.45*fs	kHz
B_{STOP}	Stop band	fs ≤ 48 kHz fs = 88.2/96 kHz	0.56*fs		7*fs 3.5*fs	kHz
	Pass band Ripple	Voice Mode Music Mode			+/-0.3 +/-0.1	dB
	Stop band Attenuation	Voice Mode Music Mode	70 55			dB
	Group delay	Voice Mode Music Mode (Note 5) fs= 88.2/96 kHz		4.3/fs 18/fs 9/fs	600	µs
	Group delay mismatch	Between left and right channel			2	µs
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	80 70			dB

Note 5 5-band-equaliser disabled.

Table 10: Electrical characteristics: Digital to analogue converter (DAC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Output Signal	Corresponding digital level 0 dBFS		1.6*AVDD		V_{PP}
SNR	Signal to Noise Ratio	A weighting		102		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS		-85		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS, 32 kHz PLL mode		-80		dB
	Channel separation			90		dB
B_{PASS}	Pass band				0.45*fs	kHz
B_{STOP}	Stop band	fs ≤ 48 kHz fs = 88.2/96 kHz	0.56*fs		7*fs 3.5*fs	kHz
	Pass band Ripple	Voice Mode Music Mode			±0.15 ±0.1	dB
	Stop band Attenuation	Voice Mode Music Mode	70 55			dB
	Group delay	Voice Mode Music Mode fs = 88.2/96 kHz		4.8/fs 18.5/fs 9/fs	650	µs
	Group delay variation	20 Hz to 20 kHz			1	µs
	Group delay mismatch	Between left and right channel			2	µs
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	70 60			dB

Table 11: Electrical characteristics: Line out and receiver amplifier

(OUT1P_L, OUT1N_L, OUT1P_R, OUT1N_R)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Input Signal	No load, single-ended No load, differential		0.8*AVDD 1.6 *AVDD		V_{PP}
	Load Impedance	single-ended output mode	500	2k	 1 200	Ω µH pF
		differential output mode	25	32	 1 200	Ω µH pF
	Frequency Response	+/- 0.5 dB	20		20k	Hz
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain		-54		15	dB
	Mute Attenuation			100		dB
	Programmable Gain Step Size			1.5		dB
	Absolute Gain Accuracy	0 dB @ 1 kHz	-0.8		0.8	dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.1		0.1	dB
	Signal to Noise Ratio	A weighting		102		dB
V_{NOISE}	Output Noise Level	20 - 20 kHz, unweighted gain < -15 dB single-ended differential		 <5.5 <4.5		µV
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS, 44.1 kHz slave mode non A-weighting		-90		
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz single-ended output	70 47			dB
		20 Hz - 2 kHz 2 kHz - 20 kHz differential output	90 70			dB

Table 12: Electrical characteristics: Dynamic charge pump

(HPCSP, HPCSN)

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDDCSP	Positive dynamic supply voltage	Positive dynamic supply voltage		VDDCP VDDCP/2 (VDDCP/3, VDDCP/4)		
VDDCSN	Negative dynamic supply voltage	Negative dynamic supply voltage		-VDDCP -VDDCP/2 (-VDDCP/3, -VDDCP/4)		
	Floating capacitors			1.0		µF
	Storage capacitors			1.0		µF

Table 13: Electrical characteristics: Headphone amplifier

(HPL, HPR)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Output Signal	No load		1.6*VDD CP		V_{PP}
	DC output offset			100		µV
P_{MAX}	Output Power per channel	VDDCP = 1.8 V, THD < 0.1%, R_L=16 Ω 1 kHz	25	30		mW_{RMS}
		VDDCP = 2.5 V, THD < 0.1%, R_L=16 Ω 1 kHz	50	58		mW_{RMS}
	Dynamic internal supply voltages	VDD/3 or VDD/4 can optionally be selected if two flying caps are available		±VDD ±VDD/2 (±VDD/3 (±VDD/4)		
IQ	Quiescent current per channel	from VDDCP		100		uA
	Load Impedance	13 < R_L < ∞	13	16	 400 500	Ω µH pF
	Frequency Response	+/- 0.5 dB	20		20k	
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain		-54		15	dB
	Mute Attenuation			100		dB
	Programmable Gain Step Size			1.5		dB
	Absolute Gain Accuracy	0 dB @ 1 kHz	-0.8		0.8	dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.1		0.1	dB
SNR	Signal to Noise Ratio	A weighting, gain = 0 dB		100		dB
V_{NOISE}	Output Noise Level	20 to 20 kHz, unweighted, gain < -15 dB		<4.5		$µV_{rms}$
THD+N	Total Harmonic Distortion Plus Noise	VDDCP = 1.8 V, -5 dBFS, R_L=16 Ω		-70		dB
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	70 50			dB
	Output power per channel	VDDCP=2.5 V, THD<1%, R_L=16 Ω, 1 kHz		72		mW

Table 14: Electrical characteristics: Phase locked loop (MCLK)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Input Jitter	cycle to cycle			35	ps
		rms			100	ps
	Input Impedance	DC impedance > 10 MΩ	300 0.5	 1	 2	Ω pF
Interface mode (MCLK is 256 Fs, PLL off)						
F_{in}	Input frequency	256 Fs 128 Fs (96 kHz)	11.289		12.288	MHz
Oscillator mode (MCLK from standard oscillator, PLL on)						
F_{in}	Input frequency		10		80	MHz
		32 kHz mode		32.768		kHz
	I2S tracking range (SRM)	Maximum mismatch of I2S word-clock			4	%
	I2S clock drift	Maximum frequency drift of I2S word clock			50	ppm/s
$V_{IN\ AC}$	MCLK Shaper range	For AC coupling with internal clock shaping	300	500	1000	mV_{PP}

Table 15: Electrical characteristics: Digital I/O

(Ta = -40 to +85ºC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
VIH	CLK, WCLK, DATIN, SK, SI, PD, MCLK Input High Voltage		0.7*VDD		VDD	V
VIL	CLK, WCLK, DATIN, SK, SI, PD, MCLK, Input Low Voltage		-0.3		0.3*VDD	V
VOH @ 1 mA	CLK, WCLK, DATOUT Output High Voltage		0.8*VDD		VDD	V
VOL @ 1 mA	CLK, WCLK, DATOUT Output Low Voltage		0		0.3	V
	MCLK Input High Voltage	DC-coupled TTL signal	0.7*VDD		VDD	V
	MCLK Input Low Voltage		-0.3		0.3*VDD	V

7 Timing characteristics

7.1 Digital audio interface timing - I2S/DSP (in master/slave mode)

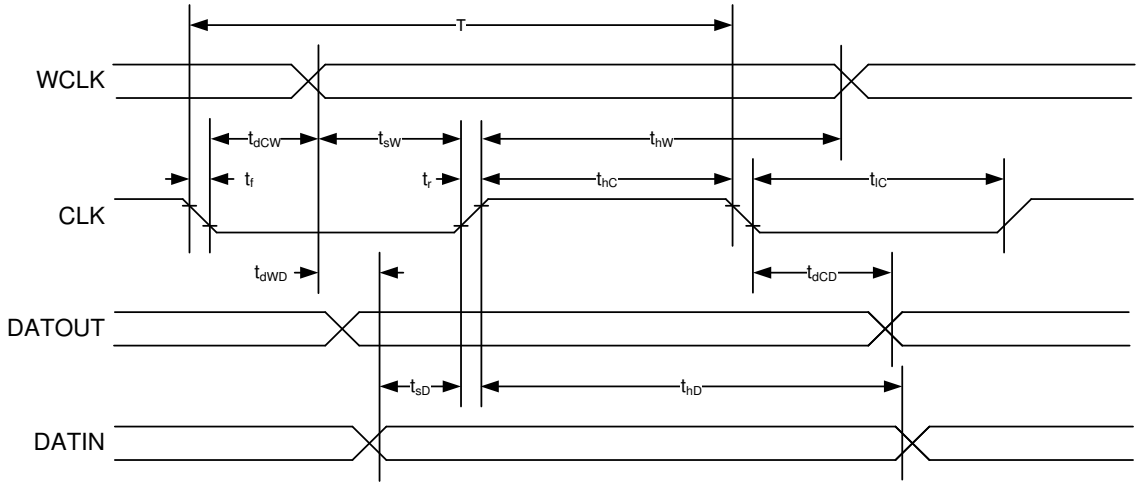

Figure 4: I2S/DSP timing diagram

Table 16: I2S/DSP timing characteristics

(Ta = -40 to +85ºC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Input impedance	DC impedance > 10 MΩ	300 1.0		 2.5	Ω pF
T	CLK period		75			ns
t_r	CLK rise time				8	ns
t_f	CLK fall time				8	ns
t_{hC}	CLK high period		40%		60%	T
t_{lC}	CLK low period		40%		60%	T
t_{dCW}	CLK to WCLK delay		-30%		+30%	T
t_{dCD}	CLK to DATOUT delay		-30%		+30%	T
t_{hW}	WCLK high time	DSP mode	100%			T
		Non-DSP mode	Word length			T
t_{lW}	WCLK low time	DSP mode	100%			T
		Non-DSP mode	Word length			T
t_{sW}	WCLK setup time	Slave mode	7			ns
t_{hW}	WCLK hold time	Slave mode	2			ns
t_{sD}	DATIN setup time		7			ns
t_{hD}	DATIN hold time		2			ns
t_{dWD}	DATOUT to WCLK delay		DATOUT is synchronised to CLK			

7.2 Digital audio control timing - 2-wire control timing

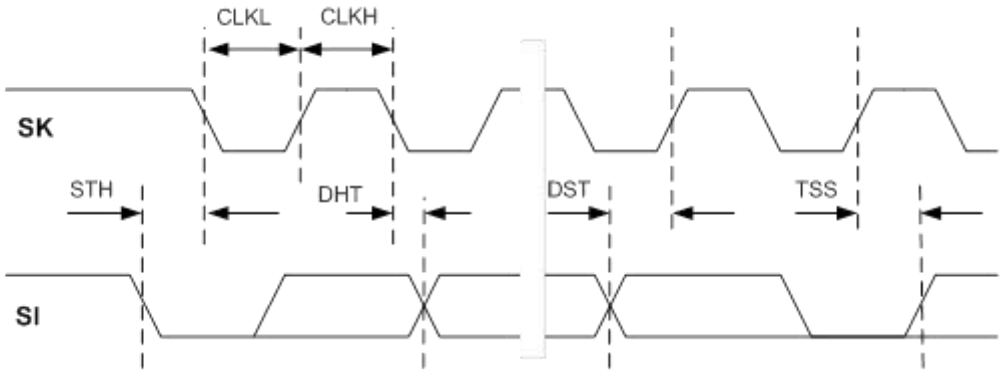

Figure 5: 2-wire control timing diagram

Table 17: 2-wire control timing characteristics

(Ta = -40 to +85ºC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Bus free time STOP to START		1.3			µs
	Bus Line Capacitive load				100	pF
Standard/Fast Mode						
	SK clock frequency		1		400	kHz
	Bus free time STOP to START		1.3			µs
	Start condition set-up time		0.6			µs
STH	Start condition hold time		0.6			µs
CLKL	SK low time		1.3			µs
CLKH	SK high time		0.6			µs
	2-wire SK and SI rise/fall time				300	ns
DST	SI set-up time		100			ns
DHT	SI hold-time		0			ns
TSS	Stop condition set-up time		0.6			µs
High Speed Mode						
	SK clock frequency		1		1700	kHz
	Start condition set-up time		160			ns
STH	Start condition hold time		160			ns
CLKL	SK low time		160			ns
CLKH	SK high time		60			ns
	HS-2-wire SK rise/fall time				40	ns
	HS-2-wire SI rise/fall time				80	ns
DST	SI set-up time		10			ns
	SI hold-time		0			ns
TSS	Stop condition set-up time		16			ns

Table 18: Start-up times after setting SC_MST_EN = 1

Source	Output	Comment	Min	Typ	Max	Unit
	VBG	VBG voltage >90% with 1 µF VBG capacitor		25		ms
All analogue inputs and DACL/R	HPL/R	Slave mode; 200 ms added delay required	200	200		ms
All analogue inputs and DACL/R	HPL/R	32 kHz PLL master mode; 200 ms added delay required		500		ms
All analogue inputs and DACL/R	OUT1L/R	Slave mode		250		ms
All analogue inputs	ADCL/R	Slave mode		200		ms
All analogue inputs	ADCL/R	32 kHz PLL master mode		600		ms