Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Ultra-Low Power Stereo Codec

General Description

DA7217 is a high-performance, low-power audio codec optimized for use in headsets or wearable devices. It has differential headphone outputs for use inside headset devices, offering excellent left to right channel separation and common mode noise rejection. DA7217 also has a stereo DAC to headphone output path and ultra-low power operating modes to support always-on audio detect applications.

DA7217 contains two analog microphone input paths, or up to four digital microphone input paths, or a combination of both. The other chip in this family, the DA7218, has single-ended headphone outputs, and has been designed with headphone detect for use in accessories.

Key Features

- High performance stereo DAC to headphone playback path with 110 dB dynamic range
- 4 mW stereo playback power consumption
- DAC digital filters with audio and voice mode options, five-band equalizer and five programmable biquad stages
- Dedicated low-latency digital sideband filter with three programmable biquad stages
- High performance microphone to ADC record path with 105 dB dynamic range
- 2.5 mW stereo record power consumption
- ADC digital filters with audio and voice mode options
- 500 µW always-on record mode with automatic level detection
- Hybrid analog / digital automatic level control to dynamically control the record level
- Shutdown mode offering current consumption during standby of 2.5 µA
- Two low-noise microphone bias regulators with programmable output voltage and ultra-low power mode
- A high efficiency two-level, true-ground charge pump for generating class-G headphone supplies
- Voice mode filtering up to 32 kHz
- Flexible digital mixing from all seven inputs to all six outputs with independent gain on each mixer path
- Ability to run the ADCs at a different sample rate to the DACs on a single I^2S interface
- Digital tone generator with built-in support for DTMF
- System controller for simplified, pop-free start-up and shutdown
- Phase-locked loop with sample rate tracking supporting MCLK frequencies from 2 MHz to 54 MHz
- Automatic tuning of on-chip reference oscillator for clock-free operation in low-power modes
- 4-wire digital audio interface with support for I^2S, four-channel I^2S, TDM and other audio formats
- 2-wire I^2C compatible control interface with support for High Speed mode up to 3.4 MHz
- 24-bit data at up to 96 kHz sample rate
- The headphone amplifier can be run directly from the supply, thus eliminating the need for charge pump capacitors

Applications

- Hearables
- Wireless and wired headphones
- Wireless and wired headsets

System Diagram

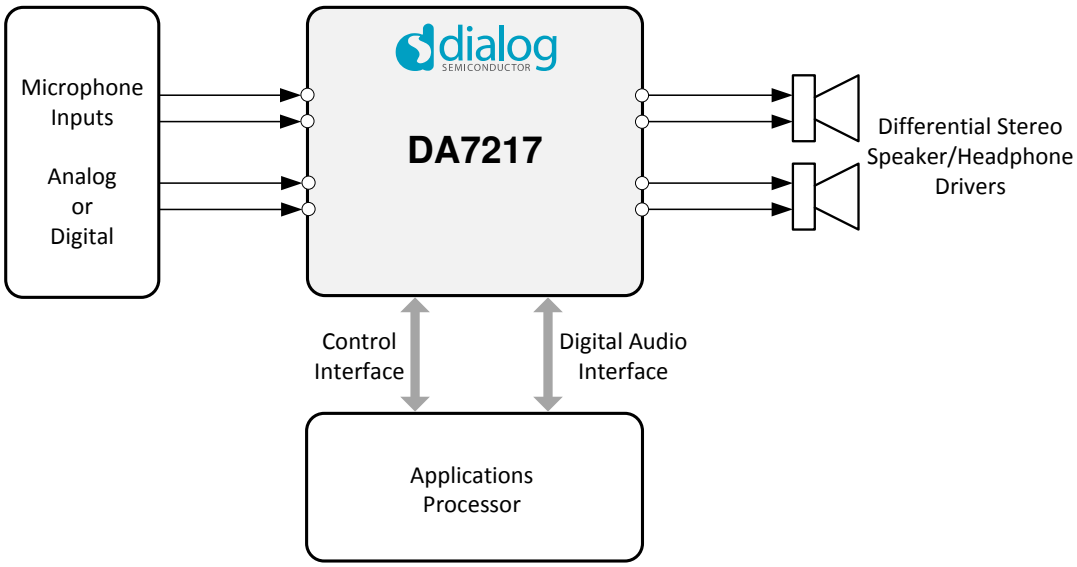

Figure 1: DA7217 with Differential Stereo Headphone Outputs

Contents

1 Terms and Definitions

ADC	Analog to Digital Converter
AGS	ADC Gain Swap (input Dynamic Range Extension)
ALC	Automatic Level Control
ANC	Active Noise Cancelling
BIQ	Biquad Filter
CIC	Cascaded Integrator and Comb
DAC	Digital to Analog Converter
DAI	Digital Audio Interface
DGS	DAC Gain Swap (output Dynamic Range Extension)
DMIC	Digital Microphone
DRE	Dynamic Range Extension
DTMF	Dual Tone Multi-Frequency
DWA	Data-Weighted Averager
HBM	Human Body Model
HPF	High-Pass Filter
I^2C	Inter-Integrated Circuit interface
I^2S	Inter-IC Sound
LDO	Low Dropout Regulator
LPF	Low-Pass Filter
MCLK	Master Clock
PC	Program Counter
PDM	Pulse Density Modulated
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio[4]
RC	Resistance-Capacitance
SC	System Controller
SDM	Sigma Delta Modulator
SNR	Signal to Noise Ratio[5]
SRM	Sample Rate Matching
SWG	Sine Wave Generator
TDM	Time Division Multiplexing
THD+N	Total Harmonic Distortion plus Noise[6]
VCO	Voltage-Controlled Oscillator

2 Terminology

[1] Crosstalk (dB) is the level difference between the active path output and the idle path measured signal level, at the test signal frequency. The active path is configured and supplied with an input signal capable of driving a full scale output, with the signal measured at the output of the specified idle path.

[2] Mute Attenuation is the difference in level between the full scale output signal and the output with mute applied.

[3] Channel Separation (dB) [left-to-right and right-to-left] is the difference in level between the active channel (driven to maximum full scale output) and the signal level measured in the idle channel at the test signal frequency. The active channel is configured and supplied with an input signal capable of driving a full scale output, with the signal measured at the output of the associated idle channel.

[4] PSRR is the ratio of a given power supply change relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.

[5] SNR is the difference in level between the maximum full scale output signal and the output with no input signal applied.

[6] THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.

All performance measurements carried out with 20 kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low-pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

3 Block Diagram

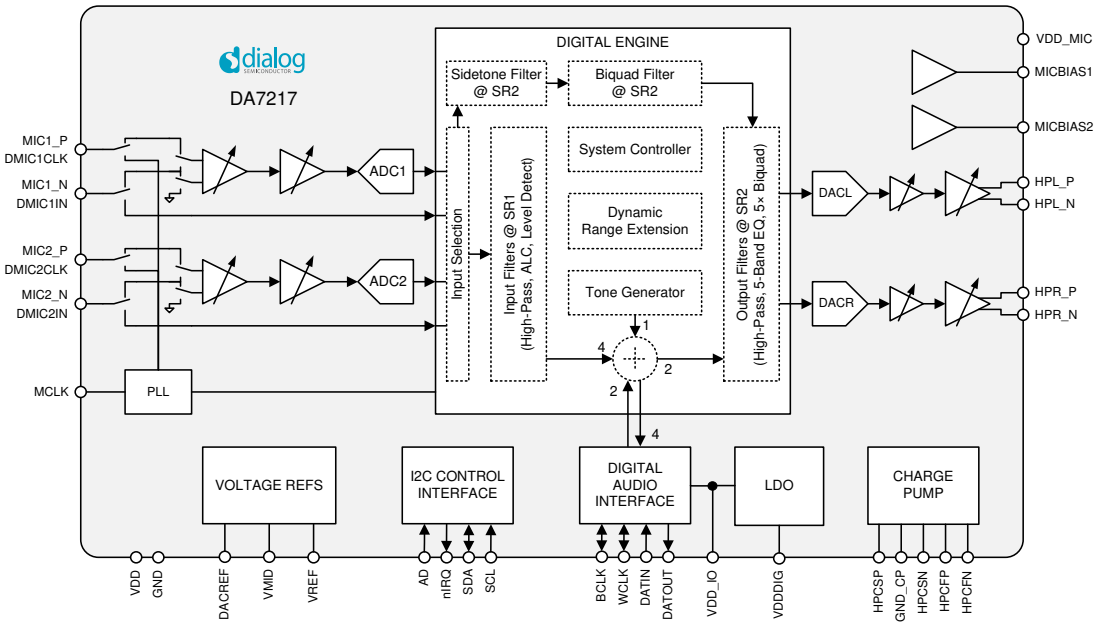

Figure 2: DA7217 Block Diagram

4 Pinout

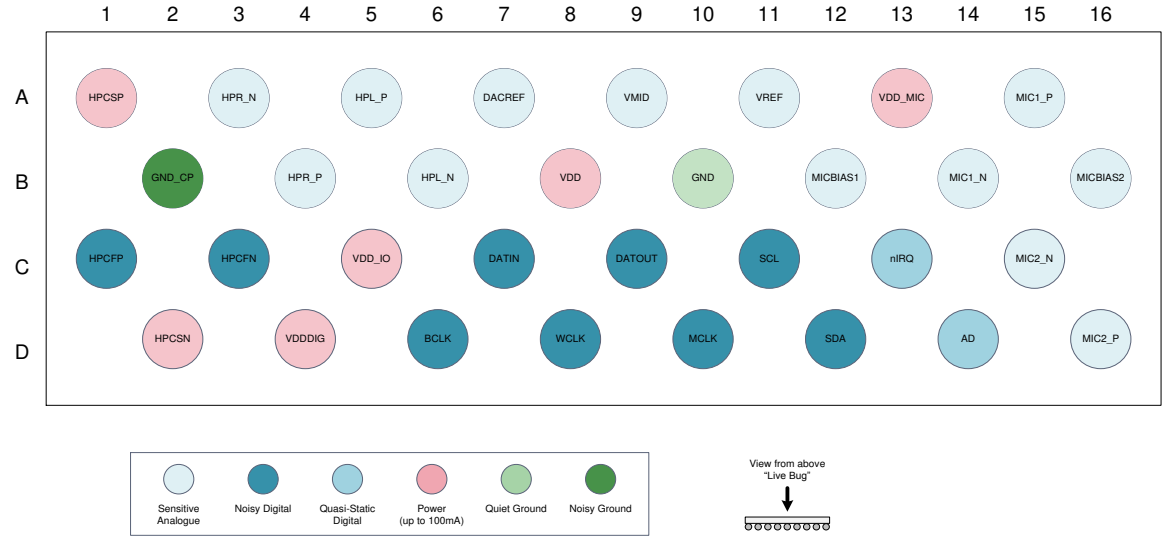

Figure 3: DA7217 Ballout Diagram

Table 1: DA7217 Pin Description

Pin No.	Pin Name	Type (Table 2)	Description
Microphone Inputs			
A15	MIC1_P DMIC1CLK	AI/DO	Differential analog microphone 1 input (Pos) Digital microphone 1 clock output
B14	MIC1_N DMIC1IN	AI/DI	Differential analog microphone 1 input (Neg) Digital microphone 1 data input
D16	MIC2_P DMIC2CLK	AI/DO	Differential analog microphone 2 input (Pos) Digital microphone 2 clock output
C15	MIC2_N DMIC2IN	AI/DI	Differential analog microphone 2 input (Neg) Digital microphone 2 data input
B12	MICBIAS1	AIO	Microphone bias output 1
B16	MICBIAS2	AIO	Microphone bias output 2
Headphone Outputs			
A5	HPL_P	AO	Differential headphone output (Left, Pos)
B6	HPL_N	AO	Differential headphone output (Left, Neg)
B4	HPR_P	AO	Differential headphone output (Right, Pos)
A3	HPR_N	AO	Differential headphone output (Right, Neg)
Charge Pump			
A1	HPCSP	AIO	Charge pump reservoir capacitor (Pos)
D2	HPCSN	AIO	Charge pump reservoir capacitor (Neg)
C1	HPCFP	AIO	Charge pump flying capacitor (Pos)
C3	HPCFN	AIO	Charge pump flying capacitor (Neg)
Digital Interface			
D12	SDA	DIOD	I^2C bi-directional data
C11	SCL	DI	I^2C clock
D14	AD	DI	I^2C slave address select (high = 1B, low = 1A)
C13	nIRQ	DIOD	Interrupt output (open drain active low)
C7	DATIN	DIO	DAI data input to DA7217
C9	DATOUT	DIO	DAI data output from DA7217
D6	BCLK	DIO	DAI bit clock
D8	WCLK	DIO	DAI word clock
D10	MCLK	DI	Master clock input
References			
A7	DACREF	AIO	DAC reference decoupling capacitor
A9	VMID	AIO	Mid-rail reference decoupling capacitor
A11	VREF	AIO	Bandgap reference decoupling capacitor
Linear Regulator			
D4	VDDDIG	AO	Output from digital supply LDO

Pin No.	Pin Name	Type (Table 2)	Description
Supplies			
B8	VDD	AI	Main analog supply
A13	VDD_MIC	AI	Supply for MICBIAS LDO
C5	VDD_IO	AI	Supply for digital interface and LDO
B2	GND_CP	AI	Ground reference
B10	GND	AI	Ground reference

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
DIOD	Digital Input/Output open drain	SPU	Switchable pull-up resistor
PU	Fixed pull-up resistor	SPD	Switchable pull-down resistor
PD	Fixed pull-down resistor		

4.1 Input Pins

4.1.1 MIC1_P (DMIC1CLK)

MIC1_P is the positive differential input for the first analog microphone channel. It can be used as a single-ended input (see Figure 8).

Alternatively for digital microphones, MIC1_P is used to provide a clock output.

4.1.2 MIC1_N (DMIC1IN)

MIC1_N is the negative differential input for the first analog microphone channel. It can be used as a single-ended input.

Alternatively for digital microphones and active noise cancelling (ANC) applications, MIC1_N is used as a pulse density modulated (PDM) data input.

4.1.3 MIC2_P (DMIC2CLK)

MIC2_P is the positive differential input for the second analog microphone channel. It can be used as a single-ended input.

Alternatively for digital microphones, MIC2_P is used to provide a clock output.

4.1.4 MIC2_N (DMIC2IN)

MIC2_N is the negative differential input for the second analog microphone channel. It can be used as a single-ended input.

Alternatively for digital microphones and ANC applications, MIC2_N is used as a PDM data input.

4.1.5 MCLK

MCLK is the master clock input pin. It is used as the main system clock either directly or via the PLL.

4.1.6 SCL

SCL is the control interface (I^2C) clock input and is used in conjunction with SDA to control the device.

4.1.7 AD

AD is used to select between one of two possible I^2C slave addresses by connecting the pin to GND or VDD_IO. (High = 1B, Low = 1A).

4.1.8 DATIN

DATIN is the data input pin which forms part of the digital audio interface (DAI). It is used to present audio playback data to the device.

4.2 Output Pins

4.2.1 nIRQ

nIRQ is the open drain active-low interrupt output to alert the host to either an accessory or a level-detect event.

4.2.2 DATOUT

DATOUT is the data output pin, which forms part of the DAI.

4.3 Bi-Directional Pins

4.3.1 SDA

SDA is the control interface (I^2C) data input/output and is used in conjunction with SCL to control the device.

4.3.2 BCLK

BCLK is the bit clock input/output pin which forms part of the DAI. It is used to clock audio data bits into or out from the device or both.

4.3.3 WCLK

WCLK is the word clock input/output pin that forms part of the DAI.

4.4 Differential Headphone Pins

4.4.1 HPL_P

HPL_P is the positive left-channel headphone output for a headphone speaker connected between HPL_P and HPL_N.

4.4.2 HPL_N

HPL_N is the negative left-channel headphone output for a headphone speaker connected between HPL_P and HPL_N.

4.4.3 HPR_P

HPR_P is the positive right-channel headphone output for a headphone speaker connected between HPR_P and HPR_N.

4.4.4 HPR_N

HPR_N is the negative right-channel headphone output for a headphone speaker connected between HPR_P and HPR_N.

4.5 Charge Pump Pins

4.5.1 HPCSP

HPCSP is the positive output from the headphone charge pump. This pin should be connected to ground via a reservoir capacitor.

4.5.2 HPCSN

HPCSN is the negative output from the headphone charge pump. If using the charge pump, this pin must be connected to ground via a reservoir capacitor. If the charge pump is not being used, then this pin should be tied directly to ground.

4.5.3 HPCFP

HPCFP is one of the flying capacitor connections required by the headphone charge pump. If the charge pump is in use it must be connected to HPCFN via a capacitor. If the charge pump is not being used, then this pin can be left floating.

4.5.4 HPCFN

HPCFP is one of the flying capacitor connections required by the headphone charge pump. If the charge pump is in use it must be connected to HPCFP via a capacitor. If the charge pump is not being used, then this pin can be left floating.

4.6 References

4.6.1 VMID

VMID is mid-rail reference decoupling capacitor connection.

4.6.2 DACREF

DACREF is the DAC reference decoupling capacitor connection.

4.6.3 VREF

VREF is the bandgap reference decoupling capacitor connection.

4.6.4 MICBIAS1

MICBIAS1 is the first of two MICBIAS outputs. This must be decoupled with a 1 µF capacitor

4.6.5 MICBIAS2

MICBIAS2 is the second of two MICBIAS outputs. This must be decoupled with a 1 µF capacitor.

4.6.6 VDDDIG

VDDDIG is the internal digital supply rail decoupling pin and is used to monitor the LDO output. This must be decoupled with a 1 µF capacitor.

4.7 Supply Pins

4.7.1 VDD

VDD is main analog supply pin. It supplies all the analog circuits except the MICBIAS outputs and the HPAMP outputs.

4.7.2 VDD_IO

VDD_IO is the supply pin for the digital input/output signals.

4.7.3 VDD_MIC

VDD_MIC is the supply pin for the MICBIAS outputs.

4.8 Ground Pins

4.8.1 GND

GND is one of the two ground reference pins (the other is GND_CP) on the device. Connect this pin to a ground plane as close as possible to the device.

4.8.2 GND_CP

GND_CP is one of the two ground reference pins (the other is GND) on the device. Connect this pin to a ground plane as close as possible to the device.

5 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings (Note 1)

Parameter	Description	Conditions	Min	Max	Unit
	Storage temperature		–65	+165	°C
T_a	Operating temperature		–40	+85	°C
V_{DD}	Main supply voltage		–0.3	+2.75	V
V_{DD_IO}	Digital IO supply voltage		–0.3	+5.5	V
V_{DD_MIC}	Microphone bias supply voltage		–0.3	+5.5	V
V_{DDIO}	Digital IO pins	SDA, SCL, AD, BCLK, WCLK, DATIN, DATOUT, MCLK, nIRQ	–0.3	V_{DD_IO} + 0.3	V
	Digital microphone IO pins	DMIC1CLK, DMIC1IN	–0.3	$V_{MICBIAS1}$ + 0.3	V
	Digital microphone IO pins	DMIC2CLK, DMIC2IN	-0.3	$V_{MICBIAS2}$ + 0.3	V
	Analog input pins	MIC1_P, MIC1_N, MIC2_P, MIC2_N	–0.3	V_{DD} + 0.3	V
	Package thermal resistance		60		°CW
V_{ESD_HBM}	ESD susceptibility	Human body model (HBM)		2	kV

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_a	Operating temperature		–25		+85	°C
V_{DD}	Main supply voltage		+1.7		+2.65	V
V_{DD_IO}	Digital IO supply voltage		+1.5		+3.6	V
V_{DD_MIC}	Microphone bias supply voltage		+1.8		+3.6	V

7 Electrical Characteristics

Unless otherwise stated, test conditions are as follows: V_{DD} = V_{DD_IO} = 1.8 V, V_{DD_MIC} = 3.3 V, V_{DDDIG} = 1.05 V, T_a = 25 °C, MCLK = 12.288 MHz, SR = 48 kHz, PLL = Bypass mode, Slave mode.

Table 5: Power Consumption

Description	Conditions (Note 1)	Min	Typ	Max	Unit
Powerdown mode			2.5	7	µA
Digital playback to headphone, no load	DACL/R to HP_L/R, quiescent		4		mW
Digital playback to headphone, with load	DACL/R to HP_L/R, 32 Ω load, 0.1 mW at 0 dBFS		7.7		mW
Microphone stereo record	MICL/R to ADCL/R		2.5		mW
Microphone stereo record and digital playback to Headphone, no load	MICL/R to ADCL/R and DACL/R to HP_L/R, quiescent		5.5		mW
Microphone stereo record and digital playback to headphone, with load	MICL/R to ADCL/R and DACL/R to HP_L/R, 32 Ω load, 0.1 mW at 0 dBFS		8.8		mW

Note 1 V_{DD} = V_{DD_IO} = V_{DD_MIC} = 1.8 V

Table 6: Electrical Characteristics: Microphone Bias

Description	Condition	Min	Typ	Max	Unit
Programmable output voltage	No load, V_{DD_MIC} > $V_{MICBIAS}$ + 200 mV	1.6		3.0	V
Output voltage step			200		mV
Output current	Output voltage droop < 50 mV	2			mA
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB
Output voltage noise	$V_{MICBIAS}$ ≤ 2.2 V		5		μV_{RMS}

Table 7: Electrical Characteristics: Microphone Amplifier

Description	Condition	Min	Typ	Max	Unit
Full-scale input signal	0 dB gain, single-ended 0 dB gain, differential		0.8 * V_{DD} 1.6 * V_{DD}		V_{PP}
Input resistance		12	15	18	kΩ
Programmable gain		−6		36	dB
Gain step size			6		dB
Absolute gain accuracy	0 dB @ 1 kHz	-0.5		0.5	dB
Gain step error	20 Hz to 20 kHz	-0.1		0.1	dB
Input noise level	Inputs connected to GND, 24 dB gain, input-referred, A-weighted		5		μV_{RMS}
Amplitude ripple	20 Hz to 20 kHz	-0.5		0.5	dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	90 70			dB

Description	Condition	Min	Typ	Max	Unit
Crosstalk	20 Hz to 20 kHz		88		dB

Table 8: Electrical Characteristics: Input Amplifier

Description	Condition	Min	Typ	Max	Unit
Full-scale input signal	0 dB gain		1.6 * V_{DD}		V_{PP}
Programmable gain		−4.5		18	dB
Gain step size			1.5		dB
Absolute gain accuracy	0 dB @ 1 kHz	-0.5		0.5	dB
Gain step error	20 Hz to 20 kHz	-0.1		0.1	dB
Amplitude ripple	20 Hz to 20 kHz	-0.5		0.5	dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	90 70			dB

Table 9: Electrical Characteristics: ADC

Description	Condition	Min	Typ	Max	Unit
Full-scale input signal	0 dBFS digital output level		1.6 * V_{DD}		V_{PP}
Signal to noise ratio	A-weighted		90		dB
Dynamic range	ADC DRE enabled, A-weighted		105		dB
Total harmonic distortion plus noise	-1 dBFS ADC output level		-85		dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 10: Electrical Characteristics: DAC

Description	Condition	Min	Typ	Max	Unit
Full-scale output signal	0 dBFS digital input level		1.6 * V_{DD}		V_{PP}
Signal to noise ratio	A-weighted		100		dB
Dynamic range	DAC DRE enabled, A-weighted		110		dB
Total harmonic distortion plus noise	-1 dBFS digital input level		-90		dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 11: Electrical Characteristics: Headphone Amplifier

Description	Condition	Min	Typ	Max	Unit
Full-scale output signal	No load		1.6 * V_{DD}		V_{PP}
DC output offset	−30 dB gain			250	µV
Maximum output power per channel (charge pump mode)	V_{DD} = 1.8 V, THD < 0.005 %, R_{LOAD} = 32 Ω, 1 kHz		30		

Description	Condition	Min	Typ	Max	Unit
	V_{DD} = 2.5 V, THD < 0.005 %, R_{LOAD} = 32 Ω, 1 kHz		58		
Maximum output power per channel (single supply mode)	V_{DD} = 1.8 V, THD < 0.1 %, R_{LOAD} = 32 Ω, 1 kHz		19		
	V_{DD} = 2.5 V, THD < 0.1 %, R_{LOAD} = 32 Ω, 1 kHz		49		
Quiescent current per channel				150	µA
Load resistance		26	32		Ω
Load capacitance				500	pF
Load inductance				400	µH
Frequency Response	20 Hz to 20 kHz	-0.5		+0.5	dB
Signal to noise ratio	V_{DD} = 1.8 V, 0 dB gain A-weighted		98		dB
	V_{DD} = 2.5 V, 0 dB gain A-weighted		100		dB
Output noise level	20 Hz to 20 kHz, < -20 dB gain			2.5	μV_{RMS}
Total harmonic distortion plus noise	V_{DD} = 1.8 V, R_{LOAD} = 32 Ω, -5 dBFS, 1 kHz		−88		dB
Channel separation [3]	V_{DD} = 1.8V, R_{LOAD} = 32 Ω, 1 kHz		-110		dB
Programmable gain		−57		6	dB
Gain step size			1.5		dB
Absolute gain accuracy	0 dB @ 1 kHz	−0.5		0.5	dB
Left/right gain mismatch	20 Hz to 20 kHz	−0.1		0.1	dB
Gain step error	20 Hz to 20 kHz	−0.1		0.1	dB
Amplitude ripple	20 Hz to 20 kHz	−0.5		0.5	dB
Mute attenuation [2]			−70		dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 12: Electrical Characteristics: Output Amplifier

Description	Condition	Min	Typ	Max	Unit
Full-scale input signal	0 dBFS output from the DAC		1.6 * V_{DD}		VPP
Programmable gain		−1.0		0	dB
Gain step size			0.5		dB
Absolute gain accuracy	0 dB @ 1 kHz	-0.5		0.5	dB
Amplitude ripple	20 Hz to 20 kHz	-0.5		0.5	dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	90 70			dB

Table 13: Electrical Characteristics: Input Filters

Description	Condition	Min	Typ	Max	Unit
Pass band				0.45 * F_S	Hz
Pass band ripple	Voice mode Music mode			±0.3 ±0.1	dB
Stop band	F_S ≤ 48 kHz F_S = 88.2 kHz or 96 kHz	0.56 * F_S		7 * F_S 3.5 * F_S	Hz
Stop band attenuation	Voice mode Music mode	70 55			dB
Group delay	Voice mode Music mode F_S = 88.2 kHz or 96 kHz		4.3 / F_S 18 / F_S 9 / F_S		s
Gain step size			0.75		dB
Programmable gain		-83.25		12	dB

Table 14: Electrical Characteristics: Automatic Level Control

Description	Condition	Min	Typ	Max	Unit
Attack rate	F_S = 48 kHz	1.6		6500	dB/s
Release rate	F_S = 48 kHz	1.6		1675	dB/s
Hold time	F_S = 48 kHz	1.3		42300	ms
Maximum threshold		−94.5		0	dBFS
Minimum threshold		−94.5		0	dBFS
Noise threshold		−94.5		0	dBFS
Threshold step size			1.5		dB
Maximum overall gain		0		90	dB
Maximum overall attenuation		0		90	dB
Maximum analog gain		0		36	dB
Minimum analog gain		0		36	dB
Gain step size			1.5		dB

Table 15: Electrical Characteristics: DAC Filter Specifications

Description	Conditions	Min	Typ	Max	Unit
Pass band				0.45 * F_S	Hz
Pass band ripple	Voice mode Music mode			±0.3 ±0.1	dB
Stop band	F_S ≤ 48 kHz F_S = 88.2 kHz or 96 kHz	0.56 * F_S		7 * F_S 3.5 * F_S	Hz
Stop band attenuation	Voice mode Music mode	70 55			dB
Group delay	Voice mode Music mode F_S = 88.2 kHz or 96 kHz		4.3 / F_S 18 / F_S 9 / F_S		s
Group delay variation	20 Hz to 20 kHz		1		µs
Left/right channel group delay mismatch			2		µs
Gain step size			0.75		dB
Programmable gain		-83.25		108	dB

Table 16: Electrical Characteristics: High-Pass Filter (Input and Output, ADC in High-Power Mode)

out_1_voice_en / in_1_voice_en	out_1_voice_hpf_corner / in_1_voice_hpf_corner	out_1_audio_hpf_corner/ in_1_audio_hpf_corner	SR Sample Rate (kHz)										
			8	11.025	12	16	22.05	24	32	44.1	48	88.2	96
0		00	0.33	0.46	0.5	0.67	0.92	1	1.33	1.84	2	3.68	4
		01	0.67	0.92	1	1.33	1.84	2	2.67	3.68	4	7.35	8
		10	1.33	1.84	2	2.67	3.68	4	5.33	7.35	8	14.7	16
		11	2.67	3.68	4	5.33	7.35	8	10.67	14.7	16	29.4	32
1	000		2.5	3.45	3.75	5	6.89	7.5	10	Voice HPF not available for sample rates above 32 kHz.			
	001		25	34.5	37.5	50	68.9	75	100				
	010		50	68.9	75	100	137.8	150	200				
	011		100	137.8	150	200	275.6	300	400				
	100		150	206.7	225	300	413.4	450	600				
	101		200	275.6	300	400	551.3	600	800				
	110		300	413.4	450	600	826.9	900	1200				
	111		400	551.3	600	800	1102.5	1200	1600				

Table 17: High-Pass Filter Settings (ADC in Low-Power Mode)

in_1_voice_en out_1_voice_en	in_1_voice_hpf_corner out_1_voice_hpf_corner	in_1_audio_hpf_corner out_1_audio_hpf_corner.	SR Sample Rate (kHz)										
			8	11.025	12	16	22.05	24	32	44.1	48	88.2	96
0		00	0.33	0.46	0.5	0.67	0.92	1	32 kHz sample rate not available in Low-Power mode	1.84	2	88.2 kHz and 96 kHz sample rates not available in Low-Power mode	
		01	0.67	0.92	1	1.33	1.84	2		3.68	4		
		10	1.33	1.84	2	2.67	3.68	4		7.35	8		
		11	2.67	3.68	4	5.33	7.35	8		14.7	16		
1	000		2.5	In low-power mode, the voice HPF is only available at a sample rate of 8 kHz									
	001		25										
	010		50										
	011		100										
	100		150										
	101		200										
	110		300										
	111		400										

Table 18: Electrical Characteristics: 5-Band Equalizer

FS (kHz)	Center Frequency (Hz) At Programmed Setting				
	Band 1	Band 2	Band 3	Band 4	Band 5
8	0	99	493	1528	4000
11.025	0	136	680	2106	5512
12	0	148	740	2293	6000
16	0	96	440	2128	8000
22.05	0	133	607	2933	11025
24	0	145	660	3191	12000
32	0	95	418	1797	16000
44.1	0	131	576	2386	22050
48	0	143	627	2596	24000
88.2	Not available				
96					

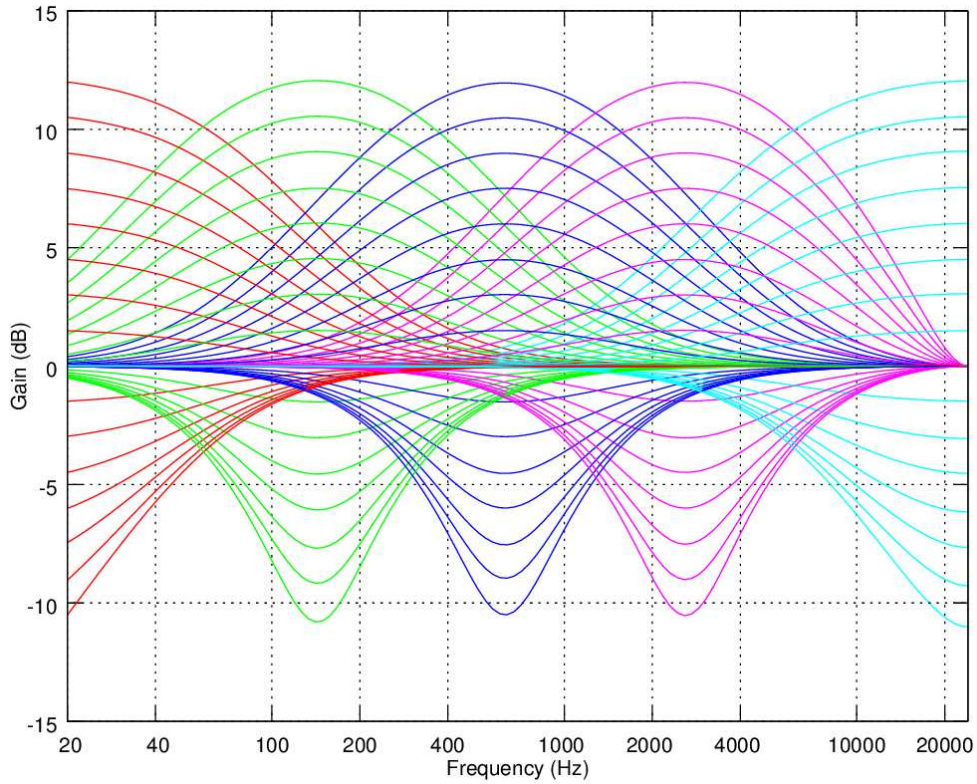

Figure 4: 5-Band Equalizer Response at 48 kHz

Table 19: PLL Mode

Description	Conditions	Min	Typ	Max	Unit
MCLK input jitter	Absolute jitter (rms) (Note 1)			540	ps
MCLK input frequency	Normal mode	2		54	MHz
SRM tracking range	DAI slave mode WCLK frequency variation	-4		4	%
SRM tracking rate	DAI slave mode WCLK drift rate			54	ppm/s

Note 1 Jitter in the 100 Hz to 40 kHz band

Table 20: Bypass Mode

Description	Conditions	Min	Typ	Max	Unit
MCLK input jitter	Absolute jitter (rms) (Note 1)			540	ps
MCLK input frequency	F_S = 11.025, 22.05, 44.1, 88.2 kHz F_S = 8, 12, 16, 24, 32, 48, 96 kHz		11.2896 12.288		MHz

Note 1 Jitter in the 100 Hz to 40 kHz band

Table 21: Tone Generator

Description	Conditions	Min	Typ	Max	Unit
Single-tone frequency	F_S = 8, 12, 16, 24, 32, 48, 96 kHz F_S = 11.025, 22.05, 44.1, 88.2 kHz	1 1		12000 11025	Hz
Single-tone frequency step	F_S = 8, 12, 16, 24, 32, 48, 96 kHz F_S = 11.025, 22.05, 44.1, 88.2 kHz		0.18 0.17		Hz
Dual-tone modulation frequency A			697 770 852 941		Hz
Dual-tone modulation frequency B			1209 1336 1477 1633		Hz
Output signal level			0		dBFS
On/off pulse duration		10		2000	ms
On/off pulse step size	10 ms to 200 ms duration 200 ms to 2000 ms duration		10 50		ms
On/off pulse repeat	Programmable Continuous		1, 2, 3, 4, 5, 6 ∞		Cycles

8 Digital Interfaces

Table 22: I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	SCL, SDA, MCLK, BCLK, WCLK, DATIN, DATOUT, AD Input HIGH voltage		0.7 * V_{DD_IO}			V
V_{IL}	SCL, SDA, MCLK, BCLK, WCLK, DATIN, DATOUT Input LOW voltage				0.3 * V_{DD_IO}	V
V_{OL}	SDA, nIRQ Output LOW voltage	I_{OUT} = 3 mA			0.24	V
V_{OH}	DMIC1CLK Output HIGH voltage		0.7 * $V_{MICBIAS1}$			
V_{OL}	DMIC1CLK Output HIGH voltage				0.3 * $V_{MICBIAS1}$	
V_{IH}	DMIC1IN Input HIGH voltage		0.7 * $V_{MICBIAS1}$			
V_{IL}	DMIC1IN Input LOW voltage				0.3 * $V_{MICBIAS1}$	
V_{OH}	DMIC2CLK Output HIGH voltage		0.7 * $V_{MICBIAS2}$			
V_{OL}	DMIC2CLK Output LOW voltage				0.3 * $V_{MICBIAS2}$	
V_{IH}	DMIC2IN Input HIGH voltage		0.7 * $V_{MICBIAS2}$			
V_{IL}	DMIC2IN Input LOW voltage				0.3 * $V_{MICBIAS2}$	

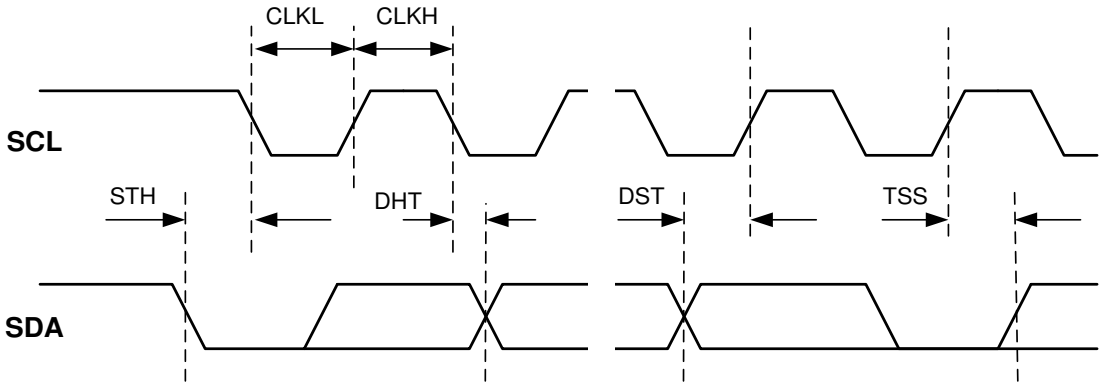

Figure 5: I²C Bus Timing

Table 23: I²C Control Bus (VDD_IO = 1.8 V)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Bus free time STOP to START		500			ns
	Bus line capacitive load				150	pF
Standard/Fast Mode						
	SCL clock frequency		0		1000	kHz
	Start condition setup time		260			ns
STH	Start condition hold time		260			ns
CLKL	SCL low time		500			ns
CLKH	SCL high time		260			ns
	SCL rise/fall time	Input requirement			1000	ns
	SDA rise/fall time	Input requirement			300	ns
DST	SDA setup time		50			ns
DHT	SDA hold time		0			ns
TSS	Stop condition setup time		260			ns
High-Speed Mode						
	SCL clock frequency		0		3400	kHz
	Start condition setup time		160			ns
STH	Start condition hold time		160			ns
CLKL	SCL low time		160			ns
CLKH	SCL high time		60			ns
	SCL rise/fall time	Input requirement			160	ns
	SDA rise/fall time	Input requirement			160	ns
DST	SDA setup time		10			ns
DHT	SDA hold time		0			ns
TSS	Stop condition setup time		160			ns