Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Audio Codec with Advanced Accessory Detect

General Description

The DA7219 is an ultra low-power audio codec with Advanced Accessory Detection (AAD), which supports sample rates up to 96 kHz at 24-bit resolution. It contains a mono microphone to analog to digital converter (ADC) path, and a stereo digital to analog converter (DAC) to headphone (HP) path.

AAD supports the detection and identification of 3-pole (headphone) and 4-pole (headset) jacks, and allows the automatic pin order switching of MIC/GND on CTIA or OMTP headsets. It also supports automatic multiple button detection.

Key Features

- Android Wired Headset v1.1 compliant
- High performance mono microphone to ADC record path with 90 dB SNR
  - ADC digital filters with Audio and Voice mode high-pass characteristics
  - Low-noise microphone bias regulator with programmable output
- High performance stereo DAC to headphone playback path with 100 dB SNR
  - DAC digital filters with Audio and Voice mode high-pass cutoff and 5-band equalizer
- Advanced Accessory Detect supports
  - 3-pole and 4-pole jack detection
  - MIC/GND polarity switching
  - Multiple button detection
  - Headphone impedance testing
- Microphone input with automatic level control
- Digital sidetone path with gain
- Digital tone generator
- System controller for simplified pop-free start-up and shut-down
- Mixed sample rates of 24 kHz ADC, 48 kHz DAC supported from a single digital interface
- Sample rates of up to 96 kHz at 24-bit resolution
- Shut-down mode for very low current consumption during standby
- Phase locked loop with WCLK tracking to generate system clock
- 4-wire digital audio interface with support for I^2S, TDM and other audio formats
- 2-wire I^2C compatible interface with support for High Speed mode up to 3.4 MHz
- 4.5 mm x 1.6 mm WLCSP RouteEasy™ package for low cost PCB manufacture

Applications

- Chromebooks
- Portable audio applications
- Tablets and eBooks
- All digital distributed systems
- Headphone accessories
- Remote controllers
- Gaming controllers

System Diagram

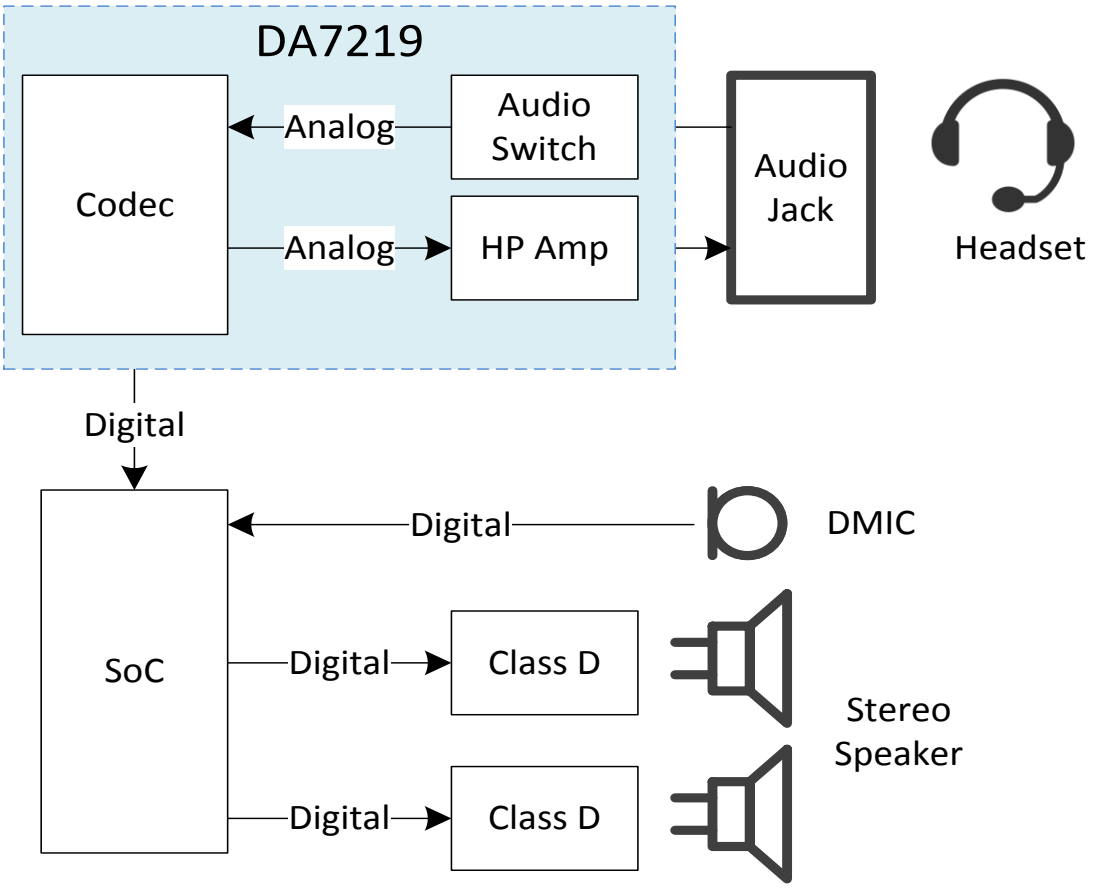

Figure 1: DA7219 in a Digital Distributed System

Contents

Figures

Tables

1 Terms and Definitions

AAD	Advanced Accessory Detect
ADC	Analog to Digital Converter
ALC	Automatic Level Control
CMRR	Common Mode Rejection Ratio
CTIA	Cellular Telecommunications Industry Association, (now known as 'The Wireless Association')
DAC	Digital to Analog Converter
DAI	Digital Audio Interface
DMIC	Digital Microphone
DTMF	Dual Tone Multi Frequency
EQ	Equalizer
FS	Sample Rate
HP	Headphones
HPF	High-Pass Filter
I^2C	Inter-Integrated Circuit Interface
I^2S	Inter-Integrated Circuit Sound
LDO	Low Dropout Regulator
MCLK	Master Clock
OMTP	Open Mobile Terminals Platform
PC	Program Counter
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio
SC	System Controller
SDM	Sigma Delta Modulator
SNR	Signal to Noise Ratio
SRM	Sample Rate Matching
SWG	Sine Wave Generator
TDM	Time Division Multiplexing
THD+N	Total Harmonic Distortion plus Noise
VCO	Voltage-Controlled Oscillator
WCLK	Word Clock

1.1 Terminology

Crosstalk (dB)

The level difference between the active path output and the idle path measured signal level, at the test signal frequency. The active path is configured and supplied with an input signal capable of driving a full scale output, with the signal measured at the output of the specified idle path.

Mute Attenuation

The difference in level between the full scale output signal and the output with mute applied.

Channel Separation (dB) [left-to-right and right-to-left]

The difference in level between the active channel (driven to maximum full scale output) and the signal level measured in the idle channel at the test signal frequency. The active channel is configured and supplied with an input signal capable of driving a full scale output, with the signal measured at the output of the associated idle channel.

PSRR

The ratio of a given power supply change relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.

SNR

The difference in level between the maximum full scale output signal and the output with no input signal applied.

THD+N

The level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.

All performance measurements carried out with 20 kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low-pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

2 References

[1] Android Wired Audio Headset Specification (v1.1)
(https://source.android.com/accessories/headset/specification.html)

3 Block Diagram

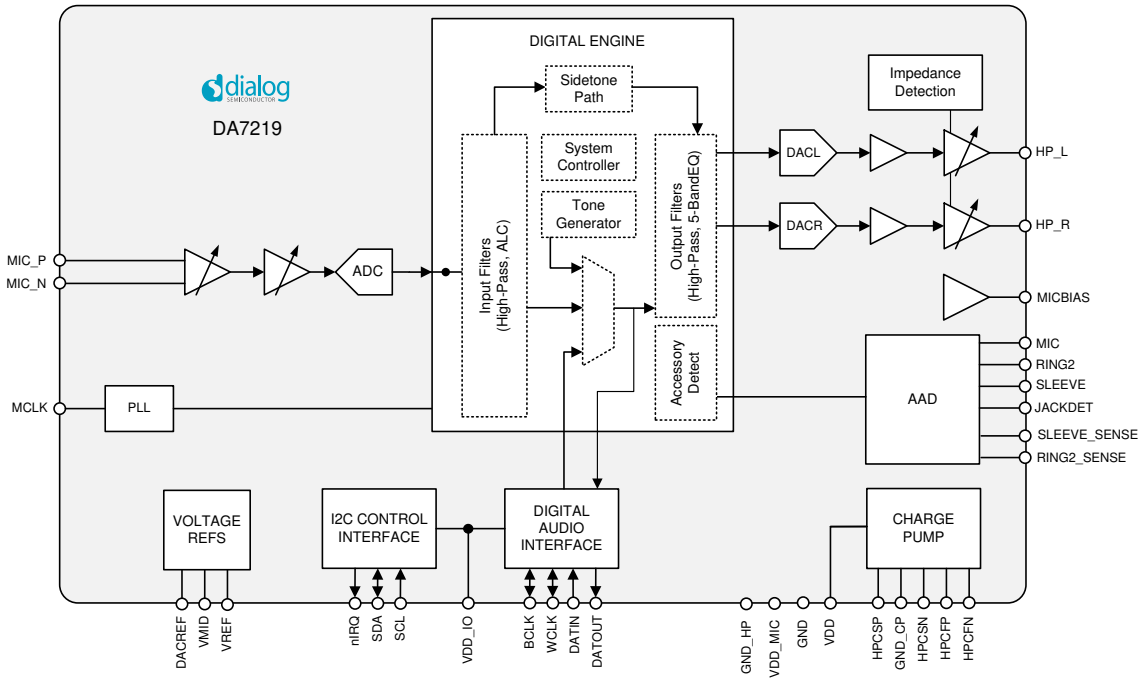

Figure 2: DA7219 Block Diagram

4 Ballout

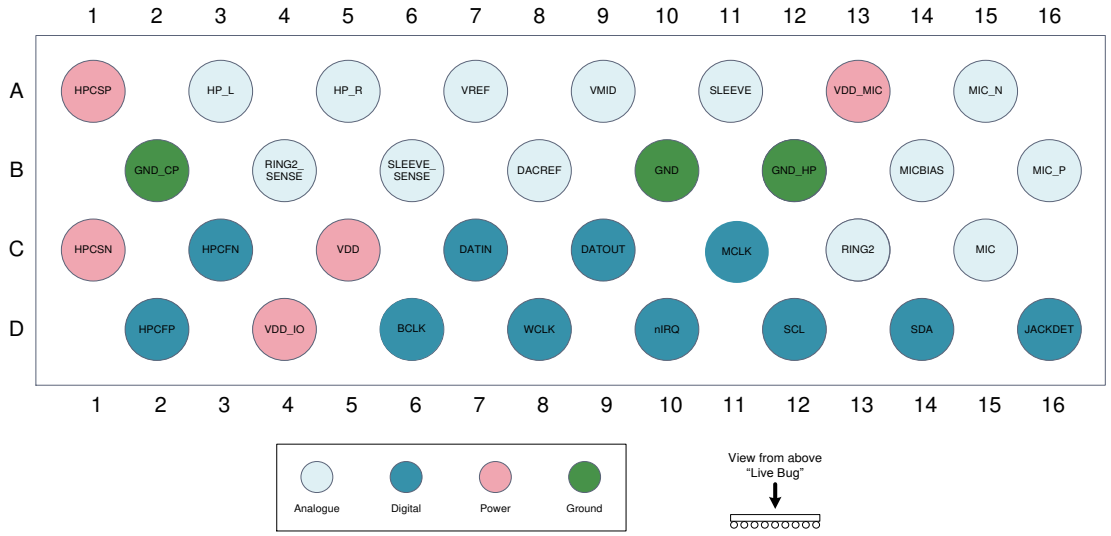

Figure 3: DA7219 Ballout Diagram

Table 1: Ball Description

Ball No.	Ball/Pin Name	Type (Table 2)	Description
Microphone Inputs			
B16	MIC_P	AI	Differential analog microphone 1 input (Pos)
A15	MIC_N	AI	Differential analog microphone 1 input (Neg)
B14	MICBIAS	AO	Microphone bias output
Accessory Detect			
D16	JACKDET	DI	Jack Detect Input from socket
A11	SLEEVE	AIO	Socket Sleeve (configured as MIC or GND)
C13	RING2	AIO	Socket Ring 2 (configured as GND or MIC)
B6	SLEEVE_SENSE	AIO	Socket Sleeve (Sense)
B4	RING2_SENSE	AIO	Socket Ring 2 (Sense)
C15	MIC	AIO	Microphone DC input
Headphone Outputs			
A3	HP_L	AO	Single-ended headphone output (Left)
A5	HP_R	AO	Single-ended headphone output (Right)
Charge Pump			
A1	HPCSP	AIO	Charge pump reservoir capacitor (Positive)
C1	HPCSN	AIO	Charge pump reservoir capacitor (Negative)
D2	HPCFP	AIO	Charge pump flying capacitor (Positive)
C3	HPCFN	AIO	Charge pump flying capacitor (Negative)
Digital Interface			
D14	SDA	DIOD	I^2C bidirectional data
D12	SCL	DI	I^2C clock

Ball No.	Ball/Pin Name	Type (Table 2)	Description
D10	nIRQ	DIOD	Interrupt output (open drain active low)
C7	DATIN	DIO	DAI data input to DA7219
C9	DATOUT	DIO	DAI data output from DA7219
D6	BCLK	DIO	DAI bit clock
D8	WCLK	DIO	DAI word clock
C11	MCLK	DI	Master clock input
References			
B8	DACREF	AIO	DAC reference decoupling capacitor
A9	VMID	AIO	Mid-rail reference decoupling capacitor
A7	VREF	AIO	Bandgap reference decoupling capacitor
Supplies			
C5	VDD	AI	Main analog and digital supply
A13	VDD_MIC	AI	Supply for MICBIAS LDO
D4	VDD_IO	AI	Supply for digital interfaces
Grounds			
B2	GND_CP	AI	Ground
B10	GND	AI	Ground
B12	GND_HP	AI	Ground

Table 2: Ball/Pin Type Definition

Ball/Pin Type	Description	Ball/Pin Type	Description
DI	Digital Input	AI	Analog Input
DIO	Digital Input/Output	AO	Analog Output
DIOD	Digital Input/Output open Drain	AIO	Analog Input/Output

5 Pin Descriptions

5.1 Microphone Pins

5.1.1 MIC_P

MIC_P is the positive differential input for the analog microphone channel. It can be used as a single-ended input if MIC_N is grounded (see

Figure 7).

5.1.2 MIC_N

MIC_N is the negative differential input for the analog microphone channel. It should be grounded when using a single-ended analog microphone configuration.

5.1.3 MICBIAS

MICBIAS is the internally generated microphone supply. This must be decoupled with a 1 µF capacitor.

5.2 Accessory Detect Pins

5.2.1 JACKDET

JACKDET is used to signal to the device when the Jack is fully inserted into the 3.5 mm jack (or alternative) socket.

The JACKDET pin is designed to be pulled either HIGH or LOW on the insertion of the jack. If using an HPLDET type headset socket additional external circuitry is required.

If not required it should be left unconnected.

5.2.2 SLEEVE

Sleeve is tested during the sense stage and then configured as either the headset microphone input or the headset ground connection.

5.2.3 RING2

RING2 is tested during the sense stage and then configured as either the headset microphone input or the headset ground connection.

5.2.4 SLEEVE_SENSE

SLEEVE sense line to guarantee accuracy over distance, cables and connectors.

5.2.5 RING2_SENSE

RING2 sense line to guarantee accuracy over distance, cables and connectors.

5.2.6 MIC

MIC is the DC input for the analog accessory detect.

5.3 Interface Input Pins

5.3.1 MCLK

MCLK is the master clock input pin. It is used as the main system clock either directly or via the PLL.

5.3.2 SCL

SCL is the Control Interface (I^2C) clock input and is used in conjunction with SDA to control the device.

5.3.3 DATIN

DATIN is the data input pin which forms part of the Digital Audio Interface (DAI). It is used to present audio playback data to the device.

5.4 Interface Output Pins

5.4.1 nIRQ

nIRQ is the open drain active-low interrupt output to alert the host to either an accessory or a level detect event.

5.4.2 DATOUT

DATOUT is the data output pin which forms part of the DAI. It is used to present audio record data to the host.

5.5 Interface Bidirectional Pins

5.5.1 SDA

SDA is the Control Interface (I^2C) data input/output and is used in conjunction with SCL to control the device.

5.5.2 BCLK

BCLK is the bit clock input/output pin which forms part of the DAI. It is used to clock audio data bits into or out from the device or both.

5.5.3 WCLK

WCLK is the word clock input/output pin which forms part of the DAI. It is used to indicate whether the data bits belong to the left or right audio channel.

5.6 Headphone Output Pins

5.6.1 HP_L

HP_L is the left-channel single-ended headphone output. It is ground-centered so the headphone speaker can be connected directly between HP_L and ground.

5.6.2 HP_R

HP_R is the right-channel single-ended headphone output. It is ground-centered so the headphone speaker can be connected directly between HP_R and ground.

5.7 Charge Pump Pins

5.7.1 HPCSP

HPCSP is the positive output from the headphone charge pump. It should be connected to GND_CP via a reservoir capacitor.

5.7.2 HPCSN

HPCSN is the negative output from the headphone charge pump. It must be connected to GND_CP via a reservoir capacitor.

5.7.3 HPCFP

HPCFP is one of the flying capacitor connections required by the headphone charge pump. It must be connected to HPCFN via a capacitor.

5.7.4 HPCFN

HPCFN is one of the flying capacitor connections required by the headphone charge pump. It must be connected to HPCFP via a capacitor.

5.8 References

5.8.1 VMID

VMID is the mid-rail reference decoupling capacitor connection.

5.8.2 DACREF

DACREF is the DAC reference decoupling capacitor connection.

5.8.3 VREF

VREF is the bandgap reference decoupling capacitor connection.

5.9 Supply Pins

5.9.1 VDD

VDD is main analog supply pin. It supplies all the analog circuits except the MICBIAS output and the HPAMP outputs.

5.9.2 VDD_IO

VDD_IO is the supply pin for the digital input/output signals. VDD_IO must be greater than or equal to VDD during device operation.

5.9.3 VDD_MIC

VDD_MIC is the supply pin for the MICBIAS. VDD_MIC must be greater than or equal to VDD during device operation.

5.10 Ground Pins

5.10.1 GND

GND is the main analog ground pin. It is the ground connection for all analog circuits with the exception of the charge pump.

5.10.2 GND_CP

GND_CP is the ground pin for the charge pump and the digital engine.

5.10.3 GND_HP

GND_HP is the ground point for the headset. When a headset is connected this pin is automatically connected internally to either RING2 or SLEEVE.

6 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
T_{STG}	Storage temperature		–65	+165	°C
T_a	Operating temperature		–40	+85	°C
V_{DD_LIM}	Main supply voltage		–0.3	+2.75	V
V_{VDD_IO}	Digital IO supply voltage		–0.3	+5.5	V
V_{DD_MIC}	Microphone bias supply voltage		–0.3	+5.5	V
V_{DDIO}	Digital IO pins: SDA, SCL, BCLK, WCLK, DATIN, DATOUT, MCLK		–0.3	V_{DD_IO} + 0.3	V
$V_{JACKDET}$	Accessory detect pins: JACKDET		–0.3	V_{DD} + 0.3	V
V_{ACCDET}	Accessory detect pins: RING2, SLEEVE, MIC, RING2_SENSE, SLEEVE_SENSE		–0.3	V_{DD_MIC} + 0.3	V
V_{MIC_P}, V_{MIC_N}	Analog input pins MIC_P and MIC_N		–0.3	V_{DD} + 0.3	V
V_{ESD_HBM}	ESD susceptibility	Human body model (HBM)	2000		V
V_{ESD_CDM}	ESD susceptibility	Charged device model (CDM)	500		V

Note 1 Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_a	Operating temperature		–25		85	°C
V_{DD}	Main supply voltage		1.7		2.5	V
V_{DD_IO}	Digital IO supply voltage	(Note 1)	VDD		3.6	V
V_{DD_MIC}	Microphone bias supply voltage	(Note 1)	VDD		3.6	V

Note 1 V_{DD_IO} and V_{DD_MIC} must be greater than or equal to V_{DD}.

8 Electrical Characteristics

Unless otherwise stated, test conditions are as follows: V_{DD} = V_{DD_IO} = 1.8 V, V_{DD_MIC} = 3.3 V, MCLK = 12.288 MHz, SR = 48 kHz, PLL = Bypass mode, T_a = 25 ºC.

Table 5: Power Consumption

Description	Conditions	Min	Typ	Max	Unit
DEEP SLEEP mode			4	10	µA
SLEEP mode	AAD on without button detection		185		µA
Digital playback to headphone, no load	DAC to HP_L/R, quiescent		3.4		mW
Digital playback to headphone, with load	DAC to HP_L/R, 16 Ω load, 0.1 mW at 0 dBFS		7.5		mW
Microphone stereo record	MIC P/N to ADCL/R		2.75		mW
Microphone stereo record and digital playback to headphone, no load	MIC P/N to ADCL/R and DACL/R to HP_L/R, quiescent		4.8		mW
Microphone stereo record and digital playback to headphone, with load	MIC P/N to ADCL/R and DACL/R to HP_L/R, 16 Ω load, 0.1 mW at 0 dBFS		8.9		mW

Table 6: Microphone Bias

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{MICBIAS}$	Output voltage	No load, V_{DD_MIC} > $V_{MICBIAS}$ + 200 mV Level programmable using micbias1_level	1.6		2.9	V
I_{BIAS}	Output current	Output voltage droop < 50 mV		2		mA
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB
V_{NO}	Output voltage noise	$V_{MICBIAS}$ ≤ 2.2 V		5		μV_{RMS}

Table 7: Microphone Amplifier

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Full-scale input signal	0 dB, singled-ended 0 dB gain, differential		0.8*V_{DD} 1.6*V_{DD}		V_{PP}
	Input resistance		12	15	18	kΩ
	Programmable gain		−6		36	dB
	Gain step size			6		dB
	Absolute gain accuracy	0 dB @ 1 kHz	-1.0		1.0	dB
	Gain step error	20 Hz to 20 kHz	-0.1		0.1	dB
VNI	Input noise level	Inputs connected to GND, 24 dB gain, input-referred, A-weighted		5		μV_{RMS}
	Amplitude ripple	20 Hz to 20 kHz	-0.5		0.5	dB
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	90 70			dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
CMRR	Common mode rejection ratio			70		dB

Table 8: Input Mix Amplifier (mixinamp)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Programmable gain		−4.5		+18	dB
	Gain step size			1.5		dB
	Absolute gain accuracy	0 dB @ 1 kHz	-1.0		+1.0	dB
	Gain step error	20 Hz to 20 kHz	-0.1		+0.1	dB
	Amplitude ripple	20 Hz to 20 kHz	-0.5		+0.5	dB

Table 9: Mono Analog to Digital Converter (adc_mono)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale input signal	0 dBFS digital output level		1.6*V_{DD}		V_{PP}
SNR	Signal to noise ratio	A-weighted		90		dB
THD+N	Total harmonic distortion plus noise	-1 dBFS analog input level		-85		dB
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 10: Stereo Digital to Analog Converter (dac_stereo)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale output signal	0 dBFS digital input level		1.6*V_{DD}		V_{PP}
SNR	Signal to Noise Ratio	A-weighted		100		dB
THD+N	Total harmonic distortion plus noise	-1 dBFS digital input level		-90		dB
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 11: Stereo Headphone Amplifier (audio_hpamp_stereo)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale output signal	No load		1.6*V_{DD}		V_{PP}
	DC output offset	−30 dB gain		250		µV
	Maximum output power per channel	V_{DD} = 1.8 V, THD < 0.1%, R_{LOAD} = 16 Ω, 1 kHz		30		mW_{RMS}
	Maximum output power per channel	V_{DD} = 2.5 V, THD < 0.1%, R_{LOAD} = 16 Ω, 1 kHz		70		mW_{RMS}
	Load resistance		13	16		Ω
	Load capacitance				500	pF
	Load inductance				400	µH
Frequency Response	20 Hz to 20 kHz		-0.5		+0.5	dB
SNR	Signal to Noise Ratio	V_{DD} = 1.8 V, 0 dB gain		98		dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
		V_{DD} = 2.5 V, 0 dB gain		100		dB
V_{NO}	Output noise level	20 Hz to 20 kHz, <20 dB gain			2.5	μV_{RMS}
THD+N	Total harmonic distortion plus noise	V_{DD} = 1.8 V, R_{LOAD} = 16 Ω, -5 dBFS, 1 kHz		−85		dB
	Channel separation	V_{DD} = 1.8 V, R_{LOAD} = 32 Ω, 1 kHz		90		dB
	Programmable gain		−57		6	dB
	Gain step size			1.0		dB
	Absolute gain accuracy	0 dB @ 1 kHz	−0.8		0.8	dB
	Left/right gain mismatch	20 Hz to 20 kHz	−0.1		0.1	dB
	Gain step error	20 Hz to 20 kHz	−0.1		0.1	dB
	Amplitude ripple	20 Hz to 20 kHz	−0.5		0.5	dB
	Mute attenuation			−70		dB
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 12: Input Filters

Parameter	Description	Conditions	Min	Typ	Max	Unit
BPASS	Pass band				0.45*FS	Hz
	Pass band ripple	Voice mode Music mode			±0.3 ±0.1	dB
BSTOP	Stop band	FS ≤ 48 kHz FS = 88.2 kHz or 96 kHz	0.56*FS		7*FS 3.5*FS	Hz
	Stop band attenuation	Voice mode Music mode	70 55			dB
	Group delay	Voice mode Music mode FS = 88.2 kHz or 96 kHz		4.3/FS 18/FS 9/FS		s
	Digital gain		-83.25		12	dB
	Digital gain step size			0.75		dB

Table 13: DAC Filter

Parameter	Description	Conditions	Min	Typ	Max	Unit
BPASS	Pass band				0.45*FS	Hz
	Pass band ripple	Voice mode Music mode			±0.3 ±0.1	dB
BSTOP	Stop band	FS ≤ 48 kHz FS = 88.2 kHz or 96 kHz	0.56*FS		7*FS 3.5*FS	Hz
	Stop band attenuation	Voice mode Music mode	70 55			dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Group delay	Voice mode Music mode FS = 88.2 kHz or 96 kHz		4.3/FS 18/FS 9/FS		s
	Group delay variation	20 Hz to 20 kHz			1	µs
	Left/right channel group delay mismatch				2	µs
	Digital gain range		-71.25		18	dB
	Digital gain step size			0.75		dB

Table 14: Automatic Level Control (ALC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Attack rate	FS = 48 kHz	1.6		6500	dB/s
	Release rate	FS = 48 kHz	1.6		1675	dB/s
	Hold time	FS = 48 kHz	1.3		42300	ms
	Maximum threshold		−94.5		0	dBFS
	Minimum threshold		−94.5		0	dBFS
	Noise threshold		−94.5		0	dBFS
	Threshold step size			1.5		dB
	Maximum overall gain		0		90	dB
	Maximum overall attenuation		0		90	dB
	Maximum analog gain		0		36	dB
	Minimum analog gain		0		36	dB
	Gain step size			1.5		dB

Table 15: Advanced Accessory Detect (AAD)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Ring2 ground switch resistance				50	mΩ
	Sleeve ground switch resistance				50	mΩ

Table 16: Reference Voltages

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{REF}	Bandgap voltage reference			1.2		V
DACREF	DAC reference			0.9*V_{DD}		V
V_{MID}	Mid-rail voltage reference			0.45*V_{DD}		V
	Charge pump positive voltage	VDD mode		1.8		V
		VDD/2 mode		0.9		V
	Charge pump negative voltage	VDD mode		-1.8		V
		VDD/2 mode		-0.9		V

Table 17: PLL Mode

Description	Conditions	Min	Typ	Max	Unit
MCLK input jitter	Absolute jitter (rms) Note 1			540	ps
MCLK input frequency	Normal mode	2		54	MHz
SRM tracking range	DAI slave mode WCLK frequency variation	-4		4	%
SRM tracking rate	DAI slave mode WCLK drift rate			54	ppm/s

Note 1 Jitter in the 100 Hz to 40 kHz band

Table 18: Bypass Mode

Description	Conditions	Min	Typ	Max	Unit
MCLK input jitter	Absolute jitter (rms) Note 1			540	ps
MCLK input frequency	F_S = 11.025, 22.05, 44.1, 88.2 kHz F_S = 8, 12, 16, 24, 32, 48, 96 kHz		11.2896 12.288		MHz

Note 1 Jitter in the 100 Hz to 40 kHz band

Table 19: Tone Generator

Description	Conditions	Min	Typ	Max	Unit
Single-tone frequency	F_S = 8, 12, 16, 24, 32, 48, 96 kHz F_S = 11.025, 22.05, 44.1, 88.2 kHz	1 1		12000 11025	Hz
Single-tone frequency step	F_S = 8, 12, 16, 24, 32, 48, 96 kHz F_S = 11.025, 22.05, 44.1, 88.2 kHz		0.18 0.17		Hz
Dual-tone modulation frequency A			697 770 852 941		Hz
Dual-tone modulation frequency B			1209 1336 1477 1633		Hz
Output programmable gain	Programmable via tone_gen_gain	-45		0	dBFS
On/off pulse duration		10		2000	ms
On/off pulse step size	10 ms to 200 ms duration 200 ms to 2000 ms duration		10 50		ms
On/off pulse repeat	Programmable Continuous		1, 2, 3, 4, 5, 6 ∞		Cycles