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DAC1005D650

Dual 10-bit DAC, up to 650 Msps; 2× 4× and 8× interpolating

Rev. 04 — 2 July 2012 Product data sheet

1. General description

The DAC1005D650 is a high-speed 10-bit dual-channel Digital-to-Analog Converter (DAC) with selectable 2×, 4× or 8× interpolating filters optimized for multi-carrier wireless transmitters.

Thanks to its digital on-chip modulation, the DAC1005D650 allows the complex I and Q inputs to be converted up from BaseBand (BB) to IF. The mixing frequency is adjusted using a Serial Peripheral Interface (SPI) with a 32-bit Numerically Controlled Oscillator (NCO). The phase is controlled by a 16-bit register.

Two modes of operation are available: separate data ports or a single interleaved high-speed data port. In the Interleaved mode, the input data stream is demultiplexed into its original I and Q data and then latched.

The DAC1005D650 also includes a 2×, 4× and 8× clock multiplier which provides the appropriate internal clocks and an internal regulator to adjust the output full-scale current.

2. Features and benefits

- Dual 10-bit resolution
- 650 Msps maximum update rate
- Selectable 2×, 4× or 8× interpolation filters
- Input data rate up to 160 Msps
- Very low noise cap-free integrated PLL
- 32-bit programmable NCO frequency
- Dual-port or Interleaved data modes
- 1.8 V and 3.3 V power supplies
- LVDS compatible clock
- Two's complement or binary offset data format
- 3.3 V CMOS input buffers
- IMD3: 79 dBc; f_s = 640 Msps; f_o = 96 MHz
- SFDR: 75 dBc; f_{data} = 80 MHz; f_s = 640 Msps; f_o = 19 MHz; PLL on
- Typical 0.95 W power dissipation at 4× interpolation
- Power-down and Sleep modes
- Differential scalable output current from 1.6 mA to 20 mA
- On-chip 1.29 V reference
- External analog offset control (10-bit auxiliary DACs)
- Internal digital offset control
- Inverse (sin x) / x function
- Fully compatible SPI port
- Industrial temperature range from −40 °C to +85 °C

3. Applications

- Wireless infrastructure: LTE, WiMAX, GSM, CDMA, WCDMA, TD-SCDMA
- Communication: LMDS/MMDS, point-to-point
- Direct Digital Synthesis (DDS)
- Broadband wireless systems
- Digital radio links
- Instrumentation
- Automated Test Equipment (ATE)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
DAC1005D650HW-C1	HTQFP100	plastic thermal enhanced thin quad flat package; 100 leads; body 14 × 14 × 1 mm; exposed die pad	SOT638-1

5. Block diagram

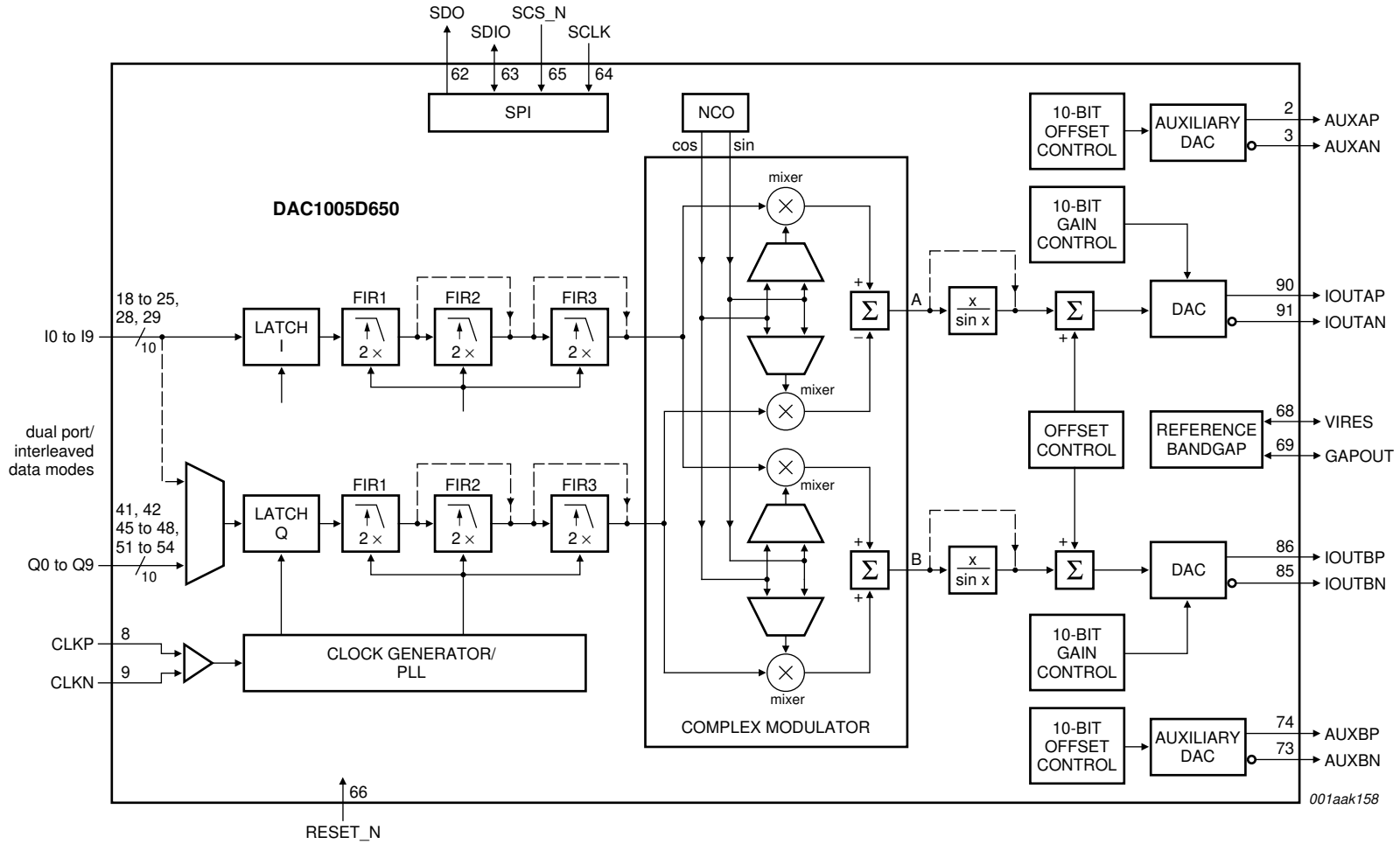


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

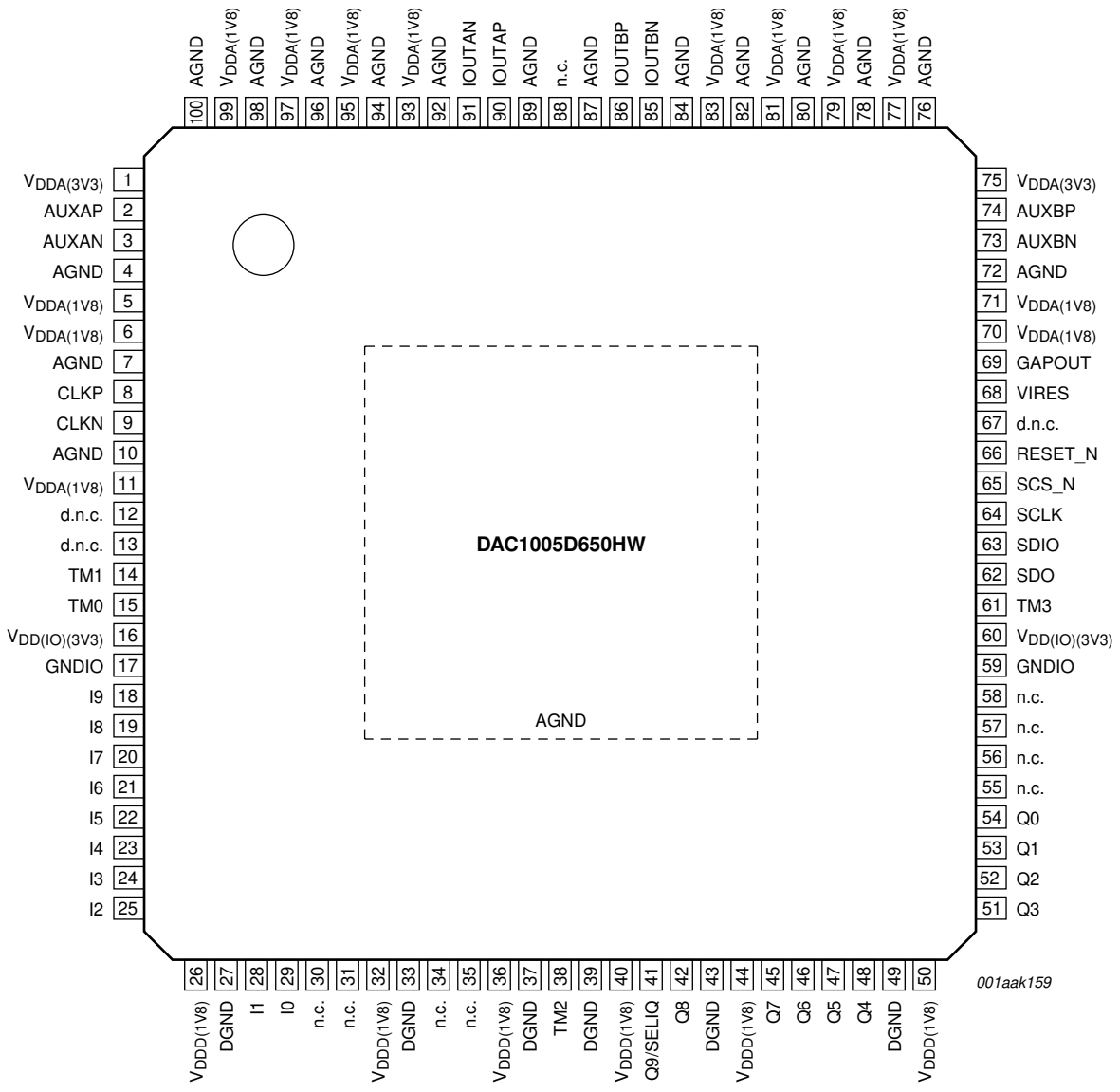


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
$V_{DDA(3V3)}$	1	P	analog supply voltage 3.3 V
AUXAP	2	O	auxiliary DAC B output current
AUXAN	3	O	complementary auxiliary DAC B output current
AGND	4	G	analog ground
$V_{DDA(1V8)}$	5	P	analog supply voltage 1.8 V
$V_{DDA(1V8)}$	6	P	analog supply voltage 1.8 V
AGND	7	G	analog ground
CLKP	8	I	clock input
CLKN	9	I	complementary clock input
AGND	10	G	analog ground
$V_{DDA(1V8)}$	11	P	analog supply voltage 1.8 V
d.n.c.	12	-	do not connect
d.n.c.	13	-	do not connect
TM1	14	I/O	test mode 1 (to connect to DGND)
TM0	15	I/O	test mode 0 (to connect to DGND)
$V_{DD(IO)(3V3)}$	16	P	input/output buffers supply voltage 3.3 V
GNDIO	17	G	input/output buffers ground
I9	18	I	I data input bit 9 (MSB)
I8	19	I	I data input bit 8
I7	20	I	I data input bit 7
I6	21	I	I data input bit 6
I5	22	I	I data input bit 5
I4	23	I	I data input bit 4
I3	24	I	I data input bit 3
I2	25	I	I data input bit 2
$V_{DDD(1V8)}$	26	P	digital supply voltage 1.8 V
DGND	27	G	digital ground
I1	28	I	I data input bit 1
I0	29	I	I data input bit 0 (LSB)
n.c.	30	I	not connected
n.c.	31	I	not connected
$V_{DDD(1V8)}$	32	P	digital supply voltage 1.8 V
DGND	33	G	digital ground
n.c.	34	I	not connected
n.c.	35	I	not connected
$V_{DDD(1V8)}$	36	P	digital supply voltage 1.8 V
DGND	37	G	digital ground
TM2	38	-	test mode 2 (to connect to DGND)
DGND	39	G	digital ground

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
$V_{DDD(1V8)}$	40	P	digital supply voltage 1.8 V
Q9/SELIQ	41	I	Q data input bit 9 (MSB) select IQ
Q8	42	I	Q data input bit 8
DGND	43	G	digital ground
$V_{DDD(1V8)}$	44	P	digital supply voltage 1.8 V
Q7	45	I	Q data input bit 7
Q6	46	I	Q data input bit 6
Q5	47	I	Q data input bit 5
Q4	48	I	Q data input bit 4
DGND	49	G	digital ground
$V_{DDD(1V8)}$	50	P	digital supply voltage 1.8 V
Q3	51	I	Q data input bit 3
Q2	52	I	Q data input bit 2
Q1	53	I	Q data input bit 1
Q0	54	I	Q data input bit 0 (LSB)
n.c.	55	I	not connected
n.c.	56	I	not connected
n.c.	57	I	not connected
n.c.	58	I	not connected
GNDIO	59	G	input/output buffers ground
$V_{DD(IO)(3V3)}$	60	P	input/output buffers supply voltage 3.3 V
TM3	61	I/O	test mode 3 (to connect to DGND)
SDO	62	O	SPI data output
SDIO	63	I/O	SPI data input/output
SCLK	64	I	SPI clock
SCS_N	65	I	SPI chip select (active LOW)
RESET_N	66	I	general reset (active LOW)
d.n.c.	67	-	do not connect
VIRES	68	I/O	DAC biasing resistor
GAPOUT	69	I/O	bandgap input/output voltage
$V_{DDA(1V8)}$	70	P	analog supply voltage 1.8 V
$V_{DDA(1V8)}$	71	P	analog supply voltage 1.8 V
AGND	72	G	analog ground
AUXBN	73	O	complementary auxiliary DAC B output current
AUXBP	74	O	auxiliary DAC B output current
$V_{DDA(3V3)}$	75	P	analog supply voltage 3.3 V
AGND	76	G	analog ground
$V_{DDA(1V8)}$	77	P	analog supply voltage 1.8 V
AGND	78	G	analog ground
$V_{DDA(1V8)}$	79	P	analog supply voltage 1.8 V

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
AGND	80	G	analog ground
$V_{DDA(1V8)}$	81	P	analog supply voltage 1.8 V
AGND	82	G	analog ground
$V_{DDA(1V8)}$	83	P	analog supply voltage 1.8 V
AGND	84	G	analog ground
IOUTBN	85	O	complementary DAC B output current
IOUTBP	86	O	DAC B output current
AGND	87	G	analog ground
n.c.	88	-	not connected
AGND	89	G	analog ground
IOUTAP	90	O	DAC A output current
IOUTAN	91	O	complementary DAC A output current
AGND	92	G	analog ground
$V_{DDA(1V8)}$	93	P	analog supply voltage 1.8 V
AGND	94	G	analog ground
$V_{DDA(1V8)}$	95	P	analog supply voltage 1.8 V
AGND	96	G	analog ground
$V_{DDA(1V8)}$	97	P	analog supply voltage 1.8 V
AGND	98	G	analog ground
$V_{DDA(1V8)}$	99	P	analog supply voltage 1.8 V
AGND	100	G	analog ground
AGND	H[2]	G	analog ground

[1] P = power supply
G = ground
I = input
O = output.

[2] H = heatsink (exposed die pad to be soldered).

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(IO)(3V3)}$	input/output supply voltage (3.3 V)		−0.5	+4.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		−0.5	+4.6	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		−0.5	+3.0	V
$V_{DDD(1V8)}$	digital supply voltage (1.8 V)		−0.5	+3.0	V
V_I	input voltage	pins CLKP, CLKN, VIRES and GAPOUT referenced to AGND	−0.5	+3.0	V
		pins I9 to I0, Q9 to Q0, SDO, SDIO, SCLK, SCS_N and RESET_N referenced to GNDIO	−0.5	+4.6	V
V_O	output voltage	pins IOUTAP, IOUTAN, IOUTBP, IOUTBN, AUXAP, AUXAN, AUXBP and AUXBN referenced to AGND	−0.5	+4.6	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		−45	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	19.8	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	7.7	K/W

[1] In compliance with JEDEC test board, in free air.

9. Characteristics

Table 5. Characteristics

$V_{DDA(1V8)}$ = $V_{DDD(1V8)}$ = 1.8 V; $V_{DDA(3V3)}$ = $V_{DD(IO)(3V3)}$ = 3.3 V; AGND, DGND and GNDIO shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at T_{amb} = 25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; PLL on; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
$V_{DD(IO)(3V3)}$	input/output supply voltage (3.3 V)		I	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		I	3.0	3.3	3.6	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		I	1.7	1.8	1.9	V
$V_{DDD(1V8)}$	digital supply voltage (1.8 V)		I	1.7	1.8	1.9	V
$I_{DD(IO)(3V3)}$	input/output supply current (3.3 V)	f_o = 19 MHz; f_s = 640 Msps; 8× interpolation; NCO on	I	-	5	13	mA
$I_{DDA(3V3)}$	analog supply current (3.3 V)	f_o = 19 MHz; f_s = 640 Msps; 8× interpolation; NCO on	I	-	48	26	mA
$I_{DDD(1V8)}$	digital supply current (1.8 V)	f_o = 19 MHz; f_s = 640 Msps; 8× interpolation; NCO on	I	-	270	309	mA
$I_{DDA(1V8)}$	analog supply current (1.8 V)	f_o = 19 MHz; f_s = 640 Msps; 8× interpolation; NCO on	I	-	330	358	mA
I_{DDD}	digital supply current	for x / (sin x) function only	I	-	67	-	mA
P_{tot}	total power dissipation	f_o = 19 MHz; f_s = 320 Msps; 4× interpolation; NCO off; DAC B off	C	-	0.53	-	W
		f_o = 19 MHz; f_s = 320 Msps; 4× interpolation; NCO off	C	-	0.82	-	W
		f_o = 19 MHz; f_s = 320 Msps; 4× interpolation; NCO on	C	-	0.94	-	W
		f_o = 19 MHz; f_s = 640 Msps; 8× interpolation; NCO off	C	-	0.95	-	W
		f_o = 19 MHz; f_s = 640 Msps; 8× interpolation; NCO on; all V_{DD}	I	-	1.18	1.4	W
		f_o = 19 MHz; f_s = 640 Msps; 8× interpolation; NCO low power on	C	-	1.07	-	W
		Power-down mode					
		full power-down; all V_{DD}	I	-	0.08	0.13	W
		DAC A and DAC B Sleep mode; 8× interpolation; NCO on	I	-	0.88	-	W

Table 5. Characteristics *…continued*

$V_{DDA(1V8)}$ = $V_{DDD(1V8)}$ = 1.8 V; $V_{DDA(3V3)}$ = $V_{DD(IO)(3V3)}$ = 3.3 V; AGND, DGND and GNDIO shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at T_{amb} = 25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; PLL on; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Clock inputs (CLKP and CLKN)[2]							
V_i	input voltage	CLKP; or CLKN $\|V_{gpd}\|$ < 50 mV	C [3]	825	-	1575	mV
V_{idth}	input differential threshold voltage	$\|V_{gpd}\|$ < 50 mV	C [3]	−100	-	+100	mV
R_i	input resistance		D	-	10	-	MΩ
C_i	input capacitance		D	-	0.5	-	pF
Digital inputs (I0 to I13, Q0 to Q13)							
V_{IL}	LOW-level input voltage		C	GNDIO	-	1.0	V
V_{IH}	HIGH-level input voltage		C	2.3	-	$V_{DD(IO)(3V3)}$	V
I_{IL}	LOW-level input current	V_{IL} = 1.0 V	I	-	40	-	μA
I_{IH}	HIGH-level input current	V_{IH} = 2.3 V	I	-	80	-	μA
Digital inputs (SDO, SDIO, SCLK, SCS_N and RESET_N)							
V_{IL}	LOW-level input voltage		C	GNDIO	-	1.0	V
V_{IH}	HIGH-level input voltage		C	2.3	-	$V_{DD(IO)(3V3)}$	V
I_{IL}	LOW-level input current	V_{IL} = 1.0 V	I	-	20	-	nA
I_{IH}	HIGH-level input current	V_{IH} = 2.3 V	I	-	20	-	nA
Analog outputs (IOUTAP, IOUTAN, IOUTBP and IOUTBN)							
$I_{O(fs)}$	full-scale output current	register value = 00h	C	-	1.6	-	mA
		default register	C	-	20	-	mA
V_O	output voltage	compliance range	C	1.8	-	$V_{DDA(3V3)}$	V
R_o	output resistance		D	-	250	-	kΩ
C_o	output capacitance		D	-	3	-	pF
$N_{DAC(mono)}$	DAC monotonicity	guaranteed	D	-	8	-	bit
ΔE_O	offset error variation		C	-	6	-	ppm/°C
ΔE_G	gain error variation		C	-	18	-	ppm/°C
Reference voltage output (GAPOUT)							
$V_{O(ref)}$	reference output voltage	T_{amb} = 25 °C	I	1.24	1.29	1.34	V
$\Delta V_{O(ref)}$	reference output voltage variation		C	-	117	-	ppm/°C
$I_{O(ref)}$	reference output current	external voltage 1.25 V	D	-	40	-	μA

Table 5. Characteristics *…continued*

$V_{DDA(1V8)}$ = $V_{DDD(1V8)}$ = 1.8 V; $V_{DDA(3V3)}$ = $V_{DD(IO)(3V3)}$ = 3.3 V; AGND, DGND and GNDIO shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at T_{amb} = 25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; PLL on; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Analog auxiliary outputs (AUXAP, AUXAN, AUXBP and AUXBN)							
$I_{O(aux)}$	auxiliary output current	differential outputs	I	-	2.2	-	mA
$V_{O(aux)}$	auxiliary output voltage	compliance range	C	0	-	2	V
$N_{DAC(aux)mono}$	auxiliary DAC monotonicity	guaranteed	D	-	10	-	bit
Input timing (see Figure 10)							
f_{data}	data rate	Dual-port mode input	C	-	-	160	MHz
$t_{w(CLK)}$	CLK pulse width		C	1.5	-	T_{data} − 1.5	ns
$t_{h(i)}$	input hold time		C	1.1	-	-	ns
$t_{su(i)}$	input set-up time		C	1.1	-	-	ns
Output timing							
f_s	sampling frequency		C	-	-	650	Msps
t_s	settling time	to ±0.5 LSB	D	-	20	-	ns
NCO frequency range; f_s = 640 Msps							
f_{NCO}	NCO frequency	register value = 00000000h	D	-	0	-	MHz
		register value = FFFFFFFFh	D	-	640	-	MHz
f_{step}	step frequency		D	-	0.149	-	Hz
Low-power NCO frequency range; f_{DAC} = 640 MHz							
f_{NCO}	NCO frequency	register value = 00000000h	D	-	0	-	MHz
		register value = F8000000h	D	-	620	-	MHz
f_{step}	step frequency		D	-	20	-	MHz
Dynamic performance; PLL on							
SFDR	spurious-free dynamic range	f_{data} = 80 MHz; f_s = 320 Msps; B = f_{data} / 2					
		f_o = 35 MHz at 0 dBFS	C	-	82	-	dBc
		f_{data} = 80 MHz; f_s = 640 Msps; B = f_{data} / 2					
		f_o = 4 MHz at 0 dBFS	I	-	76	-	dBc
		f_o = 19 MHz at 0 dBFS	I	-	75	-	dBc
		f_{data} = 160 MHz; f_s = 640 Msps; B = f_{data} / 2					
		f_o = 70 MHz at 0 dBFS	C	-	82	-	dBc

Table 5. Characteristics *…continued*

$V_{DDA(1V8)}$ = $V_{DDD(1V8)}$ = 1.8 V; $V_{DDA(3V3)}$ = $V_{DD(IO)(3V3)}$ = 3.3 V; AGND, DGND and GNDIO shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at T_{amb} = 25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; PLL on; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
$SFDR_{RBW}$	restricted bandwidth spurious-free dynamic range	f_s = 640 Msps; f_o = 96 MHz at 0 dBFS					
		2.51 MHz ≤ f_{offset} ≤ 2.71 MHz; B = 30 kHz	I	-	−89	−83	dBc
		2.71 MHz ≤ f_{offset} ≤ 3.51 MHz; B = 30 kHz	I	-	−88	-	dBc
		3.51 MHz ≤ f_{offset} ≤ 4 MHz; B = 30 kHz	I	-	−89	−81	dBc
		4 MHz ≤ f_{offset} ≤ 40 MHz; B = 1 MHz	I	-	−83	−67	dBc
IMD3	third-order intermodulation distortion	f_s = 320 Msps; 4× interpolation					
		f_{o1} = 49 MHz; f_{o2} = 51 MHz	C	[4] -	81	-	dBc
		f_{o1} = 95 MHz; f_{o2} = 97 MHz	C	[4] -	80	-	dBc
		f_s = 640 Msps; 8× interpolation					
		f_{o1} = 95 MHz; f_{o2} = 97 MHz	I	[4] 67	79	-	dBc
		f_{o1} = 152 MHz; f_{o2} = 154 MHz	C	[4] -	77	-	dBc
ACPR	adjacent channel power ratio	f_{data} = 76.8 MHz; f_s = 614.4 Msps; f_o = 96 MHz					
		1 carrier; B = 5 MHz	I	-	64	-	dB
		2 carriers; B = 10 MHz	C	-	61	-	dB
		4 carriers; B = 20 MHz	C	-	60	-	dB
		f_{data} = 153.6 MHz; f_s = 614.4 Msps; f_o = 115.2 MHz					
		1 carrier; B = 5 MHz	C	-	67	-	dB
		2 carriers; B = 10 MHz	C	-	63	-	dB
		4 carriers; B = 20 MHz	C	-	60	-	dB
		f_{data} = 153.6 MHz; f_s = 614.4 Msps; f_o = 153.6 MHz					
		1 carrier; B = 5 MHz	C	-	65	-	dB
		2 carriers; B = 10 MHz	C	-	63	-	dB
		4 carriers; B = 20 MHz	C	-	60	-	dB
NSD	noise spectral density	f_s = 640 Msps; 8× interpolation; f_o = 19 MHz at 0 dBFS					
		noise shaper disabled	C	-	−138	-	dBm/Hz
		noise shaper enabled	C	-	−139	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] CLKP and CLKN inputs are at differential LVDS levels. An external differential resistor with a value of between 80 Ω and 120 Ω should be connected across the pins (see Figure 8).

[3] $|V_{gpd}|$ represents the ground potential difference voltage. This is the voltage that results from current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground.

[4] IMD3 rejection with −6 dBFS/tone.

10. Application information

10.1 General description

The DAC1005D650 is a dual 10-bit DAC operating at up to 650 Msps. Each DAC consists of a segmented architecture, comprising a 6-bit thermometer sub-DAC and an 4-bit binary weighted sub-DAC.

With an input data rate of up to 160 MHz, and a maximum output sampling rate of 650 Msps, the DAC1005D650 allows more flexibility for wide bandwidth and multi-carrier systems. Combined with its quadrature modulator and its 32-bit NCO, the DAC1005D650 simplifies the frequency selection of the system. This is also possible because of the 2×, 4× and 8× interpolation filters that remove undesired images.

Two modes are available for the digital input. In the Dual-port mode, each DAC uses its own data input line. In Interleaved mode, both DACs use the same data input line.

Each DAC generates two complementary current outputs on pins IOUTAP/IOUTAN and IOUTBP/IOUTBN. This provides a full-scale output current ($I_{O(fs)}$) up to 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

There are embedded features which provide analog offset correction (internal auxiliary DACs), digital offset control and gain adjustment. All the functions can be set using a SPI.

The DAC1005D650 operates at both 3.3 V and 1.8 V using separate digital and analog power supplies. The digital input is 3.3 V compliant and the clock input is LVDS compliant.

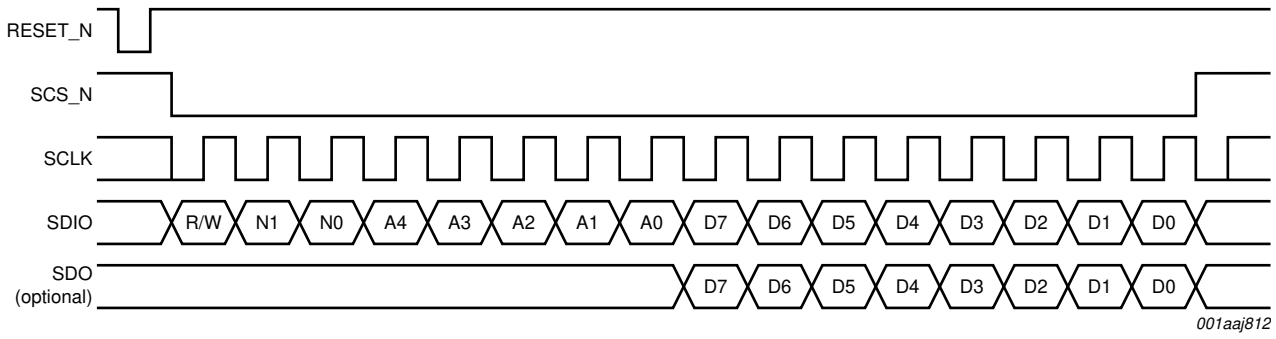
10.2 Serial interface (SPI)

10.2.1 Protocol description

The DAC1005D650 serial interface is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both write and read modes.

This interface can be configured as a 3-wire type (SDIO as bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pin, input and output port respectively). In both configurations, SCLK acts as the serial clock, and SCS_N acts as the serial chip select bar. If several DAC1005D650 devices are connected to an application on the same SPI-bus, only a 3-wire type can be used.

Each read/write operation is sequenced by the SCS_N signal and enabled by a LOW assertion to drive the chip with between 2 to 5 bytes, depending on the content of the instruction byte (see Table 7).



R/W indicates the mode access (see Table 6).

Fig 3. SPI protocol

Table 6. Read or Write mode access description

R/W	Description
0	Write mode operation
1	Read mode operation

In Table 7 N1 and N0 indicate the number of bytes transferred after the instruction byte.

Table 7. Number of bytes to be transferred

N1	N0	Number of bytes
0	0	1 byte transferred
0	1	2 bytes transferred
1	0	3 bytes transferred
1	1	4 bytes transferred

A0 to A4 indicates which register is being addressed. In the case of a multiple transfer, this address concerns the first register after which the next registers follow directly in decreasing order according to Table 9 “Register allocation map”.

10.2.2 SPI timing description

SPI can operate at a frequency of up to 15 MHz. The SPI timing is shown in Figure 4.

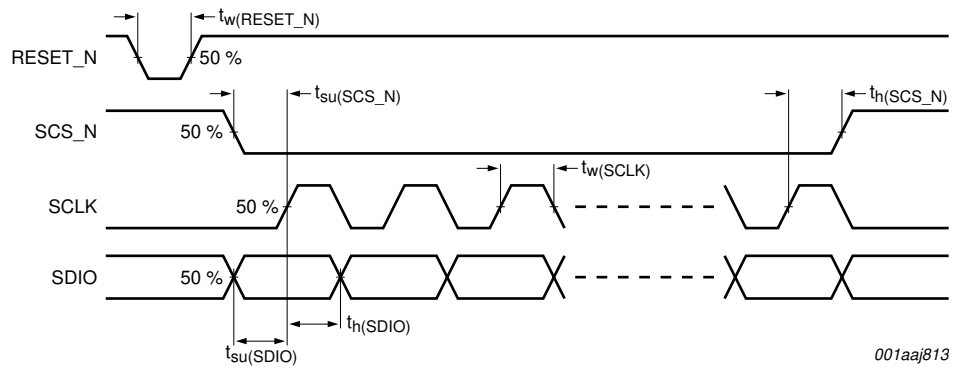


Fig 4. SPI timing diagram

The SPI timing characteristics are given in Table 8.

Table 8. SPI timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency	-	-	15	MHz
$t_{w(SCLK)}$	SCLK pulse width	30	-	-	ns
$t_{su(SCS\_N)}$	SCS_N set-up time	20	-	-	ns
$t_{h(SCS\_N)}$	SCS_N hold time	20	-	-	ns
$t_{su(SDIO)}$	SDIO set-up time	10	-	-	ns
$t_{h(SDIO)}$	SDIO hold time	5	-	-	ns
$t_{w(RESET\_N)}$	RESET_N pulse width	30	-	-	ns

10.2.3 Detailed descriptions of registers

An overview of the details for all registers is provided in Table 9.

Table 9. Register allocation map

Address		Register name	R/W	Bit definition								Default		
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex	Dec
0	00h	COMMon	R/W	3W_SPI	SPI_RST	CLK_SEL	-	MODE_SEL	CODING	IC_PD	GAP_PD	10000000	80	128
1	01h	TXCFG	R/W	NCO_ON	NCO_LP_SEL	INV_SIN_SEL	MODULATION[2:0]			INTERPOLATION[1:0]		10000111	87	135
2	02h	PLLCFG	R/W	PLL_PD	-	PLL_DIV_PD	PLL_DIV[1:0]		PLL_PHASE[1:0]		PLL_POL	00010000	10	16
3	03h	FREQNCO_LSB	R/W	FREQ_NCO[7:0]								01100110	66	102
4	04h	FREQNCO_LISB	R/W	FREQ_NCO[15:8]								01100110	66	102
5	05h	FREQNCO_UISB	R/W	FREQ_NCO[23:16]								01100110	66	102
6	06h	FREQNCO_MSB	R/W	FREQ_NCO[31:24]								00100110	26	38
7	07h	PHINCO_LSB	R/W	PH_NCO[7:0]								00000000	00	0
8	08h	PHINCO_MSB	R/W	PH_NCO[15:8]								00000000	00	0
9	09h	DAC_A_Cfg_1	R/W	DAC_A_PD	DAC_A_SLEEP	DAC_A_OFFSET[2:0]			-	-	-	00000000	00	0
10	0Ah	DAC_A_Cfg_2	R/W	DAC_A_GAIN_COARSE[1:0]		DAC_A_GAIN_FINE[5:0]						01000000	40	64
11	0Bh	DAC_A_Cfg_3	R/W	DAC_A_GAIN_COARSE[3:2]		DAC_A_OFFSET[8:3]						11000000	C0	192
12	0Ch	DAC_B_Cfg_1	R/W	DAC_B_PD	DAC_B_SLEEP	DAC_B_OFFSET[2:0]			-	-	-	00000000	00	0
13	0Dh	DAC_B_Cfg_2	R/W	DAC_B_GAIN_COARSE[1:0]		DAC_B_GAIN_FINE[5:0]						01000000	40	64
14	0Eh	DAC_B_Cfg_3	R/W	DAC_B_GAIN_COARSE[3:2]		DAC_B_OFFSET[8:3]						11000000	C0	192
15	0Fh	DAC_Cfg	R/W	-	-	-	-	-	-	MINUS_3DB	NOISE_SHPER	00000000	00	0
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
26	1Ah	DAC_A_Aux_MSB	R/W	AUX_A[9:2]								10000000	80	128
27	1Bh	DAC_A_Aux_LSB	R/W	AUX_A_PD	-	-	-	-	-	AUX_A[1:0]		00000000	00	0
28	1Ch	DAC_B_Aux_MSB	R/W	AUX_B[9:2]								10000000	80	128
29	1Dh	DAC_B_Aux_LSB	R/W	AUX_B_PD	-	-	-	-	-	AUX_B[1:0]		00000000	00	0

10.2.4 Registers detailed description

Please refer to Table 9 for a register overview and their default values. In the following tables, all default results are shown highlighted.

Table 10. COMMon register (address 00h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	3W_SPI	R/W		serial interface bus type
			0	4 wire SPI
			1	**3 wire SPI**
6	SPI_RST	R/W		serial interface reset
			0	**no reset**
			1	performs a reset on all registers except 00h
5	CLK_SEL	R/W		data input latch
			0	**at CLK rising edge**
			1	at CLK falling edge
3	MODE_SEL	R/W		input data mode
			0	**dual-port**
			1	interleaved
2	CODING	R/W		coding
			0	**binary**
			1	two's compliment
1	IC_PD	R/W		power-down
			0	**disabled**
			1	all circuits (digital and analog, except SPI) are switched off
0	GAP_PD	R/W		internal bandgap power-down
			0	**power-down disabled**
			1	internal bandgap references are switched off

Table 11. TXCFG register (address 01h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	NCO_ON	R/W		NCO
			0	disabled (the NCO phase is reset to 0°)
			1	**enabled**
6	NCO_LP_SEL	R/W		low-power NCO
			0	**disabled**
			1	NCO frequency and phase given by the five MSBs of the registers 06h and 08h respectively

Table 11. TXCFG register (address 01h) bit description *...continued*

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 2	MODULATION[2:0]	R/W		modulation
			000	dual DAC: no modulation
			001	**positive upper single sideband up-conversion**
			010	positive lower single sideband up-conversion
			011	negative upper single sideband up-conversion
			100	negative lower single sideband up-conversion
1 to 0	INTERPOLATION[1:0]	R/W		interpolation
			01	$f_s = 2f_{clk}$
			10	$f_s = 4f_{clk}$
			11	$f_s = 8f_{clk}$

Table 12. PLLCFG register (address 02h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	PLL_PD	R/W		PLL
			0	**switched on**
			1	switched off
5	PLL_DIV_PD	R/W		PLL divider
			0	**switched on**
			1	switched off
4 to 3	PLL_DIV[1:0]	R/W		PLL divider factor
			00	$f_s = 2 \times f_{clk}$
			01	$f_s = 4 \times f_{clk}$
			10	**fs = 8 ¥ fclk**
2 to 1	PLL_PHASE[1:0]	R/W		PLL phase shift of f_s
			00	**0×**
			01	120°
			10	240°
0	PLL_POL	R/W		DAC clock edge
			0	**normal**
			1	inverted

Table 13. FREQNCO_LSB register (address 03h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[7:0]	R/W	-	lower 8 bits for the NCO frequency setting

Table 14. FREQNCO_LISB register (address 04h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[15:8]	R/W	-	lower intermediate 8 bits for the NCO frequency setting

Table 15. FREQNCO_UISB register (address 05h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[23:16]	R/W	-	upper intermediate 8 bits for the NCO frequency setting

Table 16. FREQNCO_MSB register (address 06h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[31:24]	R/W	-	most significant 8 bits for the NCO frequency setting

Table 17. PHINCO_LSB register (address 07h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PH_NCO[7:0]	R/W	-	lower 8 bits for the NCO phase setting

Table 18. PHINCO_MSB register (address 08h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PH_NCO[15:8]	R/W	-	most significant 8 bits for the NCO phase setting

Table 19. DAC_A_Cfg_1 register (address 09h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	DAC_A_PD	R/W		DAC A power
			0	**on**
			1	off
6	DAC_A_SLEEP	R/W		DAC A Sleep mode
			0	**disabled**
			1	enabled
5 to 3	DAC_A_OFFSET[2:0]	R/W	-	lower 3 bits for the DAC A offset

Table 20. DAC_A_Cfg_2 register (address 0Ah) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_A_GAIN_COARSE[1:0]	R/W	-	least significant 2 bits for the DAC A gain setting for coarse adjustment
5 to 0	DAC_A_GAIN_FINE[5:0]	R/W	-	the 6 bits for the DAC A fine adjustment gain setting

Table 21. DAC_A_Cfg_3 register (address 0Bh) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_A_GAIN_COARSE[3:2]	R/W	-	most significant 2 bits for the DAC A gain setting for coarse adjustment
5 to 0	DAC_A_OFFSET[8:3]	R/W	-	most significant 6 bits for the DAC A offset

Table 22. DAC_B_Cfg_1 register (address 0Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	DAC_B_PD	R/W		DAC B power
			0	**on**
			1	off
6	DAC_B_SLEEP	R/W		DAC B Sleep mode
			0	**disabled**
			1	enabled
5 to 3	DAC_B_OFFSET[2:0]	R/W		lower 3 bits for the DAC B offset

Table 23. DAC_B_Cfg_2 register (address 0Dh) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_B_GAIN_COARSE[1:0]	R/W	-	less significant 2 bits for the DAC B gain setting for coarse adjustment
5 to 0	DAC_B_GAIN_FINE[5:0]	R/W	-	the 6 bits for the DAC B gain setting for fine adjustment

Table 24. DAC_B_Cfg_3 register (address 0Eh) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_B_GAIN_COARSE[3:2]	R/W	-	most significant 2 bits for the DAC B gain setting for coarse adjustment
5 to 0	DAC_B_OFFSET[8:3]	R/W	-	most significant 6 bits for the DAC B offset

Table 25. DAC_Cfg register (address 0Fh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
1	MINUS_3DB	R/W		NCO gain
			0	**unity**
			1	−3 dB
0	NOISE_SHPER	R/W		noise shaper
			0	**disabled**
			1	enabled

Table 26. DAC_A_Aux_MSB register (address 1Ah) bit description

Bit	Symbol	Access	Value	Description
7 to 0	AUX_A[9:2]	R/W	-	most significant 8 bits for the auxiliary DAC A

Table 27. DAC_A_Aux_LSB register (address 1Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	AUX_A_PD	R/W		auxiliary DAC A power
			0	**on**
			1	off
1 to 0	AUX_A[1:0]	R/W		lower 2 bits for the auxiliary DAC A

Table 28. DAC_B_Aux_MSB register (address 1Ch) bit description

Bit	Symbol	Access	Value	Description
7 to 0	AUX_B[9:2]	R/W	-	most significant 8 bits for the auxiliary DAC B

Table 29. DAC_B_Aux_LSB register (address 1Dh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	AUX_B_PD	R/W		auxiliary DAC B power
			0	**on**
			1	off
1 to 0	AUX_B[1:0]	R/W		lower 2 bits for the auxiliary DAC B

10.3 Input data

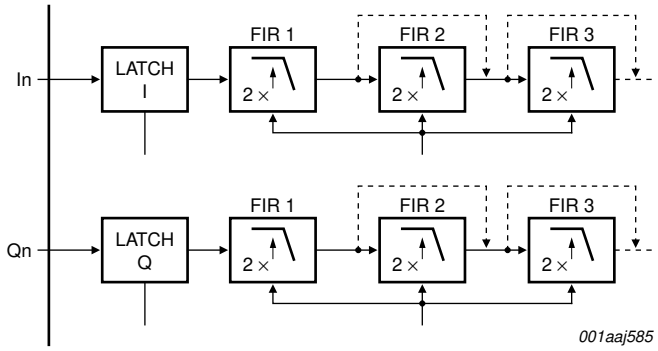
The setting applied to MODE_SEL (register 00h[3]; see Table 10 on page 17) defines whether the DAC1005D650 operates in the Dual-port mode or in the Interleaved mode (see Table 30).

Table 30. Mode selection

Bit 3 setting	Function	I9 to I0	Q9 to Q0
0	Dual-port mode (pin Q9)	active	active
1	Interleaved mode (pin SELIQ)	active	off

10.3.1 Dual-port mode

The data input for Dual-port mode operation is shown in Figure 5 “Dual-port mode”. Each DAC has its own independent data input. The data enters the input latch on the rising edge of the internal clock signal and is transferred to the DAC latch.

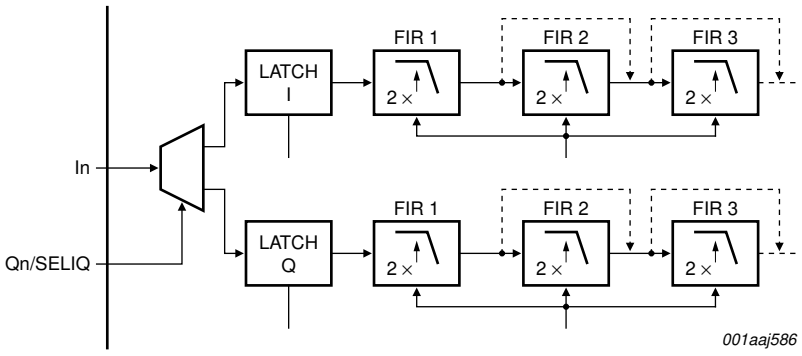


n in Qn = 0 to 9 and for In is 0 to 9.

Fig 5. Dual-port mode

10.3.2 Interleaved mode

The data input for Interleaved mode operation is shown in Figure 6 “Interleaved mode operation”.



n in Qn = 9 and for In is 0 to 9.

Fig 6. Interleaved mode operation

In the Interleaved mode, both DACs use the same data input at twice the Dual-port mode frequency. Data enters the latch on the rising edge of the internal clock signal. The data is sent to either latch I or latch Q, see Figure 6 “Interleaved mode operation” and Figure 7 “Interleaved mode timing (8x interpolation, latch on rising edge)”.

The SELIQ input (pin 41) allows the synchronization of the internally de-multiplexed I and Q channels.

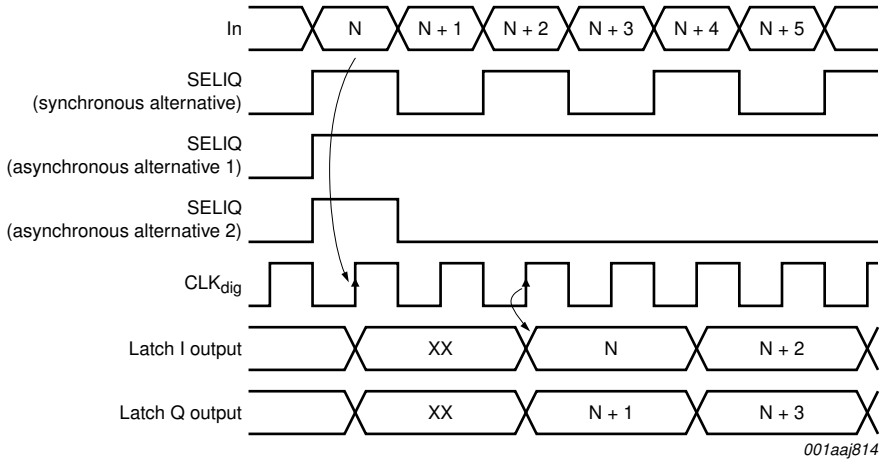


Fig 7. Interleaved mode timing (8x interpolation, latch on rising edge)

SELIQ can be either a synchronous or asynchronous (single rising edge, single pulse) signal. The first data bits following the SELIQ rising edge are sent in channel I and the following data bits are sent in channel Q. After this, the data is distributed alternately between both channels.

10.4 Input clock

The DAC1005D650 can operate with a clock frequency of 160 MHz in the Dual-port mode and up to 320 MHz in the Interleaved mode. The input clock is LVDS (see Figure 8) but it can also be interfaced with CML (see Figure 9).

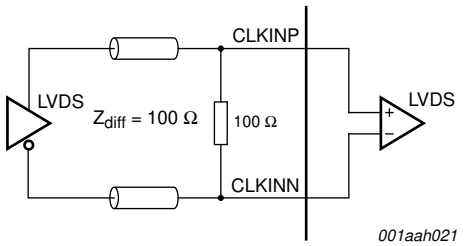


Fig 8. LVDS clock configuration

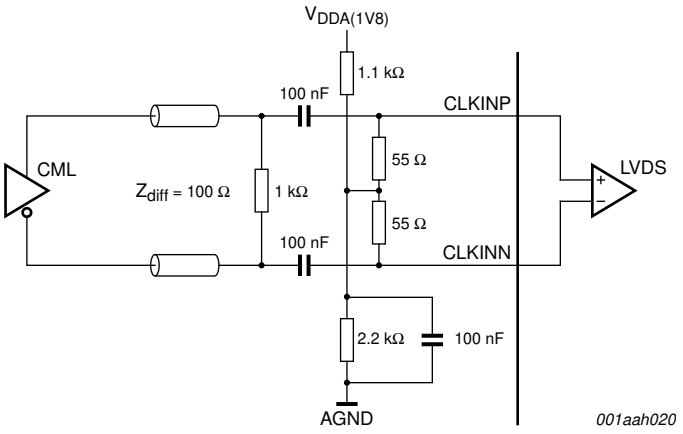
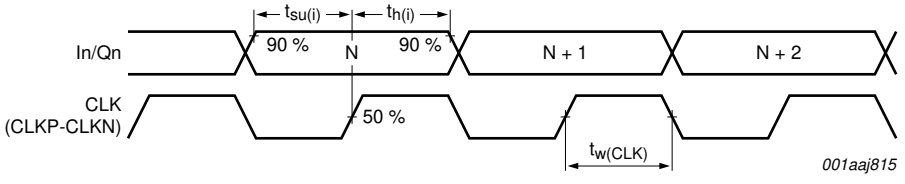


Fig 9. Interfacing CML to LVDS

10.5 Timing

The DAC1005D650 can operate at an update rate (f_s) of up to 650 Msps and with an input data rate (f_{data}) of up to 160 MHz. The input timing is shown in Figure 10 “Input timing diagram”.



n in Qn = 0 to 9 and for In is 0 to 9.

Fig 10. Input timing diagram

The typical performances are measured at 50 % duty cycle but any timing within the limits of the characteristics will not alter the performance.

In Table 31 “Frequencies”, the links between internal and external clocking are defined. The setting applied to PLL_DIV[1:0] (register 02h[4:3]; see Table 12 “PLLCFG register (address 02h) bit description”) allows the frequency between the digital part and the DAC core to be adjusted.

Table 31. Frequencies

Mode	CLK input (MHz)	Input data rate (MHz)	Interpolation	Update rate (Msps)	PLL_DIV[1:0]
Dual-port	160	160	2×	320	01 (/4)
Dual-port	160	160	4×	640	01 (/4)
Dual-port	80	80	8×	640	10 (/8)
Interleaved	320	320	2×	320	00 (/2)
Interleaved	320	320	4×	640	00 (/2)
Interleaved	160	160	8×	640	01 (/4)

The settings applied to PLL_PHASE[1:0] (register 02h[2:1]) and PLL_POL (register 02h[0]), allows adjustment of the phase and polarity of the sampling clock. This occurs at the input of the DAC core and depends mainly on the sampling frequency. Some examples are given in Table 32 “Sample clock phase and polarity examples”.

Table 32. Sample clock phase and polarity examples

Mode	Input data rate (MHz)	Interpolation	Update rate (Msps)	PLL_PHASE [1:0]	PLL_POL
Dual-port	80	2×	160	01	1
Dual-port	80	4×	320	01	0
Dual-port	80	8×	640	01	1
Interleaved	160	2×	160	01	1
Interleaved	160	4×	320	01	0
Interleaved	160	8×	640	01	1

10.6 FIR filters

The DAC1005D650 integrates three selectable Finite Impulse Response (FIR) filters which enable the device to use interpolation rates of 2×, 4× or 8×.

All three interpolation filters have a stop-band attenuation of at least 80 dBc and a pass-band ripple of less than 0.0005 dB.

The coefficients of the interpolation filters are given in Table 33 “Interpolation filter coefficients”.

Table 33. Interpolation filter coefficients

First interpolation filter[1]			Second interpolation filter[1]			Third interpolation filter[1]		
Lower	Upper	Value	Lower	Upper	Value	Lower	Upper	Value
H(1)	H(55)	−4	H(1)	H(23)	−2	H(1)	H(15)	−39
H(2)	H(54)	0	H(2)	H(22)	0	H(2)	H(14)	0
H(3)	H(53)	13	H(3)	H(21)	17	H(3)	H(13)	273
H(4)	H(52)	0	H(4)	H(20)	0	H(4)	H(12)	0
H(5)	H(51)	−34	H(5)	H(19)	−75	H(5)	H(11)	−1102
H(6)	H(50)	0	H(6)	H(18)	0	H(6)	H(10)	0
H(7)	H(49)	72	H(7)	H(17)	238	H(7)	H(9)	4964
H(8)	H(48)	0	H(8)	H(16)	0	H(8)	-	8192
H(9)	H(47)	−138	H(9)	H(15)	−660	-	-	-
H(10)	H(46)	0	H(10)	H(14)	0	-	-	-
H(11)	H(45)	245	H(11)	H(13)	2530	-	-	-
H(12)	H(44)	0	H(12)	-	4096	-	-	-
H(13)	H(43)	−408	-	-	-	-	-	-
H(14)	H(42)	0	-	-	-	-	-	-
H(15)	H(41)	650	-	-	-	-	-	-
H(16)	H(40)	0	-	-	-	-	-	-
H(17)	H(39)	−1003	-	-	-	-	-	-
H(18)	H(38)	0	-	-	-	-	-	-
H(19)	H(37)	1521	-	-	-	-	-	-
H(20)	H(36)	0	-	-	-	-	-	-
H(21)	H(35)	−2315	-	-	-	-	-	-
H(22)	H(34)	0	-	-	-	-	-	-
H(23)	H(33)	3671	-	-	-	-	-	-
H(24)	H(32)	0	-	-	-	-	-	-
H(25)	H(31)	−6642	-	-	-	-	-	-
H(26)	H(30)	0	-	-	-	-	-	-
H(27)	H(29)	20756	-	-	-	-	-	-
H(28)		32768	-	-	-	-	-	-

[1] H(n) is the digital filter coefficient.