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DAC1408D650

Dual 14-bit DAC; up to 650 Msps; 2×, 4× or 8× interpolating with JESD204A interface

Rev. 06 — 2 July 2012 Product data sheet

1. General description

The DAC1408D650 is a high-speed 14-bit dual channel Digital-to-Analog Converter (DAC) with selectable 2×, 4× or 8× interpolating filters optimized for multi-carrier WCDMA transmitters.

Because of its digital on-chip modulation, the DAC1408D650 allows the complex pattern provided through lane 0, lane 1, lane 2 and lane 3, to be converted from baseband to IF. The mixing frequency is adjusted via a Serial Peripheral Interface (SPI) with a 32-bit Numerically Controlled Oscillator (NCO) and the phase is controlled by a 16-bit register.

The DAC1408D650 also includes a 2×, 4× or 8× clock multiplier which provides the appropriate internal clocks and an internal regulation to adjust the output full-scale current.

The input data format is serial according to JESD204A specification. This new interface has numerous advantages over the traditional parallel one: easy PCB layout, lower radiated noise, lower pin count, self-synchronous link, skew compensation. The maximum number of lanes of the DAC1408D650 is 4 and its maximum serial data rate is 3.125 Gbps.

The Multiple Device Synchronization (MDS) guarantees a maximum skew of one output clock period between several DAC devices. MDS incorporates modes: Master/slave and All slave mode.

2. Features and benefits

- Dual 14-bit resolution
- 650 Msps maximum update rate
- Selectable 2×, 4× or 8× interpolation filters
- Input data rate up to 312.5 Msps
- Very low-noise cap-free integrated PLL
- 32-bit programmable NCO frequency
- Four JESD204A serial input lanes
- 1.8 V and 3.3 V power supplies
- LVDS compatible clock inputs
- IMD3: 80 dBc; f_s = 640 Msps; f_o = 140 MHz
- ACPR: 71 dBc; two carriers WCDMA; f_s = 640 Msps; f_o = 133 MHz
- Typical 1.26 W power dissipation at 4× interpolation, PLL off and 640 Msps
- Power-down mode and Sleep modes
- Differential scalable output current from 1.6 mA to 22 mA
- On-chip 1.29 V reference
- External analog offset control (10-bit auxiliary DACs)
- Internal digital offset control
- Inverse (sin x) / x function

- Two's complement or binary offset data format
- LMF = 421 or LMF = 211 support
- Differential CML receiver with embedded termination
- Synchronization of multiple DAC outputs
- Fully compatible SPI port
- Industrial temperature range from −40 °C to +85 °C
- Integrated PLL can be bypassed
- Embedded complex modulator

3. Applications

- Wireless infrastructure: LTE, WiMAX, GSM, CDMA, WCDMA, TD-SCDMA
- Communication: LMDS/MMDS, point-to-point
- Direct Digital Synthesis (DDS)
- Broadband wireless systems
- Digital radio links
- Instrumentation
- Automated Test Equipment (ATE)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
DAC1408D650HN	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-3

5. Block diagram

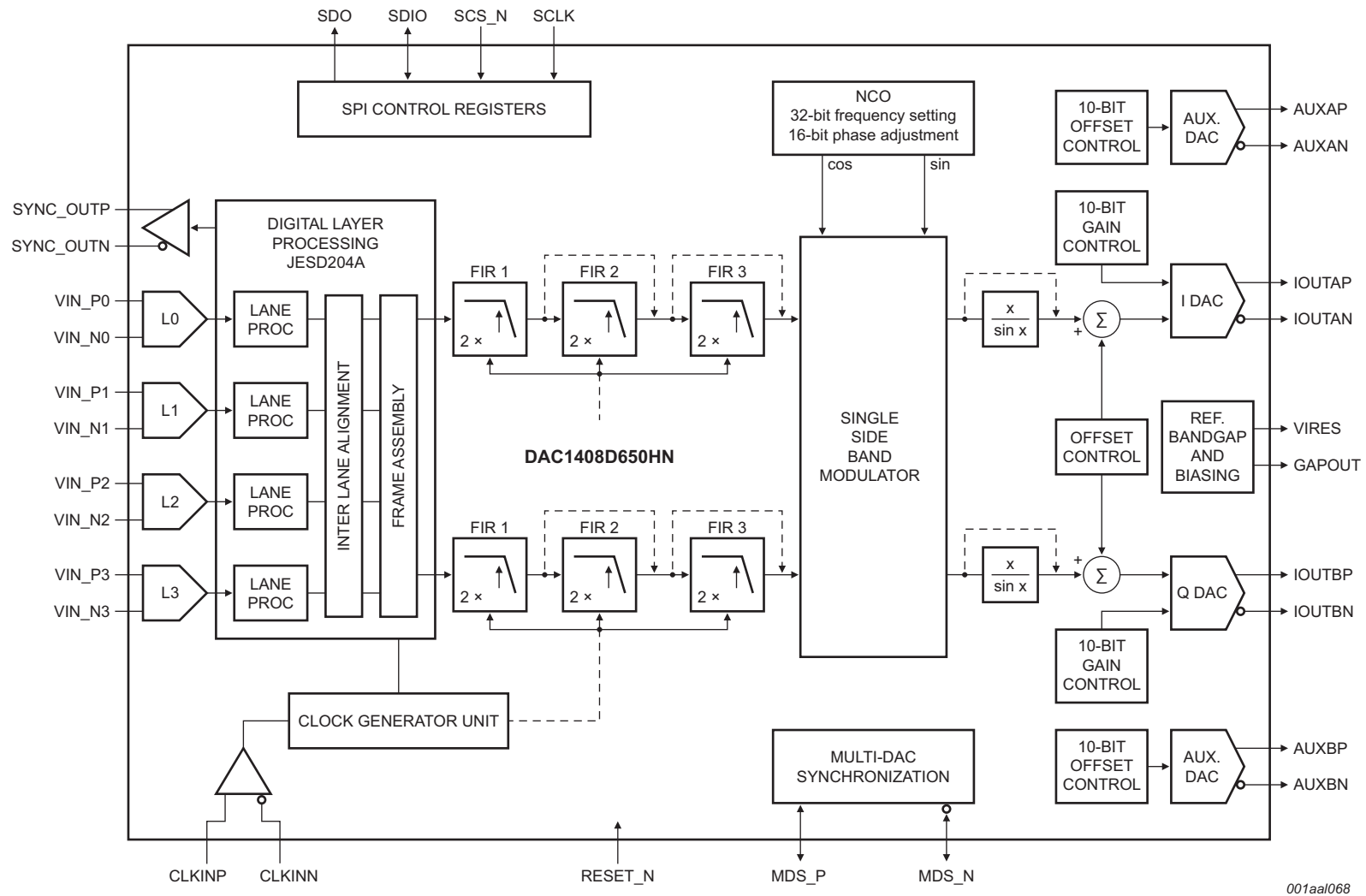


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

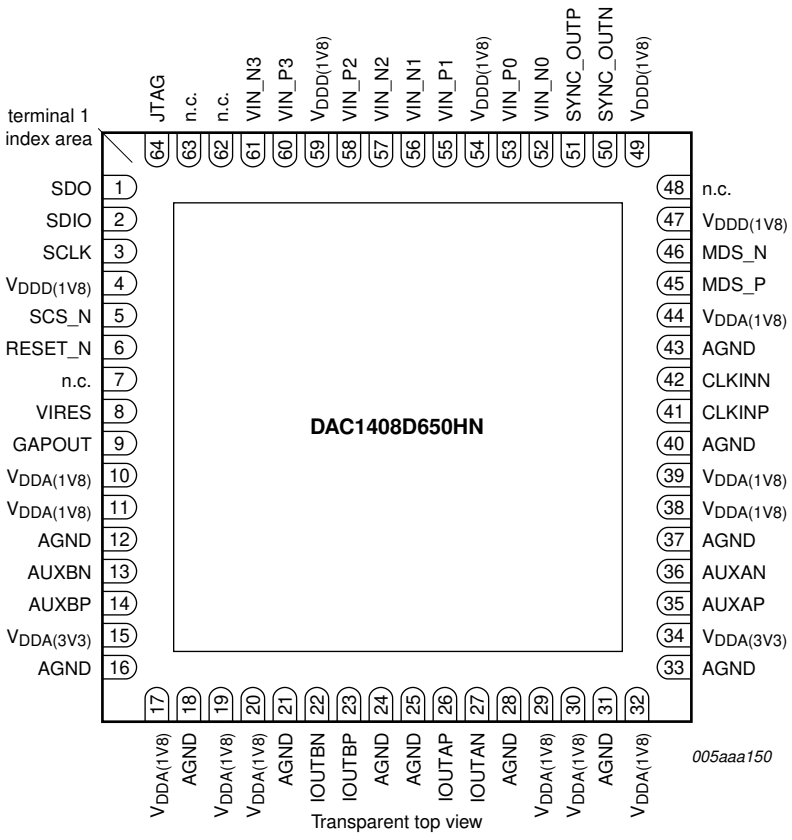


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
SDO	1	O	SPI data output
SDIO	2	I/O	SPI data input/output
SCLK	3	I	SPI clock
$V_{DDD(1V8)}$	4	P	digital supply voltage 1.8 V
SCS_N	5	I	SPI chip select (active LOW)
RESET_N	6	I	general reset (active LOW)
n.c.	7	-	not connected
VIRES	8	I/O	DAC biasing resistor
GAPOUT	9	I/O	band gap input/output voltage
$V_{DDA(1V8)}$	10	P	analog supply voltage 1.8 V
$V_{DDA(1V8)}$	11	P	analog supply voltage 1.8 V

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
AGND	12	G	analog ground
AUXBN	13	O	complementary auxiliary DAC B output
AUXBP	14	O	auxiliary DAC B output
$V_{DDA(3V3)}$	15	P	analog supply voltage 3.3 V
AGND	16	G	analog ground
$V_{DDA(1V8)}$	17	P	analog supply voltage 1.8 V
AGND	18	G	analog ground
$V_{DDA(1V8)}$	19	P	analog supply voltage 1.8 V
$V_{DDA(1V8)}$	20	P	analog supply voltage 1.8 V
AGND	21	G	analog ground
IOUTBN	22	O	complementary DAC B output current
IOUTBP	23	O	DAC B output current
AGND	24	G	analog ground
AGND	25	G	analog ground
IOUTAP	26	O	DAC A output current
IOUTAN	27	O	complementary DAC A output current
AGND	28	G	analog ground
$V_{DDA(1V8)}$	29	P	analog supply voltage 1.8 V
$V_{DDA(1V8)}$	30	P	analog supply voltage 1.8 V
AGND	31	G	analog ground
$V_{DDA(1V8)}$	32	P	analog supply voltage 1.8 V
AGND	33	G	analog ground
$V_{DDA(3V3)}$	34	P	analog supply voltage 3.3 V
AUXAP	35	O	auxiliary DAC A output current
AUXAN	36	O	complementary auxiliary DAC A output current
AGND	37	G	analog ground
$V_{DDA(1V8)}$	38	P	analog supply voltage 1.8 V
$V_{DDA(1V8)}$	39	P	analog supply voltage 1.8 V
AGND	40	G	analog ground
CLKINP	41	I	clock input
CLKINN	42	I	complementary clock input
AGND	43	G	analog ground
$V_{DDA(1V8)}$	44	P	analog supply voltage 1.8 V
MDS_P	45	I/O	multi-device synchronization
MDS_N	46	I/O	complementary multi-device synchronization
$V_{DDD(1V8)}$	47	P	digital supply voltage 1.8 V
n.c.	48	-	not connected
$V_{DDD(1V8)}$	49	P	digital supply voltage 1.8 V
SYNC_OUTN	50	O	synchronization request to transmitter, complementary output
SYNC_OUTP	51	O	synchronization request to transmitter

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
VIN_N0	52	I	serial interface lane 0 negative input
VIN_P0	53	I	serial interface lane 0 positive input
$V_{DDD(1V8)}$	54	P	digital supply voltage 1.8 V
VIN_P1	55	I	serial interface lane 1 positive input
VIN_N1	56	I	serial interface lane 1 negative input
VIN_N2	57	I	serial interface lane 2 negative input
VIN_P2	58	I	serial interface lane 2 positive input
$V_{DDD(1V8)}$	59	P	digital supply voltage 1.8 V
VIN_P3	60	I	serial interface lane 3 positive input
VIN_N3	61	I	serial interface lane 3 negative input
n.c.	62	-	not connected
n.c.	63	-	not connected
JTAG	64	I	JTAG test mode select (must be grounded)
GND	H[2]	G	ground

[1] P: power supply; G: ground; I: input; O: output.

[2] H = heatsink (exposed die pad to be soldered to GND. A minimum of 81 thermal vias are required).

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		−0.5	+4.6	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		−0.5	+2.5	V
V_{DDD}	digital supply voltage		−0.5	+2.5	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
T_j	junction temperature		−40	+125	°C

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	18.7	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	6.7	K/W

[1] Complies with JEDEC test board, in free air.

9. Characteristics

Table 5. Characteristics

$V_{DDA(1V8)}$ = V_{DDD} = 1.7 V to 1.9 V; $V_{DDA(3V3)}$ = 3.13 V to 3.47 V; AGND and GND are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; PLL off unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		I	3.13	3.3	3.47	V
$V_{DDD(1V8)}$	digital supply voltage (1.8 V)		I	1.7	1.8	1.9	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		I	1.7	1.8	1.9	V
$I_{DDA(3V3)}$	analog supply current (3.3 V)	f_o = 19 MHz; f_s = 640 Msps; 4× interpolation; NCO on	I	-	42	-	mA
$I_{DDD(1V8)}$	digital supply current, (1.8 V)	f_o = 19 MHz; f_s = 640 Msps; 4× interpolation; NCO on	I	-	354	-	mA
$I_{DDA(1V8)}$	analog supply current, (1.8 V)	f_o = 19 MHz; f_s = 640 Msps; 4× interpolation; NCO on	I	-	412	-	mA
ΔI_{DDD}	digital supply current difference	x/sin x function on; f_s = 640 Msps	I	-	52	-	mA
P_{tot}	total power dissipation	f_s = 640 Msps; 4× interpolation; NCO off; DAC Q off	C	-	0.82	-	W
		f_s = 640 Msps; 4× interpolation; NCO off	C	-	1.26	-	W
		f_s = 640 Msps; 4× interpolation; NCO on	C	-	1.51	-	W
		f_s = 625 Msps; 2× interpolation; NCO off	C	-	1.33	-	W
		f_s = 625 Msps; 2× interpolation; NCO on	C	-	1.51	-	W
		Power-down mode; f_o = 19 MHz; f_s = 640 Msps; 4× interpolation; NCO on					
		complete device; Power-down mode	I	-	0.04	-	W
		DAC A and DAC B; Power-down mode	I	-	0.62	-	W
		DAC A and DAC B; Sleep mode	I	-	0.83	-	W
Timing specifications							
$t_{d(startup)}$	start-up delay time	from full Power-down mode		-	20	-	ms
$t_{d(restart)}$	restart delay time	from Sleep mode		-	300	-	ns
t_{lock}	lock time	maximum input rate	[2]	-	11	-	µs
Clock inputs (CLKINN, CLKINP)[3]							
V_i	input voltage	range: CLK+ or CLK− $\lvert V_{gpd}\rvert$ < 50 mV[4]	C	825	-	1575	mV

Table 5. Characteristics *…continued*

$V_{DDA(1V8)}$ = V_{DDD} = 1.7 V to 1.9 V; $V_{DDA(3V3)}$ = 3.13 V to 3.47 V; AGND and GND are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; PLL off unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
V_{idth}	input differential threshold voltage	$\|V_{gpd}\|$ < 50 mV[4]	C	−100	-	+100	mV
R_i	input resistance		D	-	10	-	MΩ
C_I	input capacitance		D	-	0.5	-	pF
Digital inputs (SDIO, SCLK, SCS_N, RESET_N)							
V_{IL}	LOW-level input voltage		C	GND	-	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		C	$0.7V_{DDD}$	-	V_{DDD}	V
I_{IL}	LOW-level input current	V_{IL} = $0.3V_{DDD}$ V	I	-	1	-	µA
I_{IH}	HIGH-level input current	V_{IH} = $0.7V_{DDD}$ V	I	-	1	-	µA
Digital outputs (SDO, SDIO)							
V_{OL}	LOW-level output voltage	I_{load} = 2 mA	C	GND	-	0.13	V
V_{OH}	HIGH-level output voltage	I_{load} = 2 mA	C	1.65	-	V_{DDD}	V
Digital inputs (Vin_p/Vin_n)[5]							
$V_{I(cm)}$	common-mode input voltage		D	-	0.78	-	V
$V_{I(dif)(p-p)}$	peak-to-peak differential input voltage		D	175	-	1000	mV
Z_{tt}	V_{tt} source impedance		D	-	0.7	-	Ω
ΔZ_i	differential input impedance		D	-	100	-	Ω
Digital outputs (SYNC_OUTN/SYNC_OUTP)[6]							
$V_{o(cm)}$	common-mode output voltage		C	-	1.18	-	V
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage		C	-	0.45	-	V
Digital inputs/outputs (MDS_N/MDS_P)							
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage		D	-	600	-	mV
$C_{o(L)}$	output load capacitance	between pins GND and MDS_N or MDS_P	D	-	-	10	pF
C_I	input capacitance	between pins GND and MDS_N or MDS_P	D	-	0.3	-	pF

Table 5. Characteristics *...continued*

$V_{DDA(1V8)}$ = V_{DDD} = 1.7 V to 1.9 V; $V_{DDA(3V3)}$ = 3.13 V to 3.47 V; AGND and GND are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; PLL off unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Analog outputs (IOUTAP, IOUTAN, IOUTBP, IOUTBN)							
$I_{O(fs)}$	full-scale output current	register value = 00h (see Table 13 and Table 14)	D	-	1.6	-	mA
		register = default value (see Table 13 and Table 14)		-	20	-	mA
V_O	output voltage	compliance range	D	1.8	-	$V_{DDA(3V3)}$	V
R_o	output resistance		D	-	250	-	kΩ
C_o	output capacitance		D	-	3	-	pF
ΔE_O	offset error variation		C	-	6	-	ppm/°C
ΔE_G	gain error variation		C	-	18	-	ppm/°C
Reference voltage output (GAPOUT)							
$V_{O(ref)}$	reference output voltage		C	1.24	1.29	1.34	V
$I_{O(ref)}$	reference output current	external voltage 1.2 V	C	-	40	-	μA
$\Delta V_{O(ref)}$	reference output voltage variation		C	-	117	-	ppm/°C
Analog auxiliary outputs (AUXAP, AUXAN, AUXBP and AUXBN)							
$I_{O(aux)}$	auxiliary output current	differential outputs	I	-	2.2	-	mA
$V_{O(aux)}$	auxiliary output voltage	compliance range	D	0	-	2	V
$N_{DAC(aux)mono}$	auxiliary DAC monotonicity	guaranteed	D	-	10	-	bits
Input timing (Vin_p/Vin_n)							
f_{data}	data rate	2× interpolation	D	-	-	312.5	Msps
		4× interpolation	D	-	-	162.5	Msps
		8× interpolation	D	-	-	81.25	Msps
f_{bit}	bit rate	serial input	D	0.7	-	3.125	Gbps
Output timing (IOUTAP, IOUTAN, IOUTBP, IOUTBN)							
f_s	sampling rate		D	-	-	650	Msps
t_s	settling time	up to 0.5 LSB	D	-	20	-	ns
NCO frequency range; f_s = 650 Msps							
f_{NCO}	NCO frequency	register value = 00000000h (see Table 21 to Table 24)	D	-	0	-	MHz
		register value = FFFFFFFFh (see Table 21 to Table 24)	D	-	650	-	MHz
f_{step}	step frequency		D	-	0.151	-	Hz
Low power NCO frequency range; f_s = 650 Msps							
f_{NCO}	NCO frequency	reg value = 00000000h (see Table 21 to Table 24)	D	-	0	-	MHz
		reg value = F8000000h (see Table 21 to Table 24)	D	-	630	-	MHz

Table 5. Characteristics *…continued*

$V_{DDA(1V8)}$ = V_{DDD} = 1.7 V to 1.9 V; $V_{DDA(3V3)}$ = 3.13 V to 3.47 V; AGND and GND are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; PLL off unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
f_{step}	step frequency		D	-	20.3	-	MHz
Dynamic performances							
SFDR	spurious-free dynamic range	f_{data} = 80 Msps; f_s = 640 Msps; 8×; BW = f_{data} / 2; PLL on					
		f_o = 4 MHz at −1 dBFS	C	-	77	-	dBc
		f_{data} = 160 Msps; f_s = 640 Msps; 4×; BW = f_{data} / 2					
		f_o = 19 MHz at −1 dBFS	C	-	74	-	dBc
		f_{data} = 312.5 Msps; f_s = 625 Msps; 2×; BW = f_{data} / 2					
		f_o = 19 MHz at −1 dBFS	I	-	75	-	dBc
$SFDR_{RBW}$	restricted bandwidth spurious-free dynamic range	f_s = 640 Msps; 4× interpolation; f_o = 133 MHz at −1 dBFS; BW = 100 MHz	I	-	81	-	dBc
		f_s = 640 Msps; 4× interpolation; f_o = 133 MHz at −1 dBFS; BW = 20 MHz	C	-	84	-	dBc
IMD3	third-order intermodulation distortion	f_{o1} = 95 MHz; f_{o2} = 97 MHz; f_s = 640 Msps; 4× interpolation	C	[7] -	81		dBc
		f_{o1} = 153.1 MHz; f_{o2} = 154.1 MHz; f_s = 640 Msps; 4× interpolation	I	[7] -	77	-	dBc
		f_{o1} = 137 MHz; f_{o2} = 143 MHz; f_s = 640 Msps; 4× interpolation	C	[7] -	80	-	dBc
ACPR	adjacent channel power ratio	NCO on; 4× interpolation; f_s = 640 Msps; f_o = 96 MHz					
		1 carrier; BW = 5 MHz	C	-	75	-	dBc
		2 carriers; BW = 10 MHz	C	-	72	-	dBc
		4 carriers; BW = 20 MHz	C	-	69	-	dBc
		NCO on; 4× interpolation; f_s = 640 Msps; f_o = 133MHz					
		1 carrier; BW = 5 MHz	C	-	75	-	dBc
		2 carriers; BW = 10 MHz	C	-	71	-	dBc
		4 carriers; BW = 20 MHz	C	-	68	-	dBc

Table 5. Characteristics *…continued*

$V_{DDA(1V8)}$ = V_{DDD} = 1.7 V to 1.9 V; $V_{DDA(3V3)}$ = 3.13 V to 3.47 V; AGND and GND are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; PLL off unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
NSD	noise spectral density	f_s = 640 Msps; 4× interpolation; f_o = 133 MHz at 0 dBFS	I	-	−156	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] Delay between the deassertion of bits FORCE_RESET_FCLK and FORCE_RESET_DCLK and the deassertion of the sync signal. It reflects the delay required by DAC1408D650 to lock to a JESD204A stream. It supposes that the TX is already transmitting K28.5 characters in error-free conditions.

[3] CLKINP/CLKINN inputs are at differential LVDS levels. An external termination resistor with a value of between 80 Ω and 120 Ω (see Figure 15) should be connected across the pins.

[4] $|V_{gpd}|$ represents the ground potential difference voltage. This is the voltage that results from current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltage.

[5] Vin_p and Vin_n inputs are differential CML inputs. They are terminated internally to V_{tt} via 50 Ω (see Figure 4).

[6] SYNC_OUTP/SYNC_OUTN outputs are differential LVDS outputs. They must be terminated by a resistor with a value of between 80 Ω and 120 Ω.

[7] IMD3 rejection with −6 dBFS/tone.

10. Application information

10.1 General description

The DAC1408D650 is a dual 14-bit DAC operating up to 650 Msps. With a maximum input data rate of up to 312.5 Msps and a maximum output sampling rate of 650 Msps, the DAC1408D650 allows more flexibility for wide bandwidth and multi-carrier systems. Combined with its quadrature modulator and 32-bit NCO, the DAC1408D650 simplifies the frequency selection of the system. This is also possible because of the 2×, 4× or 8× interpolation filters which remove undesired images.

DAC1408D650 supports the following JESD204A key features:

- 10-bit/8-bit decoding
- Code group synchronization
- inter-lane alignment
- $1 + x^{14} + x^{15}$ scrambling polynomial
- Character replacement
- TX/RX synchronization management via sync signals
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device

DAC1408D650 can be interfaced with any logic device that features high speed SERDES functionality. This macro is now widely available in FPGA from different vendors. Standalone SERDES ICs can also be used.

To enhance the intrinsic board layout simplification of the JESD204A standard, IDT includes polarity swapping for each of the lanes and additionally offers lane swapping. Each physical lane can be configured logically as lane0, lane1, lane2 or lane3.

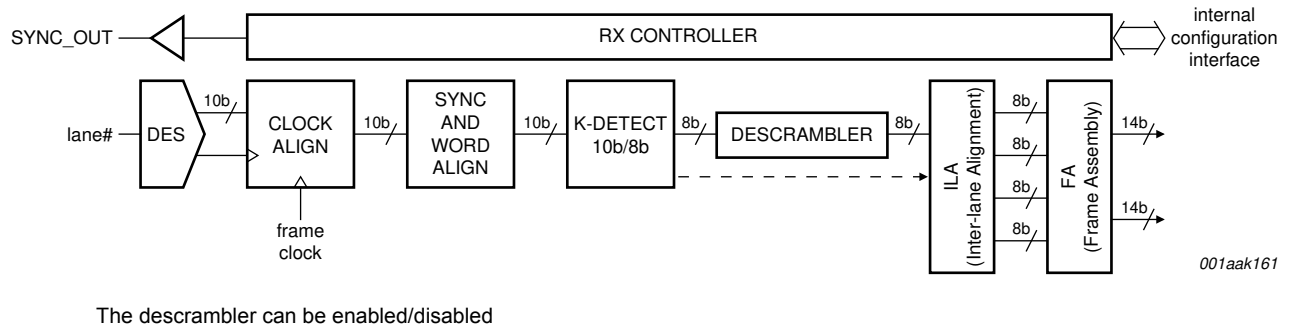
This device is MCDA-ML compliant, offering inter-lane alignment between several devices. Samples alignment between devices is maintained up to output level because of an IDT proprietary mechanism. One device is configured as the master and all the others are configured as slaves. These align their output samples automatically to the master ones. Therefore, a system with several DAC1408D650s can produce data with a guaranteed alignment of less than 1 DAC output clock period.

Each DAC generates two complementary current outputs on pins IOUTAP/IOUTAN and IOUTBP/IOUTBN. This provides a full-scale output current of up to 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

The DAC1408D650 must be configured before operating. Therefore, it features an SPI slave interface to access internal registers. Some of these registers also provide information about the JESD204A interface status.

The DAC1408D650 requires supplies of both 3.3 V and 1.8 V. The 1.8 V supply has separate digital and analog power supply pins. The clock input is LVDS compliant.

10.2 JESD204A receiver



The descrambler can be enabled/disabled

Fig 3. JESD204A receiver

The JEDEC204A defines the following parameters:

L is the number of lanes per link

M is the number of converters per device

F is the number of bytes per frame clock period

The DAC1408D650 supports both LMF = 421 and LMF = 211. The current setting is configurable via the SPI registers interface.

The complete Digital Layer Processing (DLP) adds a variable delay on each lane path. This is mainly because of the inter-lane alignment.

Table 6. Digital Layer Processing Latency

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
t_d	delay time	digital layer processing delay	D	13	-	28	cycle[2]

[1] D = guaranteed by design.

[2] Frame clock cycle.

10.2.1 Lane input

Each lane is CML compliant. It is terminated to a common voltage with an integrated 50 Ω resistor.

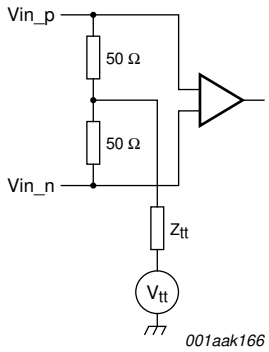


Fig 4. Lane input termination

The common-mode voltage is programmable by the SET_VCM_VOLTAGE register as shown in Table 75 on page 55.

DC coupling is only possible if both the DAC and the transmitter have the same common-mode voltage. If this is not the case, AC coupling is required.

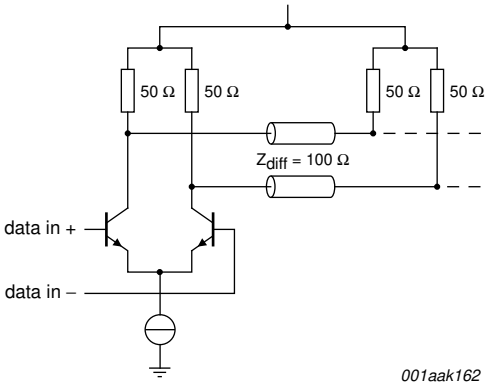


Fig 5. DC coupling

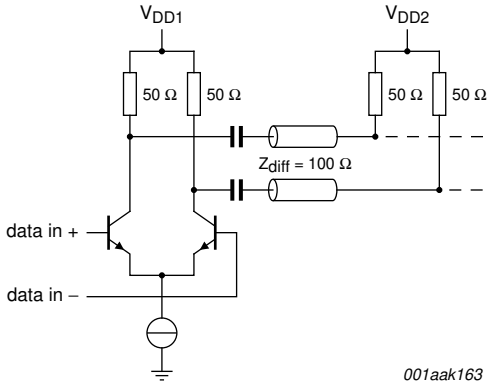


Fig 6. AC coupling

The deserializer performs the incoming data clock recovery and also the serial to parallel conversion. Therefore, each lane includes its own PLL that must first lock.

The clock alignment module transfers the data from the regenerated clock to the frame clock domain. The frequency of both clocks is the same but the phase relationship between the clocks is unknown.

10.2.2 Sync and word align

As stated in JESD204A, the transmitter and the receiver first have to synchronize. This is achieved through the SYNC_OUT signals and a sync pattern (K28.5 symbol). The receiver (i.e. DAC1408D650) first drives its SYNC_OUT outputs. The sync pattern is continuously sent until the receiver de-asserts the SYNC_OUT signal.

The lane processing makes use of the sync patterns to synchronize the data stream, determine the initial running disparity and extract the 10-bit word from the incoming data stream (word-alignment).

The SYNC_OUT signal is also used during normal operation by the DAC1408D650 to request a link reinitialization. This occurs when the 10b/8b module loses synchronization.

The SYNC_OUT signal conforms to LVDS signaling. Its common-mode voltage and its differential peak-to-peak amplitude can be programmed using SET_SYNC_LEVEL bits in the SET_SYNC registers (see Table 77 on page 55).

SYNC_OUT is asynchronous with the frame clock. There is no timing specification with respect to the CLKINP and CLKINN inputs.

10.2.3 Comma detection and word align

This stage monitors the data stream for code characters (comma detection), decodes the words to bytes (octets) and performs optional character replacement as part of frame/lane alignment monitoring and correction. This module provides the required control signals to the RX controller and ILA.

This module decodes the 10-bit words into 8-bit words (octets). The decoding table is specified in the IEEE 802.3-2005 specification. During decoding, the disparity is calculated according to the disparity rules mentioned in the same specification IEEE 802.3-2005. When the disparity counter is more than +2 or less than −2, an error is generated.

The following comma symbols are detected during data transmission irrespective of the running disparity:

/K/ = K28.5

/F/ = K28.7

/A/ = K28.3

/R/ = K28.0

/Q/ = K28.4

A flag is sent to the control interface to reflect detected commas in registers.

The following flags are also triggered according to the following definitions:

- VALID: a code group that is found in the column of the 10b/8b decoding tables according to the current running disparity.
- DISPARITY ERROR: The received code group exists in the 10b/8b decoding table, but is not found in the proper column according to the current running disparity.
- NOT-IN-TABLE (NIT) ERROR: The received code group is not found in the 10b/8b decoding table for either disparity.
- INVALID: a code group that either shows a disparity error or that does not exist in the 10b/8b decoding table.

DAC1408D650 supports character replacement whatever the state of the descrambler. When scrambling is not active, the received K28.3 /A/ or K28.7 /F/ is replaced by the previous sample. When scrambling is active, the corresponding data octet D28.3 (0xC) or D28.7 (0xFC) is used.

10.2.4 Descrambler

The descrambler is a 16-bit parallel self-synchronous descrambler based on the polynomial $1 + x^{14} + x^{15}$. This processing can be turned off.

10.2.5 inter-lane alignment

This feature removes strict PCB design skew compensation between the lanes.

10.2.5.1 Single device operation

This module handles the alignment of the four data streams. Because of inter-lane skew and each PLL per lane concept, these alignment characters may be received at different times by the receivers. After the synchronization period, the lock signal is high. This enables the receipt of K28.3 /A/ characters.

The /A/ characters provided in the initial alignment sequence are used to align the four data streams. The ILA_CNTRL register's SEL_ILA[1:0] bits select which K28.3 /A/ symbol triggers the initial lane alignment:"00" = 1st /A/ symbol, "01" = 2nd /A/ symbol, "10" = 3rd /A/ symbol, "11" = 4th /A/ symbol; Table 86 on page 61. When all receivers have received their first selected /A/, they start propagating the received data to the frame assembly module at the same point in time.

This module can compensate for up to ±7 frame clock period misalignments between the lanes.

When initial lane alignment is not supported, the manual alignment mode can be used.

After the initial ILA sequence, the lane alignment monitoring starts. If the received user data contains a K28.3 /A/ symbol:

- its position is compared to the value of the alignment monitor counter
- if two successive K28.3 /A/ symbols have been received at a wrong position, a realignment takes place
- if the buffers are empty or overflow, this is indicated by the registers ILA_BUF_ERR_LN0 to ILA_BUF_ERR_LN3

10.2.5.2 Multi-device operation

DAC1408D650 implements a multi-device inter-lane alignment that guarantees a skew of less than one output period between them.

Two modes are available: master/slave and all slave. Both make use of the MDS_P and MDS_N pins.

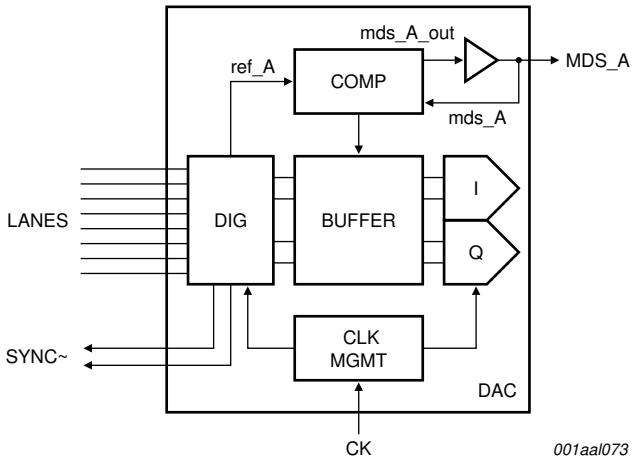


Fig 7. Multi-Device Synchronization (MDS) implementation

Each DAC device of the system generates its own reference (ref_A in Figure 7).

If configured as a slave, an early-late comparator compares the internal reference with the external reference provided by the MDS pins. The comparator controls an internal buffer that is used to delay the samples.

10.2.5.3 Master/slave mode

The external reference is provided by one of the DACs (the master DAC), which has to be configured to do this. The others are set to slave mode.

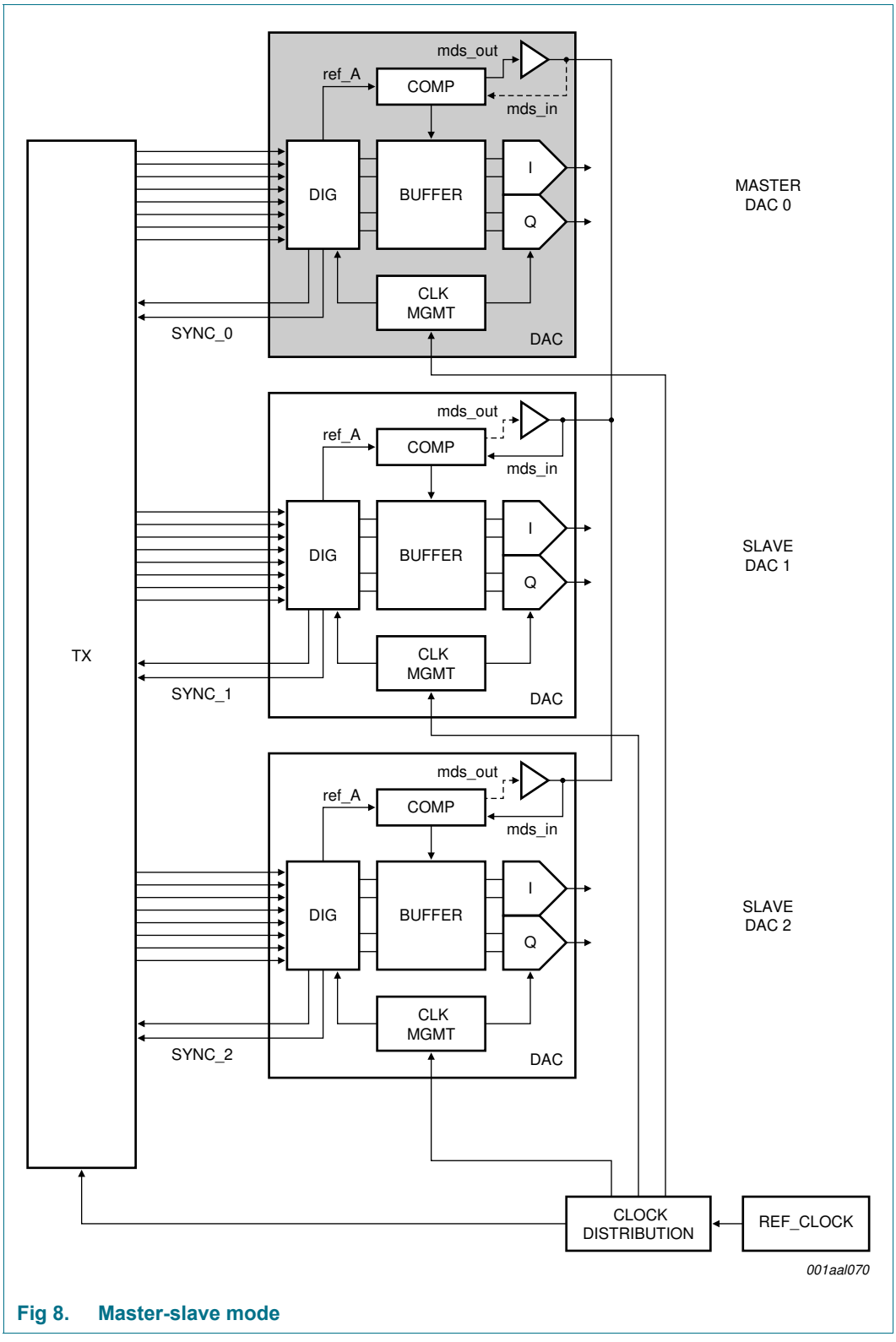


Fig 8. Master-slave mode

The MDS signal generated by the master DAC must reach all slaves within one DAC output clock period. This induces PCB layout constraints for the MDS signal and also for the clock distribution. Because trace lengths differ, the clock edges reach each of the DACs at different times.

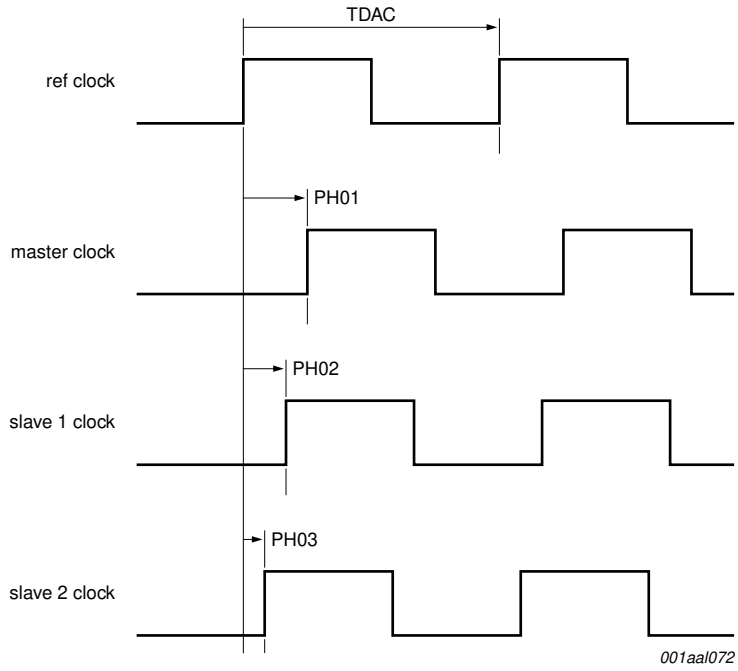


Fig 9. Clock skew case 1: Master is farthest

The worst case clock skew is given by $\delta t_1 = PH01 - PH03$, where PH0x represents the sum of the trace delay and the clock skew at the output of the clock generator.

The maximum allowable trace delay for the MDS signal is given by $\Delta t = TDAC - \delta t_1$.

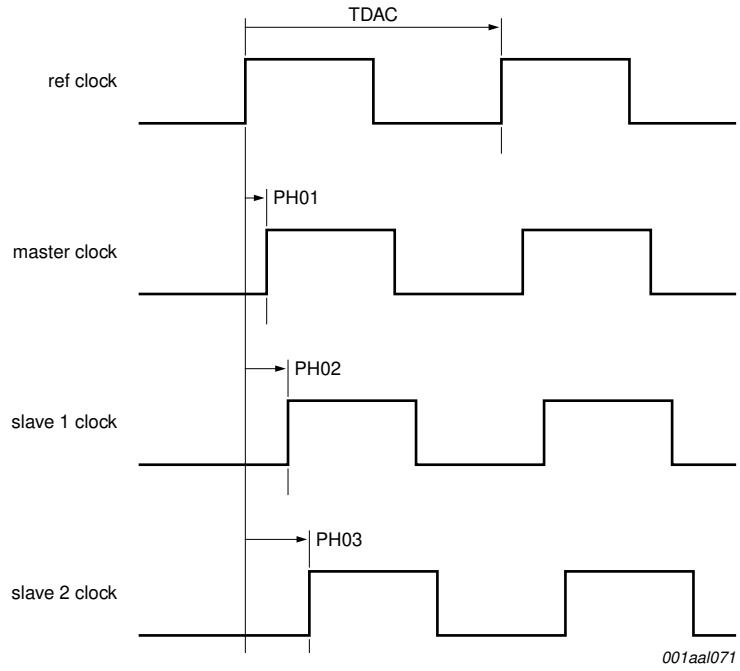


Fig 10. Clock skew case 2: Master is closest

The worst case clock skew is given by $\delta t_2 = PH03 - PH01$.

The minimum allowable trace delay for the MDS signal is given by $\Delta t = \delta t_2$.

In real applications, the master DAC can be anywhere and both conditions must be satisfied: $\delta t_2 < \Delta t_{mds} < TDAC - \delta t_1$.

Example:

- clock generator skew = ± 80 ps
- FR4 substrate ⇒ 15 cm/ns delay
- clock trace length difference = 3 cm and 4 cm
- Output sampling rate = 650 Msps

⇒ 200 ps + 80 ps < Δt_{mds} < 1538 ps – (266 ps + 80 ps)

⇒ 280 ps < Δt_{mds} < 1192 ps

⇒ 4.2 cm < L_{mds} < 17.8 cm

10.2.5.4 All slave mode

The external reference is provided by the JESD204A transmitter. All DACs are configured in slave mode.

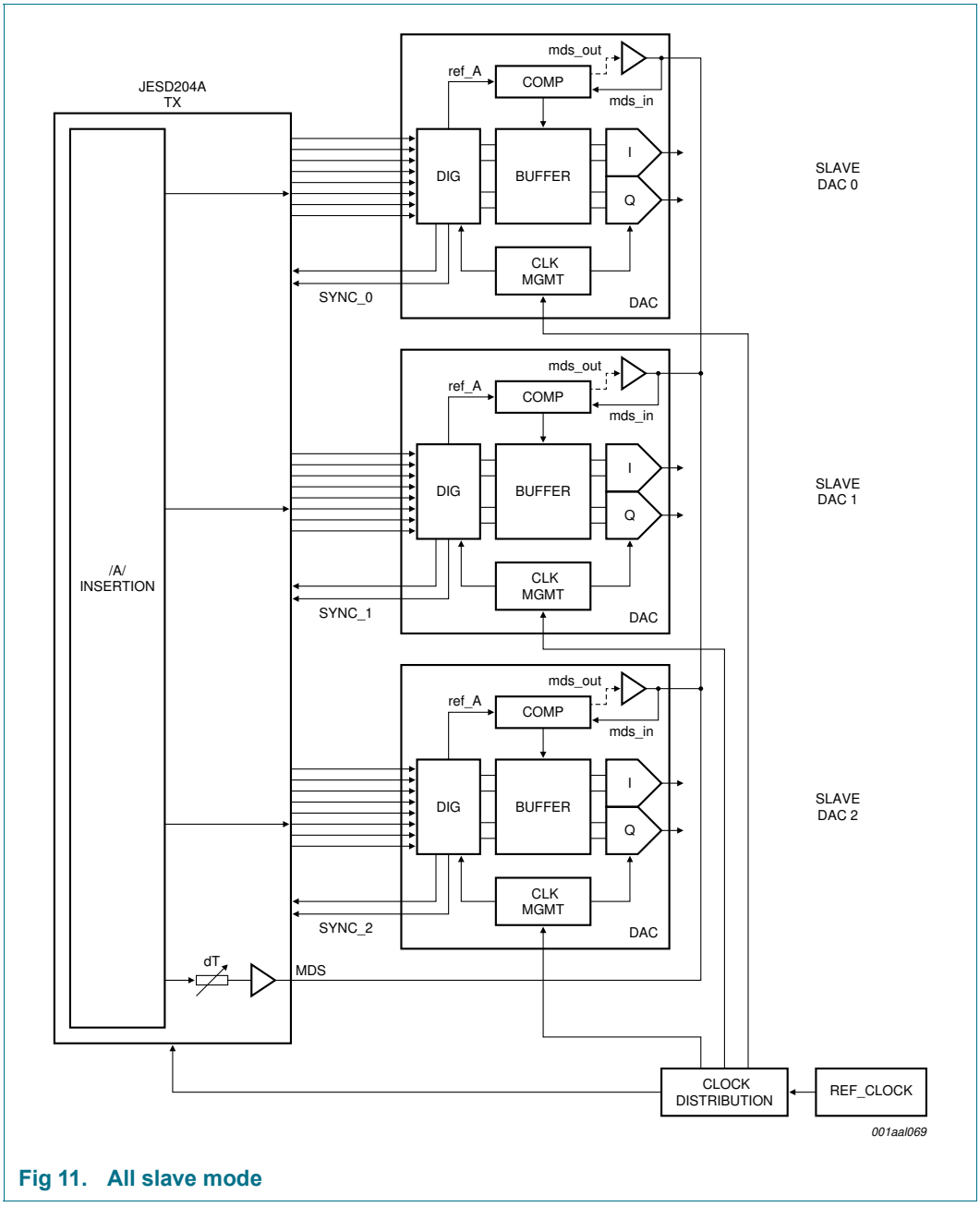


Fig 11. All slave mode

The MDS signal is now driven from the transmitter. It is generated at the end of the inter-lane alignment phase (see the JESD204A standard for details).

The transmitter must also compensate for the DAC latency. Although the DAC has an internal samples delay line, it cannot handle large delays.

In this mode, PCB layout is also important. The following delay equation applies: $\delta t < \Delta t_{mds} < TDAC - \delta t$, where δt is the clock skew considered close to DAC pins.

10.2.6 Frame assembly

DAC1408D650 supports only /F/ = 1, which means that every frame clock period carries one byte per lane. Frame assembly combines the octet of lane_0 with the six MSB bits of lane_1 and reassembles the original 14-bit sample. The same is done for lane_2 and lane_3. Tail bits are dropped.

The frame assembler also handles previously triggered errors.

If scrambling is enabled:

If a nit_err (not-in-table error) or kout_unexp (unexpected control character) occurs in lane_0 and/or lane_1, the previous 14-bit sample is repeated twice for I (lane_0, lane_1). The same is done for Q (lane_2, lane_3).

If scrambling is disabled:

If a nit_err (not-in-table error) or kout_unexp (unexpected control character) occurs in lane_0 and/or lane_1, the previous 14-bit sample is repeated once for I (lane_0, lane_1). The same is done for Q (lane_2, lane_3).

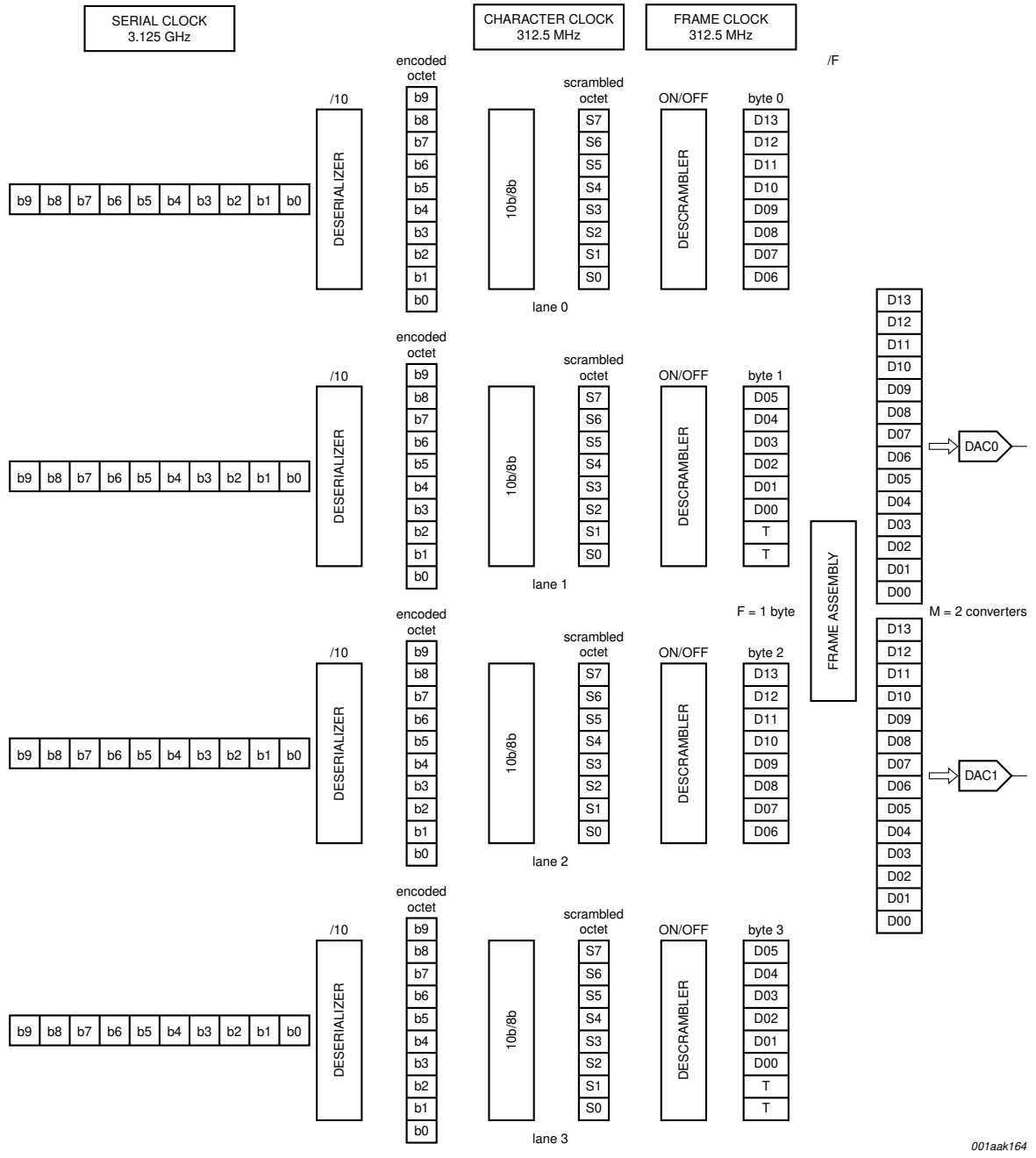


Fig 12. Frame assembly

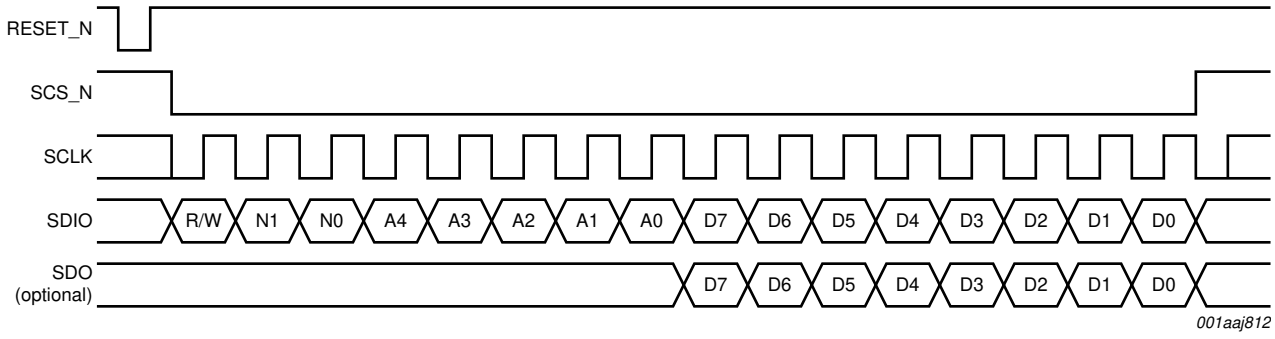
10.3 Serial Peripheral Interface (SPI)

10.3.1 Protocol description

The DAC1408D650 serial interface is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both Write mode and Read mode.

This interface can be configured as a 3-wire type (SDIO as bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pin, input and output port respectively). In both configurations, SCLK acts as the serial clock and SCS_N acts as the serial chip select bar.

Each read/write operation is sequenced by the SCS_N signal and enabled by a LOW assertion to drive the chip with two bytes to five bytes, depending on the content of the instruction byte (see Table 8).



R/W indicates the mode access, (see Table 7).

Fig 13. SPI protocol

Table 7. Read or Write mode access description

R/W	Description
0	Write mode operation
1	Read mode operation

In Table 8 below, N1 and N0 indicate the number of bytes transferred after the instruction byte.

Table 8. Number of bytes to be transferred

N1	N0	Number of bytes transferred
0	0	1
0	1	2
1	0	3
1	1	4

A[4:0] indicates which register is being addressed. In the case of a multiple transfer, this address points to the first register to be accessed. The address is then internally decreased after each following data phase.

10.3.2 SPI timing description

The SPI interface can operate at a frequency of up to 15 MHz. The SPI timing is shown in Figure 14.

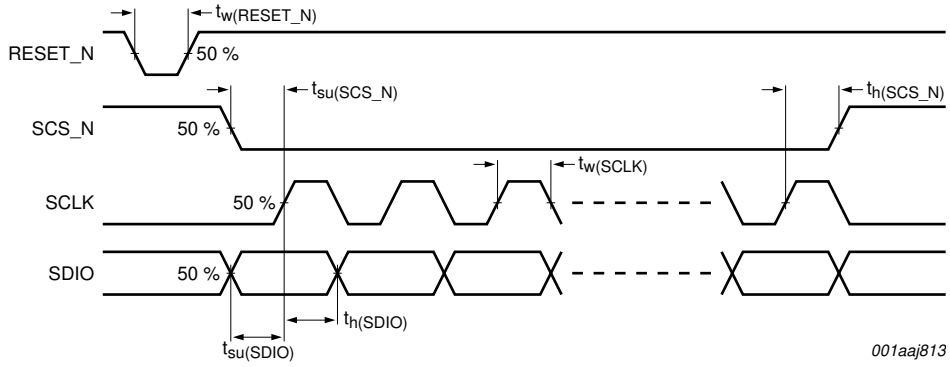


Fig 14. SPI timing diagram

The SPI timing characteristics are given in Table 9.

Table 9. SPI timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency	-	-	15	MHz
$t_{w(SCLK)}$	SCLK pulse width	30	-	-	ns
$t_{su(SCS\_N)}$	SCS_N set-up time	20	-	-	ns
$t_{h(SCS\_N)}$	SCS_N hold time	20	-	-	ns
$t_{su(SDIO)}$	SDIO set-up time	10	-	-	ns
$t_{h(SDIO)}$	SDIO hold time	5	-	-	ns
$t_{w(RESET\_N)}$	RESET_N pulse width	30	-	-	ns

10.4 Clock input

The DAC1408D650 has one differential clock input, CLKINN/CLKINP.

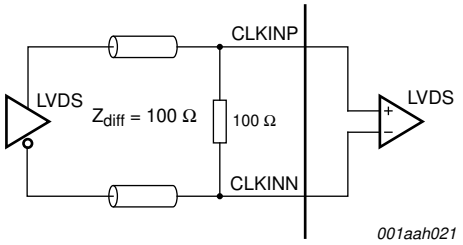


Fig 15. LVDS clock configuration

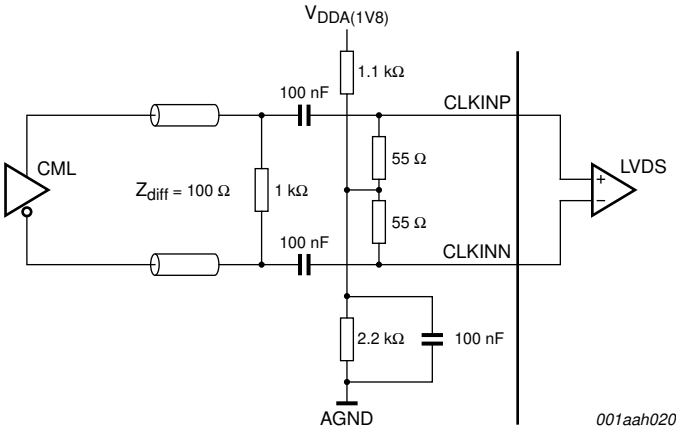


Fig 16. Interfacing CML to LVDS

The DAC1408D650 can operate with a clock frequency up to 312.5 MHz or up to 650 MHz if the internal PLL is bypassed. The clock input can be LVDS (see Figure 15) but it can also be interfaced with CML (see Figure 16). Error free data transition from one internal clock domain to another one is handled by Clock Domain Interface logic.

During the reset phase (RESET_N asserted), the clock must be stable and running. This ensures a proper reset of the complete device.

The device has no embedded power-on-reset feature. Driving the RESET_N pin to set the device to its default state is mandatory.