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DAC1617D1G0

Dual 16-bit DAC, LVDS interface, up to 1 Gsps, x2, x4 and x8 interpolating

Rev. 4 — 12 December 2012 Product data sheet

1. General description

The DAC1617D1G0 is a high-speed 16-bit dual channel Digital-to-Analog Converter (DAC) with selectable ×2, ×4 and ×8 interpolation filters. The device is optimized for multi-carrier and broadband wireless transmitters at sample rates of up to 1 Gsps. Supplied from a 3.3 V and a 1.8 V source, the DAC1617D1G0 integrates a differential scalable output current up to 34 mA.

The Serial Peripheral Interface (SPI) provides full control of the DAC1617D1G0.

The DAC1617D1G0 integrates a Low Voltage Differential Signaling (LVDS) Double Data Rate (DDR) receiver interface, with an on-chip 100 Ω termination. The LVDS DDR interface accepts a multiplex input data stream such as interleaved or folded. An internal LVDS input auto-calibration ensures the robustness and stability of the interface.

Digital on-chip modulation converts the complex I and Q inputs from baseband to IF. A 40-bit Numerically Controlled Oscillator (NCO) sets the mixer frequency. High resolution internal gain, phase and offset control provide outstanding image and Local Oscillator (LO) signal rejection at the system analog modulator output.

An inverse (sin x) / x function ensures a controlled flatness 0.5 dB for high bandwidths at the DAC output.

Multiple device synchronization allows synchronization of the outputs of multiple DAC devices. MDS guarantees a maximum skew of one output clock period between several devices.

The DAC1617D1G0 includes a very low noise capacitor-free integrated Phase-Locked Loop (PLL) multiplier which generates a DAC clock rate from the LVDS clock rate.

The DAC1617D1G0 is available in an HVQFN72 package (10 mm × 10 mm).

2. Features and benefits

- Dual-channel 16-bit resolution
- 1 Gsps maximum update rate
- Selectable ×2, ×4 and ×8 interpolation filters
- Very low noise capacitor-free integrated Phase-Locked Loop (PLL)
- Embedded Numerically Controlled Oscillator (NCO) with 40-bit programmable frequency
- Embedded complex(I/Q) digital IF modulator
- 1.8 V and 3.3 V power supplies
- LVDS DDR compatible input interface with on-chip 100 Ω terminations
- LVDS DDR input clock up to 370 MHz
- LVDS or LVPECL compatible DAC clock
- Interleaved or folded I and Q data input mode
- Synchronization of multiple DAC devices
- 3-wire or 4-wire mode SPI interface
- Differential scalable output current from 8.1 mA to 34 mA
- External analog offset control (10-bit auxiliary DACs)
- High resolution internal digital gain and offset control to support high performance IQ-modulator image rejection
- Internal phase correction
- Inverse (sin x) / x function
- Power-down mode and Sleep mode; 5-bit NCO low-power mode
- On-chip 1.25 V reference
- Industrial temperature range −40 °C to +85 °C
- 72 pins small form factor HVQFN package

3. Applications

- Wireless infrastructure: LTE, WiMAX, GSM, CDMA, WCDMA, TD-SCDMA
- Communications: LMDS/MMDS, point-to-point
- Direct Digital Synthesis (DDS)
- Broadband wireless systems
- Digital radio links
- Instrumentation
- Automated Test Equipment (ATE)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
DAC1617D1G0HN	HVQFN72	plastic thermal enhanced very thin quad flat package; no leads; 72 terminals; body 10 × 10 × 0.85 mm	SOT813-3

5. Block diagram

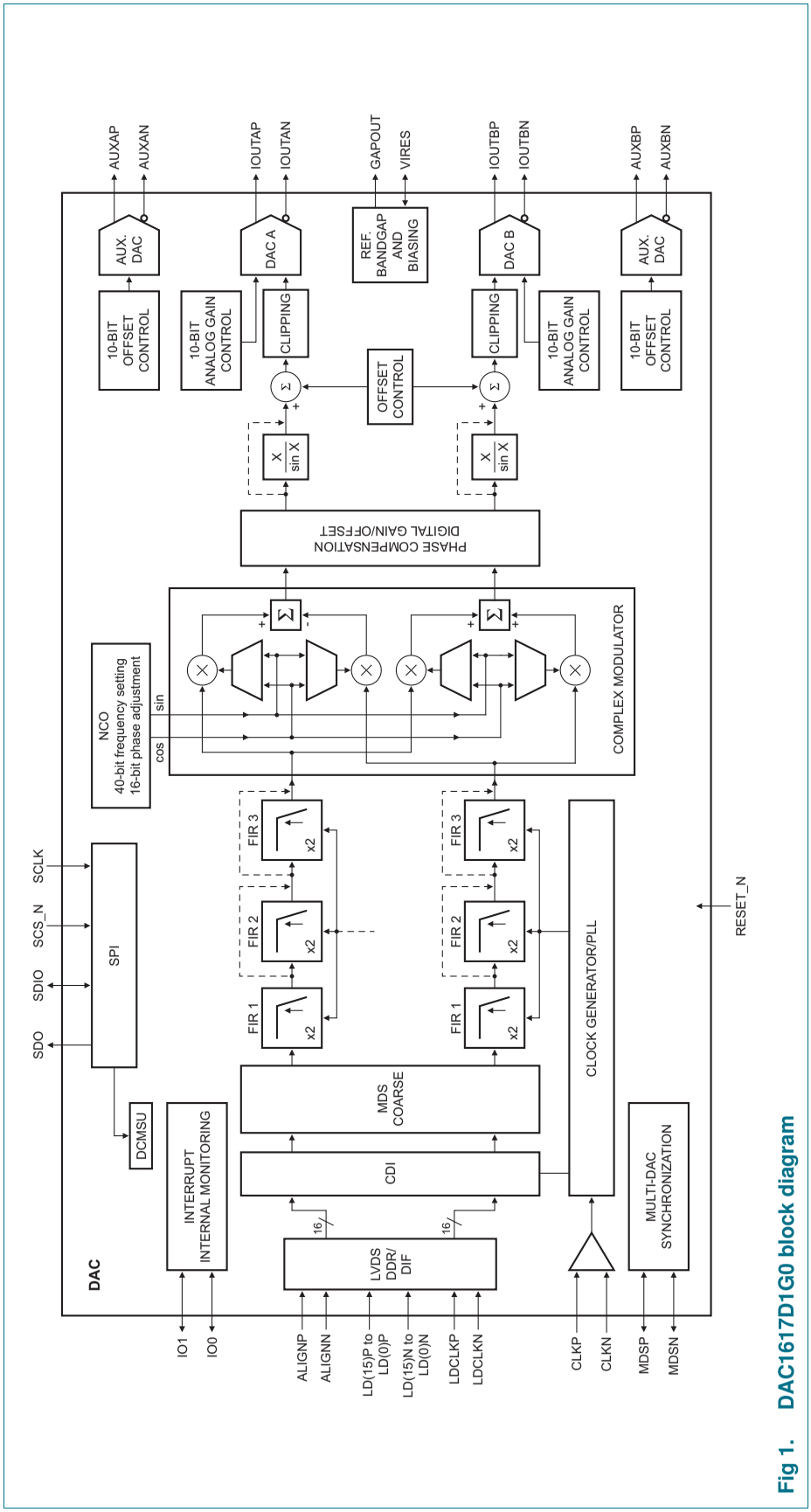
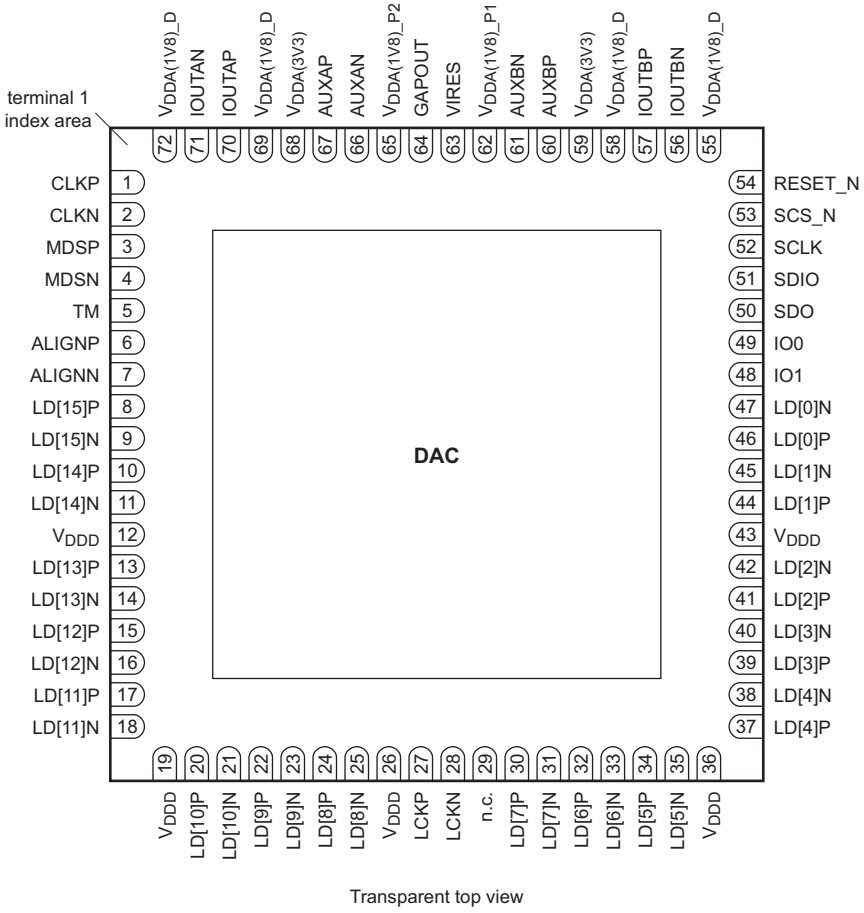


Fig 1. DAC1617D1G0 block diagram

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. DAC1617D1G0 pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
CLKP	1	I	DAC clock positive input
CLKN	2	I	DAC clock negative input
MDSP	3	IO	multi-device synchronization positive signal
MDSN	4	IO	multi-device synchronization negative signal
TM	5	I	Test mode selection (connect to GND)
ALIGNP	6	I	positive input for data alignment
ALIGNN	7	I	negative input for data alignment
LD[15]P	8	I	LVDS positive input bit 15[2]
LD[15]N	9	I	LVDS negative input bit 15[2]

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
LD[14]P	10	I	LVDS positive input bit 14[2]
LD[14]N	11	I	LVDS negative input bit 14[2]
V_{DDD}	12	P	digital power supply
LD[13]P	13	I	LVDS positive input bit 13[2]
LD[13]N	14	I	LVDS negative input bit 13[2]
LD[12]P	15	I	LVDS positive input bit 12[2]
LD[12]N	16	I	LVDS negative input bit 12[2]
LD[11]P	17	I	LVDS positive input bit 11[2]
LD[11]N	18	I	LVDS negative input bit 11[2]
V_{DDD}	19	P	digital power supply
LD[10]P	20	I	LVDS positive input bit 10[2]
LD[10]N	21	I	LVDS negative input bit 10[2]
LD[9]P	22	I	LVDS positive input bit 9[2]
LD[9]N	23	I	LVDS negative input bit 9[2]
LD[8]P	24	I	LVDS positive input bit 8[2]
LD[8]N	25	I	LVDS negative input bit 8[2]
V_{DDD}	26	P	digital power supply
LCKP	27	I	LVDS positive data clock input
LCKN	28	I	LVDS negative data clock input
n.c.	29	G	not connected
LD[7]P	30	I	LVDS positive input bit 7[2]
LD[7]N	31	I	LVDS negative input bit 7[2]
LD[6]P	32	I	LVDS positive input bit 6[2]
LD[6]N	33	I	LVDS negative input bit 6[2]
LD[5]P	34	I	LVDS positive input bit 5[2]
LD[5]N	35	I	LVDS negative input bit 5[2]
V_{DDD}	36	P	digital power supply
LD[4]P	37	I	LVDS positive input bit 4[2]
LD[4]N	38	I	LVDS negative input bit 4[2]
LD[3]P	39	I	LVDS positive input bit 3[2]
LD[3]N	40	I	LVDS negative input bit 3[2]
LD[2]P	41	I	LVDS positive input bit 2[2]
LD[2]N	42	I	LVDS negative input bit 2[2]
V_{DDD}	43	P	digital power supply
LD[1]P	44	I	LVDS positive input bit 1[2]
LD[1]N	45	I	LVDS negative input bit 1[2]
LD[0]P	46	I	LVDS positive input bit 0[2]
LD[0]N	47	I	LVDS negative input bit 0[2]
IO1	48	IO	IO port bit 1
IO0	49	IO	IO port bit 0
SDO	50	O	SPI data output

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
SDIO	51	IO	SPI data input/output
SCLK	52	I	SPI clock
SCS_N	53	I	SPI chip select (active LOW)
RESET_N	54	I	general reset (active LOW)
$V_{DDA(1V8)\_D}$	55	P	1.8 V analog power supply (DAC core)
IOUTBN	56	O	complementary DAC B output current
IOUTBP	57	O	DAC B output current
$V_{DDA(1V8)\_D}$	58	P	1.8 V analog power supply (DAC core)
$V_{DDA(3V3)}$	59	P	3.3 V analog power supply
AUXBP	60	O	auxiliary DAC B output current
AUXBN	61	O	complementary auxiliary DAC B output current
$V_{DDA(1V8)\_P1}$	62	P	1.8 V analog power supply (PLL)
VIRES	63	IO	DAC biasing resistor
GAPOUT	64	IO	band gap input/output voltage
$V_{DDA(1V8)\_P2}$	65	P	1.8 V analog power supply (PLL)
AUXAN	66	O	complementary auxiliary DAC A output current
AUXAP	67	O	auxiliary DAC A output current
$V_{DDA(3V3)}$	68	P	3.3 V analog power supply
V_{DDA1V8_D}	69	P	1.8 V analog power supply (DAC core)
IOUTAP	70	O	DAC A output current
IOUTAN	71	O	complementary DAC A output current
$V_{DDA(1V8)\_D}$	72	P	1.8 V analog power supply (DAC core)
GND	H	G	ground (exposed die pad)

[1] P: power supply; G: ground; I: input; O: output.

[2] The LVDS input data bus order can be reversed and each element can be swapped between P and N using dedicated registers (see Table 60).

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			−0.5	+4.6	V
V_{DDD}	digital supply voltage			−0.5	+2.5	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		[1]	−0.5	+2.5	V
V_I	input voltage	input pins referenced to GND		−0.5	+2.5	V
V_O	output voltage	pins IOUTAP, IOUTAN, IOUTBP, IOUTBN, AUXAP, AUXAN, AUXBP and AUXBN referenced to GND		−0.5	+4.6	V
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
T_j	junction temperature			−40	+125	°C

[1] Connect the analog 1.8 V power supply to pins VDDA1V8_D, VDDA1V8_P1, and VDDA1V8_P2.

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	16.2	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	6.7	K/W

[1] Value for six-layer board in still air with a minimum of 49 thermal vias.

9. Characteristics

Table 5. Characteristics

$V_{DDA(1V8)}$ = 1.8 V; V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		C	3.15	3.3	3.45	V
V_{DDD}	digital supply voltage		C	1.7	1.8	1.9	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		C [2]	1.7	1.8	1.9	V
$I_{DDA(3V3)}$	analog supply current (3.3 V)	Auxiliary DAC on	C	51	55	59	mA
I_{DDD}	digital supply current (1.8 V)	f_s = 983.04 67; ×4 interpolation; no NCO; MDS off	C	475	525	585	mA
		f_s = 620 Msps; ×2 interpolation; NCO on; no MDS	C	400	450	500	mA
$I_{DDA(1V8)}$	analog supply current (1.8 V)	f_s = 983.04 Msps; 1 V (p-p)	C [2]	207	218	230	mA
		f_s = 620 Msps; 1 V (p-p)	C	207	218	230	mA
P_{tot}	total power dissipation	f_s = 983.04 Msps; ×4 interpolation; NCO off; MDS off	C	-	1580	-	mW
		f_s = 983.04 Msps; ×4 interpolation; 5-bit NCO; MDS off	C	-	1500	-	mW
		f_s = 620 Msps; ×2 interpolation; 5-bit NCO; MDS off		-	1370	-	mW
		power-down using SPI register	C	-	63	-	mW
Clock inputs (pins CLKP, CLKN)							
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	C	150	-	1000	mV
R_i	input resistance		D	-	200	-	kΩ
C_i	input capacitance		D	-	1	-	pF
Digital inputs (pins LD[15]P to LD[0]P, LD[15]N to LD[0]N, LCKP and LCKN, ALIGNP and ALIGNN)							
V_i	input voltage	$\|V_{gpd}\|$ < 50 mV [3]	C	825	-	1575	mV
V_{idth}	input differential threshold voltage	$\|V_{gpd}\|$ < 50 mV [3]	C	−100	-	+100	mV
R_i	input resistance		D	-	100	-	Ω
C_i	input capacitance		D	-	0.8	-	pF
		pins LCKP and LCKN	D	-	0.9	-	pF

Table 5. Characteristics *...continued*

$V_{DDA(1V8)}$ = 1.8 V; V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Digital inputs/outputs (pins MDSN, MDSP)							
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage		C	-	500	-	mV
C_i	input capacitance	between GND and pin MDSN or MDSP	D	-	0.6	-	pF
R_i	input resistance		D	-	100	-	Ω
V_i	input voltage	$\|V_{gpd}\| < 50$ mV [3]	C	825	-	1575	mV
V_{idth}	input differential threshold voltage	$\|V_{gpd}\| < 50$ mV [3]	C	−100	-	+100	mV
Digital inputs/outputs (pins SDO, SDIO, SCLK, SCS_N, RESET_N, IO0, IO1)							
V_{IL}	LOW-level input voltage		C	GND	-	$0.3V_{DDD(1V8)}$	V
V_{IH}	HIGH-level input voltage		C	$0.7V_{DDD(1V8)}$	-	$V_{DDD(1V8)}$	V
V_{OL}	LOW-level output voltage	pins IO0, IO1, SDO and SDIO	C	GND	-	$0.1V_{DDD(1V8)}$	V
V_{OH}	HIGH-level output voltage	pins IO0, IO1, SDO and SDIO	C	$0.9V_{DDD(1V8)}$	-	$V_{DDD(1V8)}$	V
I_{IL}	LOW-level input current	maximum VIL	I	−10	-	+10	µA
I_{IH}	HIGH-level input current	maximum VIL	I	−10	-	+10	µA
C_i	input capacitance		D	-	2.2	-	pF
Analog outputs (pins IOUTAP, IOUTAN, IOUTBP, IOUTBN)							
I_{bias}	bias current	DC current	D	-	2.5	-	mA
$I_{O(fs)}$	full-scale output current	controlled by the analog GAIN registers (see Table 32)	D	8.1	-	34	mA
		default value	D	-	20	-	mA
V_O	output voltage	compliance range	D	2.3	-	$V_{DDA(3V3)}$	V
$V_{O(cm)}$	common-mode output voltage	1 V (p-p) DAC output	D	-	3	-	V
		2 V (p-p) DAC output		-	2.8	-	V
R_o	output resistance		D	-	250	-	kΩ
C_o	output capacitance	between pins OUTAN and OUTBN and pins OUTBN and OUTBP	D	-	5	-	pF
Reference voltage output (pin GAPOUT)							
$V_{O(ref)}$	reference output voltage	T_{amb} = +25 °C	I	-	1.22	-	V

Table 5. Characteristics *...continued*

$V_{DDA(1V8)}$ = 1.8 V; V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
$I_{O(ref)}$	reference output current	1.25 V external voltage	D	-	40	-	µA
Analog auxiliary outputs (pins AUXAP, AUXAN, AUXBP and AUXBN)							
$I_{O(fs)}$	full-scale output current	auxiliary DAC A; differential outputs	I	-	3.1	-	mA
		auxiliary DAC B; differential outputs	I	-	3.1	-	mA
$V_{O(aux)}$	auxiliary output voltage	compliance range	D	0	-	2.3	V
LVDS input timing							
f_{data}	data rate	$f_{s(max)}$ specification must be respected ($f_s = f_{data} \times$ interpolation factor)	C	-	-	370	MHz
$t_{sk(clk-D)}$	skew time from clock to data input	f_{DATA} = 184.32 Mhz	C	800	-	830	ps
		f_{DATA} = 245.76 MHz	C	500	-	675	ps
		f_{DATA} = 307.2 MHz	C	300	-	520	ps
		f_{DATA} = 368.64 MHz	C	150	-	500	ps
t_{su}	set-up time	manual tuning mode (see Figure 16); depends on LDCLK_DEL[3:0]					
		0000	C	−300	-	-	ps
		0001	C	−365	-	-	ps
		0010	C	−440	-	-	ps
		0011	C	−520	-	-	ps
		0100	C	−590	-	-	ps
		0101	C	−675	-	-	ps
		0110	C	−750	-	-	ps
		0111	C	−830	-	-	ps
		1000	C	−845	-	-	ps
		1001	C	−845	-	-	ps
		1010	C	−1000	-	-	ps
		1011	C	−1100	-	-	ps
		1100	C	−1220	-	-	ps
		1101	C	−1290	-	-	ps
		1110	C	−1360	-	-	ps
		1111	C	−1450	-	-	ps

Table 5. Characteristics *...continued*

$V_{DDA(1V8)}$ = 1.8 V; V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
t_{hold}	hold time	manual tuning mode (see Figure 15); depends on LDCLK_DEL[3:0]:					
		0000	C	790	-	-	ps
		0001	C	870	-	-	ps
		0010	C	950	-	-	ps
		0011	C	1055	-	-	ps
		0100	C	1140	-	-	ps
		0101	C	1230	-	-	ps
		0110	C	1360	-	-	ps
		0111	C	1460	-	-	ps
		1000	C	1900	-	-	ps
		1001	C	2075	-	-	ps
		1010	C	2250	-	-	ps
		1011	C	2400	-	-	ps
		1100	C	2560	-	-	ps
		1101	C	2740	-	-	ps
		1110	C	2900	-	-	ps
		1111	C	3000	-	-	ps
DAC output timing							
$f_{s(max)}$	sampling rate		C	1000	-	-	Msps
t_s	settling time	to ± 0.5 LSB	D	-	20	-	ns
Internal PLL timing							
f_s	sampling rate		D	50	-	1000	Msps
40-bit NCO frequency range; f_s = 1000 Msps							
f_{NCO}	NCO frequency	two's complement coding					
		register value = 8000000000h	D	-	–500	-	MHz
		register value = FFFFFFFFFFh	D	-	–0.9095	-	mHz
		register value = 0000000000h	D	-	0	-	Hz
		register value = 0000000001h	D	-	+0.9095	-	mHz
		register value = 7FFFFFFFFFh	D	-	+499.99909	-	MHz
f_{step}	step frequency		D	-	0.9095	-	mHz

Table 5. Characteristics *...continued*

$V_{DDA(1V8)}$ = 1.8 V; V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Low-power NCO frequency range; f_s = 1000 MHz							
f_{NCO}	NCO frequency	two's complement coding					
		register value = F8000000000h	D	-	–500	-	MHz
		register value = F8000000000h	D	-	–31.25	-	MHz
		register value = 00000000000h	D	-	0	-	Hz
		register value = 08000000000h	D	-	+31.25	-	MHz
		register value = 7FFFFFFFFFh	D	-	+468.75	-	MHz
f_{step}	step frequency		D	-	31.25	-	MHz
Dynamic performance							
SFDR	spurious-free dynamic range	f_{data} = 245.76 MHz; f_s = 983.04 Msps; BW = f_s / 2					
		f_o = 20 MHz at –1 dBFS	I	-	78	-	dBc
		f_{data} = 184.32 MHz; f_s = 737.28 Msps; BW = f_s / 2					
		f_o = 20 MHz at –1 dBFS		-	78	-	dBc
$SFDR_{RBW}$	restricted bandwidth spurious-free dynamic range	f_{data} = 245.76 MHz; f_s = 983.04 Msps; f_o = 150 MHz		-		-	dBc
		BW = 100 MHz		-	78	-	dBc
		BW = 180 MHz		-	78	-	dBc
IMD3	third-order intermodulation distortion	f_{data} = 245.76 MHz; f_s = 983.04 Msps; f_{o1} = 20 MHz; f_{o2} = 21 MHz; ×4 interpolation; output level = –1 dBFS	C	-	75	-	dBc
		f_{data} = 245.76 MHz; f_s = 983.04 Msps; f_{o1} = 152 MHz; f_{o2} = 155.1 MHz; ×4 interpolation; output level = –1 dBFS	I	-	75	-	dBc

Table 5. Characteristics *...continued*

$V_{DDA(1V8)}$ = 1.8 V; V_{DDD} = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse sinus x/x; no output correction; output load condition defined in Figure 29; output level = 1 V (p-p).

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
ACPR	adjacent channel power ratio	WCDMA pattern; f_s = 983.04 Msps; ×4 interpolation; f_{NCO} = 153.6 MHz					
		1 carrier; BW = 5 MHz	C	-	73	-	dBc
		2 carriers; BW = 10 MHz	C	-	70	-	dBc
		4 carriers; BW = 20 MHz	C	-	68	-	dBc
$\alpha_{isol(ch-ch)}$	isolation between channels	f_s = 1228.8 Msps; ×4 interpolation; f_{out} = 10 MHz; NCO = off; level = 0.1 dBFS; both DAC channels enabled	C	-	110	-	dBc
		f_s = 1228.8 Msps; ×4 interpolation; f_{out} = 83 MHz; NCO = off; level = 0.1 dBFS; both DAC channels enabled	C	-	95	-	dBc
		f_s = 1228.8 Msps; ×4 interpolation; f_{out} = 210 MHz; NCO = on; level = 0.1 dBFS; one DAC channel enabled; one DAC channel disabled	C	-	81	-	dBc
NSD	noise spectral density	f_s = 983.04 Msps; ×4 interpolation; f_o = 20 MHz at −1 dBFS	D	-	−158	-	dBm/Hz
		f_s = 983.04 Msps; ×4 interpolation; f_o = 153.6 MHz at −1 dBFS	D	-	−155	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] Connect $V_{DDA(1V8)\_D}$, $V_{DDA(1V8)\_P1}$ and $V_{DDA(1V8)\_P2}$ to the same 1.8 V analog power supply. Use dedicated filters for the three power pins.

[3] $|V_{gpd}|$ represents the ground potential difference voltage. This voltage is the result of current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltages.

10. Application information

10.1 General description

The DAC1617D1G0 is a dual 16-bit DAC operating up to 1000 Msps. Each DAC consists of a segmented architecture, comprising a 6-bit thermometer subDAC and a 10-bit binary weighted subDAC.

A maximum input LVDS DDR data rate of up to 370 MHz and a maximum output sampling rate of 1000 Msps ensure more flexibility for wide bandwidth and multi-carrier systems. The internal 40-bit NCO of the DAC1617D1G0 simplifies the frequency selection of the system. The DAC1617D1G0 provides ×2, ×4 or ×8 interpolation filters that are useful for removing the undesired images.

Each DAC generates two complementary current outputs on pins IOUTAP and IOUTAN and pins IOUTBP and IOUTBN. These outputs provide a full-scale output current ($I_{O(fs)}$) of up to 34 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

High resolution internal gain, phase and offset control provide outstanding image and Local Oscillator (LO) signal rejection at the system analog modulator output.

Multiple device synchronization enables synchronization of the outputs of multiple DAC devices. MDS guarantees a maximum skew of one output clock period between several devices.

All functions can be set using an SPI interface.

10.2 Serial Peripheral Interface (SPI)

10.2.1 Protocol description

The DAC1617D1G0 serial interface is a synchronous serial communication port ensures easy interface with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both write and read mode.

This interface can be configured as a 3-wire type (pin SDIO as bidirectional pin) or 4-wire type (pins SDIO and SDO as unidirectional pins, input and output port, respectively). In both configurations, SCLK acts as the serial clock and SCS_N as the serial chip select.

Figure 3 shows the SPI protocol. An SCS_N signal follows each read/write operation. A LOW assertion enables it to drive the chip with 2 bytes to 5 bytes, depending on the content of the instruction byte (see Table 7).

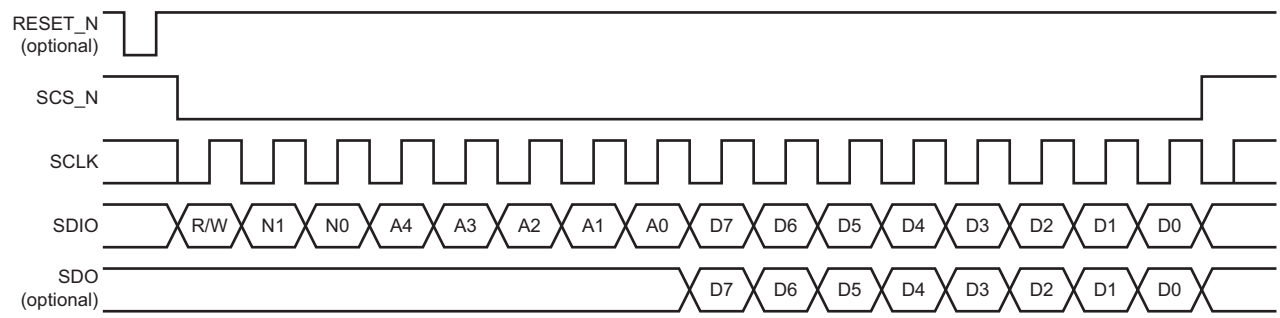


Fig 3. SPI protocol

R/W indicates the mode access (see Table 6)

Table 6. Read or Write mode access description

R/W	Description
0	Write mode operation
1	Read mode operation

Table 7 shows the number of bytes to be transferred. N1 and N0 indicate the number of bytes transferred after the instruction byte.

Table 7. Number of bytes transferred

N1	N0	Number of bytes transferred
0	0	1 byte
0	1	2 bytes
1	0	3 bytes
1	1	4 bytes

A[4:0] indicates which register is being addressed. If a multiple transfer occurs, this address concerns the first register. The other registers follow directly in a decreasing order (see Table 21, Table 35 and Table 53).

The DAC1617D1G0 incorporates more than the 32 SPI registers allowed by the address value A[4:0]. It uses three SPI register pages (page_00, page_01, and page_0A), each containing 32 registers. The 32nd register of each page indicates which page is currently addressed (00h, 01h or 0Ah).

10.2.2 SPI timing description

The SPI interface can operate at a frequency up to 25 MHz. The SPI timings are shown in Figure 4.

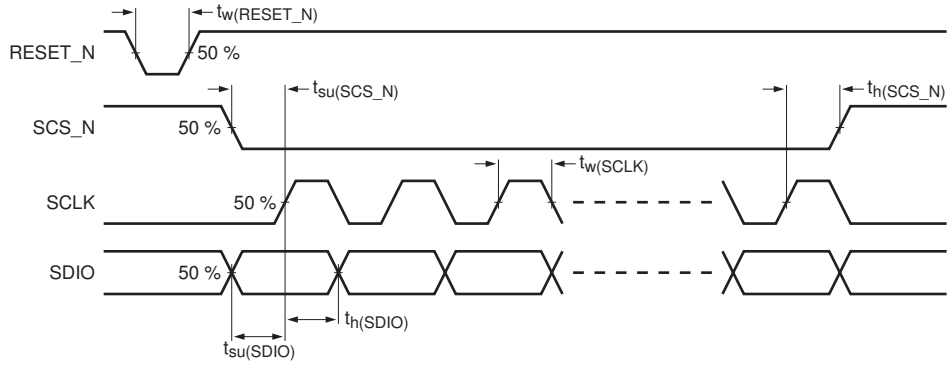


Fig 4. SPI timing diagram

The SPI timing characteristics are given in Table 8.

Table 8. SPI timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency	-	-	25	MHz
$t_{w(SCLK)}$	SCLK pulse width	30	-	-	ns
$t_{su(SCS\_N)}$	SCS_N set-up time	20	-	-	ns
$t_{h(SCS\_N)}$	SCS_N hold time	20	-	-	ns
$t_{su(SDIO)}$	SDIO set-up time	10	-	-	ns
$t_{h(SDIO)}$	SDIO hold time	5	-	-	ns
$t_{w(RESET\_N)}$	RESET_N pulse width	30	-	-	ns

10.3 Power-on sequence

There are three steps for the power-on sequence (see Figure 5):

1. The board is power-on. At the turn-on time, all DAC1617D1G0 supplies have reached their specification ranges.
2. At least 1 µs after the turn-on time pin RESET_N must be released.
3. When the DAC clock and LVDS clock are stable, the SPI configuration is sent to the DAC1617D1G0. Writing 0 in bits RST_DCLK and RST_LCLK of the register MAIN_CNTRL (see Table 54) starts the automatic calibration. 30 µs after this calibration, the DAC1617D1G0 is operational.

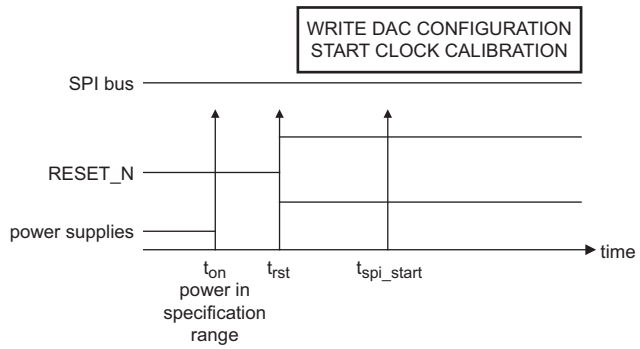


Fig 5. Power-on sequence

10.4 LVDS Data Input Format (DIF) block

The Data Input Formatting (DIF) block captures and resynchronizes data on the LVDS bus with its own LCLKP/LCLKN clock. Each LVDS input buffer has an internal resistance of 100 Ω, so an external resistor is not required. The DIF block includes two subblocks:

- **LVDS receiver:**

  Provides high flexibility for the LVDS interface, especially for the PCB layout and the control of the input port polarity and the input port mapping.

- **Data format block:**

  Enables the adaptation, which ensures the support of several data encoding modes.

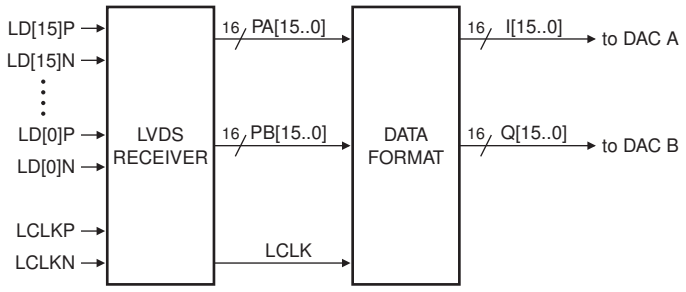


Fig 6. LVDS Data Input Format (DIF) block diagram

10.4.1 Input port polarity

The polarity of each individual LVDS input (LD[15]P to LD[0]P and LD[15]N to LD[0]N) can be changed. This ensures a much easier PCB layout design. The input polarity is controlled with bits LD_POL[15:0] (see Table 59).

10.4.2 Input port mapping

Inverting the order of the LSB and the MSB of the LVDS bus using bit WORD_SWAP in register LD_CNTRL (see Table 60) also simplifies the design of the PCB (see Table 9).

Table 9. Input LVDS bus swapping

Internal LVDS bus	External LVDS bus (WORD_SWAP = 0)	External LVDS bus (WORD_SWAP = 1)
LDI[15]P,N	LD[15]P,N	LD[0]P,N
LDI[14]P,N	LD[14]P,N	LD[1]P,N
LDI[13]P,N	LD[13]P,N	LD[2]P,N
LDI[12]P,N	LD[12]P,N	LD[3]P,N
LDI[11]P,N	LD[11]P,N	LD[4]P,N
LDI[10]P,N	LD[10]P,N	LD[5]P,N
LDI[9]P,N	LD[9]P,N	LD[6]P,N
LDI[8]P,N	LD[8]P,N	LD[7]P,N
LDI[7]P,N	LD[7]P,N	LD[8]P,N
LDI[6]P,N	LD[6]P,N	LD[9]P,N
LDI[5]P,N	LD[5]P,N	LD[10]P,N
LDI[4]P,N	LD[4]P,N	LD[11]P,N
LDI[3]P,N	LD[3]P,N	LD[12]P,N
LDI[2]P,N	LD[2]P,N	LD[13]P,N
LDI[1]P,N	LD[1]P,N	LD[14]P,N
LDI[0]P,N	LD[0]P,N	LD[15]P,N

10.4.3 Input port swapping

The LVDS DDR receiver block internally maps the incoming LVDS data bus into two buses with a single data rate (Figure 7).

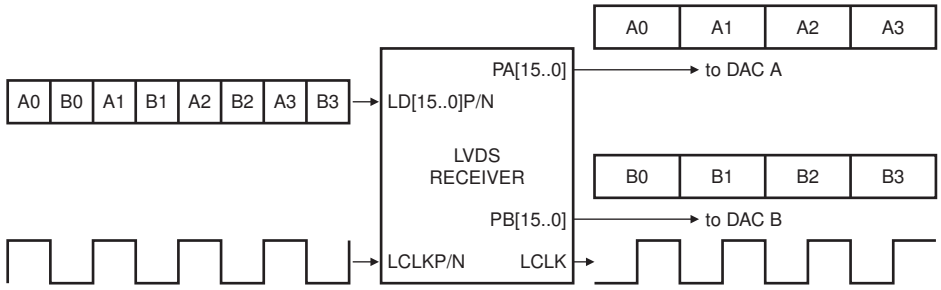


Fig 7. LVDS DDR receiver mapping LDAB SWAP = 0

These two buses can be swapped internally using bit LDAB_SWAP of register LD_CNTRL (see Table 60 and Figure 8).

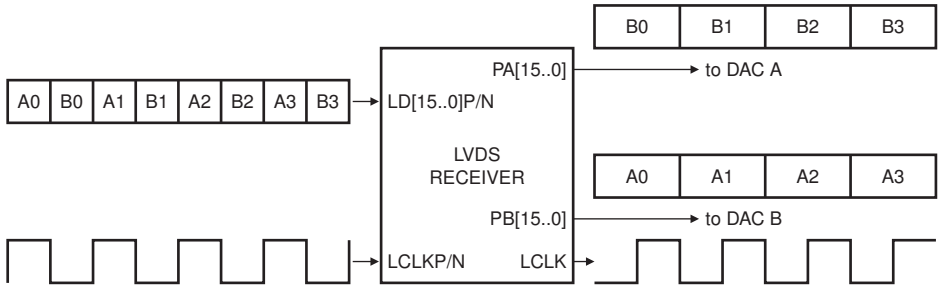


Fig 8. LVDS DDR receiver mapping LDAB SWAP = 1

10.4.4 Input port formatting

The LVDS DDR input bus multiplexes two 16-bit streams. The LVDS receiver block demultiplexes these two streams.

The two streams can carry two data formats:

- Folded
- Interleaved

The data format block is in charge of the data format adaptation (see Figure 9).

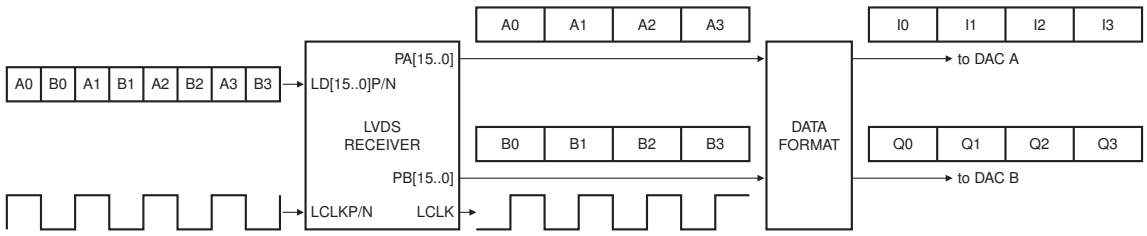


Fig 9. LVDS DDR data formats

The DAC1617D1G0 can correctly decode the input stream using bit IQ_FORMAT of register LD_CNTRL (see Table 60), because it can determine which format is used on the LVDS DDR bus.

Table 10 shows the format mapping between the LVDS input data and the data sent to the two DAC channels depending on the data format selected.

Table 10. Folded and interleaved format mapping

Data format	Data bit mapping
interleaved format (IQ_FORMAT = 1)	In[15..0] = An[15..0]; Qn[15..0] = Bn[15..0]
folded format (IQ_FORMAT = 0)	In[15..8] = An[15..8]; In[7..0] = Bn[15..8] Qn[15..8] = An[7..0]; Qn[7..0] = Bn[7..0]

10.4.5 Data parity/data enable

The ALIGN pins can be used in several ways:

- As datastream start flag for Multiple Devices Synchronization (see Section 10.13).
- As LVDS data enable which can be used to insert a DC level into the datastream. The SEL_EN bits in register LD_CNTRL (see Table 60) enable the programming of this mode. The DC level for both channels is selected using registers I_DC_LVL and Q_DC_LVL (see Table 62)
- As parity bit for the LD[15:0] to detect disruptions at the LVDS-input port bit PARITYC in register LD_CNTRL (see Table 60) enabling the control of this mode. A Parity error can generate an interrupt (INTR) reported on either IO0 or IO1 pin

10.5 Interrupt controller

The DAC1617D1G0 incorporates an interrupt controller that makes notifying a host-controller in case of an internal event. The INTR-signal can be made available on one of the IO pins. The polarity on the IO pins is programmable.

The internal event that must be tracked and generates an interrupt can be selected using the INTR_EN register (see Table 45). Two types of interrupt sources are considered:

- The ready-indicators (MAQ_RDY_B, MAQ_RDY_A, AUTO_CAL_RDY, and AUTO_DL_RDY; register INTR_FLAGS; see Table Table 47) notify the host-interface that the corresponding process (invoked by the host interface) has been finalized
- The error flags indicate that a failure has been detected. For example, on the LVDS-interface it is possible to check for parity errors and/or to monitor if the internal timing of the LVDS clock delay has changed since the calibration. Errors like these can result in critical timings within the Clock Domain Interface (CDI) which transfers the data from the LCLK to the DCLK domain

The selected event that has invoked the interrupt can be determined using the INTR_FLAGS register (see Table 47). The flags and the INTR signal are reinitialized by setting the INTR_CLEAR control bit in register INTR_CTRL (see Table 45).

10.6 General-purpose IO pins

The DAC1617D1G0 provides two general-purpose pins, IO0 and IO1. These pins can be used to observe the interrupt signal (INTR) or other internal signals (internal clocks, LVDS data, etc.). These pins can also be used as generic outputs to control external devices.

The internal signals that must be observed on these pins are selected using registers IO_MUX0, IO_MUX1, and IO_MUX2 (see Table 63 and Table 64).

10.7 Input clock

The DAC1617D1G0 operates with two clocks, one for the LVDS DDR interface and one for the DAC core.

10.7.1 LVDS DDR clock

The LVDS DDR clock can be interfaced as shown in Figure 10 because the clock buffer contains a 100 Ω internal resistor.

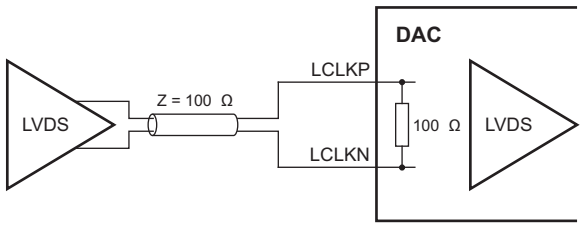
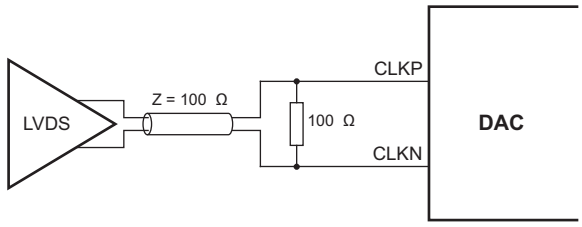


Fig 10. LVDS DDR clock configuration

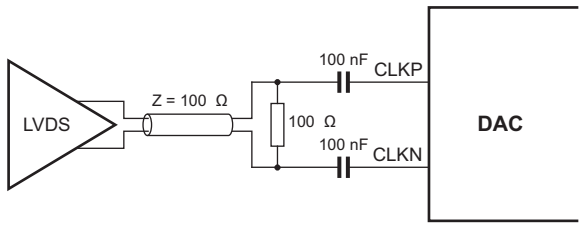
10.7.2 DAC core clock

The DAC core clock can achieve a frequency of up to 1 Gsps. It includes internal biasing to support both AC-coupling and DC-coupling. The clock can be easily connected to any LVDS, CML or PECL clock sources.

Depending on the interface selected, the hardware configuration varies (see Figure 11 to Figure 13).



a. DC-coupling



b. AC-coupling

Fig 11. DAC core clock: LVDS configuration

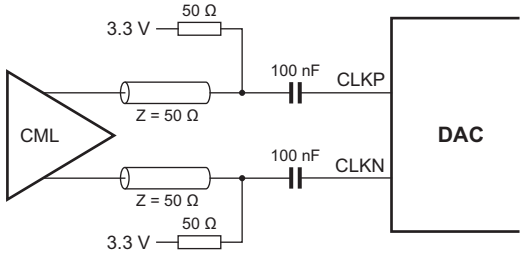


Fig 12. DAC core clock: CML configuration with AC-coupling

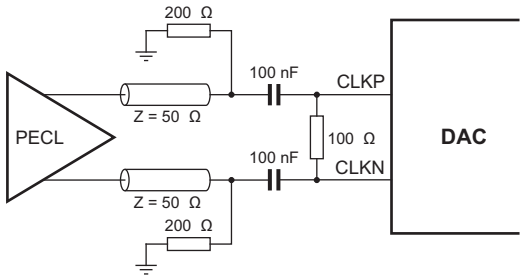


Fig 13. DAC core clock: PECL configuration with AC-coupling

10.8 Timing

The DAC1617D1G0 can operate at an update rate (f_s) of up to 1 Gsps and with an input data rate (f_{data}) of up to 370 MHz.

The sampling position of the LVDS data can be tuned using a 16-step compensation delay clock. An internal clock is generated to define the exact sampling position of the LVDS data (see Figure 14, signals LDCLKPcp and LDCLKNcp) which depends on the compensation delay.

Figure 14 shows how the compensation delay helps to recover the LVDS DDR data on both the A and B paths.

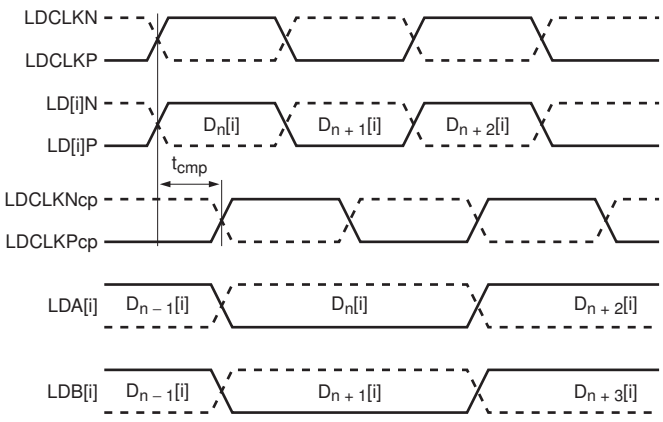
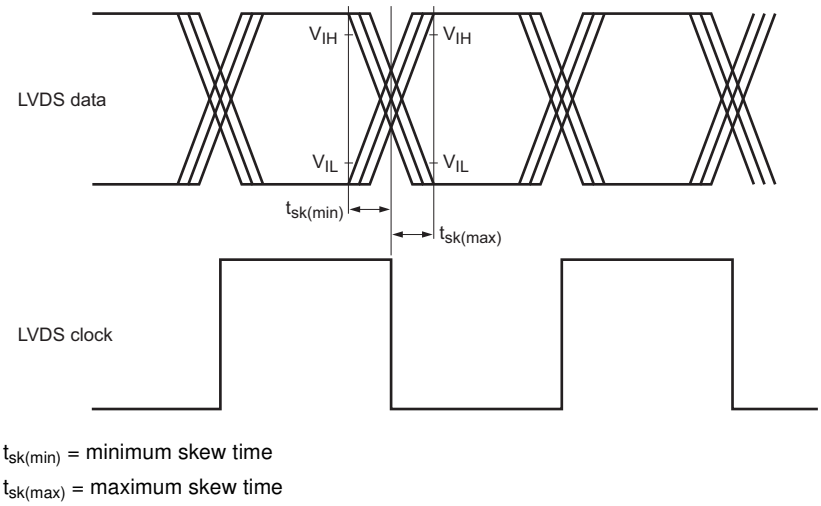


Fig 14. LVDS DDR demux timing (LVDS A and B paths not swapped; LDAB_SWAP = 0)

The compensation delay time (t_{cmp} in Figure 14) can be tuned automatically or manually. Bit CAL_CNTRL of the MAIN_CNTRL register (see Table 54) enables the switching between automatic tuning and manual tuning.

In Automatic tuning mode, the external LVDS data and clock signals are generated using the same reference clock (inside the FPGA). The LDCLK clock is similar to a data bit that toggles each time (the rising edge and falling edge of the LDCLK and LVDS data occur at the same time). In automatic tuning, the internal compensation delay time (t_{cmp}) is defined automatically to compensate the internal DAC1617D1G0 delay time optimally.

The timing requirement in automatic tuning mode is defined in Figure 15 and in Table 5.



$t_{sk(min)}$ = minimum skew time

$t_{sk(max)}$ = maximum skew time

Fig 15. Timing requirement automatic tuning

Use manual tuning mode if the LVDS data and the LDCLK clock signals provided to the DAC1617D1G0 device have a systematic delay. The compensation delay time can be adjusted to compensate for the systematic delay. The compensation delay time (t_{cmp} in Figure 14), can be defined using bits LDCLK_DEL[3:0] of register MAN_LDCLKDEL (see Table 55).

The timing requirement in manual tuning mode is defined in Figure 16 and in Table 5.

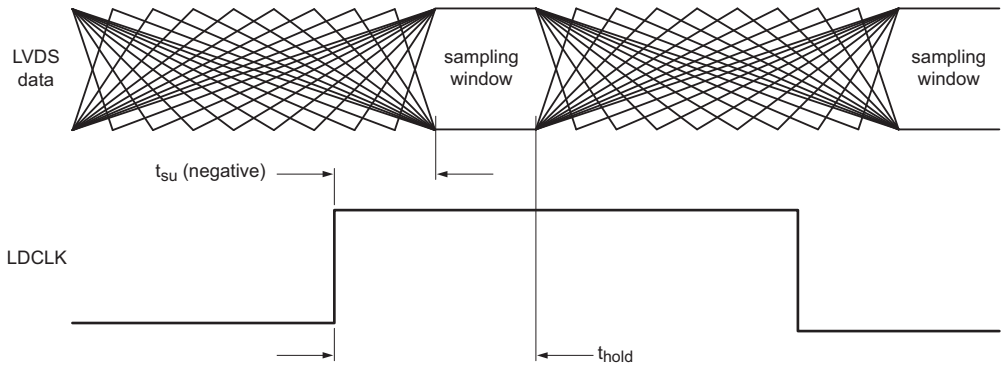


Fig 16. Timing requirement in manual tuning mode

10.9 Operating modes

The DAC1617D1G0 requires two differential clocks:

- The LVDS clock (LDCLKP, LDCLKN) for the LVDS DDR interface
- The data clock (CLKP, CLKN) for the internal PLL and the dual DAC core

In Normal mode, provide both the DAC clock and the LVDS clock to the DAC1617D1G0. Align the ratio frequency between these two clocks needs with selected ×2, ×4 or ×8 interpolation filters. The clocks provided to the DAC1617D1G0 must respect the LVDS input timing and the DAC output timing specifications as defined in Table 5.

In PLL mode, provide the LVDS clock to pins LDCLKP/LDCLKN and pins CLKP/CLKN. Depending on selected interpolation filter, the internal PLL can be set to generate the right DAC core clock frequency internally. The clocks provided to the DAC1617D1G0 pins must respect the LVDS input timing and the DAC output timing specifications as defined in Table 5. The PLL settings must also respect the maximum sampling rate of the PLL (see the sampling rate (f_s) in subsection Internal PLL timing of Table 5).

The main function of the Clock Domain Interface (CDI) is to resynchronize the input data streams to the internal clock the digital processing uses. The CDI also performs the required reformatting of the input datastreams. Set PLL, CDI, and the interpolation filters, which depend on the targeted application accordingly. Section 10.9.1 (×2), Section 10.9.2 (×4), and Section 10.9.3 (×8) explain how to set the DAC1617D1G0 to support the different upsampling modes.

10.9.1 CDI mode 0 (x2 interpolation)

CDI mode 0 (×2 interpolation) is required when the value of the LVDS DDR clock is twice the internal maximum CDI frequency. Table 11 shows examples of applications using an internal PLL or an external clock for the DAC core.

Table 11. CDI mode 0: operating modes examples

LVDS DDR rate (MHz)	I rate; Q rate (Msps)	CDI mode[1]	FIR mode[2]	SSBM rate[3] (Msps)	DAC rate (Msps)	PLL configuration		
						DAC input clock[4] (MHz)	PLL status[5]	PLL divider[6]
320	320	0	×2	640	640	320	enabled	2
320	320	0	×2	640	640	640	disabled	n.a.

[1] Bits CDI_MODE[1:0] of register MISC_CNTRL (see Table 61).

[2] Bits INTERPOLATION[1:0] of register TXCFG (see Table 23).

[3] If a Single Sideband Modulator (SSBM) is used, see bits NCO_ON and MODULATION[2:0] of register TXCFG (see Table 23).

[4] Pins CLKP and CLKN (see Figure 2).

[5] Bit PLL_PD of register PLLCFG (see Table 24).

[6] Bits PLL_DIV[1:0] of register PLLCFG (see Table 24).

10.9.2 CDI mode 1 (x4 interpolation)

CDI mode 1 (×4 interpolation) is required when the values of the LVDS DDR clock and the internal CDI frequency are equal. Table 12 shows examples of applications using an internal PLL or an external clock for the DAC core.

Table 12. CDI mode 1: operating modes examples

LVDS DDR rate (MHz)	I rate; Q rate (Msps)	CDI mode[1]	FIR mode[2]	SSBM rate[3] (Msps)	DAC rate (Msps)	PLL configuration		
						DAC input clock[4] (MHz)	PLL status[5]	PLL divider[6]
250	250	1	×4	1000	1000	250	enabled	4
250	250	1	×4	1000	1000	1000	disabled	n.a.

[1] Bits CDI_MODE[1:0] of register MISC_CNTRL (see Table 61).

[2] Bits INTERPOLATION[1:0] of register TXCFG (see Table 23).

[3] If SSBM is used, see bits NCO_ON and MODULATION[2:0] of register TXCFG (see Table 23).

[4] Pins CLKP and CLKN (see Figure 2).

[5] Bit PLL_PD of register PLLCFG (see Table 24).

[6] Bits PLL_DIV[1:0] of register PLLCFG (see Table 24).

10.9.3 CDI mode 2 (x8 interpolation)

CDI mode 2 (×8 interpolation) is required when the LVDS DDR clock is half the maximum CDI frequency or less. Table 13 shows examples of applications using an internal PLL or an external clock for the DAC core.

Table 13. CDI mode 2: operating modes examples

LVDS DDR rate (MHz)	I rate; Q rate (Msps)	CDI mode[1]	FIR mode[2]	SSBM rate[3] (Msps)	DAC rate (Msps)	PLL configuration		
						DAC input clock[4] (MHz)	PLL status[5]	PLL divider[6]
125	125	2	×8	1000	1000	125	enabled	4
125	125	2	×8	1000	1000	1000	disabled	n.a.

[1] Bits CDI_MODE[1:0] of register MISC_CNTRL (see Table 61).

[2] Bits INTERPOLATION[1:0] of register TXCFG (see Table 23).

[3] If SSBM is used, see bits NCO_ON and MODULATION[2:0] of register TXCFG (see Table 23).

[4] Pins CLKP and CLKN (see Figure 2).

[5] Bit PLL_PD of register PLLCFG (see Table 24).

[6] Bits PLL_DIV[1:0] of register PLLCFG (see Table 24).